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On the characterization of the trapped charge in FG-CMOS inverters

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Abstract In this work, an experimental comparison between measured FG CMOS inverters using the quasi-floating gate (QFG) and layout-based (L-b) techniques for charge removal in the Floating-gate (FG) and simulations through PSpice is presented. The experiment was developed through the measurements of 40 different IC's with a total of 200 FG and QFG CMOS inverters characterized on AMI C5FN 0.5 μm technology. The data obtained shows that the layout-based technique reduces the initial charge present at the FG, but presents a very small residual charge. Nevertheless, the offset associated to the charge follows a normal distribution and is predictable. Comparison between measured QFG inverters and simulations shows that the high resistance parasitic diode must be modeled accurately for a proper simulation.

Keywords Neuron-MOS · vMOS · Floating-gate transistors

1 Introduction

Nowadays, important efforts have been realized in order to eliminate the initial trapped charge at FG due to fabrication process conditions. Early UV techniques were employed to remove this charge [1–3], but the UV exposure in post-fabrication represents a serious drawback from the manufacturing perspective. Other approaches include extra circuitry and high voltages for the use of electron tunneling and/or hot electron injection [4–6]. Recently, the quasi-floating gate (QFG) concept has demonstrated not only to overcome the initial charge problem, but also set the FG to a given DC bias potential through a very high resistance. This important feature, along with the ac-coupled input signal through capacitive coupling Poly1-Poly2, allows the QFG transistor to work in a desired quiescent point [7, 8]. A serious drawback of QFG transistors is that they are not suitable for frequencies below 1 Hz range, where, the cutoff frequency depends mainly by the value of the high resistance connected to the FG.

On the other hand, a recent publication proposes a Layout-based technique (FG L-b) to deal with the initial trapped charge [9]. This technique offers to remove the initial trapped charge at expenses of no extra-circuitry or special post-process steps. Since a previous work has compared both FG transistors; without discharging technique and with the L-b technique [10], in the present work, a statistical comparison between three different techniques is carried out: FG without discharging technique, FG L-b, and QFG by means of CMOS inverters.

2 CMOS FG-inverter

An FG inverter is a typical CMOS push–pull inverter with one or more input capacitances coupled to an isolated FG, which, is shared by the NMOS and PMOS transistors, Fig. 1. The potential induced to the FG can be controlled as a weighted sum, in voltage-mode, of all input signals. This potential, which is common to the complementary MOSFET transistors, establishes the on–off state of the CMOS inverter [11, 12].

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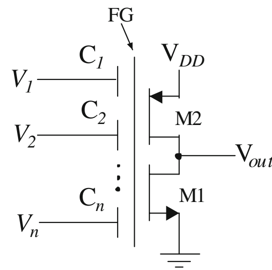

Fig. 1 FG CMOS push–pull inverter

From the charge conservation law, the potential at the FG is given by the following expression:

$$V_{\rm FG} = \frac{1}{C_T}\left[\sum_{i=1}^{n} C_i V_i + Q_{\rm par} + Q_{\rm FG}\right] \quad (1)$$

where, C_i denotes de i-th input capacitance, V_i the i-th voltage input, $Q_{\rm FG}$ the post-process FG trapped charge, $Q_{\rm par}$ the parasitic charge associated to NMOS and PMOS parasitic capacitances, and C_T is the sum of all capacitances to the FG including parasitics.

3 FG layout-based technique

The layout-based technique for discharging the FG was first proposed in [9], the idea consists of adding metal contacts to the isolated FG in the layout, a contact for each available metal level in such technology. The key element lies on the discharging path for the FG provided by the metal layer deposited over the die during the fabrication process, Fig. 2. In such a way, any substrate contact connected to such metal layer will act as a discharging trajectory. For a brief moment, the FG will be connected to substrate until the metal etching step isolate the FG again.

4 CMOS QFG inverter

The QFG concept was first introduced by [7]. Here, the main idea is to connect the FG to a DC potential through a high resistance path. In this way, the FG is fixed to a given DC value and the capacitive coupled inputs set the AC value to the FG. A high resistance from FG to P-substrate can be implemented by the parasitic N +/P$_{\rm sub}$ junction using an NMOS in cut-off, Fig. 3. This reversed diode provides a high resistance, which allows cut-off frequencies below 1 Hz.

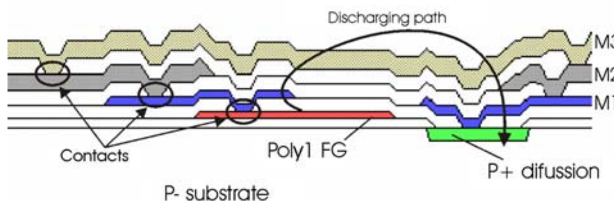

Fig. 2 The layout-based technique, which includes contacts from the FG to every metal layer

According to [7], the V$_{\rm FG}$ for a PMOS can be expressed as

$$V_{\rm FG}(s) = \frac{sR_{\rm leak}}{1 + sR_{\rm leak}C_T}\left[\sum_{i=1}^{n} C_i V_i + Q_{\rm par}\right] \quad (2)$$

where the charge $Q_{\rm par}$ in this case is given by

$$Q_{\rm par} = C_{\rm GS}\cdot V_S + C_{\rm GD}\cdot V_D + C_{\rm GB}\cdot V_B \quad (3)$$

The capacitances $C_{\rm GS}$, $C_{\rm GD}$, and $C_{\rm GB}$ are the parasitic couplings between the FG and the source (V_S), drain (V_D), and bulk (V_B), respectively.

Considering that all input voltages $V_1, V_2,\ldots,V_n$ vary in time, Eq. 2 can be solved for those potentials at DC and the initial post-process trapped charge at FG, $Q_{\rm FG}$. Since V_B and V_S are fixed to $V_{\rm DD}$ for a PMOS transistor, then, in the time domain $V_{\rm FG}|_{\rm DC,}Q_{\rm FG}$ is given by

$$V_{\rm FG}|_{{\rm DC},Q_{\rm FG}} = (C_{\rm GS}\cdot V_S + C_{\rm GB}\cdot V_B + Q_{\rm FG})\, e^{\frac{-t}{R_{\rm leak}C_T}} \quad (4)$$

Equation 4 reveals that any charge contribution to the FG due to DC will disappear after several time constants $\tau = R_{\rm leak}C_T$. The FG potential will be affected only by those capacitive coupled signals with frequency above the cutoff frequency $1/(2\pi R_{\rm leak}C_T)$. This important feature of the QFG concept makes it suitable to deal with the initial trapped charge and at the same time it causes the FG to be less sensitive to DC parasitic contribution.

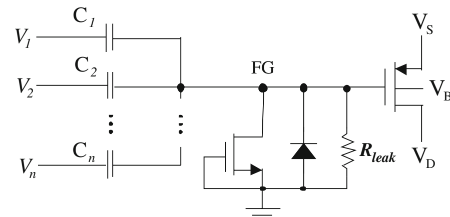

Fig. 3 QFG PMOS with multiple inputs

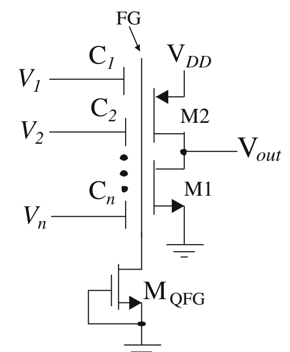

Fig. 4 QFG CMOS push–pull inverter

The QFG concept can be extended to CMOS push–pull inverters, i.e., the same structure presented in Sect. II, but, with the NMOS in cut-off tied to the FG, Fig. 4.

In the QFG Inverter, the voltage V_{FG} depends also on the input voltages V_i through capacitive couplings C_i, and parasitic capacitances related to both NMOS and PMOS transistors.

5 Simulations on PSpice

The simulations of a typical CMOS inverter, an ideal FG CMOS Inverter with $Q_{FG} = 0$ and a QFG CMOS inverter were realized using PSpice in order to make the comparisons with the fabricated devices on AMI CF5N 0.5 μm technology. The inverter was designed using an aspect ratio of 12 μm/0.6 μm for the NMOS and PMOS transistors, respectively. A single input capacitance of 186 fF was used in the design of the FG.

5.1 The FG inverter

The potential at the FG of the inverter, as shown in Fig. 4, depends on input voltages $V_1,\ldots,V_i,\ldots V_n$ through a capacitive voltage divider, C_i/C_T, in addition to the parasitic contribution. In order to simulate the ideal behavior of the FG-inverter with $Q_{FG} = 0$, the use of a macromodel is necessary. Since most circuit simulators replace capacitors by open circuits in the DC analysis, the FG results a floating node which leads to convergence problems. The use of specialized macromodels overcomes this situation; several approaches exist in literature [13–16]. In this work; we used the latter, since all NMOS and PMOS parasitic capacitances connected to the FG are considered using PSpice MOSFET model parameters, Fig. 5.

Where C_i, is the capacitive coupling to the FG for i-th input, V_i is the i-th input voltage, V_{DN}, V_{DP}, V_{SN}, V_{SP}, and V_{BN}, V_{BP} are the drain, source and substrate voltages for the NMOS and PMOS transistors, respectively. From now on, the right side subscripts N and P will denote NMOS and PMOS, respectively. C_{FDN}, C_{FDP} and C_{FSN}, C_{FSP} are the overlap capacitances between the FG and the drain or source. C_{FBN} and C_{FBP} are the overlap capacitances between the FG and the bulk along the edge of the channel, C_{OXN} and C_{OXP} are the gate oxide capacitances and C_{DEPN} and C_{DEPP}, are the depletion layer capacitances, which can be neglected after the channel begins to form under the floating gate [17]. Potentials Φ_{SN} and Φ_{SP} represent the potential of the semiconductor surface. All input voltages to the FG are referenced to substrate.

The capacitance C_{Bottom} represents the parasitic associated to FG-substrate where the FG acts as the bottom plate for input capacitances, in this case for C_1 is shown, Fig. 6. The value of C_{Bottom} is calculated from the FG layout area and the poly1-substrate capacitance per area.

Using the BSIMv3.1 parameters for AMI C5FN 0.5 μm available from MOSIS, all parasitic capacitances for the FG inverter were calculated, Table 1. The total capacitance C_T is 239 fF and the capacitive voltage divider $C_1/C_T = 0.778$.

The parasitic charge Q_{par} can be easily computed and included to the macromodel.

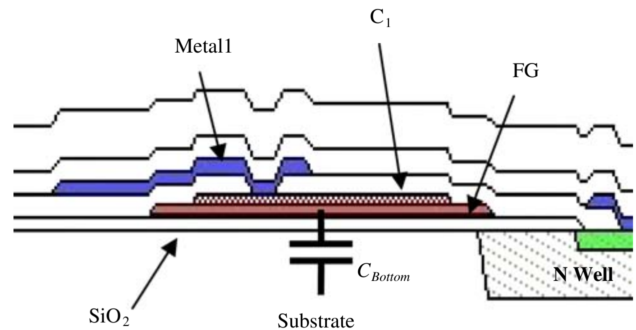

Fig. 6 C_{Bottom} parasitic capacitance composed by the bottom plate of C_1 and substrate

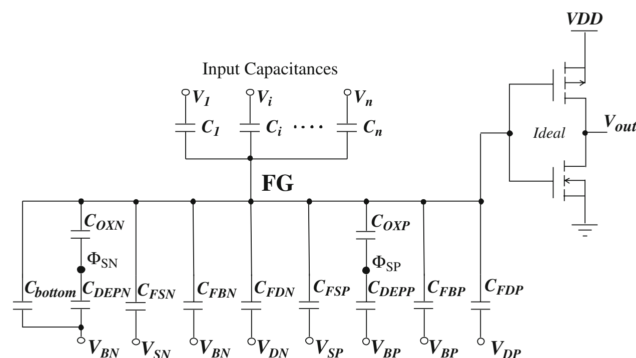

Fig. 5 FG inverter parasitic capacitances

Table 1 Values for the FG inverter parasitic capacitances

PMOS	C_{FDP}	3.6 fF
	C_{FSP}	3.6 fF
	C_{FBP}	4 fF
	C_{OXP}	10.4 fF
NMOS	C_{FDN}	2.6 fF
	C_{FSN}	2.6 fF
	C_{FBN}	4 fF
	C_{OXN}	11.5 fF
	C_{Bottom}	20 fF

$$Q_{\text{par}} = C_{\text{FSN}} \cdot V_{\text{SN}} + C_{\text{FBN}} \cdot V_{\text{BN}} + C_{\text{FDN}} \cdot V_{\text{DN}} + C_{\text{FSP}} \cdot V_{\text{SP}} + C_{\text{FBP}} \cdot V_{\text{BP}} + C_{\text{FDP}} \cdot V_{\text{DP}} + C_{\text{OXN}}(\Phi_{\text{SN}} + V_{\text{BN}}) + C_{\text{OXP}}(-\Phi_{\text{SP}} + V_{\text{BP}}) C_{\text{Bottom}} \cdot V_{\text{BN}} \quad (5)$$

Using the above information, the macromodel was developed in PSpice. Using a $V_{DD} = 3.3$ V and a triangular input signal of 80 kHz with $3.3V_{pp}$ the transient response of three different inverters was obtained, Fig. 7. The trace with circles corresponds to the typical inverter with no extra circuitry, the input voltage V_{in} necessary for an output voltage of $V_{out} = 1/2V_{DD} = 1.65$ V will be the reference data for inverters comparison, from now, this voltage will be denoted by V_{inTP}, so for the typical inverter case, $V_{inTP} = 1.55$ V.

The trace with squares is the response of the FG CMOS inverter (using the macromodel) and the transition point corresponds to $V_{inTP} = 1.58$ V. Finally, the trace with crosses is a typical inverter, but, with a capacitive voltage divider of 0.778 at the input, here $V_{inTP} = 1.92$ V. This curve gives the idea of how shifted to the right is the inverter curve with a capacitive voltage divider at the input and no DC parasitic contribution to the FG.

5.2 Simulation of the QFG inverter

In the QFG inverter circuit Fig. 3, the NMOS in cut-off provides a parasitic junction with a large resistance associated to substrate. In this case, the electrical simulator computes the DC analysis without convergence problems and as a consequence, the use of a macromodel can be avoided.

For large signal, both the junction and the FG behave as a clamping circuit, Fig. 8. Ideally, the FG signal should swing above the 0 V level, but the real behavior presents a

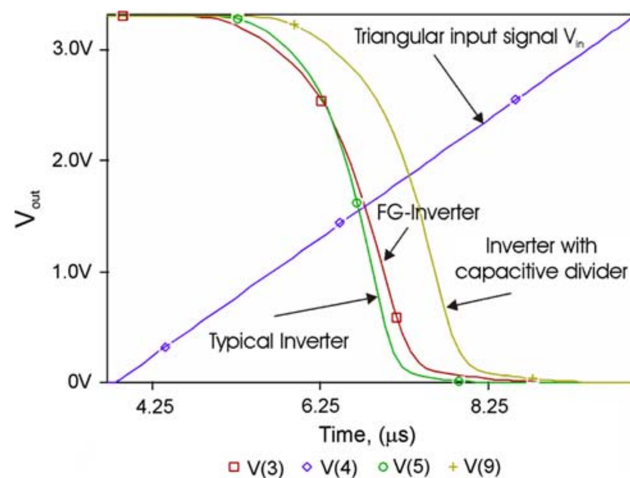

Fig. 7 Results of the FG inverter transient analysis simulation

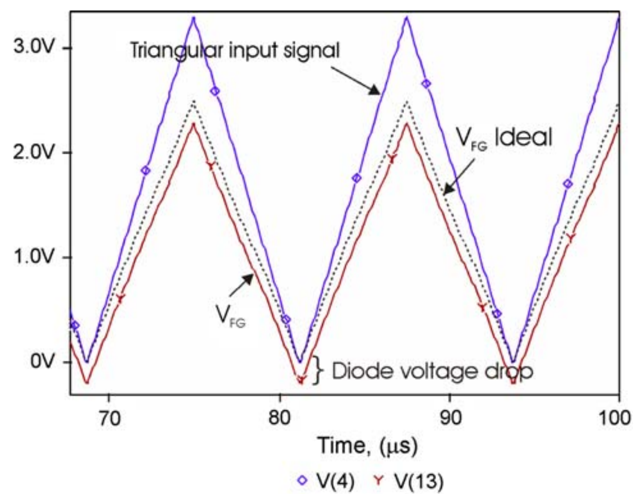

Fig. 8 Transient analysis simulation for the QFG Inverter, the circuit acts as a clamping circuit

DC offset due to the diode voltage drop. Although all DC contribution to the FG vanishes along time, the offset voltage related to the diode causes an important shift in the QFG inverter curve as will be shown.

In order to simulate the QFG inverter accurately, the parasitic diode N^+/P^- must be adequately modeled. For this purpose, the Source-Bulk junction of M_{QFG} was forward biased and measured using a Keithley 236 I–V meter. This junction exhibits the same size as the Drain-Bulk junction. The comparison made with the PSpice DC sweep simulation, including the drain area AD and the drain perimeter PD using the BSIM3v3.1 parameters, is presented in Fig. 9. In the absence of some model parameters as JS, JSSW, NJ, and IJTH, the BSIM3v3.1 model uses some default values which can cause an important difference from the real behavior in forward bias. Since the

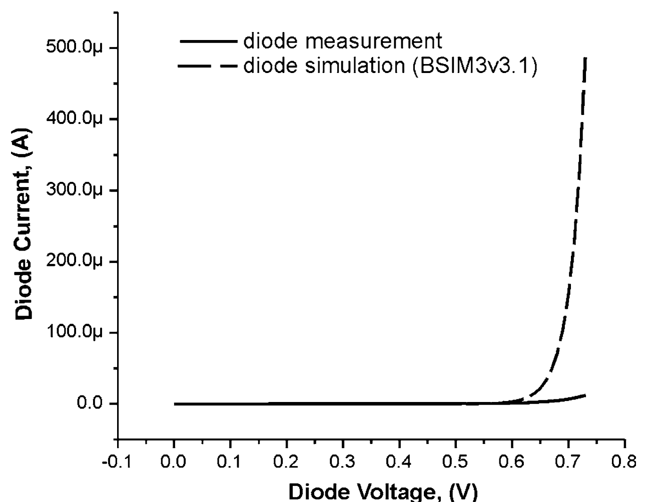

Fig. 9 Comparison between the parasitic diode measurement and simulation using the BSIM3v3.1 parameters in PSpice

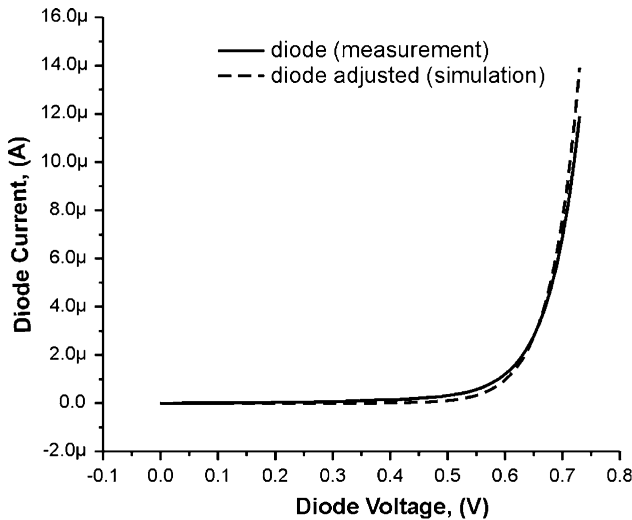

Fig. 10 Comparison of the measured parasitic diode and the adjusted model

drain-substrate and source-substrate junctions are used normally in reverse bias in the MOSFET model, those parameters involved to describe the forward bias are not carefully extracted [18].

The simulation was performed using different simulators, e.g., PSpice, AIM-Spice, T-Spice and Spectre, all of them bringing analogous results, but with an important deviation from measurements. A more detailed analysis of this situation is beyond the scope of this work; nevertheless, the diode curve was adjusted manually using the model available for discrete diodes in SPICE for a more accurate simulation, hence the parasitic diode in Fig. 3 was simulated with this discrete adjusted diode. The parameters used are as follows:

D1 1 0 DPN .0077
.MODEL DPN D(Is = 1e-14 N = 2 Rs = 0 Ikf = 44.17 m Xti = 3 Eg = 1.11 Cjo = 2e-15 M = .2 Vj = .5 Fc = .5 Isr = 1.565n Nr = 2 Bv = 100 Ibv = 100u Tt = 0)

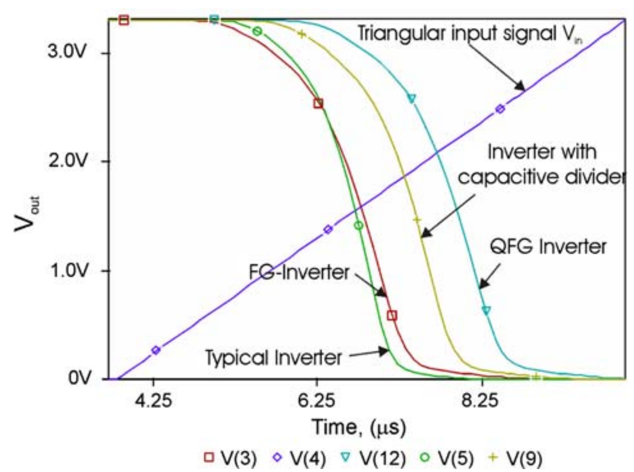

Fig. 11 Results of the QFG inverter transient analysis simulation

The comparison of the simulated discrete diode and the measurement are in Fig. 10.

The QFG inverter was simulated using this approach and the results are presented in Fig. 11. The V_{inTP} for the QFG is 2.20 V, an expected value due to the offset produced by the clamping circuit.

6 Chip design

The experiment was designed with CMOS inverters since the output in voltage mode allows the use of a conventional digital oscilloscope to realize the measurements. A shift on the measured inverter transfer curve compared with a simulated reference will be the offset voltage present at the FG related to the amount of trapped charge, this will be shown in Sect. VIII.

A test chip prototype was designed on CMOS AMI CF5N 0.5 µm in order to compare the simulations and the three different approaches of FG inverters: without discharging technique, Fig. 12(a), with the layout-based technique, Fig. 12(b) and the QFG technique, Fig. 12(c).

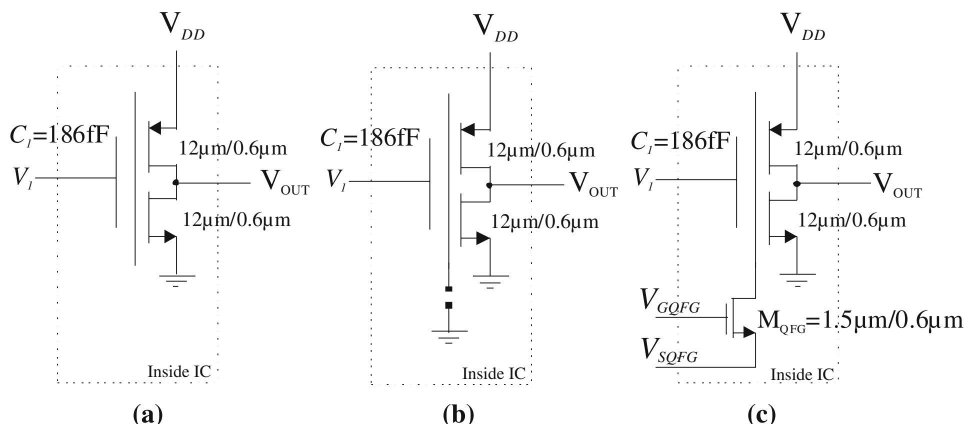

Fig. 12 FG CMOS Inverters, **a** with no discharging technique, **b** with the L-b technique, and **c** QFG inverter

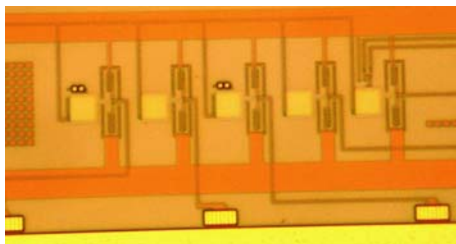

Fig. 13 Inverters microphotograph

The QFG inverter was designed with the gate and source of M_{QFG} controllable externally, thus, M_{QFG} can work in cutoff or as a pass transistor, which, with a voltage sweep on the source the output curve of the inverter can be directly obtained, i.e., as a typical inverter. This curve represents an important reference, since it acts as a point of comparison among the three different techniques.

7 Experimental results

The measurements of 80 FG inverters without discharging technique, 80 with the layout-based technique, 40 with the QFG technique, and 40 typical inverters (accessing the FG through M_{QFG}) are presented.

All of them from 40 different IC's and measured with a digital oscilloscope; a picture of the different inverters is shown in Fig. 13. The measurement was developed as simulations with $V_{DD} = 3.3$ V, a triangular input signal of $3.3V_{pp}$ with 80 kHz frequency and each inverter with a capacitive load of $C_L \approx 200$ pF, Fig. 14.

All traces were saved on the digital oscilloscope and displayed with a numerical software. The four groups in Fig. 14, follow a normal distribution and, in order to obtain a mean and a standard deviation for each one, the V_{inTP} voltage was also considered. The results are shown in Table 2.

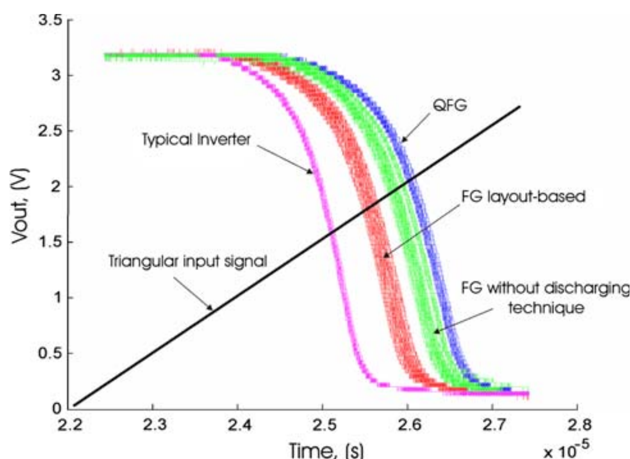

Fig. 14 Measurements results

8 Discussion

From the results shown in Table 2, each group presents a different standard deviation, the typical inverter presents the smallest, this situation arises from the fact that small transistors are used and mismatch effects are present. In the QFG inverter case, the deviation is a little bit larger; this could be explained if an added mismatch to the inverter is produced by the input capacitance, which cannot be avoided from one inverter to another. The behavior exhibited by the other two curves is different, despite of the layout-based technique; the standard deviation of these inverters is almost twice when compared with the QFG group and larger the obtained from the inverters without discharging technique. This suggests that this deviation is a consequence of charge present in the FG.

Since in both latter techniques, the fabrication process is involved on the amount of charge present at the FG, both groups could be correlated. A correlation analysis between these techniques was realized considering in this case the time t_{TP} where the inverter output voltage is $V_{out} = 1/2 \cdot V_{DD}$, from Fig. 13. A scatter plot for FG L-b vs. FG no disch. tech. using the t_{TP} for inverters in the same die is shown in Fig. 15.

The correlation analysis brings a result of $r^2 = 0.027$ which denotes a weak correlation between both FG groups.

The Analysis of Variance (ANOVA) is a set of statistical methods used mainly to compare the means of three or more independent groups. The ANOVA method was realized among the three different groups: FG L-b, QFG, and FG with no discharging technique. The analysis brings an F value of 1495.2, a large value that rejects the null hypothesis (H_o: $\mu_1 = \mu_2 = \mu_3$), which clearly indicates the three groups belong to different populations.

Comparing the mean value of V_{inTP} from the measured and the simulated inverters in Table 2, it can be noticed that the simulation of the typical inverter is almost the value of the mean obtained in measurements. However, the simulation of the FG inverter and the measured FG L-b inverter present a difference of −260 mV and with the FG with no discharging technique of −510 mV. This offset

Table 2 Results of the simulated and measured V_{inTP}

Technique	Mean (V_{inTP})	Std. Dev. (V_{inTP})
Typical inv. (meas.)	1.56 V	9.23 mV
Typical inv. (simulation)	1.55 V	–
FG inv. no dis. tech. (meas.)	2.12 V	34.57 mV
FG L-b inv. (meas.)	1.87 V	29.04 mV
FG inv. (simulation)	1.59 V	–
QFG inv. (meas.)	2.24 V	15.11 mV
QFG inv. (simulation)	2.20 V	–

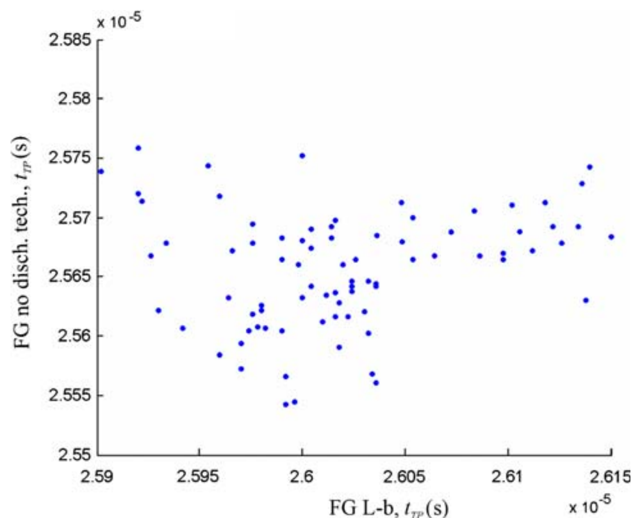

Fig. 15 Scatter plot of FG L-b vs. FG no disch. tech

present could be as mentioned above, to charge present in the FG. This charge could be explained by the fact that every etching step is achieved by the RIE or Plasma technique used normally in modern technology, where, electric fields and charge are already present [19–21]. This technological condition can lead inevitably to charge the FG in the poly1 etching step or when the last metal is etched, this, for the L-b technique case.

The difference of V_{inTP} between the simulated QFG inverter and the measured is about only 40 mV, a difference easily related to capacitance discrepancies and/or model deviations.

9 Conclusion

The use of FG transistors in analog design has been limited by the unpredictable behavior of the initial trapped charge. In this work, experimental and statistical results about the characterization of FG CMOS inverters using the three different techniques for charge removal at the FG were presented. Experimentally, the three techniques follow a normal distribution with a well defined standard deviation, these important results demonstrate that de FG post-process charge is not unpredictable [10].

The comparison of the experimental and simulated data suggests that the L-b technique reduces the charge present at the FG as compared with the FG with no discharging technique; however, a small residual charge remains. This charge should be determined experimentally for those applications where the small offset can affect the circuit performance.

For the QFG case, an important advantage is that all parasitic DC contribution to the FG vanishes along time, in this sense, the QFG is not sensitive to this effect as a true FG structure. However, the observed offset associated to the clamping circuit is the major drawback, the parasitic diode which provides the high resistance path must be modeled accurately, this, in order to obtain a good agreement between measurements and simulations.

Further device experiments including continuous operation by long periods and temperature will be reported soon.

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