Highly Linear Tunable CMOS Gm-C Low-Pass Filter

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***Abstract*—A comprehensive analysis of tunable transconductor topologies based on passive resistors is presented. Based on this analysis, a new CMOS transconductor is designed, which features high linearity, simplicity, and robustness against geometric and parametric mismatches. A novel tuning technique using just a MOS transistor in the triode region allows the adjustment of the transconductance in a wide range without affecting the voltage-to-current conversion core. Measurement results of the transconductor fabricated in a 0.5-μm CMOS technology confirm the high linearity predicted. As an application, a third-order *Gm-C* tunable low-pass filter fabricated in the same technology is presented. The measured third-order intermodulation distortion of the filter for a single 5-V supply and a 2-V_{pp} two-tone input signal centered at 10 MHz is −78 dB.**

***Index Terms*—Analog CMOS circuits, continuous-time filters, Gm-C filters, harmonic distortion, transconductors, tunable filters.**

I. Introduction

THE DESIGN of high-performance continuous-time filters satisfying the increasing demands of modern wireless and wireline communication systems is becoming a challenging task. A clear trend for communication systems is using more elaborated modulation schemes with higher data rates, which requires larger bandwidth and high linearity for the receiver front-end circuits and analog filters as well. For instance, various types of multicarrier modulation schemes are used nowadays in several communication systems like asymmetric digital subscriber line (ADSL), very high bit-rate DSL (VDSL), 802.11 a/g wireless LANs, WiMax, and digital video broadcasting (DVB). They have, in common, the use of multiple carriers over a wide bandwidth to provide robustness against the impairments of poor quality wireless and wired communication channels. These systems require high linearity in a wide bandwidth to avoid intermodulation distortion among the multiple carriers [1]–[4]. Thus, for instance, ADSL requires a third-order intermodulation distortion (IM3) that is better than −60 dB in a signal band of 1.1 MHz, which extends to 4 MHz in ADSL2+ and up to 12 MHz in VDSL systems [5].

Continuous-time filters employed for these demanding applications are currently active RC topologies. They achieve very high linearity (typical third harmonic distortion levels are around −80 dB) [6] and high signal-to-noise ratio (SNR). Moreover, due to the closed-loop operation of the amplifiers, the bandwidth is typically limited to a few megahertz. Transconducance-C (*Gm-C*) filters usually feature higher operating frequencies. This advantage arising from their open-loop operation also comes with the difficulty to achieve high linearity. However, various recent proposals try to achieve *Gm-C* filters comparable in linearity performance to active RC topologies [7]–[13].

This paper aims to contribute to this trend by analyzing how *Gm-C* filter design can approach linearity levels of active RC filters and applying such analysis to new circuit implementations. In Section II, a general discussion on how to achieve tunable *Gm-C* filters with high linearity is presented. Based on this general framework, a tunable transconductor topology which represents a good tradeoff between simplicity and performance is derived in Section III. As an application, the transconductor is employed in a third-order low-pass filter in Section IV. Section V deals with the measurement results of the transconductor and the filter, and conclusions are given in Section VI.

II. Design of Highly Linear Gm-C Filters

It is conventionally accepted that active RC filters achieve better linearity than *Gm-C* filters at the expense of less bandwidth [14], [15]. This is because active RC topologies follow the classic method for designing stable linear active circuits by means of feedback using passive linear elements. Linearity achieved in this way is very high as it depends on the voltage coefficient of the passive components as long as the gain of the active devices is high enough. Fig. 1(a) shows this approach for an active RC integrator. A single-ended topology is shown for simplicity. The virtual ground of the amplifier allows a highly linear voltage-to-current (V–I) conversion, and the resistor current $I_R = V_{\rm in}/R$ is then directly conveyed to the integrating capacitor.

Gm-C filters are claimed to achieve wideband operation and also less linearity, due to their open-loop operation. This fact has precluded the use of *Gm-C* filters for applications requiring very high linearity [14], [15]. To solve this limitation, there have been several proposals to increase the linearity of transconductors, like input attenuation (e.g., using floating-gate MOS transistors), source degeneration, nonlinear-term (polynomial) can-

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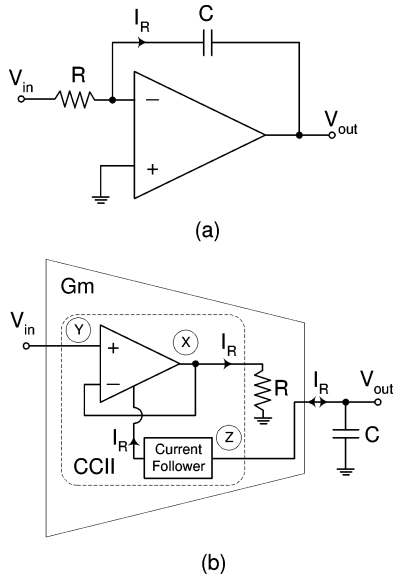

Fig. 1. (a) Active RC integrator. (b) Highly linear *Gm-C* integrator.

cellation, or a combination thereof [16]. Those based on nonlinearity cancellation require accurate matching of MOS transistors to achieve it, and they are very sensitive to second-order effects (e.g., bulk effect, channel-length modulation, and short-channel effects) affecting these transistors. Due to process variations and geometric mismatch, linearity is usually worse than 50–60 dB following this approach [16]. To decrease sensitivity to mismatch and going beyond these values, the basic trend is going back to the classic approach to achieve highly linear circuits, i.e., using feedback and passive resistors for implementing the transconductor, thus achieving a highly linear V–I conversion (e.g., [7]–[9]). Hence, as for the active RC approach, these transconductors rely on high-gain active circuits in feedback loops and passive components. In fact, the resulting filters could be considered as hybrids between *Gm-C* filters and active RC circuits, giving a good tradeoff between linearity and bandwidth. Fig. 1(b) shows a *Gm-C* integrator following this approach. Note that it is not strictly an open-loop topology, and it exploits the same principle as active RC circuits: yielding accurate V–I conversion by passive resistors and feedback amplifiers and then conveying the resistor current to the integrating capacitor. A feedback amplifier is used to implement a voltage follower that translates the input voltage to the resistor terminal, yielding a resistor current $I_R = V_{\rm in}/R$, like for the active RC integrator. The resistor current is typically made available at a high-impedance output node. However, to increase output voltage swing and/or to provide additional output impedance, a current follower is often employed to drive the integrating capacitor. The current follower senses an input current at its low-impedance input and conveys it to its high-impedance output. Note that the voltage and current followers form a second-generation current conveyor (CCII) [17] with terminals X, Y, and Z, defined by $I_Y = 0$, $V_Y = V_X$, and $I_Z = \pm I_X$, as shown in Fig. 1(b). Hence, the resulting transconductor is just a CCII with a resistor load for V–I conversion. *Gm-C* filters based on this approach can thus be considered in a loose sense as active RC filters, but the active element is a CCII with internal feedback instead of an amplifier.

The advantages of the approach in Fig. 1(b) versus that in Fig. 1(a) are as follows: First, unity-gain local feedback is employed instead of feedback around the complete amplifier, hence allowing a higher bandwidth. If properly designed, no compensation capacitor may even be required in the voltage follower since it is not capacitively loaded. Second, the negative impact of continuous tuning on linearity is, in general, lower in Fig. 1(b). This is because active RC filters usually achieve continuous tuning by replacing the passive resistor by an active implementation often based on transistors in the triode region. This choice leads to MOSFET-C topologies with less linearity and limited dynamic range for low supply voltages. In Fig. 1(b), since a replica of the resistor current I_R is sensed at a high-impedance node, it can be scaled without affecting the V–I conversion core formed by the voltage follower and the passive resistor. This fact allows highly linear tuning without affecting the bias condition of the V–I conversion core. More about this option will be discussed in Section II-B.

A. Design of Highly Linear Transconductors

Fig. 2 shows various implementations of transconductors based on the approach in Fig. 1(b). In all cases, CCIIs are arranged in a differential configuration, thus yielding a differential CCII topology, and passive resistors are properly included to implement V–I conversion. Linearity relies on the compliance of the voltage copy from terminal Y to X and of the current copy from terminal X to Z. In Fig. 2(a), [7]–[9], [11]–[13], passive resistors are connected between the X terminals. Since $V_Y = V_X$, the CCIIs replicate the differential input voltage at the resistors' terminals, thus achieving V–I conversion. Then, current at terminal X is conveyed to the high-impedance output terminal Z. Transconductance is ideally $2I_R/V_{\rm id} = 1/R$, where $V_{\rm id} = V_{\rm ip} - V_{\rm im}$. The advantage of this scheme is a high input resistance; hence, it can be applied to monolithic active filters. However, the input range is not rail to rail since the X terminals must track the input voltage. Assuming balanced inputs, voltages at node X are complementary; therefore, the common terminal of the resistors is a signal ground for differential inputs with voltage equal to the common-mode input voltage $V_{\rm icm}$. Therefore, the resistive divider can be used for the output common-mode detection of the driving stage [18]. Due to the signal ground at this node, an alternative implementation of the transconductor is shown in Fig. 2(b), which is just using two identical single-ended transconductors forming a pseudo-differential topology. However, the circuit is then sensitive to resistor mismatch, and the input common-mode voltage, if not constant, must be sensed and applied via a voltage buffer to a signal ground node to have good common-mode rejection ratio.

In Fig. 2(c) (e.g., [21]), the input is applied to two matched resistors, which are also connected to the X terminal of the CCIIs. Since the common-mode input voltage is applied to terminal Y and $V_Y = V_X$, terminals X also have such voltage; hence, nodes X are a signal ground, and a highly linear V–I conversion takes place. Then, this current is conveyed to the high-impedance output by the CCIIs. Transconductance is again $2I_R/V_{\rm id} = 1/R$. The advantage of this approach is a rail-to-rail input range, which is, in fact, limited by the driving stage and not by the circuit due to the use of input resistors. However, the

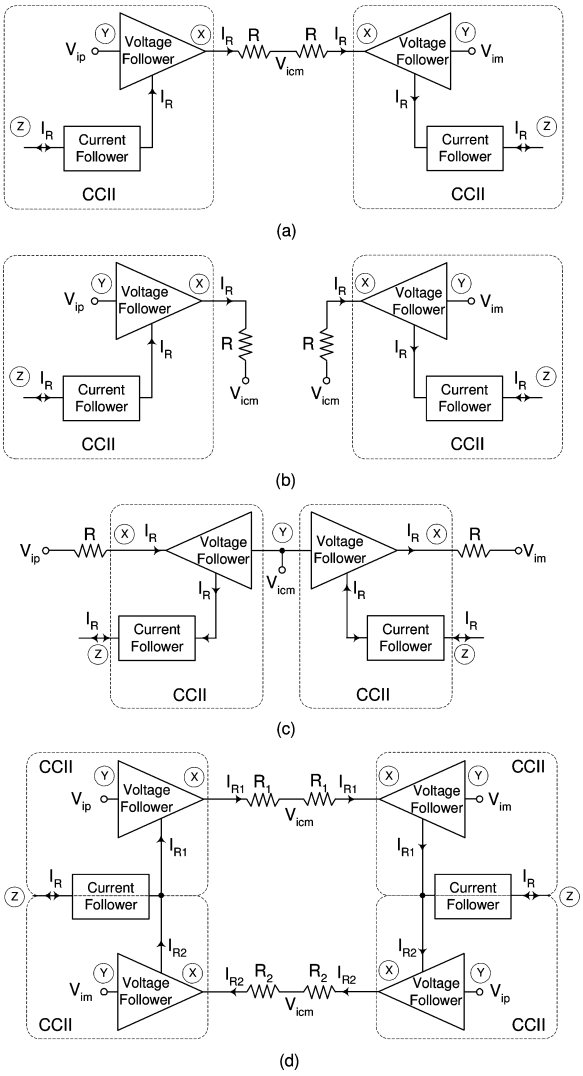

Fig. 2. CCII-based transconductors. (a) With high input resistance [7]–[9], [11]–[13]. (b) Alternative implementation of Fig. 2(a). (c) With high input range [21]. (d) Using two cross-coupled transconductors of Fig. 2(a), [5], [10].

input stage is resistively loaded. Moreover, as in Fig. 2(b), the input common-mode voltage must be sensed, and the circuit is sensitive to mismatch in the input resistors.

Fig. 2(d) shows another alternative topology based on cross-coupling two transconductors of Fig. 2(a), which is used to increase linearity [5]. The output current followers may be shared between the CCIIs, as shown. Transconductance is $2(I_{R1} - I_{R2})/V_{\rm id} = 1/R_1 - 1/R_2$. Note that low transconductance values can be obtained even with not very large resistances.

The main requirements for the voltage followers in Fig. 2 are high input impedance, low output impedance, and voltage compliance. Fig. 3 shows the different choices for the voltage followers, explicitly indicating the node where the resistor current is sensed. In all cases, but possibly in Fig. 3(c), the V–I conversion resistor acts as a source degeneration resistor. For completeness, Fig. 3(a) shows the simplest and more common implementation, a conventional source follower. The absence of feedback loop makes it fast but also less linear. The resistor

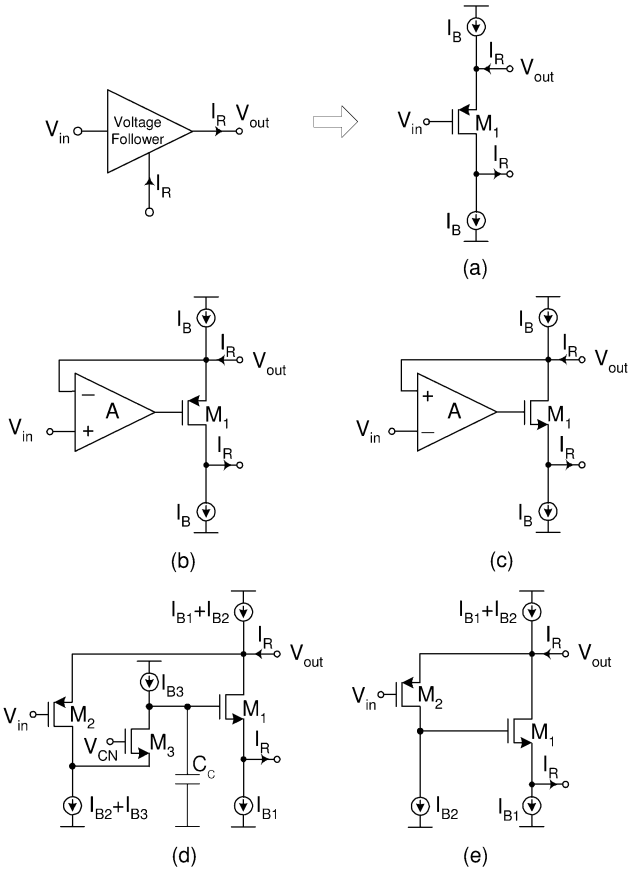

Fig. 3. Some implementations for the voltage follower. (a) Simple source follower. (b) Super Gm stage. (c) Alternative servo loop. (d) Implementation of (c) using folded cascode amplifier. (e) Implementation of (c) using common-source amplifier.

current is naturally sensed at the transistor drain. Resistance at the current-sensing node can be increased by using cascode stages at the expense of voltage headroom, leading to telescopic cascode topologies. The signal-dependent current in M_1 leads to an inaccurate transfer of the input voltage to the output terminal, yielding a small signal gain $A_V \approx 1/[1 + g_{\rm mb1}/g_{m1} + 1/(g_{m1}R_L)] < 1$ and a not very low output resistance $r_{\rm out} \approx 1/(g_{m1} + g_{\rm mb1})$. Parameters g_{m1} and $g_{\rm mb1}$ are the transconductance and the back gate transconductance, respectively, of transistor M_1. To improve linearity, g_{m1} must be increased, which leads to a prohibitively large bias current and transistor width. The term $g_{\rm mb}$ does not appear in the former expressions if the transistor is embodied in an independent well tied to its source.

A conventional cure to these drawbacks is shown in Fig. 3(b), sometimes known as servo feedback [7] or super *Gm* input stage [8], which has been widely employed with different implementations of the amplifier. In this case, input–output voltage compliance no longer relies on a constant $V_{\rm GS}$ drop in M_1, but on the action of the feedback loop. However, the circuit implementation is not simple, and compensation in the amplifier is typically required (e.g., [8]). This degrades bandwidth and increases power consumption.

An alternative voltage follower is shown in Fig. 3(c) [7]. In this case, the implementation of the amplifier may be simpler. For instance, Fig. 3(d) shows the circuit of Fig. 3(c) using a

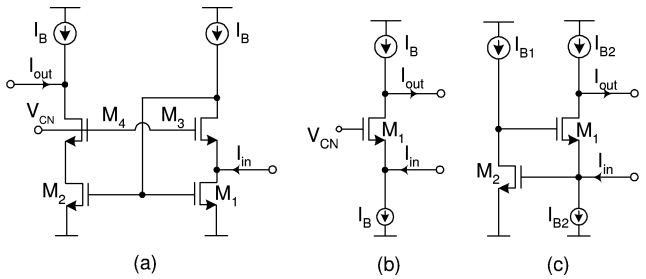

Fig. 4. Some current followers. (a) Current mirror. (b) Folding stage. (c) Regulated cascode stage.

folded cascode amplifier [19]. Despite the additional gain provided by the folding stage, such stage increases power consumption and makes a compensation capacitor necessary [19]. The simplest implementation of Fig. 3(c) which uses a single-transistor amplifier is shown in Fig. 3(e). It is faster and more power efficient than the circuit in Fig. 3(d) and still provides adequate gain to achieve high linearity, as will be evidenced later on. Hence, it will be employed in this paper. Note that the circuit is based on the super source follower [7], but in that case, the resistor current was sensed and replicated in a current mirror. This choice is not optimal as it requires the matching of the mirror transistors. In our case, the current will be sensed by a folding stage, thus making the circuit nearly mismatch insensitive.

As mentioned before and shown in Fig. 2, to improve output resistance and/or to maximize output voltage swing, the resistor current sensed in the voltage follower is often not directly the output current. A current follower is used instead, which senses current I_R at a low-impedance input (ideally a signal ground) set to a proper dc voltage and delivers it to the high-impedance output node. For instance, a current mirror, a folding stage, or a regulated cascode stage can be used for this task. Some possible implementations of them are shown in Fig. 4. Fig. 4(a) shows a possible current-mirror realization, although many other choices do exist. Despite the simplicity of this widely employed approach, there is an important drawback. Note that the design strategy employed [Fig. 1(b)] is strongly insensitive to device mismatch since it relies on high-gain feedback loops and a passive component. If a current mirror is included in the signal path, this insensitivity to mismatch is lost, as matching is required in the current-mirror transistors. Note also that, when the node of the voltage follower where the resistor current is sensed corresponds to a source terminal [e.g., Fig. 3(c)–(e)], this sensing node can be grounded, and the output transistor becomes the input stage of the current mirror. Hence, in this case, the input stage of the current mirror provides gain to the feedback loop of the voltage follower and simultaneously senses the input current. This idea is used in [7], [20], and [21].

Fig. 4(b) shows a folding stage, which is a simple yet efficient mismatch-insensitive current buffer. The regulated cascode circuit in Fig. 4(c) features lower input resistance and is also mismatch insensitive, but it reduces voltage swing at the output stage due to the stacked $V_{\rm GS}$ voltages and requires additional quiescent power consumption. Hence, the circuit in Fig. 4(b) will be employed in this paper.

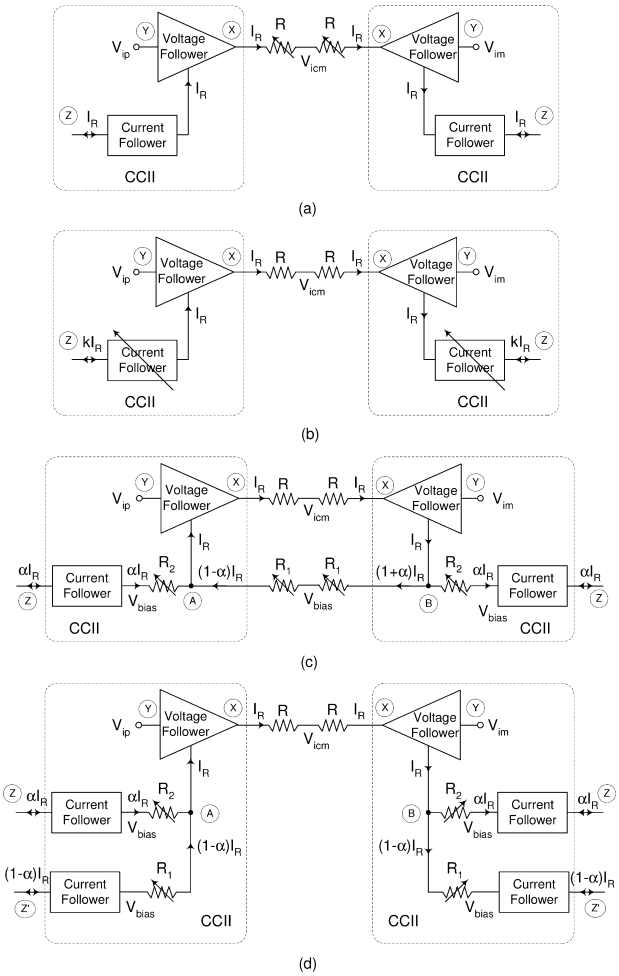

Fig. 5. Transconductor tuning. (a) Adjusting the resistor used for $V-I$ conversion. (b) Scaling the output current. (c) Using resistive current division. (d) Using resistive current splitting.

B. Design of Highly Linear Tuning Schemes

Continuous tuning of the transconductance value is usually required in *Gm-C* filters to compensate for process RC variations. Typically, a tuning range of about 50% is required for this task. Even if the transconductor features high linearity, an inefficient tuning strategy may partially waste it. Hence, the inclusion of tuning should minimize the degradation of linearity and, at the same time, preserve the performance of the transconductor (input range, bandwidth, etc.). Fig. 5 shows different continuous tuning strategies. The simplest choice, shown in Fig. 5(a), consists on varying the resistance used for V–I conversion (e.g., [22] and [23]). Unfortunately, this approach degrades linearity and makes the performance of the transconductor strongly dependent on tuning. Often, a MOS transistor in the triode region implements the variable resistor.

Fig. 5(b) shows an alternative approach based on scaling the output currents, which can be achieved by providing gain or attenuation to the current followers. This approach does not modify the inner V–I conversion core, leading to a stable performance over the whole tuning range and potentially less degradation in linearity. Current scaling can be carried out, e.g., using transconductance multipliers [7]. Another recent

implementation proposed by some of the authors consists in using programmable differential current mirrors operating in moderate inversion to achieve output current scaling [20], [21]. Other programming techniques based on this idea are also reported in [26] and [27].

Another alternative, shown in Fig. 5(c), employs a resistive divider to split the output current, thus leading to current attenuation [8], [12], [28]. If resistors are made programmable, attenuation can be adjusted. Despite the fact that tuning is based on adjusting resistance values as in Fig. 5(a), the method in Fig. 5(c) has important advantages. First, tunable resistors do not modify the V–I conversion core. Second, tuning accuracy depends on ratios of resistors and not on the absolute value of a resistor as in Fig. 5(a). This makes tuning more linear and less dependent on thermal and process variations. In addition, since tuning does not rely on the absolute value of the tuning resistors, tuning resistances can be made small so that voltage swing at the terminals of the tuning resistors is minimized. Hence, they lead to less distortion as compared with tuning the V–I conversion resistor in the transconductor or in a MOSFET-C filter, which experiences the full input-signal swing.

In Fig. 5(c), the transconductor core provides a differential output current $2I_R$ where $I_R = V_{\rm id}/2R$. Assuming that the input node of the voltage followers is a signal ground with voltage set to $V_{\rm bias}$ and applying Kirchoff's current law to nodes A and B, the resistor divider splits the transconductor currents as shown in Fig. 5(c), where

$$\alpha = \frac{1}{1 + R_2/R_1}. \tag{1}$$

Hence, the output current is attenuated by a factor α that can be adjusted by the ratio R_2/R_1, and the total transconductance is $2\alpha I_R/V_{\rm id} = \alpha/R$. Complementary voltages are generated at nodes A and B and are given by

$$\begin{aligned} V_A &= V_{\rm bias} - \alpha R_2 I_R = V_{\rm bias} - \frac{R_1 \| R_2}{R} V_{\rm id} \\ V_B &= V_{\rm bias} + \alpha R_2 I_R = V_{\rm bias} + \frac{R_1 \| R_2}{R} V_{\rm id}. \end{aligned} \tag{2}$$

Therefore, assuming matched R_1 resistors, a differential signal ground is generated at the common terminal of R_1 resistors with voltage equal to $V_{\rm bias}$. Hence, an alternative tuning scheme proposed here is shown in Fig. 5(d), where (1) and (2) remain valid. The advantage of Fig. 5(d) versus Fig. 5(c) is that an additional output current $(1 - \alpha)I_R$ is available at the output. Hence, the circuit implements two transconductors with high current efficiency sharing a common input, one with transconductance α/R and the other one with transconductance $(1 - \alpha)/R$. This feature provides increased design flexibility. The disadvantages are the additional current followers required and that the mismatch in R_1 resistors now affects linearity.

The analysis in this section aims to be a unified approach to the design of highly linear tunable transconductors based on passive resistors and local feedback. Several highly linear transconductors can be obtained by replacing, in any of the circuits in Fig. 2, a given voltage follower in Fig. 3 and a current follower in Fig. 4 and by including any of the tuning methods in Fig. 5 if tuning is implemented. In fact, most of the highly linear transconductors reported can be described as a particular realization of this common framework, as Table IV shows. In this table, only reported *Gm-C* filters achieving a measured IM3 that is better than −60 dB are included.

III. Proposed Transconductor

Based on the analysis in Section II, a new programmable transconductor that represents a good tradeoff between linearity and circuit simplicity is proposed in this section. It employs the approach shown in Fig. 2(a). The voltage follower chosen is that in Fig. 3(e), and the current follower is the folding stage in Fig. 4(b). A very simple tuning scheme is proposed, requiring only one transistor in the triode region, which is based on a modification of the scheme in Fig. 5(c). This modification is shown in Fig. 6.

A. Circuit Description

In Fig. 6(a), the proposed V–I conversion core with the tuning in Fig. 5(c) is shown. The linearity of the tunable resistor divider is achieved when the current through resistor $2R_1$ is proportional to I_R. It can be demonstrated that, as long as the voltage across the triode transistor implementing $2R_1$ is fully balanced, no distortion is generated in a first-order analysis by this tuning scheme [29]. To achieve it, in practice, voltage swings at nodes A and B should be as small as possible (with minimum limit given by noise). This swing relies on the resistance $R_A = R_{\rm B}$ seen from nodes A and B to the output and is minimized by minimizing such resistance. Simulations show that excellent linearity is obtained for maximum voltage swings at nodes A and B of about ±40 mV, which, for current swings in the range of ±1/3 mA, are obtained with a resistance $R_A = R_B \approx 120\ \Omega$. However, note that, in the scheme in Fig. 6(a), $R_A = R_B = R_2 + R_{\rm CN}$, where $R_{\rm CN}$ is the resistance seen from the source of cascode transistor $M_{\rm CN}$ which operates in saturation. This resistance is nonlinear, and its small-signal value is approximately $1/(g_{\rm mCN} + g_{\rm mbCN})$. To have $R_A = R_B \approx R_2 \approx 120\ \Omega$, the value of $R_{\rm CN}$ should be much smaller than R_2, i.e., of a few ohms. This is unfeasible for reasonable bias currents and transistor dimensions. A solution is to decrease the input resistance of the current follower by negative feedback using the regulated cascode topology of Fig. 4(c), but unfortunately, it reduces output signal swing, as mentioned in Section II-A. We propose a simpler approach shown in Fig. 6(b). Since the goal is to minimize $R_A = R_B$ and the lower bound is set by $M_{\rm CN}$, we just remove R_2, and by properly biasing and dimensioning $M_{\rm CN}$, we can obtain a value of $R_A = R_B = R_{\rm CN}$ on the order of 120 Ω. Hence, the desired small voltage swing is achieved, and for this small swing, the voltage dependence of $R_{\rm CN}$ is kept very small. This way, high linearity is achieved by a very simple circuit, i.e., just an adjustable resistance made by a MOS transistor in the triode region which diverts a part of the differential input current of the current followers.

The detailed schematic of the transconductor is shown in Fig. 6(c). All bias currents are equal. Cascode current sources are employed when high output resistance is required. Since the programming transistor leads to a decrease in output resistance which is also dependent on tuning, an additional cascode transistor $M_{\rm CN2}$ has been included. A conventional common-mode

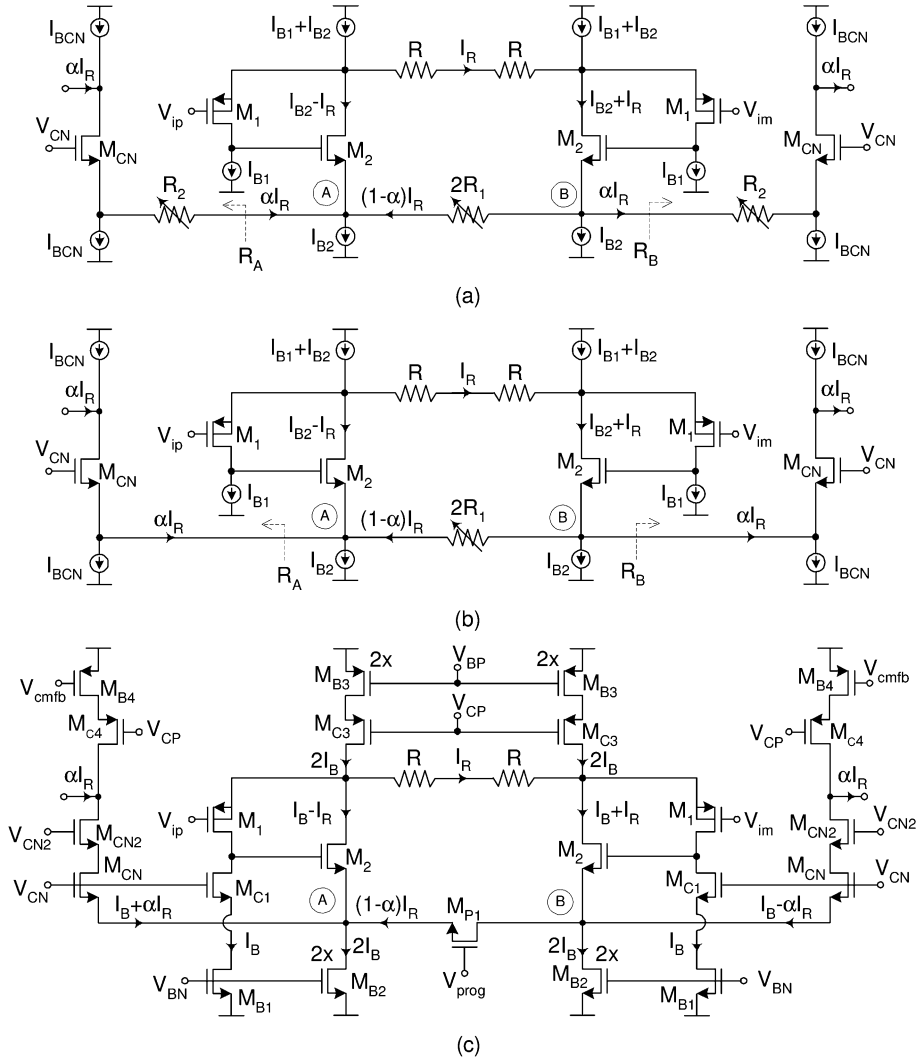

Fig. 6. Proposed transconductor. (a) Starting topology with the tuning employed in Fig. 5(c). (b) Modified tuning strategy. (c) Detailed circuit.

feedback circuit, not shown in Fig. 6(c), has been used. To improve linearity, pMOS input transistors M_1 have been embodied in independent wells connected to their respective sources, as shown in Fig. 6(c). This leads to a bulk-to-substrate capacitance which is approximately of 70 fF. This capacitance can create a zero in the transconductance. However, for the frequency range and low Q factor of the filter presented in the next section, this capacitance was not relevant.

B. Tuning Linearity Analysis

Considering mobility degradation, the drain current I_D of a MOS transistor in strong inversion and saturation is approximately

$$I_D \approx \frac{(\beta/2)(V_{\rm GS}-V_{\rm TH})^2}{1+\theta(V_{\rm GS}-V_{\rm TH})} \tag{3}$$

where

$$V_{\rm TH} = V_{\rm TH0} + \gamma\left[\sqrt{|2\phi_F + V_{\rm SB}|} - \sqrt{|2\phi_F|}\right] \tag{4}$$

is the threshold voltage and $\beta = \mu_o C_{\rm ox}(W/L)$. Parameter μ_o is the zero-field mobility, $C_{\rm ox}$ is the gate oxide capacitance per unit area, θ is the mobility reduction factor, γ is the body effect parameter, ϕ_F is the Fermi potential, and $V_{\rm TH0}$ is the threshold voltage for $V_{\rm SB} = 0$ V. Considering transistors $M_{\rm CN}$, channel-length modulation negligibly affects them since their drain is connected to an identical cascode transistor $M_{\rm CN2}$ with the same current, hence $V_{\rm DS}$ variations in $M_{\rm CN}$ are very small. Solving in (3) for the $V_{\rm GS}$ voltage of $M_{\rm CN}$

$$V_{\rm GS} = V_{\rm TH} + \frac{\theta}{\beta_{\rm CN}} I_D + \sqrt{\left(\frac{\theta}{\beta_{\rm CN}} I_D\right)^2 + \frac{2}{\beta_{\rm CN}} I_D}. \tag{5}$$

Using (5), the voltages at nodes A and B are

$$\begin{aligned} V_A \approx{}& V_{\rm CN} - V_{\rm TH} - \frac{\theta}{\beta_{\rm CN}}(I_B + I_1) \\ &- \sqrt{\frac{2I_B}{\beta_{\rm CN}}}\sqrt{1+\frac{I_1}{I_B}}\left(1+\frac{\theta^2}{4\beta_{\rm CN}} I_1\right) \\ V_B \approx{}& V_{\rm CN} - V'_{\rm TH} - \frac{\theta}{\beta_{\rm CN}}(I_B - I_1) \\ &- \sqrt{\frac{2I_B}{\beta_{\rm CN}}}\sqrt{1-\frac{I_1}{I_B}}\left(1-\frac{\theta^2}{4\beta_{\rm CN}} I_1\right) \end{aligned} \tag{6}$$

where I_1 is the current superimposed to I_B that flows through $M_{\rm CN}$, which is αI_R in the ideal case, as shown in Fig. 6(c). Using the Maclaurin series expansion for the square roots $(1 \pm I_1/I_B)^{1/2}$ in (6), applying the resulting V_A and V_B in the expression for the current $I_{\rm DP1}$ in the triode transistor $M_{\rm P1}$, and solving for $I_1 = I_R - I_{\rm DP1}$, the expression of I_1 as a function of I_R can be obtained. From this expression, it is possible to write the output current $I_{\rm od} = 2I_1$ as

$$I_{\rm od} \approx 2\alpha I_R + 2\alpha_3 I_R^3 \tag{7}$$

where parameter α corresponds (neglecting higher order terms) to the attenuation I_1/I_R and is given by

$$\alpha = \frac{1}{1 + \frac{\beta_{P1}}{(1-\varepsilon)(1+\theta V_x)I_B}\left(1 + \theta\sqrt{\frac{2I_B}{\beta_{\rm CN}}}\right)\sqrt{\frac{2I_B}{\beta_{\rm CN}}}V_x} \tag{8}$$

where

$$V_x = V_{\rm prog} - V_{\rm CN} + \sqrt{\frac{2I_B}{\beta_{\rm CN}}} + \frac{\theta}{\beta_{\rm CN}}I_B. \tag{9}$$

The transconductance of the circuit is given by $G_m = \alpha/R$. Expression (8) is valid only when $M_{\rm P1}$ is on and operates in strong inversion and triode region, for $V_{\rm prog} > V_{\rm CN} - (2I_B/\beta)^{1/2}$. If $M_{\rm P1}$ is off, $\alpha = 1$, and no attenuation takes place. Parameter ε is

$$\varepsilon = \frac{\gamma}{2\sqrt{2|\phi_F| + V_{\rm cm,AB} - V_{\rm SS}}} \tag{10}$$

and $V_{\rm cm,AB} = (V_A + V_B)/2$. Expression (10) assumes that the differential swing at nodes A and B is small such that $|V_A - V_B| \ll 2(2|\phi_F| + V_{\rm cm,AB} - V_{\rm SS})$. In this case, the variation of the difference $V'_{\rm TH} - V_{\rm TH}$ of threshold voltages in transistors $M_{\rm CN}$ is nearly proportional to $V_B - V_A$; hence, it is equivalent to a small variation of the resistance of $M_{\rm P1}$, as (8) shows.

Fig. 7 shows the comparison of α in (8) versus $V_{\rm prog}$, shown in solid line, with the simulation results (circles). Despite the relative simplicity of the model, the results are in good agreement. The slow decrease of α for large $V_{\rm prog}$, not predicted by first-order analysis, is mainly caused by mobility reduction in $M_{\rm P1}$ due to the strong vertical field in the channel for large $V_{\rm prog}$. This can be noticed by the dashed curve in Fig. 7 that corresponds to (8) once mobility degradation is removed. The velocity saturation of carriers in the channel is less important in this case due to the low $V_{\rm DS}$ values and the nonminimum L.

Albeit (8) reflects a weak dependence of α on $V_{\rm cm,AB}$, which could potentially lead to distortion, this is not the case as, due to the small swings at nodes A and B, $V_{\rm cm,AB}$ is almost constant. From (6), the maximum deviation of $V_{\rm cm,AB}$ from its quiescent value $V^Q_{\rm cm,AB}$ (i.e., for $I_1 = 0$) is

$$V^{\max}_{\rm cm,AB} - V^Q_{\rm cm,AB} \approx \frac{1}{8}\sqrt{\frac{2I_B}{\beta_{\rm CN}}}\left(1 - \frac{\theta^2 I_B}{\beta_{\rm CN}}\right)\left(\frac{I_1}{I_B}\right)^2. \tag{11}$$

For the technology, component dimensions, and bias condition chosen, this deviation is in the worst case (no attenuation) and for $I_1^{\max} = \pm I_B/3$ of 3.7 mV from (11), i.e., close to the 3.1 mV obtained in simulation. However, attenuation is not completely signal independent due to the higher order terms in the output current, of which the third-order term is the dominant one as (7) reflects. From the same analysis, it is found (not considering reactive effects) that the third-order harmonic distortion (HD3) of the differential output current $I_{\rm od} = 2I_1$ when $I_R = I_0 \cos\omega_0 t$ is

$$HD3 \approx \frac{\alpha^3}{32}\frac{\beta_{P1}}{(1-\varepsilon)(1+\theta V_x)}\sqrt{\frac{2I_B}{\beta_{\rm CN}}}\left|V_{\rm prog} - V_{\rm CN} - \frac{\theta I_B}{\beta_{\rm CN}}\right|\frac{I_0^2}{I_B^3} \tag{12}$$

with α in (8). Like (8), it is only valid for approximately $V_{\rm prog} > V_{\rm CN} - (2I_B/\beta)^{1/2}$. When $M_{\rm P1}$ is off, the tuning circuit does not operate, and no distortion is introduced by it. Note that the linearity of the proposed tuning scheme increases for large I_B's and when transistors $M_{\rm CN}$ have much larger transconductance than $M_{\rm P1}$. This is intuitively satisfying as, in this case, the voltage swing in V_A and V_B is reduced for large $M_{\rm CN}$ transistors. The influence of the body effect is small because the $V_{\rm SB}$'s in $M_{\rm P1}$ and in the $M_{\rm CN}$ transistor with the smallest source voltage are the same. For the other $M_{\rm CN}$ transistor, $V_{\rm SB}$ is different, but not much as signal swing at nodes A and B is small, and it mainly leads to an effective increase of β_{P1} via ε as (10) and (12) reflect. When $V_{\rm prog}$ increases, the term α^3 in (12) decreases but also the expression inside the modulus increases. The net effect is that HD3 does not vary so much with α for the transistor dimensions employed in our implementation. The simulated HD3 at 1 MHz does not deviate more than 6 dB from the formula in (12) for $V_{\rm prog}$ in the range of 2–5 V, thus validating the former analysis. Note that, neglecting mobility reduction, the minimum for HD3 in (12) when the transistor $M_{\rm P1}$ is on is for $V_{\rm prog} = V_{\rm CN}$, regardless of the sizes of $M_{\rm P1}$ and $M_{\rm CN}$. It is also intuitively satisfying as, in this case, both $M_{\rm P1}$ and $M_{\rm CN}$ have the same gate and bulk voltage, and due to the symmetry of the MOS transistor, the current division is almost linear regardless of the operating region of the transistors, as demonstrated by Bult and Geelen [30]. In practice, due to second-order effects and the additional distortion of the V–I conversion core, there is still distortion for this condition. In summary, the weak nonlinearity of the resistances R_A and R_B implemented by the

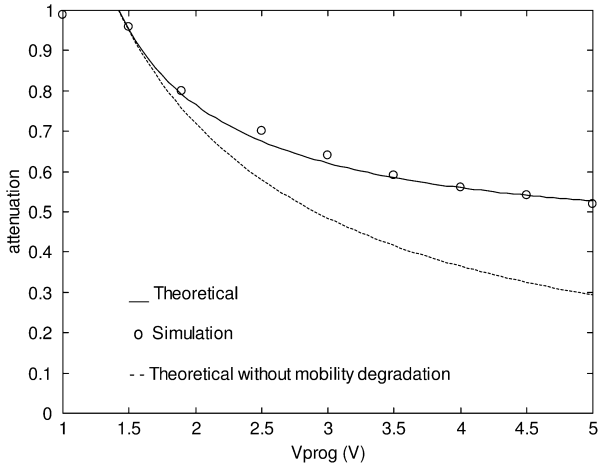

Fig. 7. Attenuation a versus $V_{\rm prog}$.

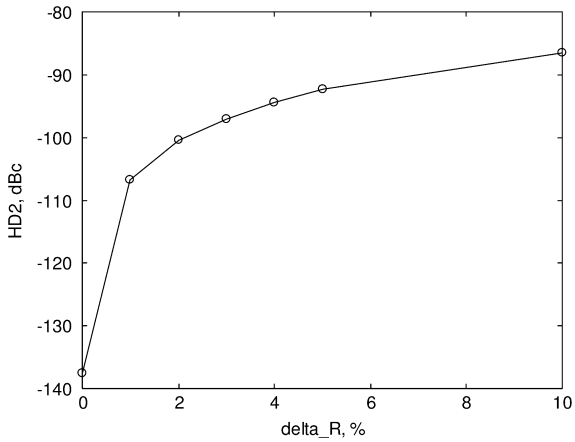

Fig. 8. HD2 versus deviation in the R values of the two resistors in Fig. 6(c).

cascode transistors does not significantly degrade linearity in this tuning arrangement, as confirmed also by simulations and experimental measurements. Note also that the tuning method does not scale bias currents, hence simplifying the output stage and making its behavior less dependent on tuning. This is in contrast to current scaling techniques that usually scale both the signal and bias currents.

C. Geometric and Parametric Mismatches

Transistor mismatch may occur due to process gradients. However, since the proposed transconductor relies on transistors arranged in high-gain feedback loops, mismatch in geometric or process parameters is of minor concern as long as the loop gain is kept high. Moreover, the avoidance of current mirrors in the output stage leads to a circuit not requiring matching conditions in any transistor in the signal path, making this topology nearly insensitive to mismatch. However, when tuning is set (i.e., $\alpha < 1$), matching in transistors $M_{\rm CN}$ is required as the resistance seen from nodes A and B to the output should be the same for proper current division. Hence, conventional layout techniques to reduce mismatch are employed. The worst case for matching the sensitivities of transistors $M_{\rm CN}$ is for minimum α. Worst case simulations ($V_{\rm prog} = 5$ V) of the transconductor for a 1-MHz input of 2 $V_{\rm pp}$ show that a 2% mismatch in the aspect ratio of transistors $M_{\rm CN}$ leads to an increase in the second harmonic from a negligible value to -86 dBc, which is still below the third harmonic for this setting of α. Furthermore, if the common-mode feedback circuit uses the resistor divider in Fig. 6(c) to sense the common-mode voltage of the driving stage, matching is required in resistors R to avoid the effect of the common-mode distortion coming from the driving stage, which would increase even-order distortion. Simulations for an input signal of 100 kHz and 2 $V_{\rm pp}$ show that such mismatch only affects even-order distortion. Fig. 8 shows the increase in HD2 versus the mismatch in resistors $R(\%)$ obtained from these simulations. Note that, for typical matching achievable in integrated resistors, HD2 does not become significant. Note also that, obviously, if other common-mode sensing techniques are used, matching in these resistors is not required.

D. Maximum Input and Output Swings

To enforce saturation in the transistors, the input voltage cannot reach the lower bound given by $V_{\rm SS} + V_{\rm GS}^{M2} + V_{\rm DSsat}^{\rm MB2} - |V_{\rm TH}^{M1}|$ or the upper bound given by $V_{\rm DD} - |V_{\rm DSsat}^{\rm MB3}| - |V_{\rm DSsat}^{\rm MC3}| - |V_{\rm GS}^{M1}|$, where $V_{\rm DSsat}^{\rm Mi}$ is the $V_{\rm DS}$ saturation voltage of transistor $M_{\rm i}$. These values assume that cascode bias voltages $V_{\rm CP}$ and $V_{\rm CN}$ are optimally set to achieve these limits. Hence, assuming that the input common-mode voltage is set to the middle of these limiting values, the maximum input swing is

$$V_{\rm in,swing} = V_{\rm DD} - V_{\rm SS} - |V_{\rm GS}| - 4|V_{\rm DS,sat}|. \tag{13}$$

The differential input swing is twice this value. Concerning the output branch, the maximum output voltage is $V_{\rm DD} - V_{\rm SDsat}^{\rm MB4} - V_{\rm SDsat}^{\rm MC4}$, and the minimum one is $V_{\rm SS} + V_{\rm DSsat}^{\rm MB2} + V_{\rm DSsat}^{\rm MCN} + V_{\rm DSsat}^{\rm MCN2}$, once more assuming optimal $V_{\rm CP}$ and $V_{\rm CN}$ values. Hence, assuming that output common-mode voltage is set to the middle of these limits, the maximum voltage swing at the output stage is $(V_{\rm DD} - V_{\rm SS}) - 5|V_{\rm DS,sat}|$. However, the transconductor and load resistor, as well as the tuning attenuation α may limit the output voltage swing to a lower value given by $(\alpha R_L/R)V_{\rm in,swing}$ where $V_{\rm in,swing}$ is the input swing and R_L is the load resistor. Hence, the maximum output swing for a given R_L, R, and α will be the smaller of two voltages

$$V_{o,\rm swing} = \min\left[\frac{\alpha R_L}{R}\left(V_{\rm DD}-V_{\rm SS}-|V_{\rm GS}|-4|V_{\rm DS,sat}|\right), V_{\rm DD}-V_{\rm SS}-5|V_{\rm DS,sat}|\right]. \tag{14}$$

The maximum swing of the differential output voltage is twice this value.

E. SNR

The main sources of noise in CMOS analog circuits are thermal and flicker noise. Due to the relatively large *WL* values of the transistors and the high bandwidth of the transconductor, noise is dominated by the contribution of the thermal noise of the transistor channels and passive resistor. Considering thermal noise and assuming, as usual, that noise sources are uncorrelated, the approximate expression for the output noise density of the transconductor is

$$\frac{\overline{i_{N,\rm out}^2}}{\Delta f} \approx \frac{16}{3}k_BT\left[g_{\rm mb4}+\alpha^2\left(g_{\rm mb1}+g_{\rm mb2}+g_{\rm mb3}+\frac{1}{g_{m1}R^2}\right)+\frac{g_{\rm mCN}}{(1+g_{\rm mCN}r_{P1})^2}+\frac{3}{2}\left(\frac{\alpha^2}{R}+\frac{1}{r_{P1}}\right)\right] \tag{15}$$

where k_B is the Boltzmann's constant, T is the absolute temperature, $g_{\rm mi}$ is the small-signal transconductance of transistor $\rm M_i$, $\alpha \le 1$ is the attenuation of the tuning circuit, and $2r_{P1}$ is the resistance of the tuning transistor. The output noise current

TABLE I
FILTER SPECIFICATIONS

Type	Chebyshev
Order	3
3-dB Frequency range	12 MHz – 6 MHz
Passband ripple	0.5 dB
Stop Band	72 MHz
THD	< -75 dB
SNR	> 75 dB

is mainly dominated by the current sources. Since g_m is proportional to $1/(V_{\rm GS}-V_{\rm TH})$, large $V_{\rm GS}-V_{\rm TH}$ values in the current sources allow the reduction of noise, although it also reduces signal swing. For a large attenuation (small α), the output noise current is dominated by the noise current of $M_{\rm B4}$ (since it is not attenuated) and the tuning transistor (as r_{P1} decreases when α decreases).

The noise density in (15) can be expressed as $4k_BT\Gamma G_m$, with Γ as the excess noise factor. Since $G_m=\alpha/R$, such factor is

$$\Gamma=\frac{4}{3}\frac{R}{\alpha}\left[g_{\rm mb4}+\alpha^2\left(g_{\rm mb1}+g_{\rm mb2}+g_{\rm mb3}+\frac{1}{g_{m1}R^2}\right)+\frac{g_{\rm mCN}}{(1+g_{\rm mCN}r_{P1})^2}+\frac{3}{2}\left(\frac{\alpha^2}{R}+\frac{1}{r_{P1}}\right)\right]. \quad (16)$$

Considering only thermal noise and assuming that the output swing in (14) is not reaching the limit $(V_{\rm DD}-V_{\rm SS})-5|V_{\rm DS,sat}|$, the output SNR ($\rm SNR_o$) of the transconductor is as shown in (17) at the bottom of the page, where A is the amplitude of the input voltage and B_N is the equivalent noise bandwidth. Note that $\rm SNR_o$ is maximized for maximum $\alpha=1$, since attenuation reduces the output signal but does not reduce the noise contribution of M_{B4} and the tuning circuit transistors. The signal-to-noise-plus-distortion ratio is also maximum for $\alpha=1$ since distortion is minimal when transistor M_{P1} is off.

IV. FILTER IMPLEMENTATION

As an application of the transconductor of Section III, a third-order tunable *Gm-C* low-pass filter has been designed with the specifications given in Table I corresponding to a VDSL channel filter. A frequency-tuning capability of one octave has been provided using the new programmability technique explained before. The application is a good benchmark for the proposed transconductor due to the stringent linearity requirements.

The scheme of the fabricated filter is shown in Fig. 9. The first two transconductors along with the first pair of grounded capacitors is a first-order integrator, and the subsequent four transconductors plus the other four capacitors form a Tow–Thomas second-order section. The last transconductor is

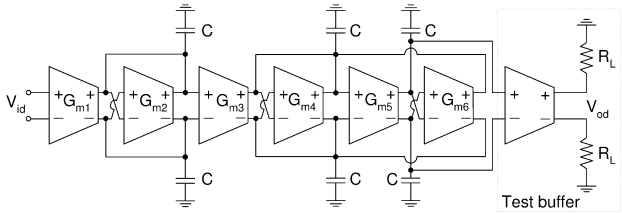

Fig. 9. Fully differential *Gm-C* third-order low-pass filter.

identical to the ones of the filter and was used as a highly linear buffer in order to measure the output, avoiding the loading of the filter with the pad capacitance and not requiring external buffers that can introduce higher distortion levels than the ones we are trying to measure. The output load was a resistor $R_L=R$ in order to have the input and output voltages at approximately the same value when $\alpha=1$, i.e., when G_m is at the highest value.

The filter transfer function is given in (18). Poly–poly capacitors of 8 pF in common-centroid arrangement were used, and the transconductance values were set to $G_{m1}=G_{m2}=G_{m4}$ and $G_{m3}=G_{m5}=G_{m6}$; therefore, two different transconductors were designed

$$H(s)=\frac{V_{\rm od}(s)}{V_{\rm id}(s)}=\frac{G_{m1}/C}{s+G_{m2}/C}\,\frac{G_{m3}G_{m5}/C^2}{s^2+(G_{m4}/C)s+G_{m5}G_{m6}/C^2}. \quad (18)$$

The dimensions of $M_{\rm P1}$ in the transconductors were selected to reduce the nominal transconductance by 50%, (i.e., to get $1\le\alpha\le 0.5$). Hence, the filter cutoff frequency can be tuned in one octave, from a nominal value of 12 to 6 MHz. The nominal Q is 1.5.

V. MEASUREMENT RESULTS

The proposed tunable transconductor and *Gm-C* filter have been fabricated in a standard 0.5-μm CMOS technology with three metal layers, poly–poly capacitors, and high-resistance polysilicon resistors that were used to build the V–I conversion resistors R. The microphotograph of the circuit is shown in Fig. 10. The filter and the transconductor occupy approximately 1.5 and 0.18 mm^2 of the die area, respectively. As discussed in Section III-C, the transconductor has a natural robustness against mismatch; therefore, only basic matching techniques were used in the circuit layout design. However, matching in the passive devices of the filter is required as usual.

Measurement results were obtained using a carefully prepared test setup for both circuits due to the low expected harmonics. A highly linear signal generator was required, and also, a low-pass passive filter at its output was used to reduce the generator harmonics. The balanced input voltage of the circuit was

$$\rm SNR_o=\frac{\overline{V^2_{out,rms}}/R_L}{R_L\overline{i_n^2}}\approx\frac{3A^2}{32k_BR^2TB_N\left[\frac{g_{\rm mb4}}{\alpha^2}+g_{\rm mb1}+g_{\rm mb2}+g_{\rm mb3}+\frac{1}{g_{m1}R^2}+\frac{g_{\rm mCN}}{\alpha^2(1+g_{\rm mCN}r_{P1})^2}+\frac{3}{2}\left(\frac{1}{R}+\frac{1}{\alpha^2r_{P1}}\right)\right]} \quad (17)$$

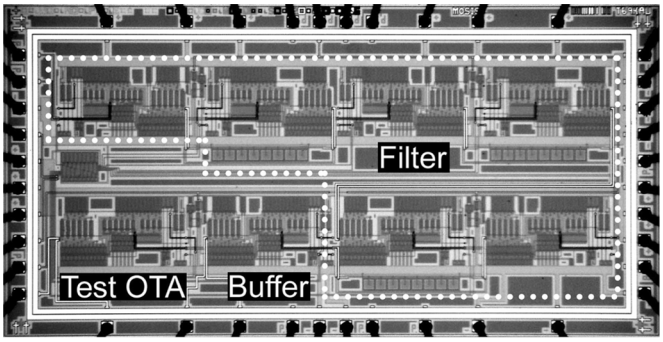

Fig. 10. Filter microphotograph.

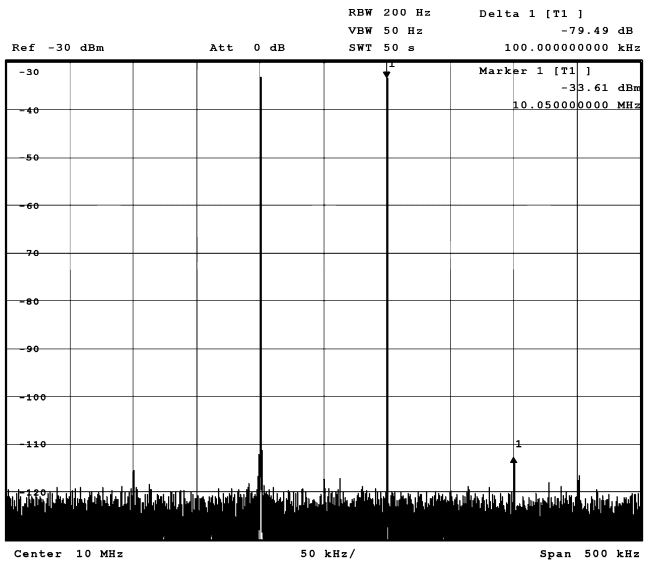

Fig. 11. Experimental IM3 measurement for a single transconductor. The intermodulation component is at −79.49 dB for a 2-$V_{\rm PP}$ input signal. The input test tones are at 9.95 and 10.05 MHz.

TABLE II
TRANSISTOR ASPECT RATIOS AND BIAS SETTINGS FOR THE TRANSCONDUCTOR

Transistor	W/L (μm/μm)	Bias condition	
M1	392.4 / 1.2	I_B	1 mA
M2	302.4 / 1.2	V_{DD}	5 V
M_{C3}, M_{C4}	781.2 / 1.2	V_{CN2}	2.2 V
M_{CN},M_{CN2}, M_{C1}	302.4 / 1.2	V_{CN}	1.7 V
M_{B3}, M_{B4}	781.2 / 1.2	V_{CP}	3.2 V
M_{B1}, M_{B2}	262.8 / 1.2	V_{icm}	1.8 V
M_{P1}	22.5 / 1.2	$2R$	3.0 kΩ

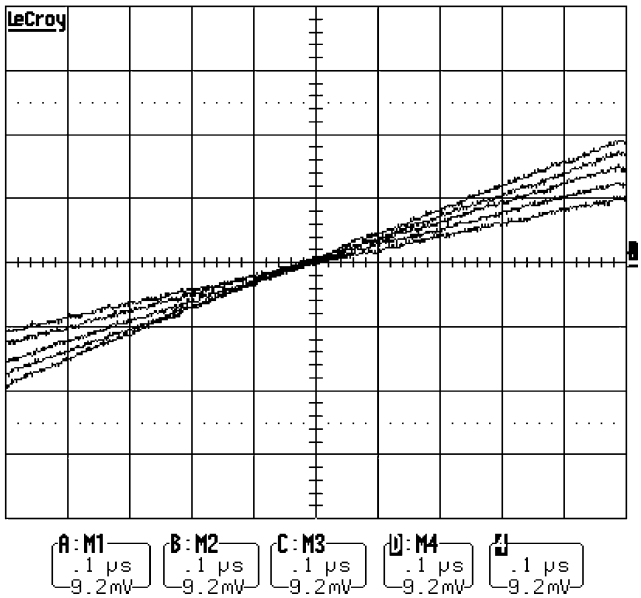

Fig. 12. Measured dc characteristics of the transconductor.

generated from a single-ended signal by means of an off-chip transformer, and the differential output voltage was converted to a single-ended signal by another transformer.

A. Transconductor Measurement Results

The transconductor was tested with a bias current of 1 mA and a 5-V supply voltage. The transistor dimensions and the bias condition are listed in Table II. The spectrum of the output signal of the nominal transconductor for a differential two-tone input signal at 9.95 and 10.05 MHz, with a 2-V peak-to-peak input amplitude is shown in Fig. 11. The measured IM3 is better than −79 dB. For a two-tone input around 1 MHz, the results were similar. The performance of the circuit is not significantly affected by the increase in frequency, and IM3 is almost constant up to 10 MHz.

In Fig. 12, the dc transfer characteristics of the transconductor for different programming voltages $V_{\rm prog}$ are shown. They have been obtained by applying a very low frequency triangular input. The tuning capability of the circuit can be noticed. The transconductance can be reduced to 50%.

The simulated transconductance G_m is shown in Fig. 13, showing the linear range. It can be seen that a linear behavior is obtained for a large differential input-signal range of approximately 2.8 V. Transconductance goes approximately from a maximum value of 660 μA/V to 330 μA/V. Measurements confirm that the transconductance tuning range covers an octave; thus, this range is in good agreement. The measured transconductance values match reasonably with simulations, within the expected tolerance limits of the polysilicon resistance in the technology.

B. Filter Measurement Results

The *Gm-C* filter was measured with the same test setup as the transconductor. In Figs. 14 and 15, the measured filter magnitude and phase responses are shown, respectively, evidencing the one-octave tuning capability. The −3-dB cutoff frequency range goes from 12 to 6 MHz. The attenuation in the passband is due to the transformer used for differential-to-single-ended conversion in the external setup.

In Fig. 16, the filter output spectrum using a 2-V peak-to-peak input signal with two tones of 9.9 and 10 MHz is shown. The measured IM3 is −78.08 dB. The filter IM3 was measured at several frequencies with an input signal of 2 $V_{\rm pp}$, remaining almost constant in the entire passband, e.g., it was −78.3 dB (just 0.22 dB better) at 1 MHz. Fig. 17 shows the measured IM3

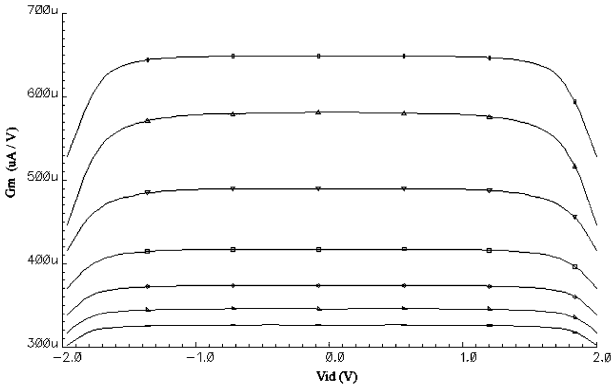

Fig. 13. G_m variation of the proposed transconductor.

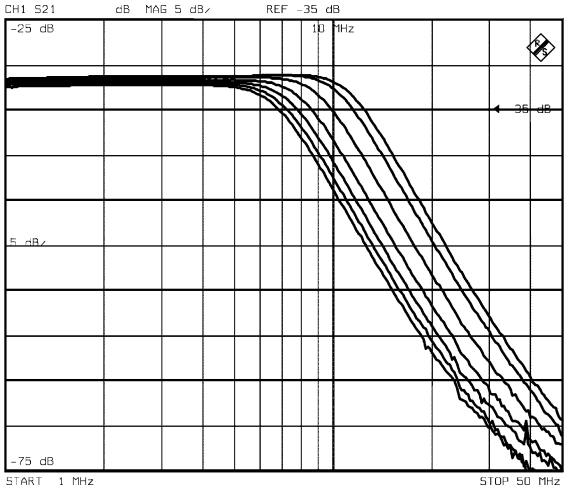

Fig. 14. Measured filter magnitude response.

Fig. 15. Measured filter phase response.

versus the tuning voltage ($V_{\rm prog}$), showing the slight loss of linearity with the programmability. It can be noticed that IM3 is better than −67 dB in the whole tuning range. This measurement was made with a 2-$V_{\rm pp}$ input-signal amplitude of two

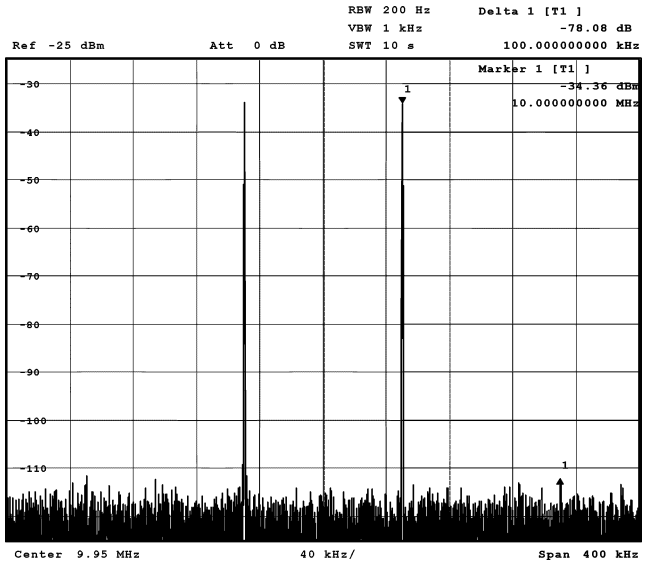

Fig. 16. IM3 measurement for the filter. The intermodulation component is at −78.08 dB for a 2- $V_{\rm pp}$ input. Input test tones are at 9.9 and 10 MHz.

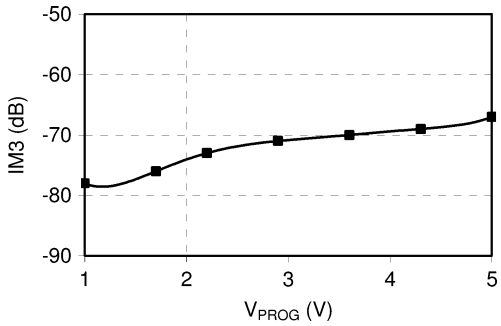

Fig. 17. Measured IM3 versus tuning voltage.

tones near the cutoff frequency for each programmed value of such frequency.

Table III summarizes the measured performance for the filter and the transconductor. The value obtained from (17) for the SNR of the transconductor for a 2-$V_{\rm pp}$ input is 76.1 dB. This is only an approximate value obtained by hand analysis and using the MOS square law to estimate the transconductance values from the dimensions and bias currents of Table II and neglects flicker noise. As shown in Table III, the measured SNR for the complete filter is 70.1 dB. The simulated SNR is 72.2 dB. The difference is attributed to the additional external noise from the test setup. Note that the target SNR of Table I is not achieved. To solve it, from (17), decreasing the g_m of the current sources would help, but then, the increase of the overdrive voltage $V_{\rm GS}-V_{\rm TH}$ required would reduce the output swing. Hence, a proper tradeoff between noise reduction and output swing is required. Additionally, the gain of the preamplifier stage of the filter could be slightly increased, thus relaxing the SNR requirements of the filter at the expense of a slight increase in filter linearity requirements.

Table IV shows a comparison between the proposed *Gm-C* tunable filter and the previously reported ones. Only *Gm-C* filters achieving IM3 better than −60 dB are included. As indicated in the table, the topology of the transconductors used

TABLE IV
COMPARISON WITH OTHER HIGHLY LINEAR *GM-C* FILTERS

Reference	Transconductor				Filter					
	Type	Voltage Follower	Current Follower	Tuning	Technol.	Order	Supply (Volts)	Filter IM3 (@Vin @freq.)	Power /pole (mW)	Area (mm^2)
Willinghan 1993 [7]	Fig. 2(a)	Fig. 3(c)	Current Mirror	Fig. 5(b)	BiCMOS 2μm	7	10	-72 dB (10 Vpp @1MHz)	157	25.8
Chang 1997 [8]	Fig. 2(a)	Fig. 3(b)	Regulated Cascode	Fig. 5(c)	CMOS 0.7μm	14	5	-61 dB (4 Vpp @0.6MHz)	5	4.8
J.-Y. Lee 2000 [9]	Fig. 2(a)	Fig. 3(c)	Current Mirror	Current division	CMOS 0.35μm	3	3.3	-63 dB (2 Vpp @0.3MHz)	22	0.69
Lewinski 2004 [10]	Fig. 2(d)	Fig. 3(a)	Regulated Cascode	Fig. 5(c)	CMOS 0.35μm	2	3.3	-68 dB (1.3 Vpp @20MHz)	26	0.45
Mensink 1997 [11]	Fig. 2(a)	Fig. 3(a)	Folded Cascode	Fig. 5(a)	CMOS 0.5μm	3	3.3	-60dB (1 Vpp @1MHz)	4	0.15
Chen 2006 [5]	Fig. 2(d)	Fig. 3(a)	Folded Cascode	Fig. 5(c)	CMOS 0.5μm	3	3.3	-65 dB (1 Vpp @20MHz)	9.4	0.46
Huang 2006 [12]	Fig. 2(a)	Fig. 3(a) Adapt. bias	Regulated Cascode	Fig. 5(c)	CMOS 0.35μm	2	3.3	-65 dB (1.4 Vpp @26MHz)	17	0.23
Lewinski 2007 [13]	Fig. 2(a)	Fig. 3(a) W. aux. DP	No	Discrete 4 -bit	CMOS 0.35μm	2	3.3	-75 dB (1 Vpp @20MHz)	17	0.45
This Work 2008	Fig. 2(a)	Fig. 3(e)	Folded Cascode	Fig. 6(b)	CMOS 0.5μm	3	5	-78 dB (2 Vpp @10MHz)	60	1.5

TABLE III
SUMMARY OF EXPERIMENTAL RESULTS

Technology	0.5μm CMOS
Power Supply	5 V
Transconductor	
IM3 @ 10MHz, 2Vpp	-79.49 dB
G_m tuning range	660 – 330 μA/V
Power consumption	30 mW
Die area	$0.18mm^2$
CMRR @ 1 MHz	61 dB
PSRR+ @ 1 MHz	62 dB
PSRR- @ 1 MHz	54 dB
Filter	
In-band IM3 (9.9 MHz&10MHz, 2Vpp)	-78.08 dB
Out-of-band IM3 (14 MHz&18MHz, 2Vpp)	-74 dB
In-band IIP3 @ 10MHz	33 dBm
Cutoff freq. range	6 MHz–12 MHz
Die area	$1.5mm^2$
CMRR @ 1 MHz	61 dB
PSRR+ @ 1 MHz	45 dB
PSRR- @ 1 MHz	45 dB
THD @ 1.5 MHz, 1V	-78.2 dB
Eq. input noise @ 1 MHz	64 nV/√Hz
Dynamic range @ 0.1% IM3, 12MHz BW	79.3 dB
SNR (12MHz BW)	70.1 dB

for the other filters can be derived from the general analysis of Section II. It can be noticed that the proposed filter compares favorably in terms of intermodulation distortion.

VI. DISCUSSION AND CONCLUSION

A general analysis of a class of highly linear *Gm-C* filters based on passive resistors has been presented. It has been shown that several of the highly linear transconductors proposed to date can be described from this framework. Based on such analysis, a simple and highly linear transconductor has been proposed. The circuit is nearly insensitive to transistor mismatch and includes a new and simple method for tuning the transconductance. Measurement results of the transconductor show an IM3 of −79.49 dB for a two-tone 2-V_{pp} input signal at 10 MHz. As an application example, a third-order *Gm-C* low-pass filter with frequency tuning has been presented. The filter is a practical demonstration that *Gm-C* filters with linearity performance comparable to active RC implementations can be achieved.

A supply voltage of 5 V was used to maximize the input and tuning ranges as the circuit can operate reliably at 5 V in this technology and power consumption in our application (VDSL analog front end) is not critical. However, lower supply voltages can be employed. The minimum supply requirements of the filter are $|V_{GS}| + 4|V_{DS,sat}|$ (approximately 1.5 V in our technology) but, in this extreme case, there is no headroom for the input swing (13), and the tuning range is very limited. We have recently resized and fabricated the transconductor and filter for a DVB-H receiver using the same technology. Measurement results show that the good features of the circuit can also be achieved in this case, with a measured filter IM3 of −72.1 dB for two input tones of 1 V_{pp} at 950 and 1050 kHz, with a supply voltage of 3.3 V, a cutoff frequency of 4.1 MHz, and a power consumption of 1.6 mW/pole (i.e., 37.5 times smaller than for the filter version presented in this paper).

The transconductor can be readily translated to more advanced technologies since it is inherently robust against second-order effects, as $V-I$ conversion is achieved in a passive resistor to which input voltage is translated using high-gain local feedback loops. Second-order effects in modern technologies (particularly short-channel effects) mainly affect transistors. Since the passive resistor still has similar performance in these technologies and provided that gain of the feedback loops employed is high enough, performance degradation in deep submicrometer technologies is modest. This is

in contrast to other techniques for designing transconductors which rely on the cancellation of nonlinear terms and thus rely on a certain nonlinear behavior of the transistor (usually compliance to an $I-V$ square law). In this latter case, the impact of gate length scaling in modern technologies is critical.

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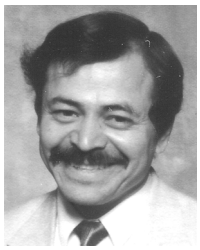

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