Reliability Characteristics of W–La_2O_3 Structures Compared with those of HfO_2-Based Gate Oxides

J. Molina, F.J. De La Hidalga, P. Rosales, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori and H. Iwai

***Abstract* – In this paper, we report and compare the reliability results obtained for W–La_2O_3 gated Metal-Oxide-Semiconductor (MOS) devices with those of HfO_2–based systems reported in literature. Reliability issues like stress-induced leakage current (SILC), interface-states generation (Dit), threshold voltage shift (ΔVth) and time to breakdown (t_{bd}) were compared and analyzed for both dielectrics in order to obtain a more specific assessment of their resistance to electrical degradation and breakdown.**

I. Introduction

In the last years, the research of high-k materials for ultra-large-scale integration devices below 100 nm has been mainly focused on the Hf-based oxides because of their high thermal stability when deposited on silicon substrates, high values of relative dielectric constant for near-stoichiometric HfO_2 and also for Hf-silicates, high conduction and valence band offsets to silicon, etc. All of these properties have resulted in very good performance of the transistors fabricated with these dielectric materials: reduction of gate leakage current for low equivalent oxide thickness regime (EOT<1nm), high carrier channel mobility, low Vth, etc. Nonetheless, the reliability evaluation of Hf-based oxides (mainly HfO_2, HfSiN, HfSiON) has produced a wide span of reliability results that although consistent, have demonstrated that these dielectrics present serious reliability issues related to their degradation when subjected to electrical stress. In the best scenario, a broad look into some of the main reliability results presented in literature for Hf-based oxides has helped to identify what are its main weak and strong points related to the degradation and breakdown of these dielectric materials. In this paper, we compare some of the results for Hf-based oxides published in literature with those obtained by our La_2O_3-gated MOS devices.

II. Experimental

MOS capacitors and transistors were fabricated on n-type (100) oriented silicon wafers with resistivity of 1–5 Ω·cm. Thin films of La_2O_3 were deposited on HF-last or hydrogen-terminated n-type silicon substrates by electron-beam evaporation using molecular beam epitaxy (MBE) system (Anelva I) at 300°C. The pressure in the chamber during the deposition was around $1x10^{-7}$ Pa. Also, in-situ sputtering of tungsten was done at 150W rf power in a contiguous chamber immediately after the dielectric deposition in order to avoid exposure of La_2O_3 surface to the environment. Because of this, the physical thickness of La_2O_3 cannot be measured by ellipsometry but by transmission electron microscopy. During the deposition of the metal, an argon flow of 1.33 Pa was used. Patterning of the gate electrodes was done by reactive-ion etching using SF_6 gas with a 30W power. Finally, post-metallization annealing (PMA) was done in dry N_2 ambient at 500°C for 5 min. For all the La_2O_3 samples, current-voltage and time-dependent dielectric breakdown (TDDB) characteristics were obtained with a semiconductor parameter analyzer (Agilent 4156C). La_2O_3 film thicknesses with EOT= 1.5 to 1.6 nm (after PMA) were obtained and compared in terms of its reliability characteristics with respect to several Hf-based oxide systems reported in literature.

III. Results and Discussion

Initially, the PMA annealing of La_2O_3 films reduces this high-k insulator to a La-silicate film interfaced to a SiO_2-based interfacial layer (IL) underneath [1]. Thus, the final stacked structure is of the $LaSi_xO_y$-SiO_2-Si type, which in turn, increases the final EOT but enhances its final electrical characteristics as well. On the other hand, the introduction of a more chemically inert metal like tungsten as gate electrode can improve some electrical characteristics of the MOS devices by reducing the formation of an IL between La_2O_3 and the metal itself. Also, the final thermal treatments applied to an already metallized La_2O_3-gated MOS device will have several effects on its physical and electrical characteristics [2]. In this respect, the introduction of PMA compared to annealing before metallization (PDA or post-deposition annealing) for tungsten-gated La_2O_3 MIS devices, has resulted in better electrical characteristics both in terms of chemical stability and reliability.

In the following paragraphs, reliability results for Hf-based oxides will be presented along with the results obtained for our La-based oxide systems. Figure 1(a), shows the SILC degradation for an HfO_2 oxide [3] with similar EOT to our deposited La_2O_3 film after PMA. Of course, several other references can be compared to our La_2O_3 in order to observe the general trend of SILC behavior for all these films (check for instance, references [4] and [5]). We can see from fig. 1(a) that after only one

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second of constant voltage stress with CVS= 3.6 V, the leakage current for this particular sample has dramatically increased when compared to its original or fresh state.

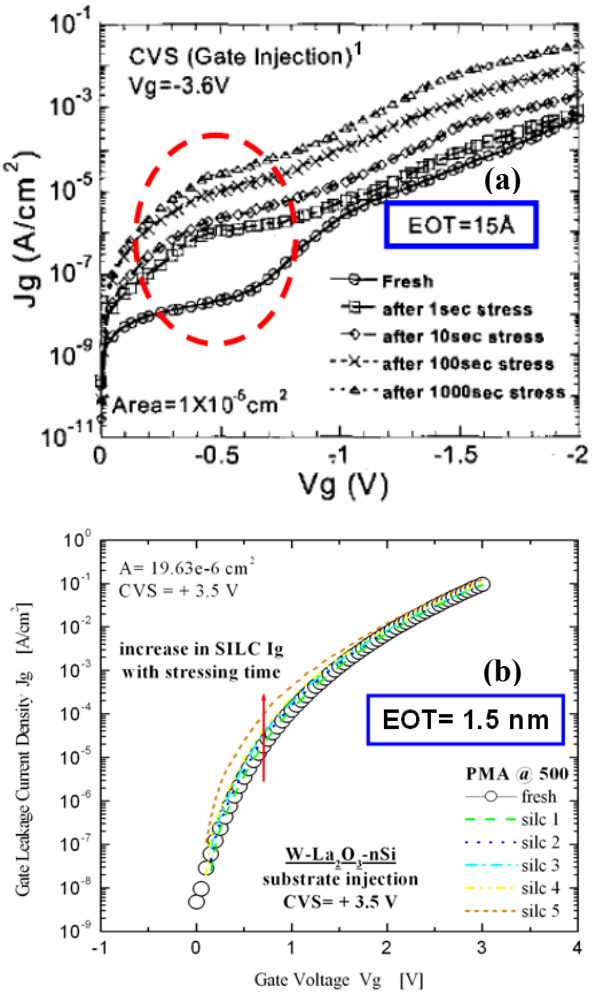

Fig. 1. (a) **HfO_2**.- SILC degradation for HfO_2 with EOT= 1.5 nm. SILC increases dramatically even after the first seconds of CVS applied to the sample [3].
(b) **La_2O_3**.- SILC degradation for La_2O_3-based oxide with EOT= 1.5 nm. SILC increases monotonically with a CVS= 3.5 V with a stressing time up to 1000 sec.

On the other hand, fig. 1(b) shows that the increase in SILC after CVS is less abrupt for La_2O_3 under the same stressing conditions and with the same EOT. By comparing SILC of MOS devices with similar EOT, less degradation in gate leakage current after stress is found for La_2O_3-gated MOSCAP compared to HfO_2. Also, by considering other results in the literature with closely similar EOT for HfO_2-gated devices, the exponential increase in SILC degradation can be clearly observed [4] and [5].

Similarly, the increase in the density of interface-states generation D_{it} for HfO_2-based systems after stress shows an exponential increase with respect to a La_2O_3-based system. In fig. 2(a), the exponential increase in D_{it} after stress is clearly observed even for samples annealed after relatively high forming gas PMA temperatures [5]. Even though La_2O_3 presents an initially higher density of interface–states D_{it}, see fig. 2(b), additional generation of D_{it} during stress is lower compared to HfO_2. This general trend for HfO_2 can also be compared in reference [6]. Dit comparison for both oxides is shown next.

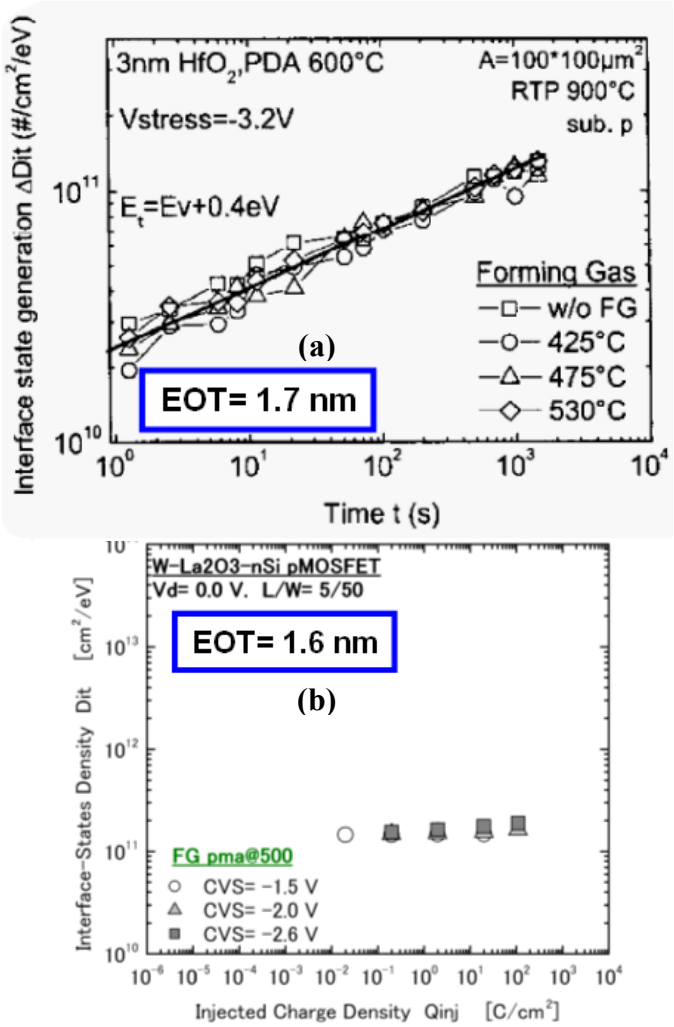

Fig. 2. (a) **HfO_2**.- D_{it} generation for HfO_2 with EOT= 1.7 nm. Exponential increase in D_{it} is observed for HfO_2 even after high temperature forming gas annealing [5].
(b) **La_2O_3**.- D_{it} generation for La_2O_3-based oxide with EOT= 1.6 nm. Even though the initial Dit generation is relatively higher, additional Dit generation is rather slow.

From figures 2(a) and 3(a), we can see that there is both exponential D_{it} generation and exponential threshold voltage Vth shift during the stressing of Hf-based oxides on silicon. Both of these degradation effects are worsened (higher D_{it} generation and higher Vth shift are observed) with stress, temperature, quality of the interface between the Hf-based oxide and the silicon underneath as well as with the scalability of the oxide under evaluation. One of the reliability factors that severely degrade and compromise the stability of Hf-based MOSFET devices is the large Vth shift that occurs from severe charge trapping during both positive and negative bias applied to the gate of these devices. From the corresponding figures, we can see that Hf-based oxides compromise the long-term stability of the MOSFET device by increasing the voltage necessary for channel inversion and thus, directly increasing the gate leakage current as well. All of these

effects result in undesirable higher power dissipation which worsens for the ultra-thin oxide regime [7].

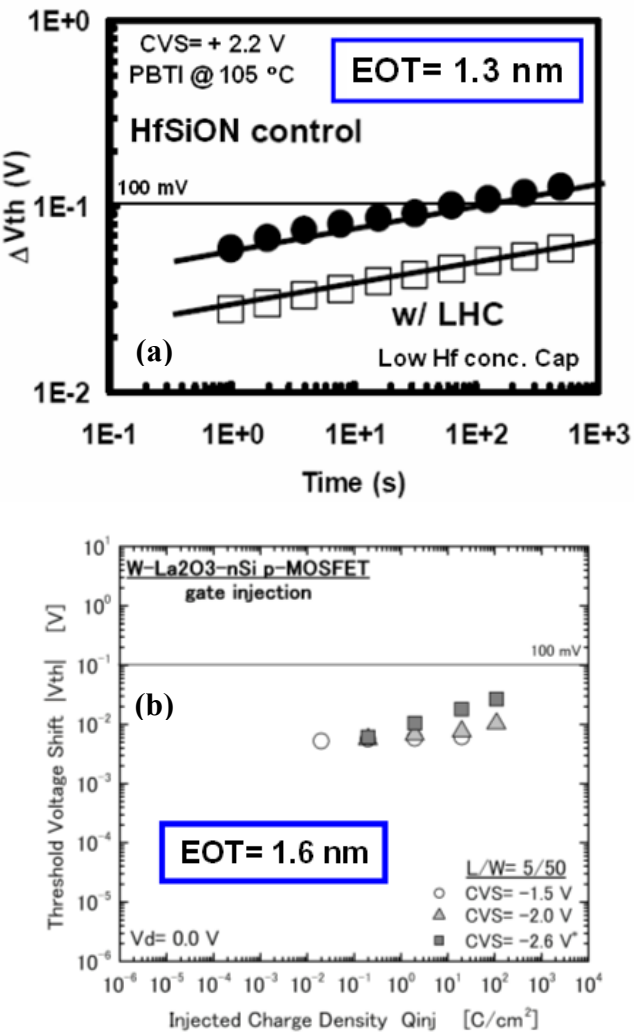

Fig. 3. (a) **HfO_2**.- Vth shift characteristic of HfSiON-gated MOSFET devices with EOT= 1.3 nm. Exponential increase in Vth is observed for both samples [7].
(b) **La_2O_3**.- Vth shift of La_2O_3-based oxide with EOT= 1.6 nm. Exponential increase in Vth after stress is observed after high-stressing conditions are reached.

From fig. 3(a) we can observe a dramatic increase in Vth after stress for a relatively thin dielectric film (EOT= 1.3 nm) which is subjected to both high electrical and temperature stressing conditions. Scaling of these oxides' thickness down to the very low regime (EOT< 1nm) will surely pose a serious limit with respect to the stability of the MOSFET devices fabricated. Exponential increase in Vth after stress can also be found for the HfSiON-SiO_2 stacked structure shown in reference [8], which shows an EOT= 1.6 nm, similar to our La_2O_3-gated MOS devices.

On the other hand, figure 4(a) shows that by extrapolating time to breakdown t_{bd} data of HfO_2-gated oxides [3] and small area p-MOSFET devices [9], the continuous operation for both samples is guaranteed before the complete breakdown of the metal/high-k stack. It is interesting to note that by stressing very small area devices with higher temperature conditions, the lifetime is not severely shortened since fewer numbers of defects are expected when smaller area sizes are used.

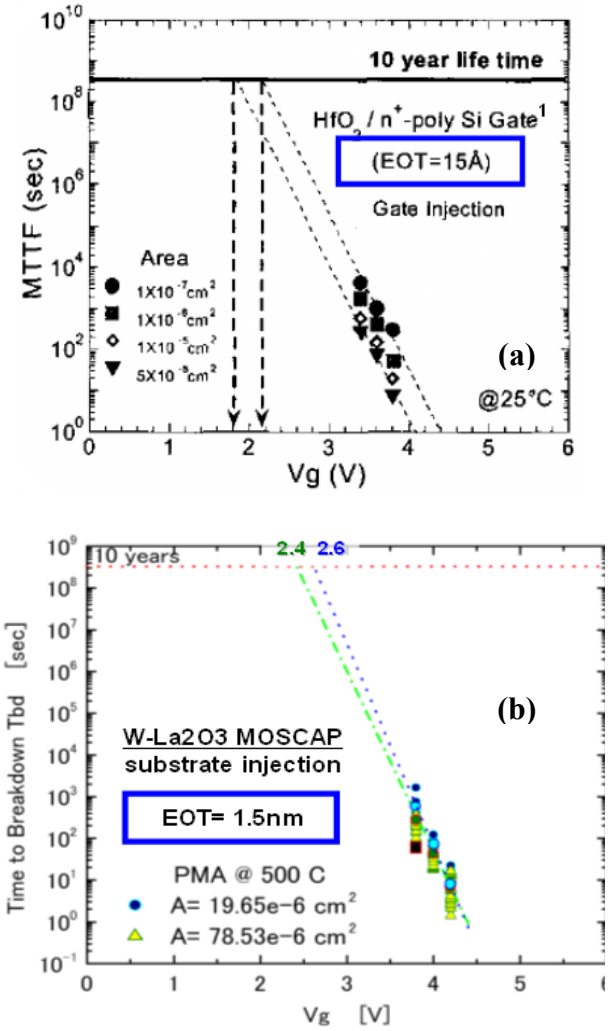

Fig. 4. (a) **HfO_2**.- Time to breakdown data for HfO_2-gated MOS devices with EOT= 1.5 nm. Smaller area capacitors show a slightly higher resistance to oxide breakdown [3].
(b) **La_2O_3**.- Time to breakdown data extrapolation for La_2O_3-gated MOS devices with EOT= 1.5 nm. Smaller area capacitors show a higher resistance to breakdown.

Similarly, time to breakdown data t_{bd} for La_2O_3-based oxides seems to be enhanced once the gate area is scaled down so that fatalistic breakdown for these thin films is reached after a relatively high gate voltage is applied, see figure 4(b). For both high-k oxides, a 10-year extrapolation of the time to breakdown data ensures the operation of MOSFETs gated with both dielectrics even if the Vg > 1 V. In the case of La_2O_3, slightly higher gate voltages (compared to those found for HfO_2 with same EOT [3]) can be applied before the final breakdown of the dielectric film. Nonetheless, degradation of the La_2O_3-based oxides before breakdown seems to worsen once the gate area of the MOS device under evaluation is reduced. [10]. This is important because even though smaller area devices produce longer lifetimes to breakdown during higher-voltage stressing conditions, see Fig. 4(b), the

stressing of W–La_2O_3 stacks during lower CVS (as compared to the CVS used for lifetime projection) does not breaks down the oxide but the damage induced in the dielectric results in an inversely proportional dependence of SILC increase with respect to gate area. This implies that even with long-lasting lifetimes for oxides with smaller areas, their electrical degradation before breakdown will ultimately impose a serious limit towards their use for smaller-area devices. Additionally, even though La_2O_3-based oxides presents better reliability properties compared to those presented for HfO_2-based oxides, the reliability characterization for La_2O_3 has been done only at room temperature. Therefore, reliability tests with small gate length MOSFETs at higher temperature are necessary in order to obtain hot-carrier injection reliability data for MOSFETs using this oxide.

IV. Conclusions

Even though HfO_2 has been implemented as the direct replacement to SiO_2 in order to overcome high leakage current in the ultra-thin regime, La_2O_3–gated MOS devices present better reliability characteristics which make it a serious candidate for the replacement of HfO_2 in future high-k based generation devices. Finally, even though La_2O_3-based smaller area devices produce longer lifetimes to breakdown during higher-voltage stressing conditions, the stressing with lower CVS does not breaks down the oxides but the damage induced in the dielectrics results in an inversely proportional dependence of SILC increase with respect to gate area. This will impose a serious barrier which must be overcome in order to use La_2O_3 materials for MOS devices with scaled-down areas. Surely enough, all these reliability problems for La_2O_3-based insulators will be solved by the time when the La_2O_3 is introduced into the commercial devices, as the case of Hf-based oxides.

Acknowledgements

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