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Modeling and Characterizing Interconnects for High-Speed Signaling Using Equivalent Circuit Representations

by

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Abstract

Nowadays, computational systems are demanding high performance operating frequencies with a high-density interconnect (HDI) scheme. As a result the impact of the common-mode noise present in these systems in the signal integrity has become a major concern. Differential interconnects have demonstrated to be a reliable solution due to its property of being less susceptible to this type of noise. Nevertheless, these interconnects consists of two signal traces to carry the data with an electromagnetic coupling between them. For this reason, studying the coupling between the signal traces is mandatory these days for optimizing the corresponding interconnects. Moreover, it is of great interest to study the coupling mechanisms between these two signal traces and how it can be modeled with lumped circuits. In this regard, the purpose of this thesis is to propose new methodologies to implement equivalent circuit models in commercial circuit simulators, with their corresponding parameters extraction processes for this interconnects. Consequently, a new topology for the characterization of a differential launch structure and the implementation of a model for the homogeneous part of a differential transmission line which considers the effect of the current distribution in the inductance of the line are presented as a result of this thesis.

Chip design as well as fabrication technologies have experienced a tremendous evolution in recent years allowing the transmission of data at very high data rates within the tens of Gbps. Thus, the losses associated to a transmission line are reaching unacceptable levels letting current high-speed electronic systems unable to handle higher frequencies signals, becoming these interconnects the bottleneck when designing high-speed interconnection channels. For this reason, electronic systems performance at high frequencies has to improve by identifying the effects that negatively influence the corresponding electrical performance. In order to this, equivalent circuit models for differential transmission lines used in complex devices such as HDI PCBs or packages can be used in the analysis to carry out an optimization of the interconnection channel.

Thus, within this project several prototypes were fabricated to carry out an exhaustive analysis of the coupling present in a differential line and how this will affect the signal integrity in a practical interconnection channel implemented in PCB technology. This analysis includes not only experimental studies of these structures, but also full-wave simulations of the 3D-models corresponding to these structures correlating both approaches. Furthermore, the proposal are validated in both the frequency and time domain to ensure the quality of the models.

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A mi esposa Carolina, sin ti este sueño no hubiese sido posible.

Contents

Preface

Current requirements for data processing have made the electronic systems to trend toward faster and higher density devices with lower operational voltages. In this regard, differential interconnections have become a reliable solution to deal with these difficulties. However, interconnection channels embedded in these structures are reaching its limits. In fact, as clock rates present in modern PCs continue to rise into the gigahertz range, data rates requirements are in the tens of gigabits per second. Thus, the levels of common-mode noise that become apparent at these frequencies need to be considered in the design of the interconnections. For this reason, the fabrication of differential interconnections capable to guide broadband signals without degrading the signal integrity to unacceptable levels is necessary.

This project started four years ago in the INAOE, and has motivated another two PhD dissertations in this area. Several techniques to represent and characterize differential interconnections have been studied and analyzed, allowing also proposing new methodologies with their corresponding parameter extraction processes for circuit-oriented modeling of these interconnections manufactured in PCB. In addition, as a result of this project two articles have been submitted to international refereed magazines and one more was presented in a prestigious conference related to the research area.

I have written this thesis under the genuine belief that it can serve as a guide for the implementation of reliable high-frequency differential interconnections models, but also to motivate continuing scientific research in the field of interconnections design in Mexico, which is one of the most important research areas in the world.

Miguel Angel Tlaxcalteco Matus

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Chapter 1

Introduction

Current requirements for faster data processing have originated that high-speed interconnect phenomena that circuit designers historically have ignored begin to dominate performance, and unexpected problems arise that dramatically increase the complexity of the design. In this regard, reducing the parasitics associated with interconnects as well as using different signaling schemes for reducing the sensitivity to noise have been proposed for achieving these improvements. For this reason, the correct design of the transmission lines between the different input/outputs (I/Os) of the electronic systems results in accomplishing the signal integrity requirements and thus yielding higher data transmission rates.

For implementing high-performance electronic systems at a relatively low cost, printed-circuit-board (PCB) technology has been widely used in the electronics industry for many years. However, the ever increasing speed of the data processing introduces undesirable effects that degrade the integrity of the transmitted signals. Hence, in order to design optimal interconnects, it is very important to match the line impedances so that the insertion and return losses can be reduced. For this reason, much research has been carried out for systematically design interconnection channels while taking into consideration the aspects that allow the signal to be applied effectively; e.g., geometry, materials, isolation, etc. This suggests that the improvement of transmission line interconnects is an important field of opportunity for microwave engineers.

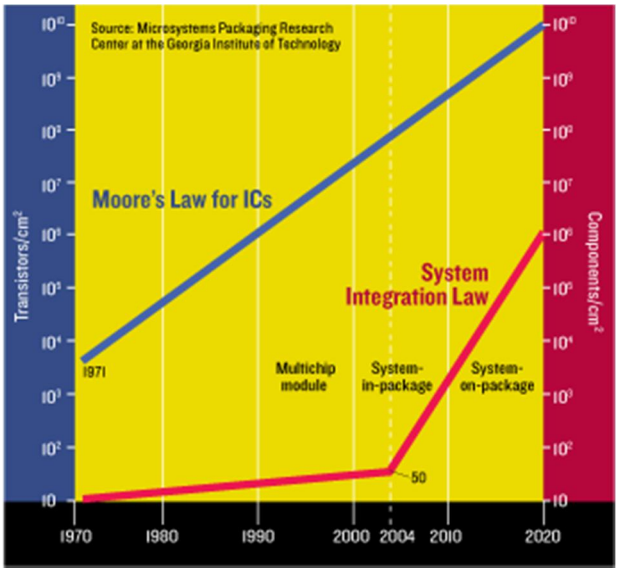


Fig. 1.1 Moore's Law predicting the number of transistors found in an IC [1].

As is well known, the number of transistors within an integrated circuit (IC) increases in accordance to Moore's Law [2], which is depicted in Fig. 1.1. Since this scaling prediction can also be extended to the speed of data processing, Moore's Law is commonly used to predict the bandwidth requirements for interconnects, which has recently reached the range of tens of gigahertz in computing applications. In this regard, until recently, interconnects used in ICs have provided adequate bandwidths for preserving the integrity of propagated signals. However, as the clock rates continue to rise within the microwave range, important problems are becoming apparent, such as distortion, resonances, crosstalk, and radiation. Furthermore, the complexity of the advanced structures and the increased density of the devices complicate the corresponding analysis as well as the design of communication channels within high-speed circuits. These are some reasons why the correct characterization and modeling of interconnects, when analyzed as transmission lines, present in current technologies become mandatory from a signal integrity point of view.

1.1 High-Frequency Interconnection Systems

In modern multilayer PCBs as in other technologies for integrating electronic systems, different types of interconnections are used. As can be seen in Fig. 1.2, three of the main types of interconnections are copper wiring, fiber-optic, and wireless communication systems [3-5]. These systems present several advantages and disadvantages depending on the requirements for a particular electronic device, as will be explained next.

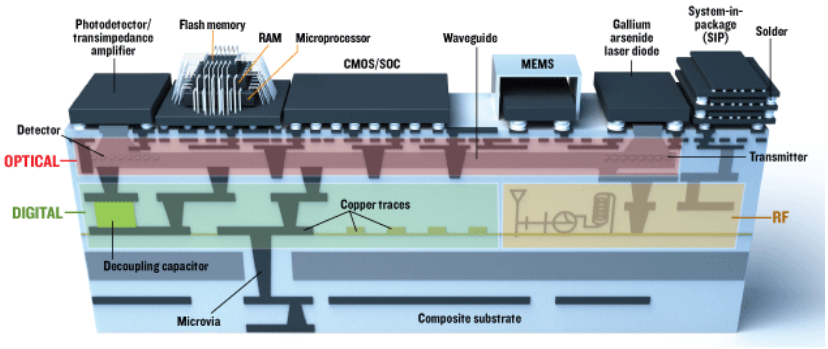


Fig. 1.2 Illustration of a system-on-package test bed that combines three types of circuits within its different layers [1].

When using optical fibers in a communication system, basically, it consists of modulate light beams and transmit these beams through the glass fiber. It possesses many benefits such as a high operating frequency within the range of hundreds of gigahertz, the immunity to electromagnetic interference and the low attenuation loss over long distances. Nevertheless, the main disadvantage of optical fibers is its high cost, especially for the

optical transmitters and receivers. In addition, the fabrication process that involves a fiber-optic communication system is not always compatible with IC fabrication processes. Hence, in spite of the many applications it has in modern communications systems, fiber-optic transmission is not commonly found in PCBs or ICs [6].

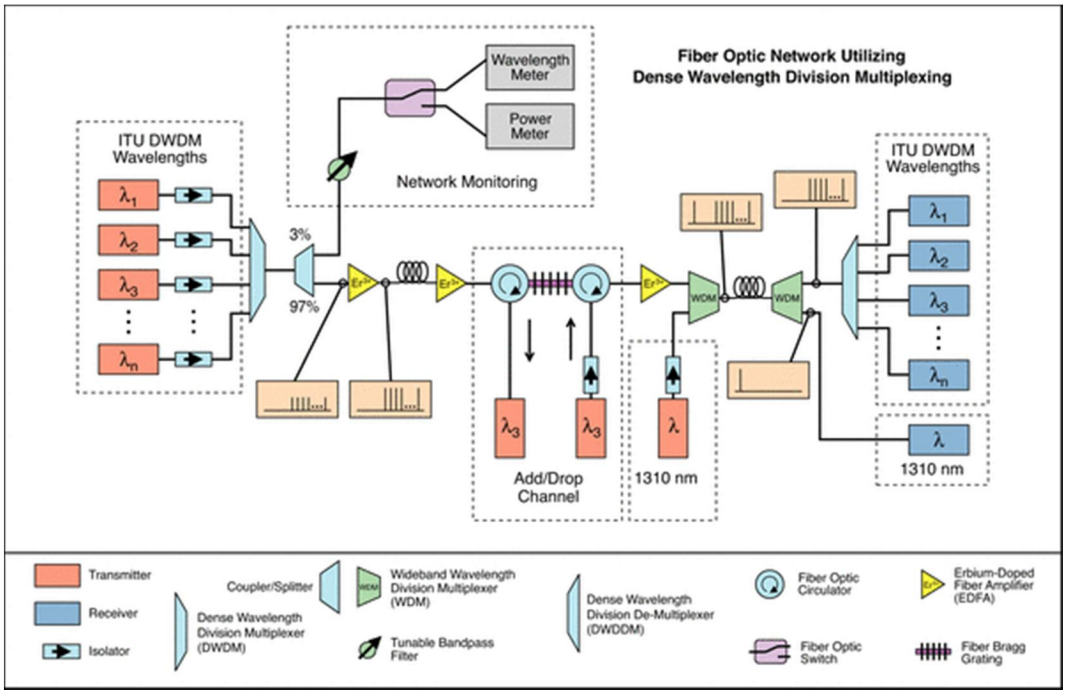


Fig. 1.3 Conceptual example of a fiber-optic network [7].

On the other hand, implementing a wireless communication system for this type of applications is simpler. It allows transferring information between two or more points without physical electrical conductors. This system uses radio waves to reach the destination point; nonetheless, in special cases other electromagnetic wireless technologies can be used (i.e. light, magnetic or electric fields and even sound). This technology has multiple applications nowadays such as: mobile telephony, wireless data communications (i.e. Wi-Fi, cellular data services, mobile satellite communications and wireless sensor networks), wireless energy transfer, wireless medical technologies and computer interface devices. The most obvious advantage of this systems is the flexibility it provides due to the lack of wires. In addition, it can be said that it is relatively easy to use and the cost of this technology is achievable. Nevertheless, these systems may find some compatibility issues, also in certain networks such as Ethernet, its performance is lower than that achieved using wires. Moreover, the main disadvantage is the challenge involved with privacy protection, since anyone within the coverage zone could try to penetrate the wireless network [8].

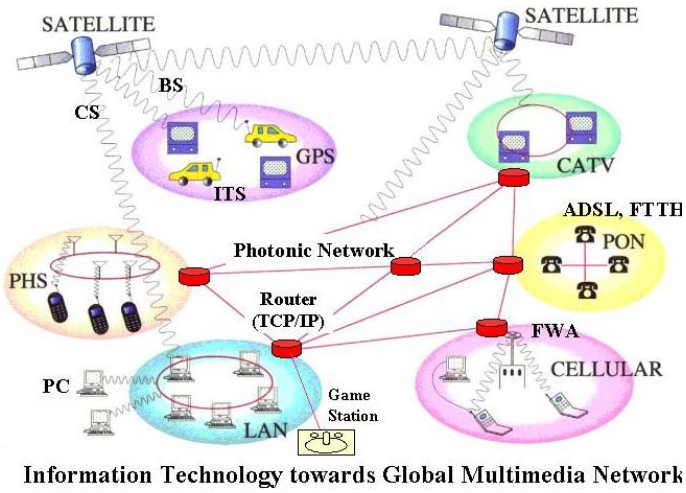


Fig. 1.4 Sketch of a wireless network connecting several electronic devices in current technologies [9].

Finally, cooper wiring is the simplest communication system involved in PCBs and ICs. It uses conductors of electric currents, mainly fabricated with cooper, to carry signals from one point to another. In this regard, other conductors used to interconnect two points in an electronic device includes: silver, aluminum, and gold. Using cooper wiring to make interconnections in a PCB leads to several drawbacks; for instance, it is susceptible to electromagnetic interference, its frequency operation range is not as high as that of the fiber-optic case, and it presents high losses at high frequencies, among other things. However, cooper wiring, or metallic wiring in general terms, possesses two main advantages: affordable cost and compatibility with the PCBs and ICs fabrication processes. In fact, this technology is the cheapest solution to implement a communication system, not only due to the low cost of cooper but also because the relatively low cost of the electronic circuitry used to implement receivers and transmitters. Furthermore, this system implementation is fully compatible with CMOS fabrication processes, which are the most used technology in the development of electronic devices. For these reasons, cooper wiring is the most used communication system implemented in the development of electronic circuits. Thus, although cooper wiring presents drawbacks regarding the considerably high metal losses at high frequencies, its advantages allow for its widespread use nowadays even in high-frequency advanced electronic devices when following a systematic and appropriate design. Thus, some approaches have emerged to minimize or at least to mitigate the effects of this technologies' drawbacks. In this regard, using different signaling schemes helps to reduce the impact of these drawbacks in the integrity of the transmitted signals. For instance, if the interconnect is designed for propagating differential signals, more robustness to crosstalk noise is achieved. For this reason, three of the most common wired high-frequency signaling schemes will be discussed in the next section.

1.2 High-Frequency Signaling Schemes

In order to transfer information from one output to an input between electronic stages, several signaling schemes can be used. Each scheme presents advantages and disadvantages related, for instance, to the number of signal traces used to carry the information or the level of shielding to noise. In this regard, the most common signaling schemes used in modern ICs are the single ended and the differential. In addition, eigenmodal signaling has emerged as a promising approach. At present, these three signaling schemes are the most representative to carry signals through transmission lines and will be discussed afterwards.

When the interconnections within a data bus are implemented with a dedicated transmission line for each signal path, the scheme is said to be single ended as can be seen in Fig. 1.3. This signaling scheme is the simplest way to transmit signals from one point to another inside the system. Typically, data buses designed using single-ended interconnects present a good performance for data rates up to approximately 1 to 2 Gbps [10]. However, as data rates increase, it becomes more difficult to maintain the signal integrity between the required tolerances since current digital systems are very noisy [11]. In fact, this scheme is severely affected by the simultaneous switching noise (SSN) caused by the I/O circuits used to drive digital information onto the bus [12]. Furthermore, there are many other sources of noise that can severely affect the integrity of the signals, such as crosstalk and the negative impact of non-ideal current return paths [10]. In case that the interconnection is intended for propagating single-ended signals, each data bit is transmitted on a single transmission line and latched into the receiver with the bus clock. The decision of whether the bit is a logic 0 or 1 is determined by comparing the received waveform to a reference voltage (v_{ref}). If the received waveform at certain time presents a voltage greater than v_{ref}, it results into a logic 1; otherwise, the result is a logic 0. Nevertheless, the noise that couples with the driver, receiver, transmission lines, reference planes, or clock circuits will degrade the transmitted waveform eventually introducing errors. Thus, if the magnitude of the noise is large enough, misinterpretation of the digital states will occur, resulting in bit errors. This is depicted at the bottom of Fig. 1.3.

A strategy used to reduce the effect of the coupled noise into the system is using two dedicated transmission lines for signal path on the bus. In this case, each transmission line must drive signals 180° out of phase between them. This is known as transmission in odd mode, and the difference between the voltages is used to recover the original signal by means of a differential amplifier. Thus, the misinterpretation of digital states due to noise present in single-ended signaling is minimized. This technique is called differential signaling and is depicted in Fig. 1.4.

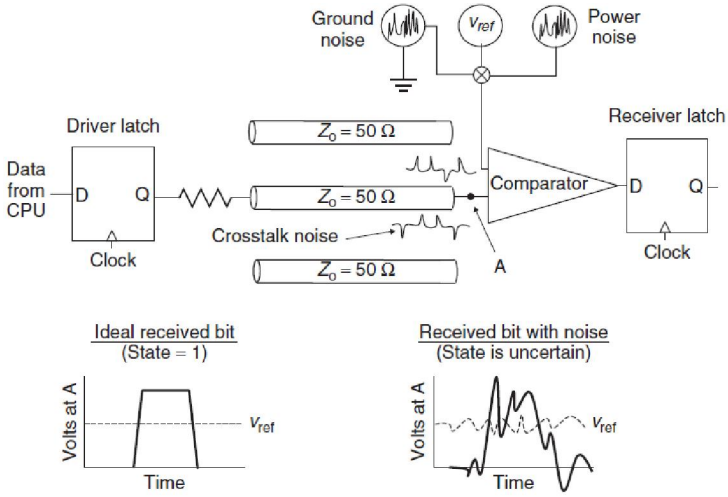


Fig. 1.3 How system noise can severely degrade the signal integrity on single-ended buses. The ideal versus noisy receiver voltages compared to the reference voltage [10].

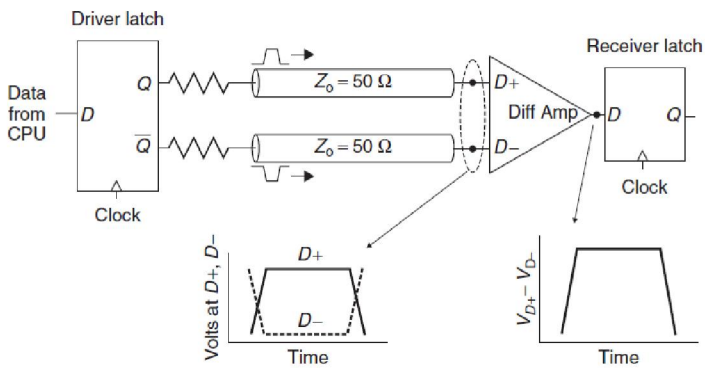


Fig. 1.4 Differential signaling where each bit is transmitted from the driver to a receiver using a pair of transmission lines driven in odd mode. The signal is recovered at the receiver with a differential amplifier [10].

Regarding the representation to allow the mathematical modeling, single and differential signaling can be defined as a two-line system by means of the even- and odd-mode signals. However, when the system has *n* coupled lines the concept of even- and odd-mode signals cannot be applied directly since this system can propagate *n* distinct modes. Thus, a modal analysis can be performed to analyze the behavior of the coupled system. Using the modal decomposition technique, it is possible to obtain the eigenvectors and eigenvalues of the system [10]. It is important to point out that the eigenvectors are orthogonal, so that the behavior of the coupled line system can be treated as a set of *n* isolated transmission lines. Once the system is decomposed, the modal voltages and currents can be computed for each line. This methodology is the basis of the eigenmodal transmission. In this case, the signal voltages are obtained with the modal analysis in such a way that the modes propagated by the transmission lines are orthogonal. Since the crosstalk between the transmission lines using this signaling scheme is avoided, this approach can be used in modern data buses like

PCI, USB and SATA. Furthermore, as a result of the lack of coupling between the signal traces, the spacing between the traces can be reduced and a higher interconnection density can be achieved. Despite this important benefit, the use of the eigenmodal transmission is not widely implemented in electronic devices due to the increment in the complexity of the design of the receivers and transmitters. In this regard, additionally to the common drivers used for the receiver and the transmitter, an encoder and a decoder are needed to achieve this transmission scheme. This is depicted in Fig. 1.5. The encoder converts the single-ended to eigenmodal signals to be transmitted through the transmission line system. Afterwards, the decoder converts back the eigenmodal to single-ended signals and completes the delivery to the receiver. Nevertheless, bear in mind that the transfer function used to encode the single-ended signals needs to be present in the decoder as well, so that the desired single-ended signals can be obtained at the receiver.

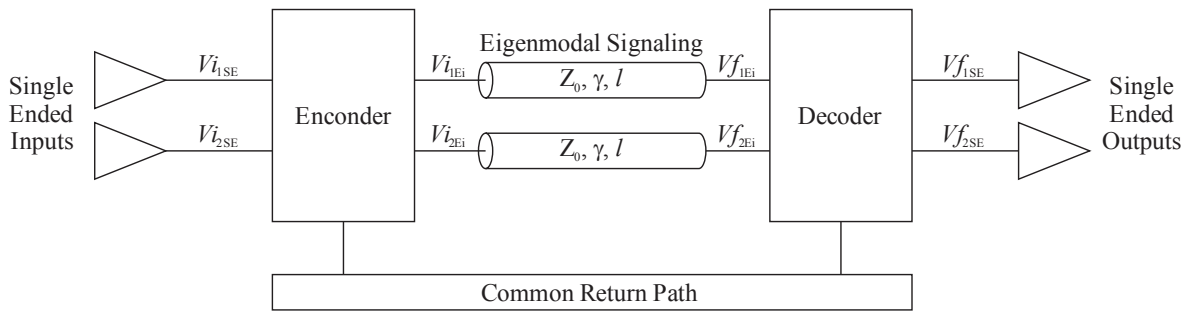


Fig. 1.5 Block diagram of a two-line signaling link exemplifying the eigenmodal signaling scheme concept [13].

In accordance to the advantages and disadvantages for each signaling scheme discussed in this section, it is possible to understand why the differential signaling is the most used signaling scheme in current electronic devices. This scheme presents a certain level of noise shielding without increasing very much the complexity of the design. Therefore, the study and analysis of differential interconnects continues being an important research area for signal integrity engineers.

1.3 Differential Interconnects

As mentioned above, differential interconnects are the standard for high-speed data buses. For this reason, this type of interconnects is commonly found in modern PCBs as in other advanced electronic devices. These interconnects are basically two transmission lines placed very close one from the other and exhibit coupling of signal energy. In spite of the associated increment of space, which is very valuable in advance designs, these interconnects allow to transmit signals at higher data rates with substantially reduced

common-mode noise. Therefore, these interconnects are extensively used in modern computers as a part of high-speed data buses. However, this is not the only electronic device using differential interconnects. These interconnects are also used for portable devices such as mobile phones, tablets and media players. Bear in mind, that most of these devices use USB ports, which is a differential bus. Moreover, recent televisions and video projectors present HDMI interfaces to transfer audio and video without uncompressing the data, so that the quality of the information is not affected. For the particular case of this interface, differential pairs are used to carry the signals from one point to another; this is shown in Fig. 1.6. Other differential buses include: the Serial Advanced Technology Attachment (SATA), used to connect mass storage devices such as hard disk and optical drives, the Peripheral Component Interconnect Express (PCIe), used to connect peripheral components in a computer, and the Intel QuickPath Interconnect (QPI), which is a point-to-point processor interconnect. In this regard, current differential buses manage data rates up to 8 Gbps (e.g., Intel QPI), whereas single-ended buses manage data rates up to 2 Gbps. Additionally, PCIe Generation 4 is estimated to reach data rates up to 16 Gbps. Thus, models for differential interconnects covering these frequency ranges are needed to allow the corresponding validation and characterization.

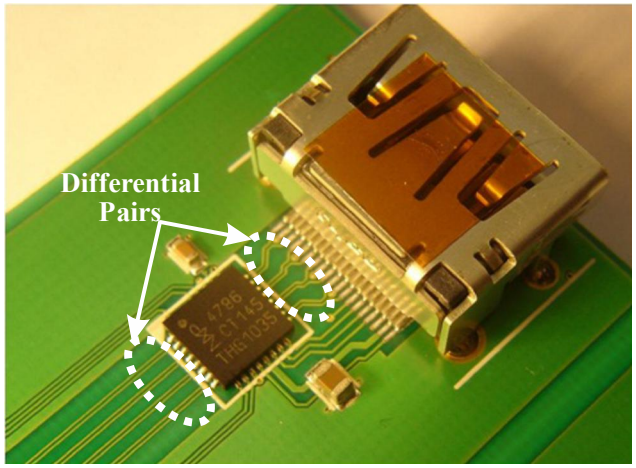


Fig. 1.6 Photograph of a PCB exhibiting a part of an HDMI bus using differential transmission line pairs [14].

In order to assess the performance of differential interconnects, the experimental *S*-parameters used for developing and implementing the corresponding models to evaluate these interconnects are measured using a four-port vector network analyzer (VNA) [15-16]. For this purpose, probing pads or coaxial connectors are typically used to launch and receive RF signals. In case that a differential device presents single-ended terminations at each one if its ports, the corresponding theory used for de-embedding and calibration can straightforwardly be applied to obtain the corrected differential *S*-parameters [16-17]. Unfortunately, single-ended lines of considerable length are required to connect the probing

pads to the differential device, increasing the area of the prototype and introducing parasitics that reduce the measurement certainty [18]. For this reason, the use of differential launch structures has emerged to overcome the drawbacks introduced by single-ended terminations. Photographs of these two types of terminations are shown in Fig. 1.7. This motivated the development of an analytical equivalent circuit model and parameter extraction methodology for a differential transition in this dissertation.

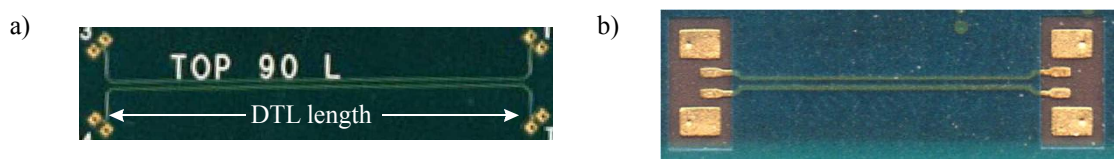


Fig. 1.7 Differential transmission line presenting a) ground-signal-ground (GSG) configured pad terminations, and b) GSSG configured pad terminations.

In addition to the modeling of differential transmission line terminations, the correct modeling of the transition-free sections of these lines is also of great importance to evaluate the performance of differential interconnection channels. Usually, the coupling between the two signal traces is represented with a set of inductance (L) and capacitance (C) matrices for an electrically short section. For instance, for a two-line system, the L and C matrices are:

$$L = \begin{bmatrix} L_{11} & L_{12} \\ L_{21} & L_{22} \end{bmatrix} \quad C = \begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{bmatrix} \tag{1.1}$$

where L_{11} and L_{22} are the self inductances of each single line per unit length, L_{12} and L_{21} are the mutual inductances between lines 1 and 2 per unit length. Analogously to the inductance, C_{11} and C_{22} are the capacitances of the lines and are defined as the capacitances to ground for each line plus the sum of the mutual capacitances (either C_{12} or C_{21}); mathematically, $C_{11} = C_{1G} + C_{12}$. The equivalent circuit to represent this concept is depicted in Fig. 1.8. In this case, most of the times the values for the elements in the L and C matrices are obtained using electromagnetic solvers. Even though the extraction of these elements using an electromagnetic solver may consider the corresponding frequency dependence, other effects such as the proximity and skin effect as well as the impact of the current distribution in the inductance of the lines are usually neglected. In fact, an inaccurate modeling of these elements would lead into an incorrect dispersion characterization resulting in a non-causal model. Therefore, in this dissertation, the development and parameter extraction of an *RLGC* model for a differential transmission line considering these effects will be presented.

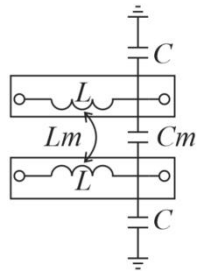


Fig. 1.8 Equivalent circuit used to represent an electrically short section of a differential transmission line pair neglecting the metal and dielectric losses.

1.4 Purpose of This Work

As discussed throughout this chapter, the advances in high-speed interconnects for implementing electronic systems are remarkable. For this reason, the aim of this work is contributing to the study of signal integrity issues presented on PCB through the analysis and modeling of differential transmission lines. This is supported with an exhaustive and systematic model-experiment correlation by means of a theoretical understanding of the physical phenomena occurring in these interconnects. Once this is achieved, an equivalent circuit model considering the operating mode for a differential launch structure as well as for the homogeneous part of the differential transmission line is proposed. The results of this project can be used for either designing, analyzing or optimizing a differential interconnect at microwave frequencies.

1.5 Description of this Document

This thesis is organized as follows. Chapter 2 presents a brief overview on the noise existing in modern complex electronic devices (i.e., packages and high-density interconnects PCB), and its coupling mechanisms. Chapter 2 also presents practical approaches to minimize the effect of the noise on the signal integrity such as using electromagnetic band-gaps structures or differential interconnects. Chapter 3 presents the electromagnetic modeling of differential transmission lines. In this chapter, the description of the methodologies employed in this work, and the analysis of the mixed-mode parameters transformation is detailed. Chapter 4 presents the comparison between experimental results and equivalent circuit modeling used in the proposal. Finally, chapter 5 presents general conclusions.

Chapter 2

Undesirable Coupling within a PCB

As the operation frequencies increase and the voltage of the signals decrease in high-speed digital systems, the degradation of signals due to electromagnetic noise becomes more significant. In this regard, PCBs are prone to the effect of several types of noise; some of them are: ground bounce noise (GBN), simultaneous switching noise (SSN), and noise originated by signals travelling through vias [19]. The latter is noise radiated by vias that propagates throughout the cavities formed by the power/ground planes, and it reaches the edges of the board, coupling to nearby structures resulting in electromagnetic interference (EMI) problems [20]. Therefore, a good understanding of these types of noise is essential to take action to preserve the signal integrity by reducing the risk of noise coupling to signal traces.

Fig. 2.1 shows a basic example of how SSN is coupled into a signal trace. Once the SSN is generated by the ICs switching at the top layer, this noise can travel to inner layers through the power/ground vias and be radiated into the cavities created between the power/ground planes. When SSN is present in the cavities of a multilayer system, a signal via can couple this noise into the signal, degrading its integrity. Moreover, a via can act as an antenna radiating and receiving signals, resulting in multimode propagation. As is well known, this multimode propagation affects considerably the signal integrity in a high-speed channel due to dispersion.

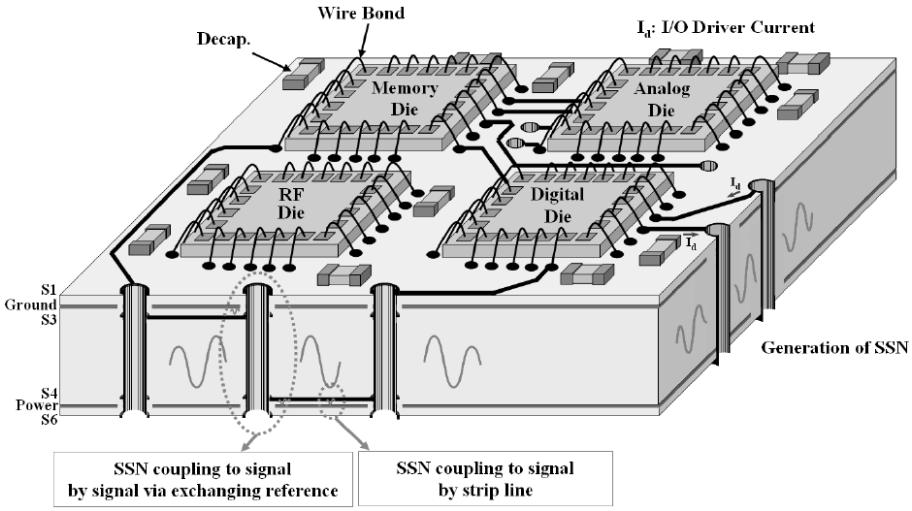


Fig. 2.1 SSN coupling into a signal via with reference plane exchange through a power/ground plane pair in an SoP [21].

The noise coupling mechanisms are thoroughly studied in high-speed interconnection design [21-23] and will be discussed in this chapter. Thus, a clear overview of the effects that may occur in complex transitions is provided. In addition, two approaches to deal with the coupling of noise to signal traces such as electromagnetic band-gap structures (EBGs) and differential signaling will also be discussed in this chapter.

2.1 Noise Originated in Via Transitions

Current advanced PCB and package structures are built in low-loss substrates to reduce the electric losses at high frequencies [24]. Unfortunately, low-loss dielectrics and parallel metal planes used as ground-planes for the interconnects form an ideal environment to develop via radiation, which is very common in packages [25]. Via radiation causes that part of the signal leaks away from the desired propagation path, originating a partial loss of the signal power. Fig. 2.2 shows this effect. In this case, the parasitic propagation is radial with a magnitude that decreases with the distance from the via. This effect is also common in PCB structures. For this reason, the analysis of this type of parasitic propagation is necessary to improve the performance of interconnects that may interact with noisy vias.

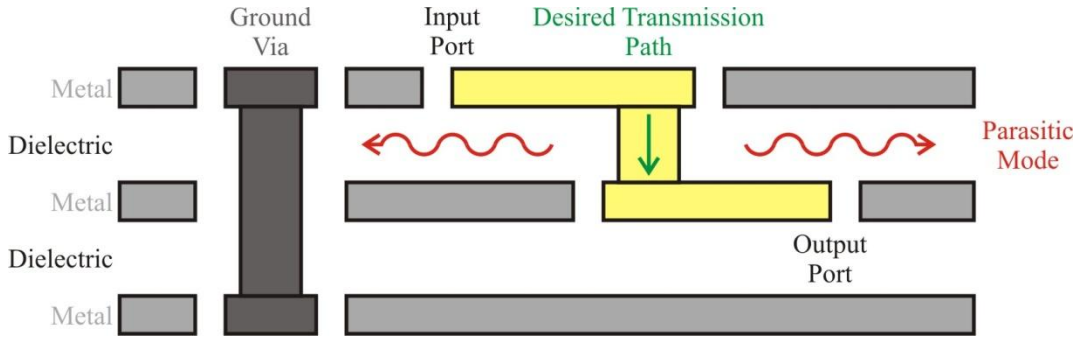


Fig. 2.2 Sketch of the side view of a package that conceptually illustrates the origin of the parallel plate mode (PPM) excitation.

Fig. 2.2 suggests that a via can be treated as an antenna element. In fact, since a radiating antenna can be seen as a device that converts electromagnetic waves traveling through a transmission line into waves radiated to free space [26], some similarities between a monopole antenna and a via embedded between multilayered substrates can be noticed. This concept is depicted in Fig. 2.3. For instance, in an interconnection channel a via may present a similar behavior when routing a signal through multilayer environments and radiation occurs. Furthermore, in many cases this structure can be modeled as a monopole antenna embedded within a dielectric substrate. Since antennas are inherently bi-directional, they can transmit and receive signals. Thus, at certain frequencies vias embedded in a substrate can be seen as antennas either propagating or coupling parasitic

modes, resulting in EMI problems for the interconnection channel due to the multimode propagation.

On the other hand, parasitic mode propagation caused by vias, may originate GBN or SSN within packages [27, 28]. For this reason, the proper design of vias and the corresponding environment is very important when optimizing packages. Furthermore, SSN and a high Q of the resonator formed between the parallel planes may yield resonances [28]. In general, these resonances are caused by the fact that the parasitics associated with a transition may behave as a reflective element (i.e., either an open or a short circuit). In this case, the transition can be seen as an energy-storage structure at given frequencies. In practical cases, the performance of packages may be severely degraded as a result of ring and cavity resonances [28]. Ring resonances occur when parallel plate modes are coupled with other structures at the edges of the package [29, 30], whereas cavity resonances occur when the package behaves as a rectangular cavity [31]. These resonances originate large spikes in the insertion-loss versus frequency curves, similar to those observed in the response of a notch filter (see Fig. 2.4). The presence of a second resonance is result of the propagation of higher order modes, which have a higher cutoff frequency that the principal mode of propagation. For this reason, the insertion loss is lower in the second resonance than in the first resonance. In particular, this second order effect causes huge damage to the performance of high-speed interconnection channels, and is considered one of the worst effects introduced by vias [32].

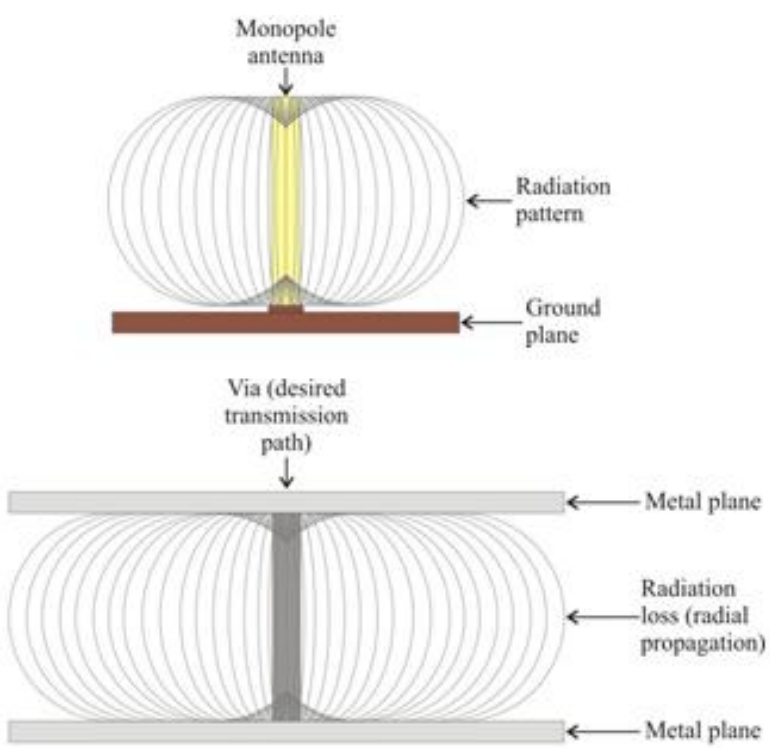


Fig. 2.3 Analogy between a monopole antenna and a via embedded in a substrate.

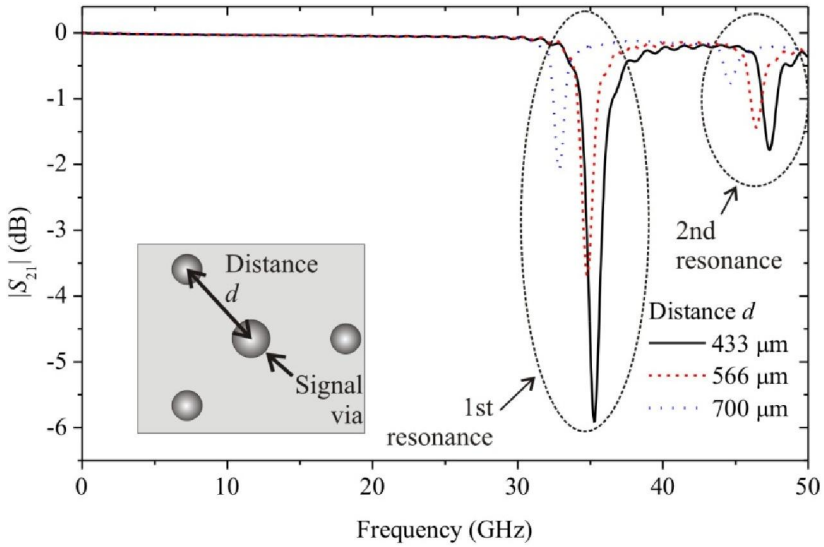


Fig. 2.4 Insertion loss versus frequency curves for a triangle configuration of vias, with a center-to-center distance between the signal and ground vias varying from 433 to 700 microns [32]. As can be seen, resonances occur at certain frequencies causing a loss in the transmission.

In accordance to the previous discussion, the systematic design of the electrical transitions plays a key role in achieving the desirable performance for an interconnection channel. So, different techniques can be used to reduce the impact of the unwanted effects introduced by vias; among these are [33, 34]:

- placing a bypass capacitor near the vias (see Fig. 2.5), trying to keep the capacitive coupling between all the reference planes, and maintain the high- frequency traces in the same plane;
- reducing the dielectric thickness so that the parasitic mode propagation occurs at frequencies outside the useful bandwidth, and
- using a proper configuration of the ground via array for maintaining the signal energy confined [32].

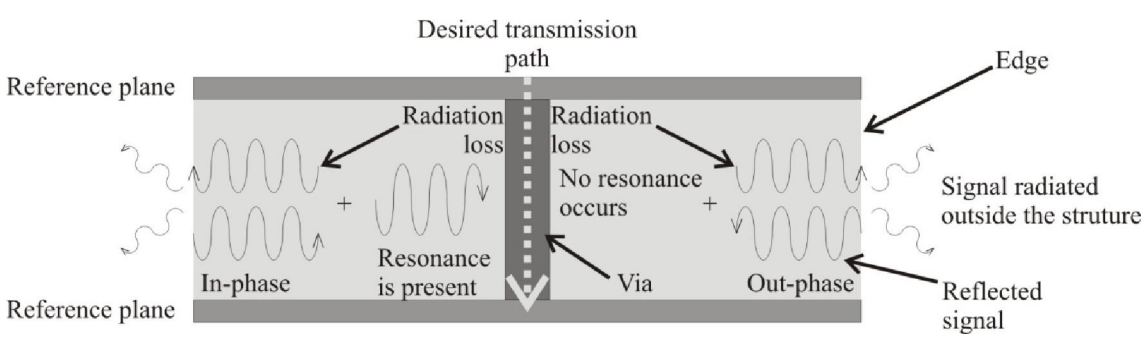


Fig. 2.4 Sketch illustrating the origin of resonances in a via in a multilayer structure. When the traveling signal due to radiation loss reaches the edge of the structure, part of the signal is radiated outside the structure whereas the other part is reflected back. If traveling and reflected signals are in-phase, the resonance is present in the transmission; on the other hand, if both are out of phase no resonances occur.

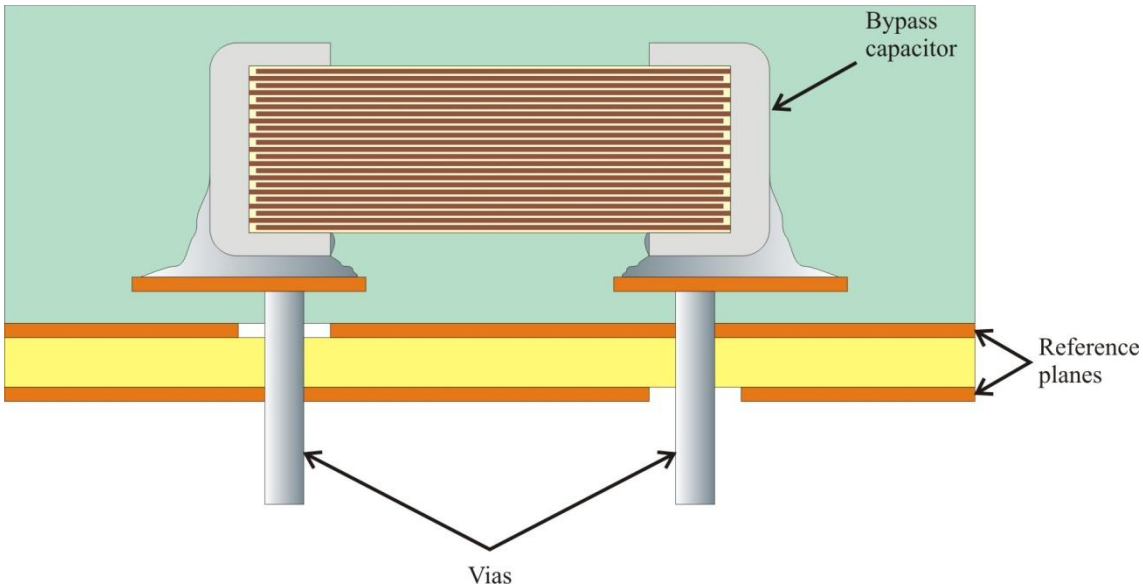


Fig. 2.5 Sketch of a bypass capacitor in the uppermost plane [34].

As mentioned through this section, vias can cause serious damages in the signal integrity especially when interact with SSN. For this reason, it is important to study the SSN origin and propagation.

2.2 Simultaneous Switching Noise (SSN)

When multiple drivers switch, charging and discharging currents occur within the power distribution network (PDN), a voltage drop is induced in the chip/package PDN. However, when pull-up and push-down devices simultaneously switch creating a direct path between the power and ground lines, the ground voltage raises momentarily. This apparent shift in the ground potential to a non-zero value is known as SSN or ground bounce [35]. Additionally, since a direct path for the current is created between power and ground, a short circuit may occur producing a catastrophic failure. SSN is typically very difficult to quantify since it depends on the operation of the IC as well as the geometry of the system [12]. A basic equation to model this noise is:

$$V_{SSN} = N L_{tot} \frac{dI}{dt} \tag{2.1}$$

where V_{SSN} is the SSN voltage, N is the number of drivers switching, L_{tot} is the equivalent inductance of the created current path, and I is the current per driver. Therefore, when a large number of signals switch at the same time, the power supply must be able to deliver enough current to satisfy the sudden demand. This current flows through a loop presenting an inductance L_{tot}, which is formed between the device ground and the system ground (see

Fig. 2.6). Therefore, the higher L_{tot} is, the higher the amplitude of noise will be. As a result, a noise V_{SSN} is induced onto the power supply and its effect is present at the driver output. This problem is significant when the ground bounce is present at the output buffers in a '1-0' transition. If the amplitude of the noise is higher than the voltage input low threshold (V_{IL}) at the driver's input, the glitch will be recognized as a valid logic '1'. The same case applies to a '0-1' transition; this is called as V_{CC} bounce. Nevertheless, ground bounce is considered more often in the electronic device design since the noise margin for the high logic state is more sensitive [35].

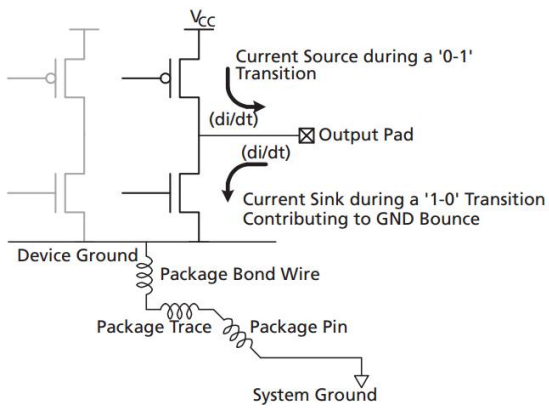


Fig. 2.6 A switching output buffer exhibiting a parasitic inductance L_{tot} [35]. In this particular case, L_{tot} is the sum of the parasitic inductances of the package bond wire, the package trace, and the package pin.

As mentioned before, SSN can be very difficult to characterize. A careful examination of the device as well as the power delivery system plus detailed simulations and measurements are necessary to get reasonable magnitudes of SSN. Fortunately, some approaches to model and analyze SSN are available in the literature [14, 36-38]. For instance, Fig. 2.7 shows a generic model that can be used to evaluate SSN in a CMOS bus. The capacitors, $C_{I/O}$, are the inherent on die-capacitance for each I/O cell. L_{chip} represents any inductance seen on the chip between the CMOS gate and the power bus. $L_{pwr\ bus}$ represents the inductance of the power distribution on the die and package. $L_{gnd\ bus}$ represents the series inductance of the ground distribution on the die and on the package. L_{vdd} and L_{gnd} pin represent the inductance of the power and ground pins on the package. $L_{PCB\ plane}$ represents the inductive path between the pin and the nearest decoupling capacitor. L_{cap} represents the series inductance of the decoupling capacitors, and C_{vdd} represents the board-level decoupling capacitors. Finally, L_{out} represents the series inductance of the package seen at the I/O outputs. It should be noted that all values for the mutual inductances should be included in this model. Furthermore, the number of gates simulated should equal the number of gates that share the same power and ground pins.

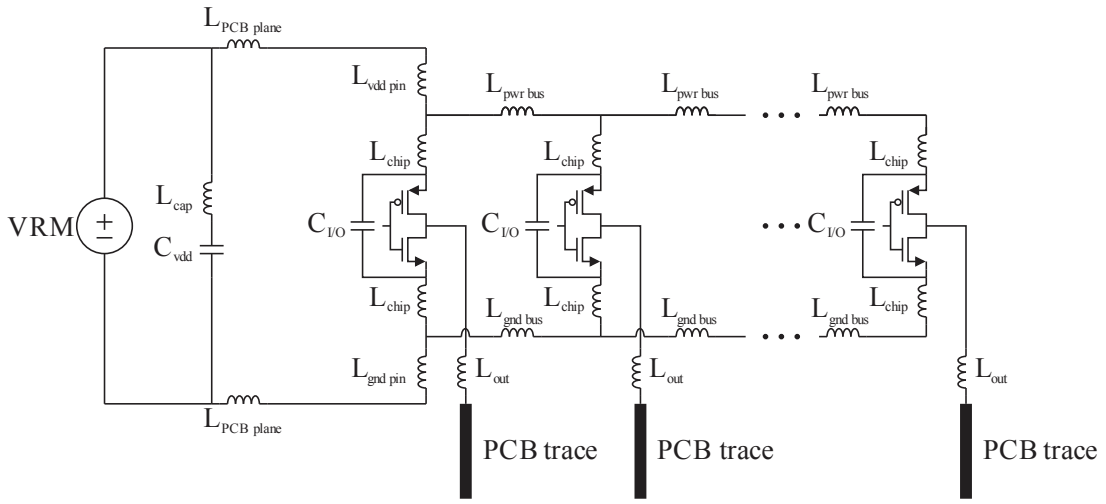


Fig. 2.7 Model used to evaluate component-level SSN for a CMOS-driven bus [14].

Some general rules can be used to reduce the effects of SSN [14]:

1. Using differential output drivers and receivers for critical signals such as strobes and clocks. A differential output consists of a pair of signals that are always switching opposite in phase (odd mode). A differential receiver is simply a circuit that triggers at the crossing of two signals. This will eliminate common-mode noise and increase the signal quality dramatically. Differentially routed transmission lines will also be less sensitive to noise and nonideal return paths because the odd mode sets up a virtual ground between the signals. It will also help even out the current drawn from the power supply.

2. Maximizing the on-die capacitance. This will provide a charge reservoir that is not isolated by inductance. If the on-die capacitance is large enough, it will act like a local battery and compensate for a sudden demand in current.

3. Keeping the decoupling components close to the critical areas. Use land-side or die-side capacitors, if possible. Place the board capacitors as close as possible to the power and ground pins.

4. Assigning I/O pins so there is minimum local bunching of output pins. Choose a pin-out that maximizes the coupling between signal and power/ground pins. Maximizing the number of power and ground pins. Place power and ground pins adjacent to each other. Since current flows in opposite directions in power and ground pins, the total inductance will be reduced by the mutual inductance.

5. Reducing the edge rates. This step must be carefully taken into account and a compromise must be done between speed and generation of EM emissions.

Slower edges are more susceptible to core noise. Laboratory measurements have shown that core noise can couple into the pre-driver circuitry during a rising or falling transition and cause jitter. The slower the transition, the more chance noise will be coupled onto the edge.

6. Provide separate power supplies for the core logic of a processor and the I/O. This will minimize the chance of SSN coupling into the core (or vice versa) and causing latches to switch state falsely.

As can be seen through the last two sections of this chapter, noise propagated by vias and SSN can impact severely the signal integrity. For this reason, some approaches have been developed to minimize the propagation or at least to control the coupling to signal traces of this effect. For instance, the use of complex structures such as electromagnetic bandgap structures (EBGs) or the usage of differential signaling are two of the most promising approaches to achieve this. These techniques will be discussed below.

2.3 Structures for Reducing EMI on PCB

As mentioned above, SSN has become a significant issue for high-speed electronic devices. As the data rates and the clock frequencies continue rising, the wideband suppression of power/ground noise coupling is required [39]. In this regard, EBGs have demonstrated to be an efficient solution for wideband power/ground noise suppression in multilayer packages and PCBs [40, 41]. Basically, an EBG structure is an artificial periodic object that prevents or assists the propagation of electromagnetic waves in a specified frequency band for all incident angles and all polarization states [42]. EBGs have several applications besides wideband power/ground noise suppression when considered as: photonic crystals, artificial magnetic conductors, frequency selective surfaces, and metamaterials. The simplest EBG structure is the so called “mushroom-like” structure [43]. This structure is shown in Fig. 2.8, and consists of a lattice of metal plates connected to a solid metal sheet by vertical conducting vias and it is particularly designed to suppress surface waves.

On the other hand, as mentioned in previous sections, noisy vias propagating SSN in a cavity formed by power/ground planes can lead into several signal integrity issues. Thus, a proposed solution is to place a ground via array surrounding the noisy via to confine the parasitic radiation inside the array. Bear in mind, however, that placing ground vias inside multilayer structures introduces new boundary conditions for the structure, which in some cases originate a waveguide behavior. Fig. 2.9 illustrates a case in which ground vias form waveguide paths around a vertical transition within a package. For this reason, in order to prevent the propagation of electromagnetic waves in parasitic modes within the multilayer

structures, ground vias must be placed as close as possible to the signal via in such a way that the cutoff frequency of the fundamental waveguide mode is sent to frequencies so high that are outside the useful bandwidth. However, this is not always feasible and a parasitic propagation is present at relatively low frequencies. In this regard, periodic structures compatible with substrate integrated waveguide (SIW) technology can be used to generate electromagnetic bandgaps at the desired frequency and avoid the propagation of the SSN into the cavities [44].

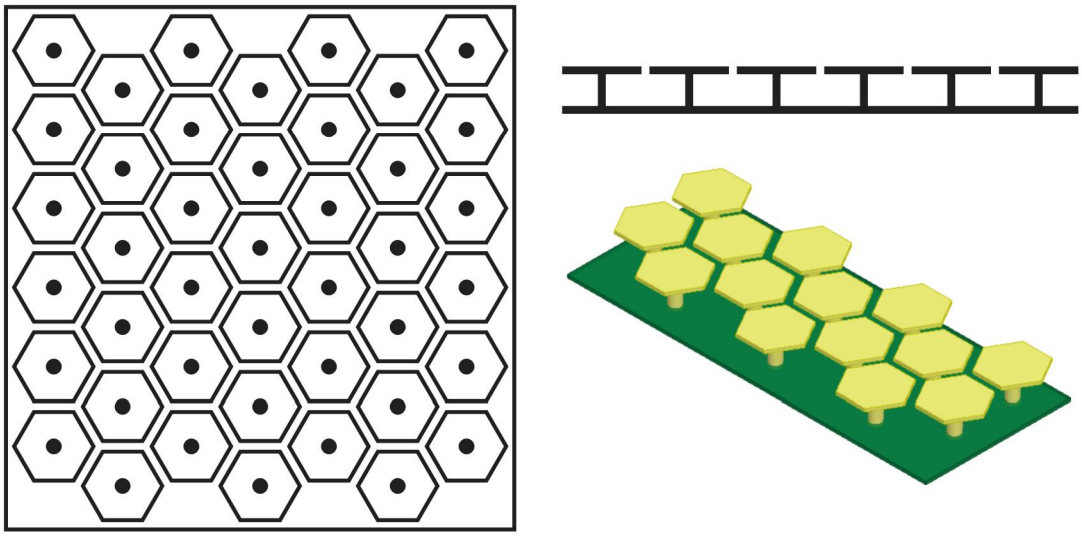


Fig. 2.8 Top, lateral, and perspective views of a mushroom-like EBG exhibiting a triangular lattice of hexagonal metal plates.

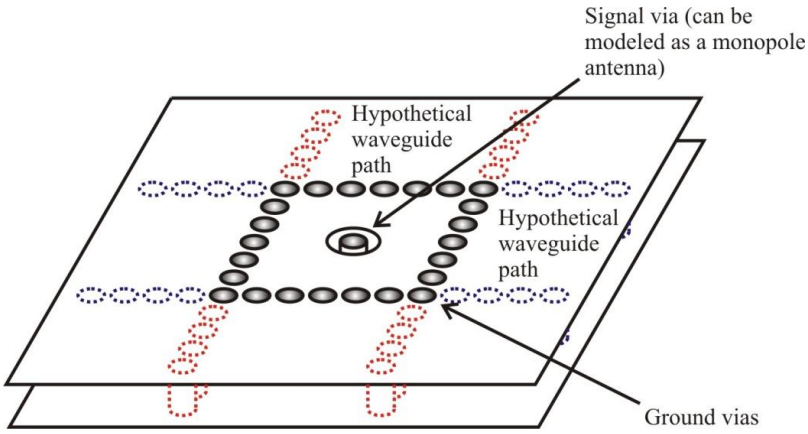


Fig. 2.9 Structure of a vertical interconnect including one signal via and several ground vias. Notice also the hypothetical SIWs that may lead to undesired horizontal propagation.

2.3.1 Characterization and modeling of a SIW Band-Stop Filter Using Equivalent Circuits

When modulating the effective width of a SIW, a rejection band around a central resonance frequency is created acting as a band-stop filter due to the perturbation of the wave impedance [44]. This modulation in the width of the SIW forms an opening known as iris, which, also determines the resonant frequency of this filter [45]. For instance, Fig. 2.10 shows three structures used for generating an SIW filter. The ideal structure with solid sidewalls is depicted in Fig. 2.10 (a), forming a regular rectangular waveguide varying in width along its length. In this case, the iris and the modulation of the width is well-defined. Thus, the dimensions and the total number of irises along the SIW determine the corresponding transfer function. Unfortunately, the structure depicted in Fig. 2.10 (a) is not compatible with conventional PCB technology. Alternatively, other structures such as that shown Fig. 2.10 (b) have been proposed, which use drilled metallic vias to emulate metallic solid sidewalls [44]. However, even though this structure is compatible with conventional PCB technology, the relatively small size of the required drilled vias increases the fabrication cost. For this reason, a second alternative can be seen in Fig. 2.10 (c) [45, 46]. In this structure, the change in width along the SIW structure is achieved by using vias with a considerable bigger diameter than in the previous case, which makes it a more cost-efficient solution. On the other hand, in order to model these structures, several unit cells are concatenated to represent the complete structure. The unit cell used for this last structure is depicted in Fig. 2.10 (d), and the equivalent circuit shown in Fig. 2.10 (e) is proposed to model it [47]. This model allows to obtain the electrical components associated to an iris cell, and the inductance related to the change in the width of the SIW.

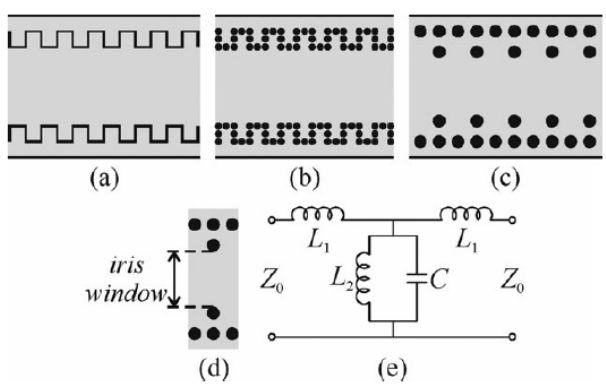


Fig. 2.10 Sketches for three different implementations of an SIW filter: (a) using solid sidewalls, (b) using small ground vias, and (c) using large ground vias. The unit cell used for the third case and the corresponding model are shown in (d) and (e) respectively.

In the model shown in Fig. 2.10 (e), the inductive element L_2 represents the change in width of the waveguide, whereas L_1 considers the interaction of a signal traveling through

the waveguide with the posts of the iris window (i.e., the posts act as scatterers). Notice that the model presents also a capacitance C, which allows to take into account the dependence on frequency of the iris impedance due to the fact that the scatterer is not perfectly square. Furthermore, because the width of the scatterer is relatively small, the effect of the iris can be concentrated at the middle of the unit cell. In this regard, the inductances L_1 and L_2, and the capacitance C can be obtained as follows. Once the S-parameters of the structure are obtained, a deembedding process is applied to remove the effect of the sections of waveguide present at the edges of the structure. The resulting set of S-parameters is converted to Z-parameters. Hence, L_2 and C are obtained from the next linear regression:

$$\frac{\omega}{\mathrm{Im}(Z_2)} = \frac{1}{L_2} - \omega^2 C \tag{2.2}$$

where $\omega = 2\pi f$. Then, L_1 is obtained from the $\mathrm{Im}(Z_{11} - Z_{12})/\omega$ versus ω^2 curve.

On the other hand, it is important to mention that the bandgap not only depends on the modulation of the iris window, but also on the number of unit cells concatenated in the structure. In fact, the magnitude of the rejection increases as the number of cells in cascade connection increases. Moreover, this magnitude is also affected by changing the iris window. For instance, Fig. 2.11 (a) shows $|S_{21}|$ versus frequency data obtained from full-wave simulations of a particular case. Thus, each one of the curves presented in Fig. 2.11 (a) corresponds to 12 unit cells of the same size in cascade connection; for each curve, a different iris window is considered.

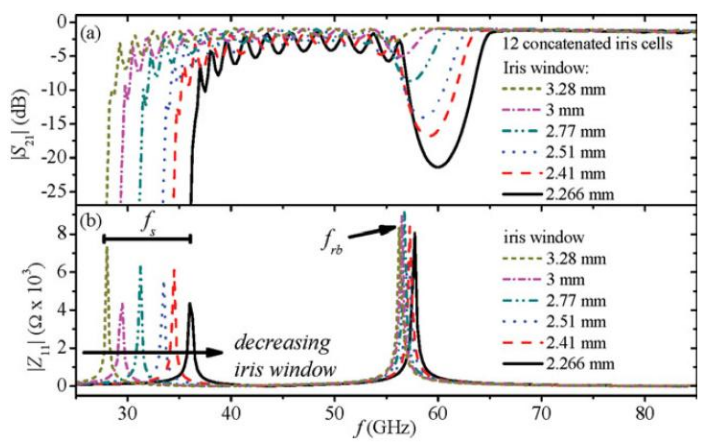


Fig. 2.11 Corresponding simulations for the unit cells (a) comparison of the bandgap response for several iris window values, and (b) magnitude of Z_{11} obtained from the simulated unit cell when modulating the iris window.

To systematically observe the impact of varying the iris window on the characteristics of the SIW filter, the following analysis is carried out. As a first approach, the frequency of

resonance for the filter can be approximately determined from the transmission curves shown in Fig. 2.11 (a). However, the relative low rejection occurring when the iris window is small difficulties the precise calculation of this frequency. Nevertheless, $|Z_{11}|$ obtained from a conversion from *S*- to *Z*-parameters allows to accurately determine not only the cutoff frequency for the rejection band (i.e., f_{rb}) but also the cutoff frequency of the SIW itself (i.e., f_s). Fig. 2.11 (b) shows $|Z_{11}|$ for the six simulated structures. As can be seen, both frequencies, f_s and f_{rb}, are easily identified in this case. Notice that the impact of varying the iris window is more noticeable for f_s because the cuttoff wavelength for allowing signal propagation is shorter as the effective width of the SIW is made smaller, whereas f_{rb} is more dependent on the periodicity of the scatterers.

In order to verify the proposed methodology, two different SIW filters fabricated on a PCB are used. The detail of the layout for the fabricated structures are shown in Fig. 2.12. Notice that two types of structures are shown: (a) modulating the iris width by increasing the size of the vias (referred to as inline vias) at the desired location, and (b) modulating the iris width by placing additional ground vias (referred to as offline vias) at the desired location. For the implementation of the model for the structures, an approach that considers the coupling between a via and a cavity is used to perform a deembedding of the launch sections is used [48]. Fig. 2.13 shows the comparison between the measured *S*-parameters and the simulations using the proposed equivalent circuit presented above. As can be seen, an excellent agreement is achieved in the complete useful band. In addition, it is possible to see the impact of the modulation of the iris in response to the rejection band.

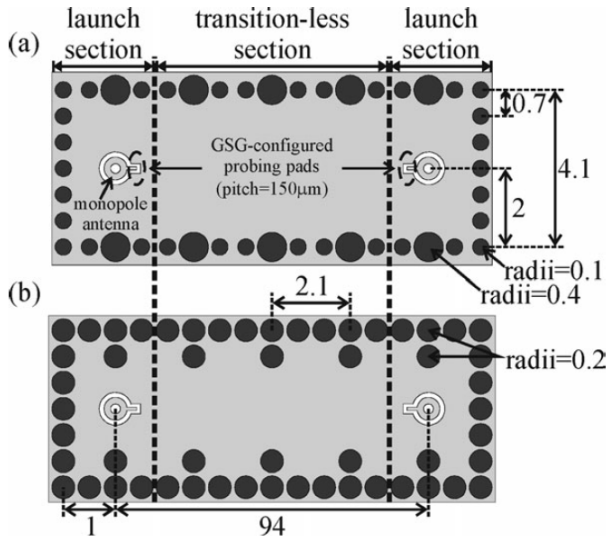


Fig. 2.12 Layouts for the SIW filters presenting: (a) inline scattering vias, and (b) offline scattering vias (all the dimensions are given in millimeters). Bear in mind that both figures represent simplified sketches, the total number of irises is 67 in reality.

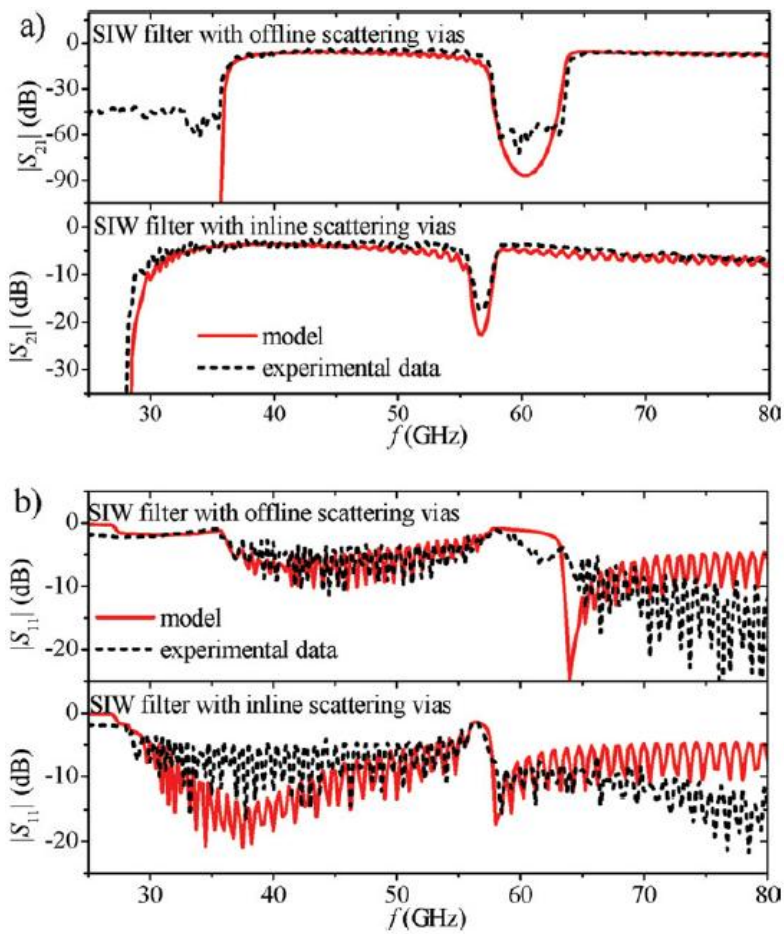


Fig. 2.13 Comparison between the measured and simulated (a) insertion losses and (b) return losses for the fabricated SIW filters.

As discussed above, placing ground vias surrounding signal vias prone to originate noise may undesirably cause a path for this noise. However, the created waveguide environment can be designed so that the EBG can reject electromagnetic waves within a frequency range. Therefore, the EBG can be designed to reject noise within a band that coincides with the signal frequency. In fact, the operating frequency of the signal can be shielded from noise. Nevertheless, using complex structures such as EBGs usually requires additional metal layers and much space to be implemented. As it is well known, both the area and the metal levels are very valuable in the design of an electronic device. Therefore, another approaches such as differential signaling have been adopted to overcome these drawbacks.

2.4 Differential Signaling

As mentioned in the previous chapter, single-ended channels present remarkable disadvantages when implemented in high-speed buses. This is one of the reasons why

modern high-speed buses use differential signaling to transmit information. Basically, differential signaling is the transmission of two complementary signals over identical coupled traces [34]. This means that differential interconnects deliver equal but opposite AC voltages and currents on the two traces, called a differential pair. Fig. 2.14 illustrates this scheme. In spite of the fact that this signaling scheme requires two signal traces to send a single string of digital signals, differential signaling presents attractive advantages such as the rejection to common-mode noise. This advantage is very appreciated by signal integrity engineers since it allows to increase the transmission data rates.

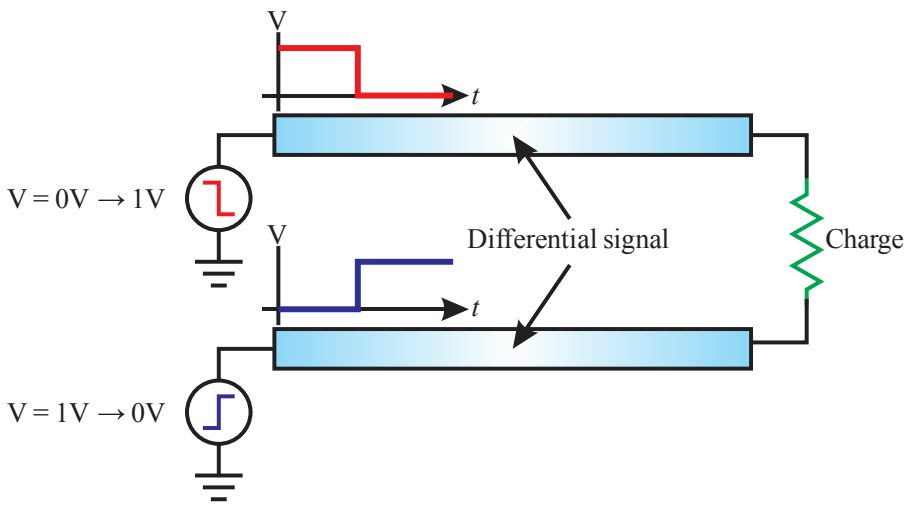


Fig. 2.14 Sketch of the simplified differential signaling scheme.

Differential signaling is very effective for removing common-mode noise, which is defined as the noise present at the end of both traces in a differential pair [10]. It means that if the differential pair is designed properly and one of the signal traces is close enough to the other, the noise present in the positive terminal (i.e., *D*+) will be approximately equal to the noise present in the negative terminal (i.e., *D*-). Therefore, at the moment to do the subtraction in the receiver's differential amplifier, this noise will be eliminated. Mathematically, this is:

$$v_{diff} = \left(v_{D+} + v_{noise}\right) - \left(v_{D-} + v_{noise}\right) = v_{D+} - v_{D-} \tag{2.3}$$

where v_{diff} is the voltage at the output of a differential amplifier and v_{noise} is the noise coupled with each trace of a differential pair. As can be seen, the common-mode noise is removed. Fig. 2.15 shows an example of this concept depicting a differential interconnect with noise present on the ground plane. In this figure, the noise is common to both terminals of the driver, and is coupled to the traces forming the differential pair. Fig. 2.16 shows a time-domain simulation of the electric circuit depicted in Fig. 2.15. In this case, a sequence of bits are injected at the input of the differential amplifier. Notice in Fig. 2.16 (a)

that the magnitude of common-mode noise is so large that makes the single-ended waveforms v_{D+} and v_{D-} undistinguishable to the naked eye. However, since this noise is present in common mode and as a result it affects in the same way both terminals of the differential receiver, the bit sequence can be recovered when the signals are subtracted by a differential amplifier as expressed by (2.3). Fig. 2.16 (b) shows the result of this approach. Notice that the signal integrity is preserved and the bits can be easily interpreted. In this regard, differential signaling represents a powerful solution to minimize the negative impact of noise coupling to the signal traces. Nevertheless, as mentioned above, the differential pairs must be properly designed to ensure obtaining the benefits that this signaling scheme provides. One of the most important considerations that must be taken into account is the length of the differential pairs. If the length of the signal traces within a differential pair are not the same, a negative effect called skew will be appear. Skew is a variation in the timing (i.e., propagation time) from one terminal to another. As a result the common-mode noise subtraction will not be optimal since the magnitude of the noise is different in both terminals and it is not going to be fully removed. This concept is explained in Fig. 2.17. Other important aspect in the design of the differential pairs is the differential crosstalk. Despite the fact that crosstalk noise is mostly common-mode noise, it also has a differential component since the distance between an aggressor and each side of the pair usually differs in real prototypes. Therefore, the noise coupled at each side of the differential pair will be slightly different and is not going to be rejected by the differential amplifier. In this regard, also if the signal traces are far away one from the other it is possible that the noise coupled into these traces will be different since different noise sources can be involved.

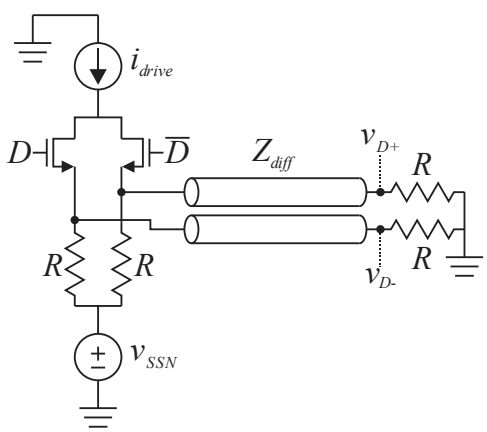


Fig. 2.15 Differential driver and interconnect with SSN present on the ground plane.

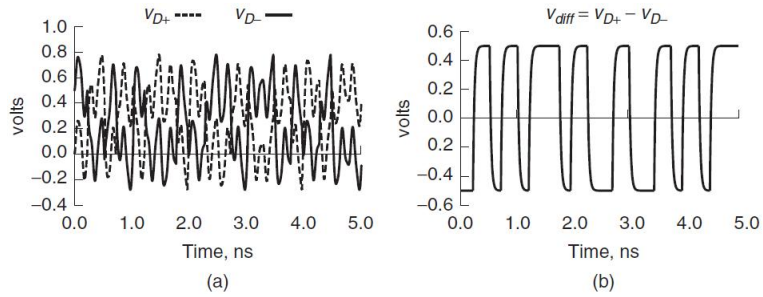


Fig. 2.16 Example of how differential signaling effectively eliminates common-mode noise. In this case, the waveforms presented in (a) are single-ended waveforms shown in the differential receiver terminals and (b) is the differential waveform after the subtraction of both single-ended waveforms [10].

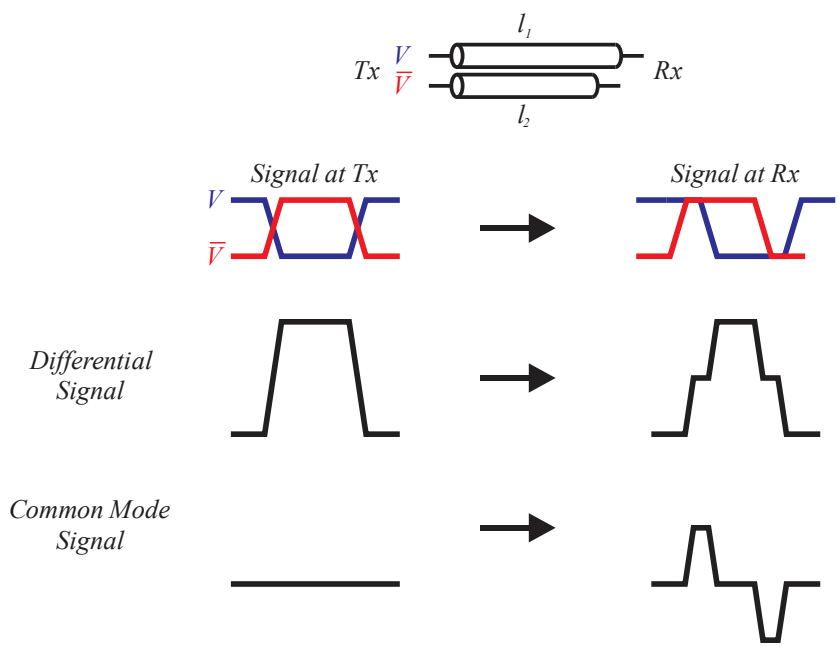


Fig. 2.17 Illustration of the skew effect caused by the asymmetry of the traces in a differential pair, common-mode noise is still present at the receiver.

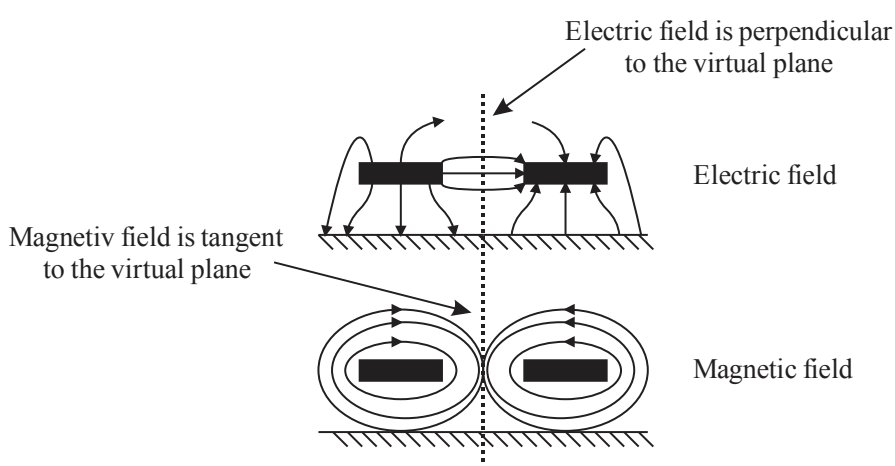


Fig. 2.18 Configuration of field lines for an odd-mode signal.

If the differential pair is well designed, additionally to the common-mode noise rejection another advantage of the differential signaling is the creation of a virtual reference plane. Due to the complementary nature of the electric and magnetic field proper of the odd mode transmission, a virtual reference plane is observed between the signal traces. Fig. 2.18 shows the field patterns of a differential pair propagating odd mode signals. Notice that halfway between the traces a virtual plane which is normal to the electric fields and tangent to the magnetic field lines is created. This plane is of great value when a nonideal reference is present through the path of the differential pair since one trace acts as the return path of the other. Some common examples of a nonideal reference include connector transitions, via arrays, layer transitions, and routing over a slot in the reference plane. This advantage will be exploited during the modeling of differential pairs within the next chapter.

2.5 Conclusions

With the sensibility of current electronic devices to common-mode noise that become more significant as the data rates increases and the operating voltages decreases, the signal integrity must be preserved in order to guarantee the correct functionality of the system. For this reason, some of the coupling mechanism for noise within PCB and packages were studied here in simple structures. Nevertheless, this gives a good insight about the possible issues which may occur in more complex structures.

After the physical origin of common-mode noise coupling onto signal traces and vias was well understood, some techniques to reduce the negative impact of this noise in the signal integrity were reviewed, such as placing EBG structures in the metal planes and the use of differential signaling. Finally, it can be concluded that the study of common-mode noise coupling mechanisms caused by the simultaneous switching of the drivers within an IC and parasitic radiation of vias in multilayer environments is of great importance in the advance of the design of high-speed electronics system.

Chapter 3

Electromagnetic Modeling of Differential Transmission-Lines

Currently, much effort for the advance in computation technologies has been focused on the miniaturization of the components and in the design of low-power consumption ICs. The achieved progress is a direct result of the exponential growth of computational systems [10]. In fact, the expected data rate for computer systems in the near future is about 16 Gbps for differential buses (see Fig. 3.1), which requires a frequency bandwidth of at least 24 GHz [49]. However, signals travelling at these data rates present wavelengths that are comparable to the dimensions of IC packages [50]. In addition, as mentioned in previous chapters, the circuit's low-voltage operating levels are also comparable to noise levels. Moreover, the compact space of current systems makes electromagnetic coupling between transmission lines and neighbor devices likely to occur. Consequently, electromagnetic modeling of differential transmission lines (DTLs) used in modern high-speed buses is necessary in order to determine the impact of the corresponding effect on the signal integrity within actual interconnection channels.

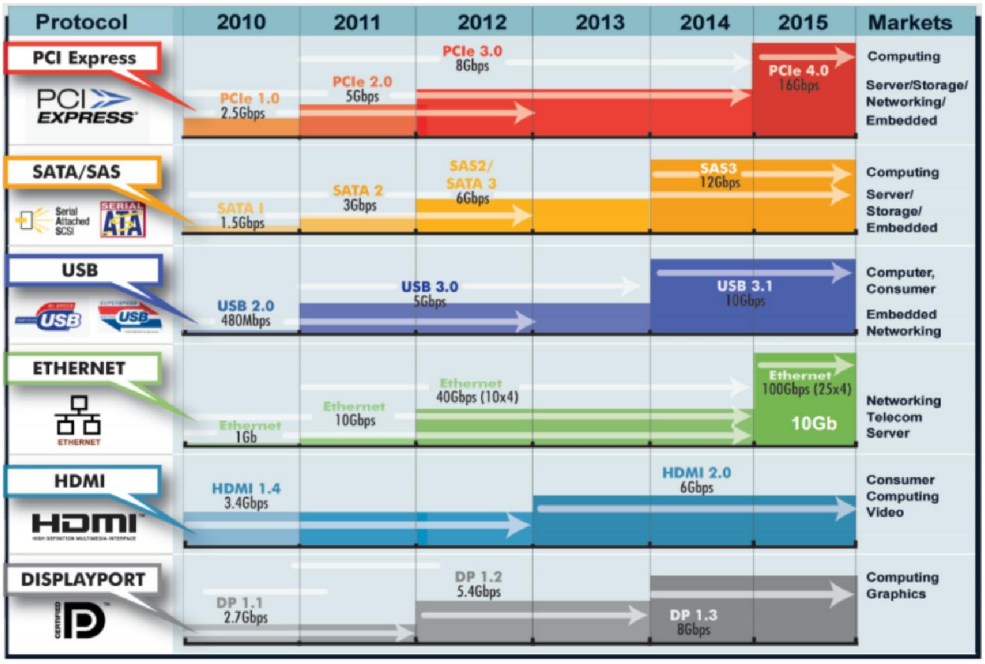


Fig. 3.1 Roadmaps for data buses and extrapolation showing the expected data rates in the near future [49].

Several modeling and characterization methods have been reported to analyze DTLs [51-55]. However, these approaches are based on low-order models either neglecting

important effects present in an actual prototype operating at high frequencies or fully relying on correlating closed-form models with simulated data obtained from electromagnetic field solvers. Alternatively, other approaches intend to obtain SPICE-compatible models by using non-linear data fitting, leading many times to non-physical significance of the equivalent circuit model of a DTL.

Fig. 3.2 shows DTLs with typical terminations used to perform the corresponding measurements using microwave probes. As can be seen in Fig. 3.2 a), the ports are disposed in such a way that the coupling between them can be neglected and single-ended probes can be used to perform the measurements. However, the bending of the transmission line used to achieve the separation of the ports introduces a discontinuity in the path of the signal. This discontinuity may yield considerably differential-to-common mode conversion when the DTL is intending to solely propagate differential signals, degrading the signal integrity. Moreover, to simplify model implementations, usually the effect of the single-ended lines used to access the termination from the uniform DTL is neglected, leading to an incorrect representation of the DTL. On the other hand, Fig. 3.2 b) shows a DTL terminated with differential launch structures. In this case, the effect of the bending as well as that the segment of single-ended line to connect the DTL are not present. Nevertheless, due to the lack of shielding between the signal pads, a coupling between these center pads exist. Therefore, this originates crosstalk that must be considered and modeled within the characterization of the DTL. For this reason, in order to provide an alternative easy-to-implement representation of a differential transmission line, methodologies for the characterization and modeling of these interconnects are proposed in this chapter. Hence, the proposal allows to determine the equivalent circuit model for a differential launch structure used to feed a DTL when single-ended terminations are not present. In addition, the classical *RLGC* model for a single-ended transmission line is used to model the homogeneous part of the DTL, but including the current-distribution dependence of the inductance as will be shown later within this chapter. Thus, from the analysis of these elements at microwave frequencies, the elements that negatively influence the performance of the interconnection can be identified and quantitatively assessed. In this regard, the obtained results are useful for optimizing differential interconnection channels.

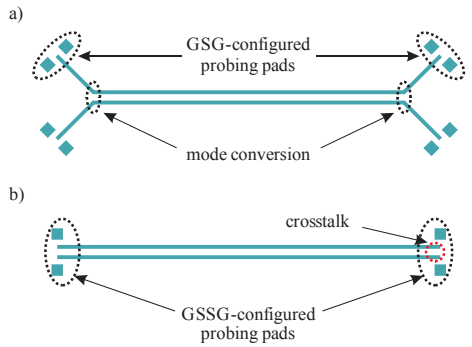


Fig. 3.2 Sketch of a DTL presenting a) single-ended and b) differential terminations.

3.1 Single-Ended to Mixed-Mode *S*-Parameters Transformation

As mentioned in previous chapters, a very useful approach to study coupled-line systems is the modal analysis. In general, for a four-port interconnect formed by two coupled lines, the mixed mode *S*-parameters consider the two supported modes of the structure: the differential and the common mode, as well as the mode conversion between them. These parameters play a key role in the design of differential RF devices such as DTLs. Mixed-mode *S*-parameters were reported in a generalized form in 2006 [56], and in 2008 a study of their mathematical properties was presented [57], making possible the use of this mathematical formalism for advanced modeling of interconnects.

As mentioned above, a DTL can be seen as a four-port network. Nevertheless, with the modal analysis this four-port network can be split into two two-port networks, one corresponds to the differential and the other to the common propagation mode. This concept is illustrated in Fig. 3.3.

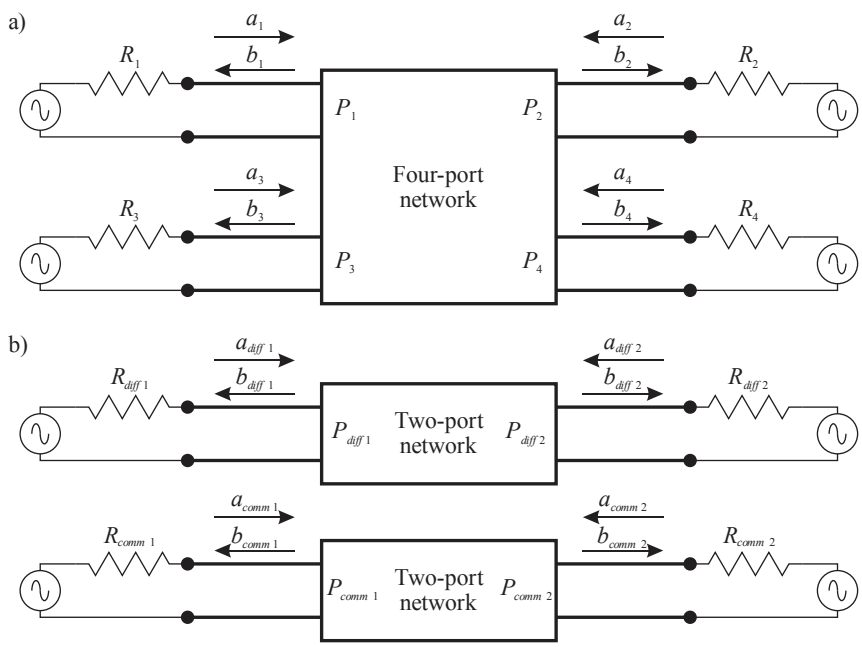


Fig. 3.3 Four-port network: a) single-ended representation, and b) mixed-mode representation.

Notice in Fig. 3.3 b) that both fundamental modes are represented, the differential and common mode. In this regard, $a_{diff\,1}$ and $a_{diff\,2}$ are the differential power waves going toward the ports, $b_{diff\,1}$ and $b_{diff\,2}$ are the differential power waves going in the opposite direction, whereas $a_{comm\,1}$ and $a_{comm\,2}$ are the common power waves going toward the ports, whereas $b_{comm\,1}$ and $b_{comm\,2}$ are the common power waves coming outside the ports. In addition, $R_{diff\,1}$ and $R_{diff\,2}$ are the equivalent reference impedances at the output ports when the system is propagating differential signals; conversely, $R_{comm\,1}$ and $R_{comm\,2}$ are the equivalent reference impedances for the common mode case. In this regard, modal analysis presents the

advantage of allowing the representation of a multi-port device using two-port network theory, which greatly simplifies the analysis of DTLs since single-ended concepts can be applied straightforwardly to each propagation mode. Thus, in order to explain the difference between single-ended multi-port *S*-parameters and those allowing the separation of common and differential modes, the two cases are explained afterwards.

The four-port network shown in Fig. 3.3 a) can be represented by a 4×4 single-ended *S*-parameter matrix ($\mathbf{S}_{4p}$), which allows to write the vector representing the power waves coming out at each port ($\mathbf{b}_i$) in terms of the incident power waves at each port ($\mathbf{a}_i$) in the following way:

$$\mathbf{b}_i = \mathbf{S}_{4p} \times \mathbf{a}_i \tag{3.1}$$

or in its expanded form given by:

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix} \tag{3.2}$$

Conversely, when taking advantage of the modal analysis, the mixed-mode *S*-parameter matrix ($\mathbf{S}_{mm}$) allows to write the vector representing the power waves coming out of each port in Fig. 3.2 b) in differential (b_{DDi}) and common (b_{CCi}) modes in terms of the incident power waves incident at the corresponding ports (i.e., a_{DDi} and a_{CCi}). In an expanded form, the corresponding matrix equation is:

$$\begin{bmatrix} b_{DD1} \\ b_{DD2} \\ b_{CC1} \\ b_{CC2} \end{bmatrix} = \begin{bmatrix} S_{DD11} & S_{DD12} & S_{DC11} & S_{DC12} \\ S_{DD21} & S_{DD22} & S_{DC21} & S_{DC22} \\ S_{CD11} & S_{CD12} & S_{CC11} & S_{CC12} \\ S_{CD21} & S_{CD22} & S_{CC21} & S_{CC22} \end{bmatrix} \cdot \begin{bmatrix} a_{DD1} \\ a_{DD2} \\ a_{CC3} \\ a_{CC4} \end{bmatrix} \tag{3.3}$$

which can also be written by grouping the four corners of $\mathbf{S}_{mm}$, which yields:

$$\begin{bmatrix} b_{DD1} \\ b_{DD2} \\ b_{CC1} \\ b_{CC2} \end{bmatrix} = \begin{bmatrix} [\mathbf{S}_{DD}] & [\mathbf{S}_{DC}] \\ [\mathbf{S}_{CD}] & [\mathbf{S}_{CC}] \end{bmatrix} \cdot \begin{bmatrix} a_{DD1} \\ a_{DD2} \\ a_{CC3} \\ a_{CC4} \end{bmatrix} \tag{3.4}$$

In this last equation, $\mathbf{S}_{DD}$ is the 2×2 matrix which contains the pure differential mode information regarding to the four-port network. Similarly, $\mathbf{S}_{CC}$ is the 2×2 matrix which contains the pure common mode information of the network. On the other hand, there are

two other matrices in the mixed-mode *S*-parameters matrix; $\mathbf{S}_{DC}$ contains the information of how much energy is being converted to common mode when differential signals are being propagating through the network and $\mathbf{S}_{CD}$ considers the opposite mode conversion case. For instance, if a DTL is propagating signals in differential mode and mode conversion is present, a waste of energy is present since not all the power given by the source is being used to transmit the signals. For this reason, it is desired that mode conversion does not exist or at least it could be minimized as much as possible.

The definition presented above is considering power waves, which is usual for *S*-parameters. Nevertheless, the mixed-mode *S*-parameters can also be defined in terms of the modal voltages and currents as follows:

$$\begin{aligned}
v_{CC1} &= \frac{v_1 + v_2}{2} \\
v_{CC2} &= \frac{v_3 + v_4}{2} \\
i_{CC1} &= i_1 + i_2 \\
i_{CC2} &= i_3 + i_4 \\
v_{DD1} &= v_1 - v_2 \\
v_{DD2} &= v_3 - v_4 \\
i_{DD1} &= \frac{i_1 - i_2}{2} \\
i_{DD2} &= \frac{i_3 - i_4}{2}
\end{aligned} \tag{3.5}$$

where v_1 to v_4, and i_1 to i_4 are the voltages and currents at the ports P_1 to P_4 defined in Fig. 3.3 a), whereas the voltages and currents with the subscripts *DD* and *CC* correspond to the differential and common mode ports as defined in Fig. 3.3 b).

Now, consider that the power waves at all the ports are referenced to the characteristic impedance of the single-ended transmission lines (Z_0), the single-ended and modal voltages and currents can be expressed by:

$$\begin{aligned}
v_i &= \sqrt{Z_0}\left(a_i + b_i\right), \quad \left(i = 1,2,3,4\right) \\
i_i &= \frac{1}{\sqrt{Z_0}}\left(a_i - b_i\right), \quad \left(i = 1,2,3,4\right)
\end{aligned} \tag{3.6}$$

$$
\begin{aligned}
v_{DDi} &= \sqrt{Z_{0DD}}\left(a_{DDi} + b_{DDi}\right), \quad \left(i = 1,2\right) \\
i_{DDi} &= \frac{1}{\sqrt{Z_{0DD}}}\left(a_{DDi} - b_{DDi}\right), \quad \left(i = 1,2\right) \\
v_{CCi} &= \sqrt{Z_{0CC}}\left(a_{CCi} + b_{CCi}\right), \quad \left(i = 1,2\right) \\
i_{CCi} &= \frac{1}{\sqrt{Z_{0CC}}}\left(a_{CCi} - b_{CCi}\right), \quad \left(i = 1,2\right)
\end{aligned}
\tag{3.7}
$$

where the differential and common mode impedances can be written in terms of the impedance of the line when considered as a single-ended structure as in Fig. 3.3 b); this is $Z_{0DD} = 2Z_0$ and $Z_{0CC} = Z_0/2$ which is usually found in the literature.

After replacing (3.6) into (3.7), the following expressions for the power waves can be obtained:

$$
\begin{aligned}
a_{DD1} &= \frac{1}{\sqrt{2}}\left(a_1 - a_2\right) \\
b_{DD1} &= \frac{1}{\sqrt{2}}\left(b_1 - b_2\right) \\
a_{DD2} &= \frac{1}{\sqrt{2}}\left(a_3 - a_4\right) \\
b_{DD2} &= \frac{1}{\sqrt{2}}\left(b_3 - b_4\right) \\
a_{CC1} &= \frac{1}{\sqrt{2}}\left(a_1 + a_2\right) \\
b_{CC1} &= \frac{1}{\sqrt{2}}\left(b_1 + b_2\right) \\
a_{CC2} &= \frac{1}{\sqrt{2}}\left(a_3 + a_4\right) \\
b_{CC2} &= \frac{1}{\sqrt{2}}\left(b_3 + b_4\right)
\end{aligned}
\tag{3.8}
$$

which can be rearranged into a matrix form as:

$$
\begin{bmatrix} b_{DD1} \\ b_{DD2} \\ b_{CC1} \\ b_{CC2} \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix}
\tag{3.9}
$$

$$\begin{bmatrix} a_{DD1} \\ a_{DD2} \\ a_{CC1} \\ a_{CC2} \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix} \tag{3.10}$$

if the constant matrix is defined as:

$$\mathbf{M} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} \tag{3.11}$$

(3.9) and (3.10) can be expressed as:

$$\begin{bmatrix} b_{DD1} \\ b_{DD2} \\ b_{CC1} \\ b_{CC2} \end{bmatrix} = \mathbf{M} \begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix}; \quad \begin{bmatrix} a_{DD1} \\ a_{DD2} \\ a_{CC1} \\ a_{CC2} \end{bmatrix} = \mathbf{M} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix} \tag{3.12}$$

combining (3.12) with (3.2), it is possible to obtain the following expression:

$$\begin{bmatrix} b_{DD1} \\ b_{DD2} \\ b_{CC1} \\ b_{CC2} \end{bmatrix} = \mathbf{M}\mathbf{S}_{\mathrm{SE}}\mathbf{M}^{-1} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix} \tag{3.13}$$

where $\mathbf{S}_{\mathrm{SE}}$ is the single-ended *S*-parameter matrix defined in (3.2). Finally, comparing (3.4) and (3.13), it is possible to see that:

$$\begin{bmatrix} [\mathbf{S}_{DD}] & [\mathbf{S}_{DC}] \\ [\mathbf{S}_{CD}] & [\mathbf{S}_{CC}] \end{bmatrix} = \mathbf{M}\mathbf{S}_{\mathrm{SE}}\mathbf{M}^{-1} \tag{3.14}$$

This formulation allows to analyze the fundamental modes supported by a DTL using single-ended *S*-parameters. In fact, the most important matrix when working with systems of two coupled lines is $\mathbf{S}_{DD}$, since this matrix gives information about the differential mode. Nonetheless, $\mathbf{S}_{CC}$ is also relevant because it provides information about how the network behaves when common mode signals are injected. On the other hand, as is mentioned above $\mathbf{S}_{DC}$ and $\mathbf{S}_{CD}$ provide information about the mode conversion and may be relevant if this is high enough.

Coupled lines are usually designed to be driven in differential mode since the common mode is similar to use single-ended signaling but with the corresponding increase in the prototype area. However, the common mode information is also important to be considered when modeling DTLs in order to have all the information related to the four-port network. Thus, it is important to define two other concepts related to the differential and common signaling scheme: the even and odd mode impedance. The odd mode is excited in the coupled transmission line when a differential signal is propagated through the line, conversely, the even mode is excited when a common signal is propagated. In this regard, the single-ended characteristic impedance (Z_0) is the impedance the signal experiences when a single line is not coupled to an adjacent line, whereas the odd mode impedance (Z_{0o}) and the even mode impedance (Z_{0e}) are the impedance the signal experiences when a single line is coupled to an adjacent line for the odd and even mode respectively. Nevertheless, these impedances are defined for one line in a couple pair. For this reason, two other concepts need to be defined: the differential mode impedance (Z_{diff}) and the common mode impedance (Z_{comm}). Z_{diff} is the impedance "seen" between a pair of lines when driven differential signals, while Z_{comm} is the impedance "seen" between a pair of lines when driven common signals. As is mentioned in Chapter 2, when a coupled line is driving differential signals one trace can be seen as a return path for the other creating a series connection for the current, so, Z_{diff} is twice the value of Z_{0o}. On the other hand, Z_{comm} is half the value of Z_{0e} since both traces drive the current in the same direction making a parallel connection. These definitions are important since Z_{diff} and Z_{comm} are the impedances the signal experiences through the coupled line from the modal point of view.

Now that mixed-mode *S*-parameters and the definition of differential and common mode impedances have been discussed within this section, it is possible to analyze DTLs from a modal point of view. As shown within the next sections, modal analysis simplifies the analysis of differential interconnects, allowing to model and characterize them.

3.2 Modeling of Differential Launch Structures

Accurately modeling devices, electrical transitions and terminations in differential configuration has recently taken much importance. In this regard, the experimental *S*-parameter data used for developing and implementing the corresponding models are measured using a four-port vector network analyzer (VNA) [15, 16]. For this purpose, probing pads are typically used to avoid the considerable parasitics associated with other type of structures used to launch and receive RF signals (e.g., coaxial connectors). As mentioned above, in case that a differential device presents single-ended terminations at each one of its ports, the corresponding theory used for the de-embedding and calibration processes can straightforwardly be applied to obtain the corrected differential *S*-parameters [16, 17]. Unfortunately, single-ended lines of considerable length are required to connect

the probing pads to the differential device, increasing the area of the prototype and introducing parasitics that reduce the measurement certainty [18]. Even though existing theory can be extended to the differential case by using a four-port to mixed-mode S-parameter transformation, this evident advantage has only been explored for modeling homogeneous transmission lines (TLs) by obtaining the propagation constant and characteristic impedance [17], and for implementing *RLGC* equivalent circuit models [58]. Conversely, despite the importance of the modeling of the transition/termination differential structures in currently available methodologies, this topic has been barely explored in the literature [59]. Thus, using mixed-mode *S*-parameters, the development of analytical equivalent circuit model and parameter extraction methodology for a differential termination is presented next.

If the DTL has a symmetry axis in the cross-section along their lengths, this DTL is considered as a balanced line. Basically, a balanced line consists of two conductor traces designed to present equal impedance. Additionally, balanced lines present the property of greatly reducing mode-conversion [60]. Thus, assuming that the DTL presents symmetry, the common-to-differential and differential-to-common mode conversion can be neglected for practical purposes (i.e. $\mathbf{S}_{DC}$ and $\mathbf{S}_{CD}$ = 0). Nevertheless, it is important to verify this assumption with experimental data. Therefore, the modal decomposition of the four-port network shown in Fig. 3.3 can be applied, so that, the 4-port transmission line-based DUT can be separated into two two-port DUTs. In this case, each propagation mode occurring in the transmission line can be represented using the block model depicted in Fig. 3.4. As can be seen, the transmission line is represented by means of a modal complex propagation constant γ_m, a modal characteristic impedance Z_m, and a length l. In addition, also notice that the line is embedded between two adapters associated with the signal launchers. Therefore, each cascade model can be described in terms of the *ABCD* parameters as [61]

$$\mathbf{T}_{Xnm} = \mathbf{L}_m \mathbf{T}_{nm} \mathbf{R}_m \tag{3.15}$$

where $\mathbf{L}_m$ and $\mathbf{R}_m$ are the matrices associated with the left and right adapters respectively, $\mathbf{T}_{nm}$ is the matrix corresponding to the uniform transmission line (UTL) section, the subscript n is added to distinguish between the parameters obtained from lines with different lengths used later, and the subscript m stands for the differential and common mode correspondingly. In addition, using transmission line theory, $\mathbf{T}_{nm}$ can be expressed as

$$\mathbf{T}_{nm} = \begin{bmatrix} \cosh(\gamma_m l_{\mathrm{n}}) & Z_m \sinh(\gamma_m l_{\mathrm{n}}) \\ Z_m^{-1} \sinh(\gamma_m l_{\mathrm{n}}) & \cosh(\gamma_m l_{\mathrm{n}}) \end{bmatrix} \tag{3.16}$$

The complex values for γ_m and Z_m of a UTL can be determined using previously reported methods [62]. Thus, $\mathbf{T}_{nm}$ can be easily obtained for a given line length.

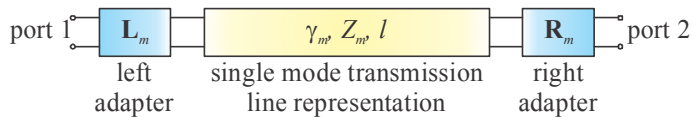


Fig. 3.4 Cascade model for a transmission line embedded between two electrical discontinuities.

In the case of the adapters, consider a typical differential launch structure. For instance, Fig. 3.5 shows a sketch of a GSSG-configured probing pad also illustrating the equivalent circuit model for this type of transitions. In this regard, this model is based on the representation used for a CPW-to-microstrip transition introduced in [62] and shown in the right part of Fig. 3.5. This model considers the interaction between a single signal pad and two adjacent ground pads, obtaining excellent results at gigahertz frequencies. For this reason, the model proposed here for the differential launch structure uses this concept for each signal pad, but also accounting for the interaction between the signal pads using a mutual inductance and a mutual capacitance. For parameter extraction purposes, taking advantage of the four-port to mixed-mode transformation, the four-port network used to represent the differential launch structure can be divided into two two-port modal *S*-parameter sets. Therefore, the equivalent circuit for a single ended CPW-to-microstrip transition can be used for each mode, after that, the modal network parameters can be used to obtain the four-port network as shown later. Thus, according to the modal network equivalent circuit, the *ABCD* parameters for the adapters can be expressed as

$$\mathbf{L}_m = \begin{bmatrix} 1+zy & z \\ y & 1 \end{bmatrix}; \quad \mathbf{R}_m = \begin{bmatrix} 1 & z \\ y & 1+zy \end{bmatrix} \tag{3.17}$$

where $z = j\omega L_m$ and $y = j\omega C_m$. Notice that L_m represents the inductive effect of the signal trace, whereas, $\mathbf{L}_m$ is the matrix related with the right adapter. Thus, $\mathbf{L}_m$ and $\mathbf{R}_m$ can be directly obtained from experimental $\mathbf{T}_{Xnm}$ matrices associated with two lines of different lengths as proposed hereafter.

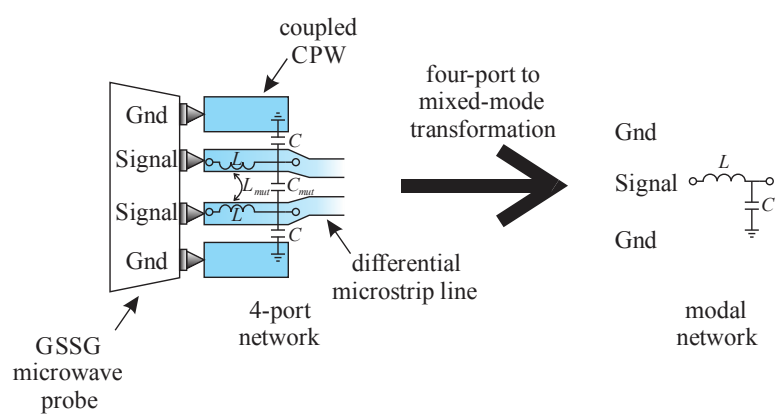


Fig. 3.5 Modal equivalent network of a differential launch structure after a four-port to mixed-mode transformation.

Substituting (3.16) and (3.17) into (3.15) and simplifying yields

$$\mathbf{T}_{Xnm} = \begin{bmatrix} A_{nm} & B_{nm} \\ C_{nm} & D_{nm} \end{bmatrix} = \begin{bmatrix} d\cosh(\gamma_m l_n) + e\sinh(\gamma_m l_n) & f\cosh(\gamma_m l_n) + g\sinh(\gamma_m l_n) \\ h\cosh(\gamma_m l_n) + k\sinh(\gamma_m l_n) & p\cosh(\gamma_m l_n) + q\sinh(\gamma_m l_n) \end{bmatrix} \quad (3.18)$$

where $d = 2yz + 1$ and $h = 2y$. Whereas e, f, g, k, p, and q can also be written in terms of y, z, Z_m and l_n; however, these parameters are not used in this formulation.

Involving terms associated with two DTLs differing only in length, a system of linear equations (SLE) can be written involving C_{nm} as

$$\begin{aligned} C_{1m} &= h\cosh(\gamma_m l_1) + k\sinh(\gamma_m l_1) \\ C_{2m} &= h\cosh(\gamma_m l_2) + k\sinh(\gamma_m l_2) \end{aligned} \quad (3.19)$$

This SLE is solved for h and k, and the solution for h is:

$$h = \frac{C_{1m}\sinh(\gamma_m l_2) - C_{2m}\sinh(\gamma_m l_1)}{\cosh(\gamma_m l_1)\sinh(\gamma_m l_2) - \cosh(\gamma_m l_2)\sinh(\gamma_m l_1)} \quad (3.20)$$

Thus, since $y = j\omega C_m$ and $h = 2y$,

$$C_m = \mathrm{Im}\left(\frac{h}{2\omega}\right) \quad (3.21)$$

Similarly, a SLE can be written for A_{nm} where d can be obtained (by involving the terms corresponding to two lines) as

$$d = \frac{A_{1m}\sinh(\gamma_m l_2) - A_{2m}\sinh(\gamma_m l_1)}{\cosh(\gamma_m l_1)\sinh(\gamma_m l_2) - \cosh(\gamma_m l_2)\sinh(\gamma_m l_1)} \quad (3.22)$$

Thus, L_m can be determined from $d = 2yz + 1$ as

$$L_m = \mathrm{Im}\left(\frac{d-1}{2y\omega}\right) \quad (3.23)$$

At this point, both the differential and common mode cascade models depicted in Fig. 3.4 are fully characterized in a separate way when (3.21) and (3.23) are applied to experimental data. However, the objective of this work is to model a complete differential launch structure simultaneously considering both modes. For this reason, an equivalent circuit model that represents the electromagnetic coupling between the signal traces is required. Obtaining this representation is achieved using a simplified version of the

lumped-element *RLGC* circuit model for a symmetric differential line proposed in [58], which results in the following methodology [63].

Using the values for L_{mutual} and C_{mutual} obtained from the differential and common mode equivalent circuit model, it is possible to determine the parameters of the π-network shown in Fig. 3.5 as:

$$\begin{aligned} C &= C_{cc} / 2 \\ C_{mutual} &= C_{dd} - C_{cc} / 2 \\ L &= L_{cc} + L_{dd} / 4 \\ L_{mutual} &= L_{cc} - L_{dd} / 4 \end{aligned} \tag{3.24}$$

where the subscripts *dd* and *cc* are added to distinguish between the parameters obtained from the differential and common mode respectively. It is important to point out that the methodology discussed here is explained using a GSSG configuration for the probing pads; however, this study can be applied to any differential launch structure provided if this is symmetric. This assumption is valid since (3.24) corresponds to a symmetric differential line.

Once the equivalent circuit model of the differential launch structure is obtained, the DTL can be fully characterized. The mixed-mode *S*-parameters obtained from (3.16) for a line of particular length can be converted back to four-port single-ended *S*-parameters so that single ended sets can be cascaded for modeling the complete structure. In fact, the equivalent circuit for the transitions is added to each corresponding port of the four-port SE S-parameters so that the DTL is modeled. However, the homogenous part of the DTL represented by means of the propagation constant and characteristic impedance of each mode in (3.16) can also be modeled using an equivalent circuit model, which is more practical from a CAD point of view. An approach dealing with this is discussed in the next section.

3.3 Homogeneous Differential Transmission Line Modeling

As mentioned above, modeling DTLs is necessary to represent differential interconnects at high frequencies. Hence, approaches to obtain the DTL model parameters as a function of geometry and frequency have been proposed [64, 51]. For simplicity, these parameters are typically considered as weakly dependent on frequency, which yields poor accuracy at microwave frequencies. This problem is attributed to the strong dependence of the interconnect series impedance on the distribution of the current within the metal traces [65]. On the other hand, numerical and analytical approaches to obtain the per-unit-length *RLGC* parameters for DTLs have been proposed. However, these approaches either require a priori

knowledge of the material properties and effective dimensions of the structures or fully rely on full-wave simulations [66]. Moreover, the tabular W-element transmission line model used by HSPICE to simulate a multiline-coupled system requires data associated with the coupling resistance and conductance between signal traces, which are not easy to determine without a field solver. For this reason, a methodology to model the *RLGC* parameters obtained directly from measured data for the common and differential propagation modes in DTLs is presented in this dissertation. This methodology considers the current distribution in the signal traces including skin and proximity effects as well as the impact of the metal roughness.

Following the methodology of the previous section, it is possible to obtain the propagation constant (γ_m) and characteristic impedance (Z_m) for the common ($m = cc$) and differential ($m = dd$) modes. Afterwards, the *RLGC* elements for each mode were calculated as:

$$\begin{aligned} R_m &= \mathrm{Re}\left(\gamma_m Z_m\right) \\ L_m &= \mathrm{Im}\left(\gamma_m Z_m\right)/2\pi f \\ G_m &= \mathrm{Re}\left(\gamma_m / Z_m\right) \\ C_m &= \mathrm{Im}\left(\gamma_m / Z_m\right)/2\pi f \end{aligned} \tag{3.25}$$

For the case of the shunt elements in the models for common (i.e., C_{cc} and G_{cc}) and differential mode (i.e., C_{dd} and G_{dd}) propagation, available representations in the frequency domain are appropriate when considering effective values for the permittivity and loss tangent [65], which can be extracted once the characteristic impedance is experimentally obtained as in [67]. This is:

$$Z_C = \frac{\beta}{\omega C} - j\frac{\alpha - \beta \tan\delta_{eff}}{\omega C} \tag{3.26}$$

where C is the capacitance of the line and $\tan\delta_{eff}$ is the effective loss tangent experienced by the signal. It is important to mention that both C and $\tan\delta_{eff}$ are roughly independent of frequency which is valid for transmission lines fabricated in typical PCB substrates within the tens of gigahertz [67]. Thus, once C and $\tan\delta_{eff}$ are defined using (3.24), the conductance can be obtained as:

$$G = \omega C \tan\delta_{eff} \tag{3.27}$$

On the other hand, for the series resistance in common (R_{cc}) and differential mode (R_{dd}) propagation, the effect of the metal-dielectric surface roughness present on PCB originates a frequency-dependent behavior different from the expected proportionality to the square root of frequency. Thus, the following equation can be used for R_{cc} and R_{dd} [65, 10]:

$$R_m = K_{Hm} k_{Tm} \sqrt{f} \tag{3.28}$$

where k_{Tm} is a proportionality constant related to the skin effect and K_{Hm} is a frequency-dependent coefficient that incorporates the skin and surface roughness effects. Now, the typically used model for the inductance dictates that [65, 10]:

$$L_m = L_{\infty m} + L_{\text{int}} = L_{\infty m} + \frac{K_{Hm} k_{Tm}}{2\pi\sqrt{f}} \tag{3.29}$$

where $L_{\infty m}$ is the inductance at high frequencies. In (3.27), L_{int} is affected by the surface roughness, which is considered by the frequency dependent K_{Hm} parameter. However, at high frequencies the denominator defining L_{int} increases in a more accentuated way approximately proportional to $\sqrt{f}$. Thus, L_m will tend to $L_{\infty m}$ at high frequencies. Actually, when (3.29) is used to model a modal inductance, it has been found that it exists a noticeable discrepancy with the experimentally obtained data from (3.23) at low frequencies [68]. This is due to the fact that (3.27) assumes that the current flowing through the signal traces and the ground plane forms inductance loops of constant area for a given frequency. This lacks of validity at relatively low frequencies as explained hereafter.

In a recent work [69], it has been shown that the series resistance and inductance have a strong frequency dependence, especially for on-chip interconnects. This is associated with the proximity and skin effects related to the geometry of the ground plane and the signal trace. This effect is mainly attributed to the current distribution in the ground plane and how the current is getting more concentrated below the signal trace as frequency rises. This is valid also for transmission lines built in PCB, although the frequency dependence is not so evident. For this reason (3.29) usually acceptably represents the inductance of single-ended lines. However, when the system consists of coupled lines, the current distribution in the signal traces also adds a proximity effect that influences the inductance of the line. Thus, extending the concepts introduced in [69] to coupled lines, three different current loops can be defined to consider the non-homogeneous current distribution into the signal traces. For instance, Fig 3.6 illustrates the two operating modes of an edge-coupled DTL conceptually detailing the corresponding current density distribution. Notice that the cross section of the signal traces is divided into three different regions presenting widths w_1, w_2, and w_3 with their corresponding inductance components. Thus, since in common mode propagation the traces carry current in the same direction, the concentration of charge carriers is more intense at the external edges of the lines and tends to decrease towards the internal edges as frequency increases. The opposite occurs for the differential mode. Furthermore, each region originates a current loop with different area and thus of different inductance. Only when separately analyzing these inductances, (3.27) can be applied for each section. However, by combining the effect of each one of the inductance components, a model for the effective inductance can obtained for both propagation modes [69].

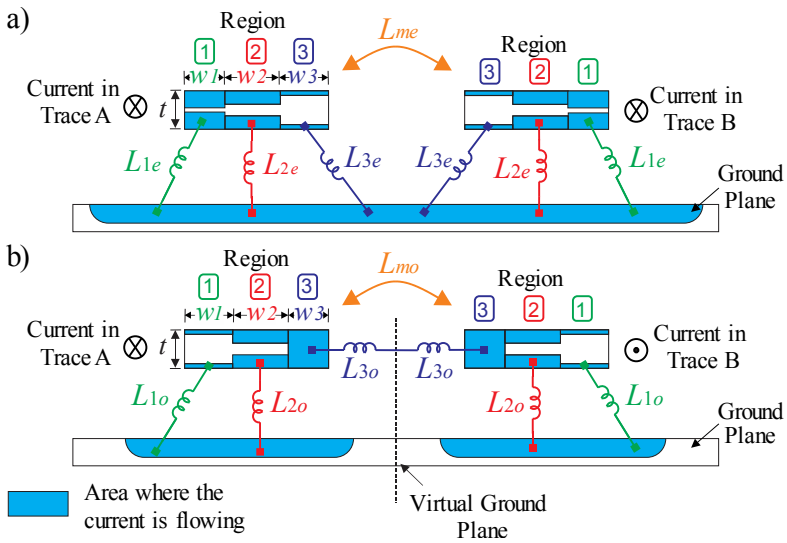


Fig. 3.6 Depiction of the current density distribution and the corresponding inductance components for a DTL: a) common, and b) differential mode.

According to Fig. 3.6 a), the self-inductance of the traces 'A' and 'B' in common mode is

$$L_{Acc} = L_{Bcc} = \left(\frac{1}{L_{1cc}} + \frac{1}{L_{2cc}} + \frac{1}{L_{3cc}} \right)^{-1} \tag{3.30}$$

In this mode, the effective inductance of the DTL involves the parallel connection of L_{Acc} and L_{Bcc} since the current flows in the same direction. Thus, when considering the coupling coefficient (k) between the signal traces [10], the effective inductance in common mode is $L_{cc} = 0.5\ L_{Acc}\ (1 + k)$. On the other hand, as illustrated in Fig. 3.6 b), in differential mode the inductance can be analyzed by identifying a virtual ground plane due to the magnetic field configuration in this mode. In this case, the self-inductance of traces 'A' and 'B' is

$$L_{Add} = L_{Bdd} = \left(\frac{1}{L_{1dd}} + \frac{1}{L_{2dd}} + \frac{1}{L_{3dd}} \right)^{-1} \tag{3.31}$$

Bear in mind that the inductances in the regions indicated in Fig. 3.6 may be considerably different for the different propagation modes. Now, since the current in differential mode flow in opposite directions, the effective inductance of the DTL involves the series connection of L_{Add} and L_{Bdd}. Again, considering k, the effective inductance in differential mode is $L_{dd} = 2\ L_{Acc}\ (1 - k)$.

At this point, it has been shown that L_{cc} and L_{dd} can be calculated using identical equations. Thus, substituting (3.27) into the equation for the modal inductance yields

$$L_m = \left(\left(L_{1\infty} + \frac{K_H k_1}{2\pi\sqrt{f}} \right)^{-1} + \left(L_{2\infty} + \frac{K_H k_2}{2\pi\sqrt{f}} \right)^{-1} + \left(L_{3\infty} + \frac{K_H k_3}{2\pi\sqrt{f}} \right)^{-1} \right)^{-1} \tag{3.32}$$

$$= \frac{\left(2\pi L_{1\infty}\sqrt{f} + K_H k_1\right)\left(2\pi L_{2\infty}\sqrt{f} + K_H k_2\right)\left(2\pi L_{3\infty}\sqrt{f} + K_H k_3\right)}{2\pi\sqrt{f}\left(4\pi^2 f\left(L_{1\infty}L_{2\infty} + L_{1\infty}L_{3\infty} + L_{2\infty}L_{3\infty}\right) + 2\pi K_H\sqrt{f}\left(k_1L_{2\infty} + k_1L_{3\infty} + k_2L_{1\infty} + k_2L_{3\infty} + k_3L_{1\infty} + k_3L_{2\infty}\right) + K_H^2\left(k_1k_2 + k_1k_3 + k_2k_3\right)\right)}$$

This last equation, however, involves several frequency dependent parameters that are also dependent on the propagation mode. In order to simplify (3.32), the products between two or more inductances are neglected since the resulting values are too small within frequency range of interest (i.e., $L_{x\infty} \times L_{y\infty} \approx 0$). Thus, applying this assumption to (3.32) to provide a model that can be more easily implemented, the following equation can be obtained [68]:

$$L_m \approx \frac{aK_{Hm}^2 + bK_{Hm}\sqrt{f}}{cK_{Hm}\sqrt{f} + df} \tag{3.33}$$

where $a = k_1k_2k_3$, $b = 2\pi\,(k_1k_3L_{2\infty} + k_2(k_1L_{3\infty} + k_3L_{1\infty}))$, $c = \pi\,(k_1k_3 + k_1k_2 + k_2k_3)$ and $d = 2\pi^2\,(L_{1\infty}(k_2 + k_3) + L_{2\infty}(k_1 + k_3) + L_{3\infty}(k_1 + k_2))$. On the other hand, K_{Hm} is calculated from the metal roughness [65]. The only drawback present when using (3.33) is that a curve fitting optimization is required to obtain the values of *a*, *b*, *c* and *d*. However, the validation with experimental data within the next chapter will show that an excellent model-experiment correlation for the inductance for both propagation modes is achieved when using this approach.

3.4 Interactions Between the Signal and Power Distribution Network and the Impact of the Differential Signaling

Data rates involving multi-gigahertz frequencies and low operating voltages, and the miniaturization of the devices accentuate the impact of noise including crosstalk, SSN, signal reflections, and power/ground noise. For this reason, the use of differential signaling has been encouraged for high-speed buses due to its common-mode noise rejection property. In this regard, it is useful to quantify the advantages of using differential signaling versus the SE counterpart in simple planar interconnects. Thus, in this section an experiment to systematically expose this is shown here by employing a full-wave electromagnetic solver (in this case HFSS [70]). The structure depicted in Fig. 3.7 was simulated in order to obtain the data in the frequency domain to be used later in time domain simulations to obtain intuitive but strictly quantitative figures of merit. The structure depicted in Fig. 3.7 consists of an edge-coupled stripline embedded between a ground plane and a power plane in which an aggressor signal is induced, attacking the signal traveling in the line. Once the *S*-parameters are obtained from the 3D simulation, the resulting six-port network containing the frequency domain data is used to obtain time

domain data using a circuit simulation software. Fig. 3.8 shows the schematic of the performed time domain simulation; as can be seen, four ports correspond to the edge-coupled stripline (i.e., P1-P4) and two ports correspond to the power plane (i.e. P5-P6). For the stripline, a pseudo-random bit sequence is chosen to feed it whereas a sine wave is induced at the power plane. This sine wave represents the voltage fluctuations in the voltage rail impacting the signal integrity in the stripline [71]. Therefore, the experiment consists in transmitting a differential- and a common-mode signal and compares the resulting eye diagrams, especially the eye height in which the induced noise impact is important.

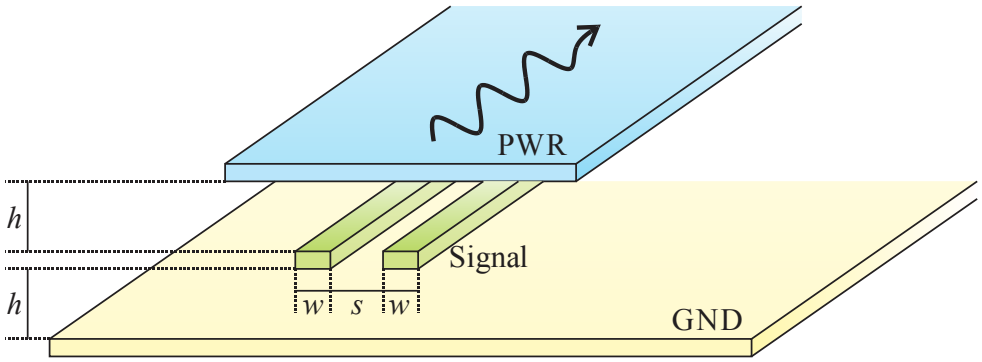


Fig. 3.7 Sketch of the structure simulated to quantify the impact of using differential signaling. The length of the stripline simulated is 10 cm.

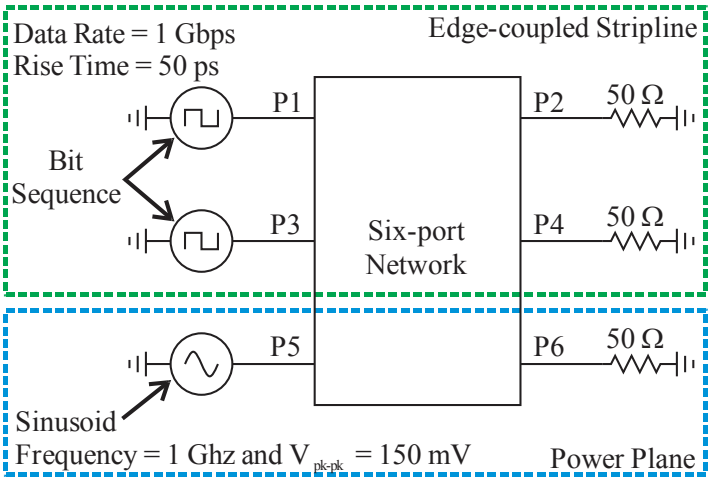


Fig. 3.8 Model implementation to perform time domain simulations from frequency domain data.

When the line is transmitting common-mode signals, both sources connected to P1 and P3 generate the same bit sequence. Thus, the original signal is recovered by dividing by two the sum of the voltages at P2 and P4. Notice that transmitting a common-mode signal is

equivalent to using single-ended signaling. As can be seen in Fig. 3.9, a significant amount of noise is added to the signal. As a result, the eye is reduced and for this particular case, the eye height is approximately 750 mV with a 1 V original signal. It is important to point out that this simulation considers only the homogenous part of the transmission line, whereas for a real channel it is necessary to consider the losses originated by the vertical transitions, connectors, electrical properties of the materials, second order effects related to drivers, etc. In this sense, having a loss in the eye height like the one shown in Fig. 3.9 might not seem so significant, however, considering the losses for the lengths found in real multi-transitioned channels may cause the link to fail when evaluating the particular metrics for a real bus.

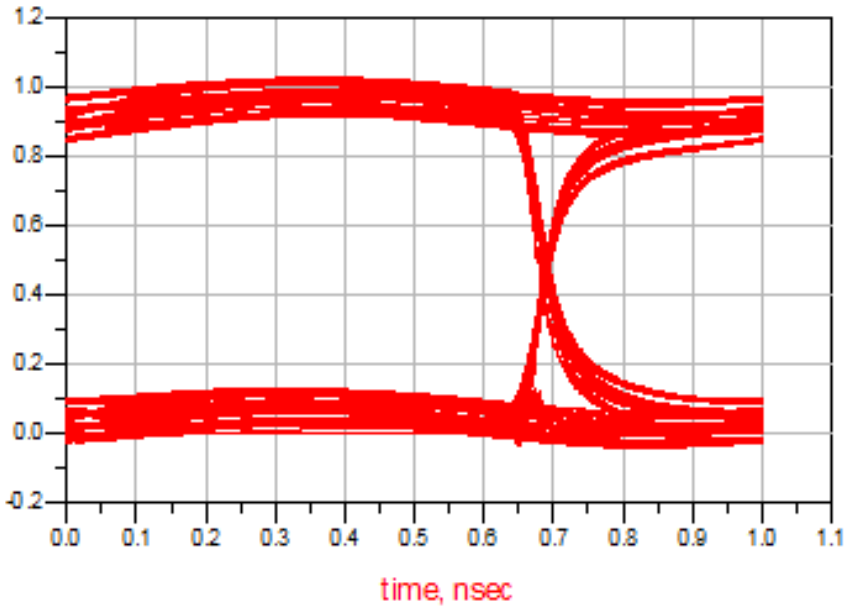


Fig. 3.9 Eye diagram from a time domain simulation using common-mode signaling.

On the other hand, when the line is transmitting differential signals, one source delivers the complementary signal of the other. This means that the bit sequence generated by one source will be the inverse on the other for a binary logic point of view. In this case, the original signal is recovered by dividing by two the subtraction of P2 minus P4. Fig. 3.10 shows the computed eye diagram for the differential signaling case. As can be seen, in this figure, the amount of noise added to the signal is much less. In this case, the eye height is approximately 900 mV; so, the gain in the opening of the eye is about 150 mV when compared to the common-mode case. This clearly evidences the main reason why differential signaling is the preferred data transmission scheme for modern high-speed buses.

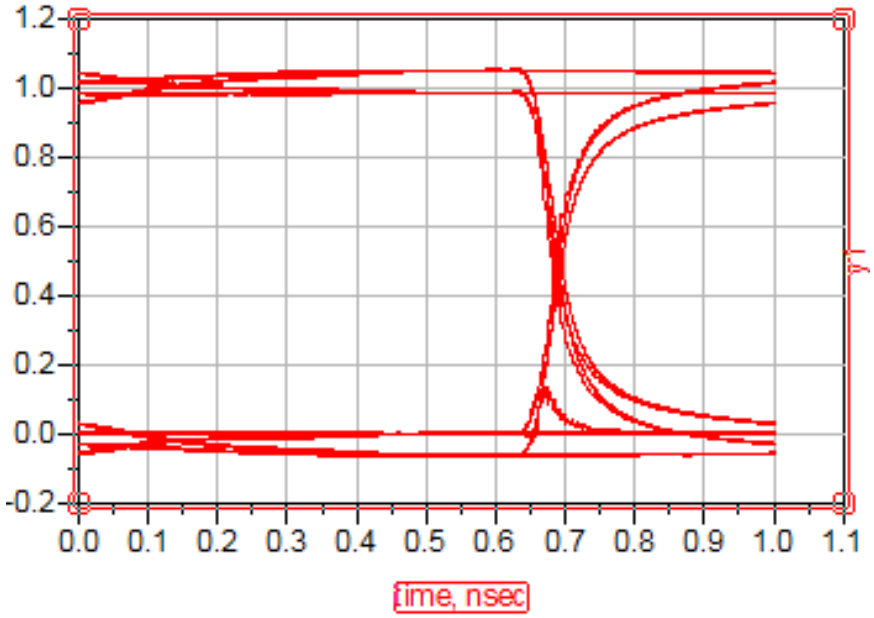


Fig. 3.10 Eye diagram from a time domain simulation using differential-mode signaling.

As can be seen throughout this section, using differential signaling is very helpful for transmitting signals within the multi-GHz frequency range. Moreover, a co-design methodology which involves signal and power integrity has been emerged when differential signaling is not available. For instance, current memory buses like DDR uses single-ended signaling due to its high density routing reaching data rates below 3 GHz. Additionally, in current devices there exist some rules of thumb when routing high-speed buses such as: avoid routing below or near to noisy power planes where a large amount of current is passing, if this cannot be avoided the recommended distance to the power plane is three times or at least two times the distance to the ground plane in order to force the signal to be referenced practically only to ground. Thus, even using differential signaling, it is important to bear in mind the interaction between the power and signal distribution networks in order to achieve a good signal integrity.

3.5 Conclusions

In this chapter, the equivalent circuit model proposed for a differential launch structure was derived. This approach considers the electromagnetic coupling present within the signal pads. This methodology takes advantage of the modal decomposition to manage each mode as a separate channel also discussed in this chapter.

In addition, a methodology to model a DTL considering the current-distribution dependent inductance on PCB was also presented. This study shows that the current

distribution will be dependent on the mode of propagation present in the DTL. Moreover, this current distribution as well as the coupling mechanisms specific to each propagating mode makes that current approaches to model the inductance of a single-ended line cannot be used to represent a modal inductance. As a result, using both approaches discussed through this chapter a DTL can be fully characterized using circuit-oriented models, which are intuitive and simple. Thus, commercial circuit simulators can be used to simulate a DTL whit all the advantages it has such as fast and low computational cost simulations.

Finally, an example of the impact in the eye height between using single-ended and differential signaling was presented. This study was performed by using a structure proposed in this thesis, which allows to observe how the noise is added to the signal and also points out the main advantage of using differential signaling. Besides, it is mentioned the importance of performing a co-design methodology involving power and signal integrity to achieve a good signal integrity of the transmitted data.

Chapter 4

Experimental Results

In order to demonstrate the accuracy of the proposed models for differential interconnects presented in Chapter 3, several DTLs with differential launch structures as adapters were fabricated on HDI technology. In this regard, a validation of these models was performed by reproducing measurements of scattering parameters up to 20 GHz and time domain waveforms with rise times in the order of picoseconds for the prototyped DTLs. With this purpose, a commercial circuit simulator was used so that block models for interconnects can be implemented to obtain results within the ranges of interest. The selected simulator is Agilent's Advanced Design System (ADS) because of its widely used in academy as well as in industry research teams [72]. In fact, the popularity of ADS is because of its reliability for performing model validations in both frequency and time domains. In this case, for the frequency domain, the validation of the proposal was carried out in both magnitude and phase of the *S*-parameters. Thus, it is demonstrated here that the proposal accurately reproduces experimental four-port single-ended and mixed-mode *S*-parameters. Furthermore, in the time domain is where the proposal presents its main advantage since accurate causal results are obtained, whereas most available models fail to achieve this goal.

4.1 Prototypes and Measurements

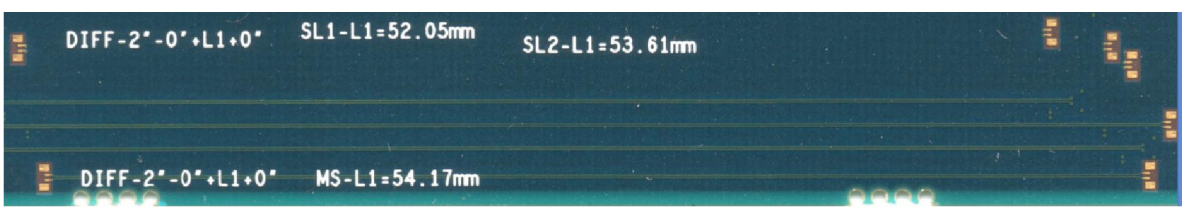


Fig. 4.1 High density interconnect (HDI) board showing the fabricated DTLs.

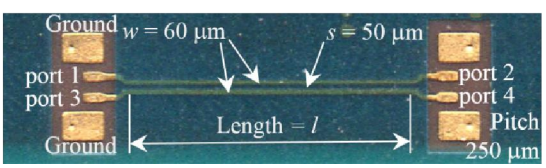


Fig. 4.2 Structure, dimensions and definitions used for the fabricated DTLs.

Fig. 4.1 shows the top view of the HDI board containing the fabricated DTLs used in this work. These lines present the same cross-section but different lengths and the PCB substrate is made of polyamide material with a thickness of 60 μm. The nominal relative permittivity and loss tangent for the substrate material at 5 GHz are ε_r = 4.3 and tanδ = 0.035, respectively, whereas the root mean square metal-dielectric surface roughness is h_{rms} = 0.5 μm. Details showing the dimensions of the DTLs including the terminations are shown in Fig. 4.2; notice that the lines present GSSG pad terminations with a pitch of 250 μm, and l = 53 mm, 79 mm, and 140 mm.

S-parameters were measured to the fabricated lines from 0.01 to 20 GHz using a four-port vector network analyzer (VNA). For this purpose, the VNA setup was calibrated up to the probe tips using an impedance-standard-substrate (ISS) and the short-open-load-thru (SOLT) procedure, which also allowed to establish a 50-Ω reference impedance. This calibration is necessary to allow the straightforward determination of the *ABCD*-parameters used in the proposed modeling and characterization methodologies. It is important to mention that the effect of the probing pads is not removed from the measurements since the modeling of the differential transitions is part of this dissertation.

4.2 Characterization and Modeling of the Differential Launch Structure

For the first step to obtain the experimental data to model the differential launch structure, the measured *S*-parameters were transformed from the four-port to the mixed-mode form to allow the separate analysis of the differential and common mode signal propagation as explained in the previous chapter. Due to the symmetry and tight couple of the signal traced in the fabricated DTLs, mode conversion is negligible within the considered frequency range. This is verified in Fig. 4.3, which shows that the corresponding matrix elements (i.e., the subsets $\mathbf{S}_{CD}$ and $\mathbf{S}_{DC}$) present magnitudes below –30 dB and can be neglected for practical purposes. In this regard, practical considerations in current interconnect design methodologies establish that mode conversion can be neglected when the corresponding S-parameters present magnitudes below –20 dB [73]; under this consideration, less than 10 percent of the power signal is converted into the other mode. For the prototypes fabricated here, where magnitudes below –30 dB are obtained for these parameters, less than 3 percent of the power signal is converted between propagation modes, which makes feasible to use the abovementioned criterion. An interesting observation in Fig. 4.3 is the fact that the mixed-mode *S*-parameters matrix is reciprocal, which means that $\mathbf{S}_{CD} = \mathbf{S}_{DC}^{-1}$, which is physically expected and is one indicative of the correctness of the data.

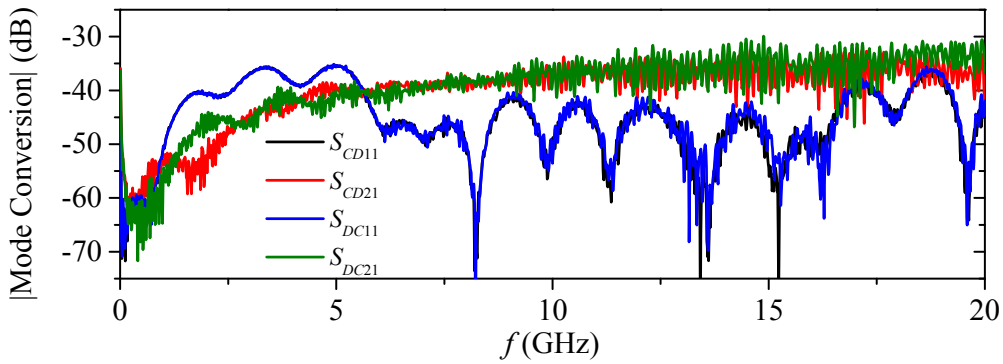


Fig. 4.3 Measured data showing negligible mode conversion (below –30 dB) for the fabricated DTLs.

Fig. 4.4 shows the GSSG configured probing pad used in to feed the fabricated DTLs. This differential launch structure is basically a differential CPW-to-microstrip transition as described in Chapter 3, Section 2. Therefore, the methodology proposed in that section can be applied straightforwardly to this prototype by separately analyzing each propagation mode. So, in order to determine the parameters of the equivalent circuit model of this transition firstly it is necessary to obtain the fundamental parameters of the transmission line for each mode using a line-line method; these parameters are the characteristic impedance (Z_c) and the complex propagation constant ($\gamma = \alpha + j\beta$). Fig. 4.5 and Fig. 4.6 show the experimental Z_c and γ, respectively for the measured DTLs. Notice that γ is a complex number, the real part (α) represents the attenuation suffered by the signal when it passes through the transmission line, whereas the imaginary part (β) represents the delay the signal suffers when passing through the transmission line. For this reason, Fig. 4.6 shows two sets of curves versus frequency for the modal complex propagation constant (i.e., one set for each mode).

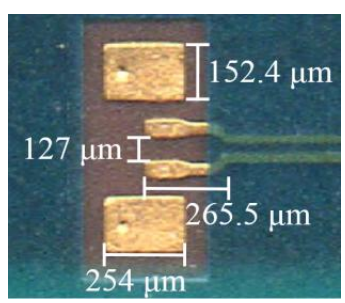


Fig. 4.4 Photograph of the transition used to feed the DTLs.

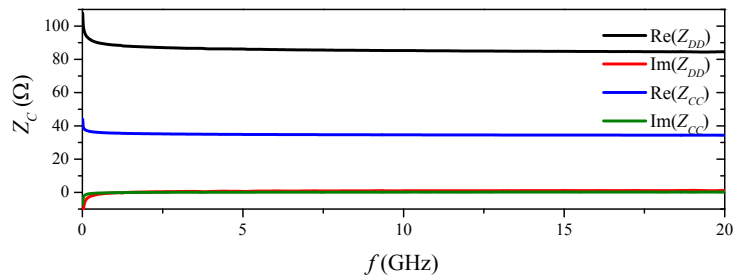


Fig. 4.5 Experimental characteristic impedance versus frequency for the homogeneous part of the DTL.

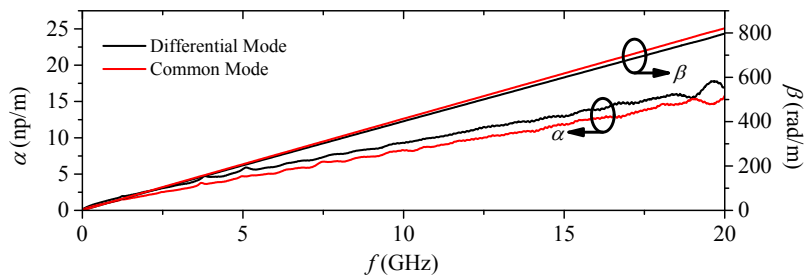


Fig. 4.6 Experimental attenuation and phase delay versus frequency for the homogeneous part of the DTL.

Once Z_c and γ are determined from experimental data for each mode, the methodology proposed in Chapter 3 is applied to obtain the equivalent circuit model of the differential launch structure. In this fashion, the shunt and series parameters used to represent the transition under study are obtained and the corresponding results are shown in Fig. 4.7 and Fig. 4.8, respectively. To illustrate the meaning of these parameters in an explicit way, Fig. 4.9 shows the block models for the modal representations of the DTL as well as for the complete differential structure with the respective equivalent models for the terminations.

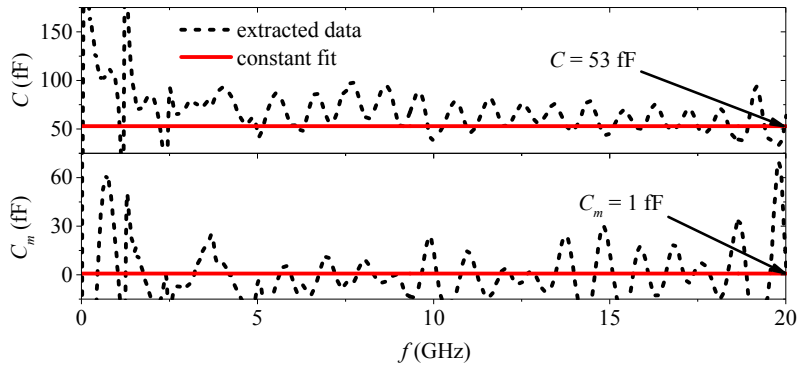


Fig. 4.7 Extracted capacitance and mutual capacitance of the differential launch structure using the proposed method.

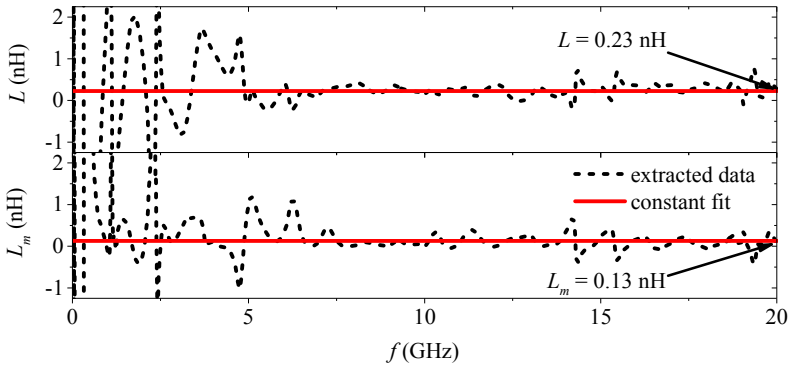


Fig. 4.8 Extracted inductance and mutual inductance of the differential launch structure using the proposed method.

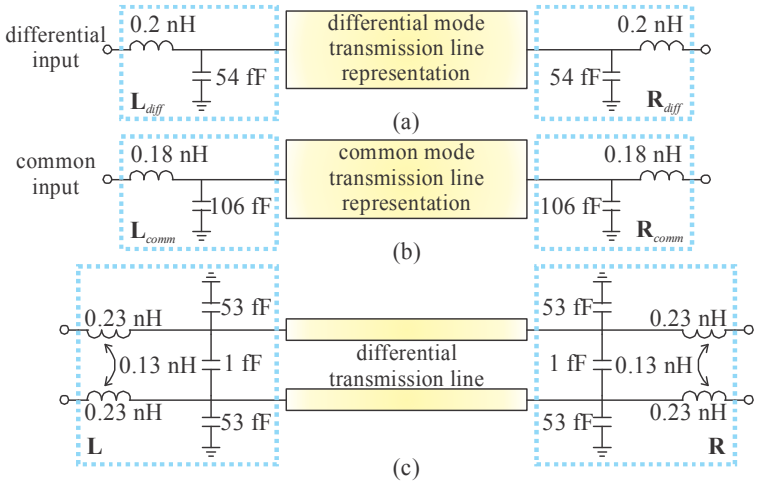
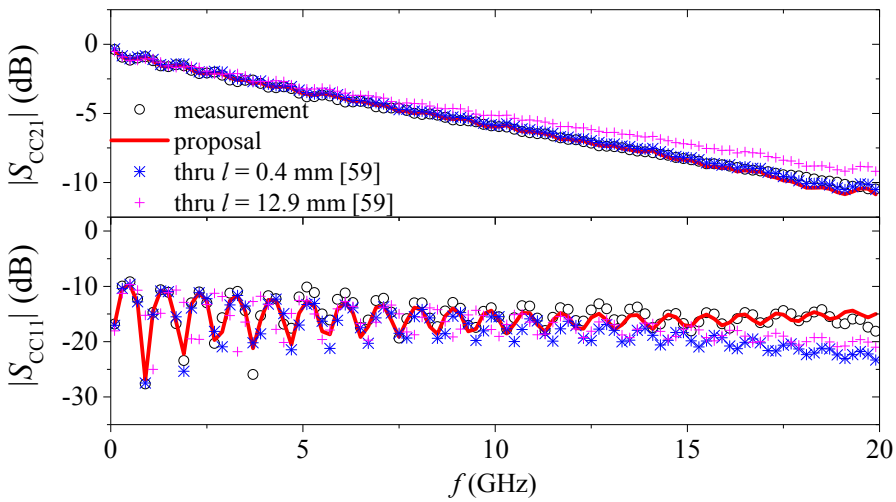


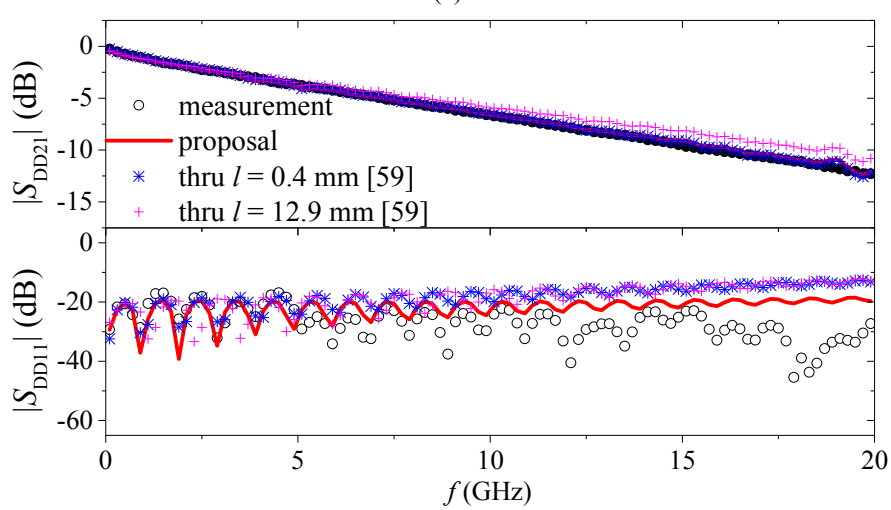
Fig. 4.9 Equivalent circuit models associated with the DTL including the coplanar waveguide to microstrip (CPW-M) transition and considering: (a) differential mode propagation, (b) common mode propagation, and (c) both modes simultaneously.

Once the experimental data associated with the differential CPW-to-microstrip transition is determined, the model for the complete structure was implemented in ADS for one of the characterized lines and the resulting simulation was compared with measured data in Fig. 4.10. Notice that an excellent correlation between the simulated and measured return and insertion losses ($|S_{11}|$ and $|S_{21}|$, respectively) is observed for both the differential and common modes. On the other hand, a comparison with the method proposed in [59] is also presented in Fig. 4.10. This last method uses only a thru test fixture to obtain the values of the elements that represent the transition assuming that the transitions can be connected with a zero-length line. Errors are introduced when assuming this since the electrical transition between the launch and the line is not considered. This problem is accentuated as the length of the line considered as a thru structure is increased as can be seen also in Fig. 4.10.

By means of a full-wave electromagnetic solver (i.e. Ansys' HFSS [70]), two thru test fixtures with the same dimensions for the transition described in the previous section but lengths of l = 0.4 mm and l = 12.9 mm were respectively simulated. As can be seen in Fig. 4.10, similar results are obtained for the methodology proposed in this work and the method proposed in [59] assuming that the thru structure is the line presenting l = 0.4 mm. In this case, a slight difference is observed in the return loss parameters. At first, the method in [59] seems to be a very efficient alternative to model this type of transitions; however, when a longer line is considered as the thru structure (l = 12.9 mm), the difference in the results increases significantly. Consequently, this methodology cannot be applied straightforwardly when an electrically short thru is not available.



(a)



(b)

Fig. 4.10 Simulated return and insertion losses for the line with l = 78.7 mm are compared with experimental data: (a) common, and (b) differential mode.

On the other hand, it is important to analyze the DTL not only in the frequency domain but also in the time domain in order to provide a more complete characterization of the structure. In this case, for analyzing the response of a DTL in the time (*t*) domain using the transfer function in the frequency domain, an inverse fast Fourier transform (iFFT) can be applied to the data. Thus, following the recommendations described in [65], a model to perform *t*-domain simulations was implemented in ADS using the experimental *S*-parameters of the DTLs, but also those obtained using the proposal and the method described in [59]. In this regard, Fig. 4.11 shows the corresponding *t*-domain waveforms. As can be noticed, the experimental data, the model proposed here, and the method described in [59] using a short line as thru exhibit similar results. On the other hand, when using a long line as thru, a significant difference is present. Eye diagrams are also obtained from simulations in the *t*-domain using experimental data and the proposal; the results are plotted in Fig. 4.12. As can be seen, similar results are obtained in both cases since the difference between the margins of the eye height and eye width in the two diagrams are around one percent.

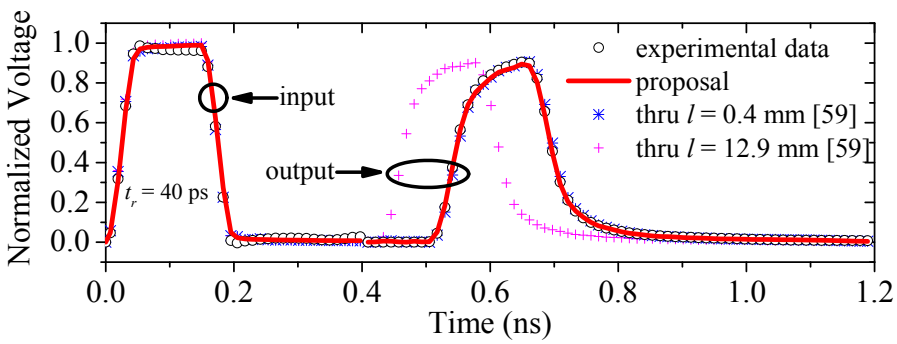


Fig. 4.11 Confrontation in the *t*-domain of the waveforms obtained by applying iFFT to data in the frequency domain for the DTL with l = 78.7 mm. The data used for the transformation correspond to three cases: experimental data, data obtained using the proposal, and data obtained using the method proposed in [59].

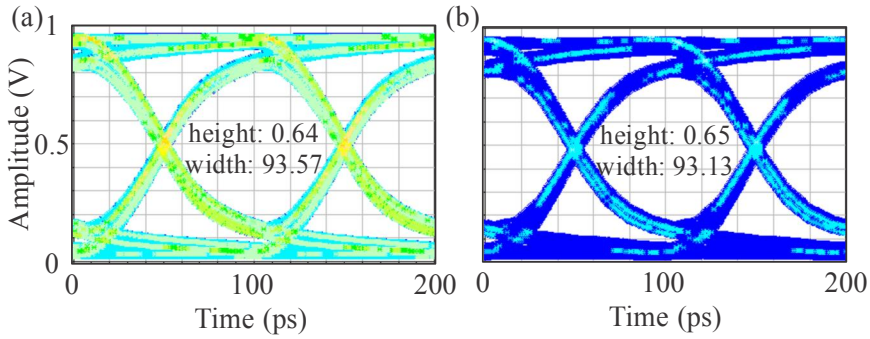


Fig. 4.12 Eye-diagrams obtained from the *t*-domain waveforms shown in Fig. 4.11. A data rate of 10 Gbps was assumed to be propagated through the DTL in differential mode. In this case, the considered data was obtained from the transformations applied to: (a) measured data, and (b) proposal.

4.3 Characterization and Modeling of an Homogeneous DTL

Following with the characterization of the measured DTLs, now that Z_c and γ are obtained for each mode, it is possible to obtain the *RLGC*-model parameters of the homogenous part of the DTL with the methodology described in Chapter 3. Fig. 4.13 shows these parameters obtained using (3.23). As mentioned in Chapter 3, using previously reported approaches for *R*, *G*, and *C*, excellent model–experiment correlation are achieved for these three elements within the entire bandwidth of interest in both propagation modes. This can be verified in Fig. 4.13. Conversely, Fig. 4.14 shows the model-experiment confrontation in the *f*-domain for the inductance.

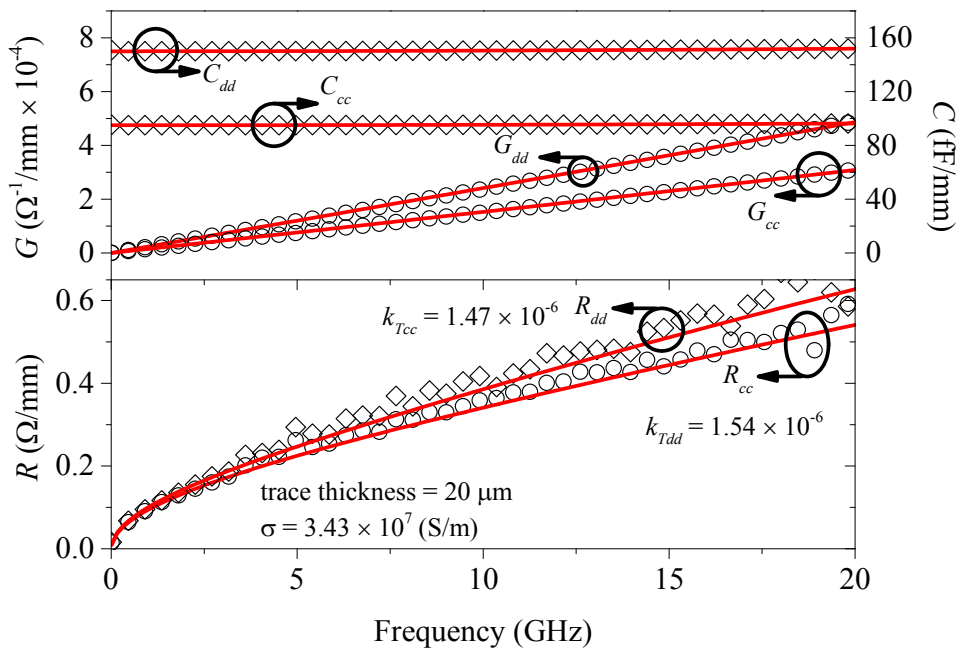


Fig. 4.13 Curves showing the model-experiment correlation for G_m, C_m, and R_m. Symbols represent the experimental data and solid lines represent the models.

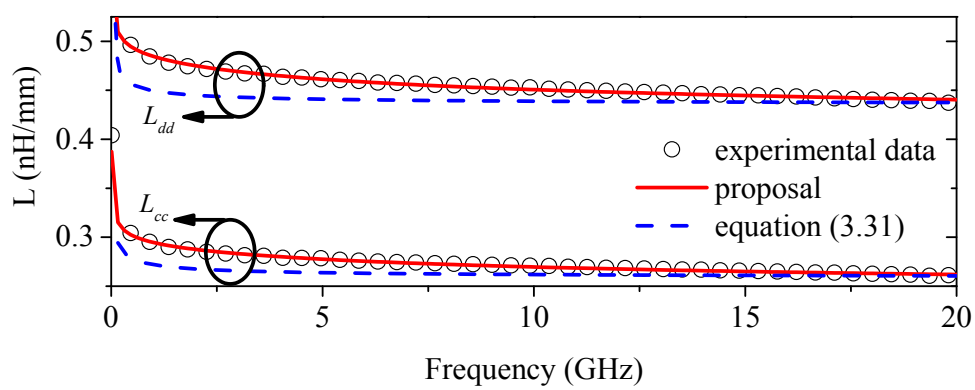


Fig. 4.14 Curves showing the model-experiment correlation for the inductance in common and differential propagation modes.

As can be seen, when using the traditional model for the inductance defined in (3.27), a noticeable discrepancy below 10 GHz is observed. This discrepancy is associated with an incorrect representation of the effect of the current distribution occurring for each propagation mode. In this regard, at relatively high frequencies, the current distribution is saturated at the edges of the signal trace and the inductance can be approximately reproduced using (3.27), where the value of the inductance is practically a constant. In contrast, when using the proposed equation (3.31), excellent correlation is achieved within the entire bandwidth of interest since now the current distribution behavior is considered. In this case, after performing the curve fitting optimization, the values of the parameters *a*, *b*, *c* and *d* in (3.31) are:

Constants	Common Mode	Differential Mode
a	$1.30 \times 10^{-2}\ \Omega^3$	$1.27 \times 10^{-2}\ \Omega^3$
b	$2.23 \times 10^{-5}\ \mathrm{H}\Omega^2$	$1.31 \times 10^{-5}\ \mathrm{H}\Omega^2$
c	$9.01 \times 10^{4}\ \Omega^2$	$8.80 \times 10^{4}\ \Omega^2$
d	$1.19 \times 10^{-1}\ \mathrm{H}\Omega$	$1.19 \times 10^{-1}\ \mathrm{H}\Omega$

Table 4.1 Constants obtained to represent *L* for both propagation modes.

Once the *RLGC*-model parameters for both modes are obtained and represented using the models described before, the number of stages to represent the DTLs are calculated. In order to achieve this, several *RLGC* cells are concatenated and simulated in Agilent's ADS to obtain the *S*-parameters of the complete structure for the differential and common mode propagation. For instance, for this particular experiment, the number of concatenated cells is 156, that allows representing a total length of 78 mm, whereas the physical length of the characterized DTL is 78.7 mm. Afterwards, the single-ended *S*-parameters of the DTL are obtained by means of a mixed-mode to four-port *S*-parameter transformation. Fig. 4.15 shows that an excellent correlation between the simulated and measured return and insertion losses as well as the near- and far-end crosstalk (S_{11}, S_{21}, S_{31}, and S_{41} respectively) is achieved in magnitude and phase when using the proposed model to represent the DTL's inductance. Fig. 4.16 shows that also accuracy is achieved when modeling the mixed-mode *S*-parameters. In this regard, since Fig. 4.15 and 4.16 show that an excellent agreement is obtained for the single-ended and mixed-mode *S*-parameters, this means that the mode conversion is low enough to assume its negligible effect and treat the differential and common mode as two independent single-ended channels. In addition, it is interesting to observe that the simulations obtained when using (3.27) yield similar results, exhibiting only a barely noticeable difference. These results could lead to incorrectly establish that the

error associated with an inappropriate modeling of L can be neglected. Nevertheless, model–experiment correlation in the frequency domain only guarantee the behavior of the *RLGC* elements in frequency and does not imply that the model is causal which is an important property when implementing electric models for practical purposes. In this regard, analysis in the *t*-domain must be performed to verify the validity of a model under actual circumstances.

As mentioned above, a *t*-domain analysis needs to be performed in order to verify the behavior of the *RLGC* model and guarantee that the model represents correctly the DTL in this domain. For this reason a sanity check for the proposal must be done to guarantee *t*-domain simulations with good quality.

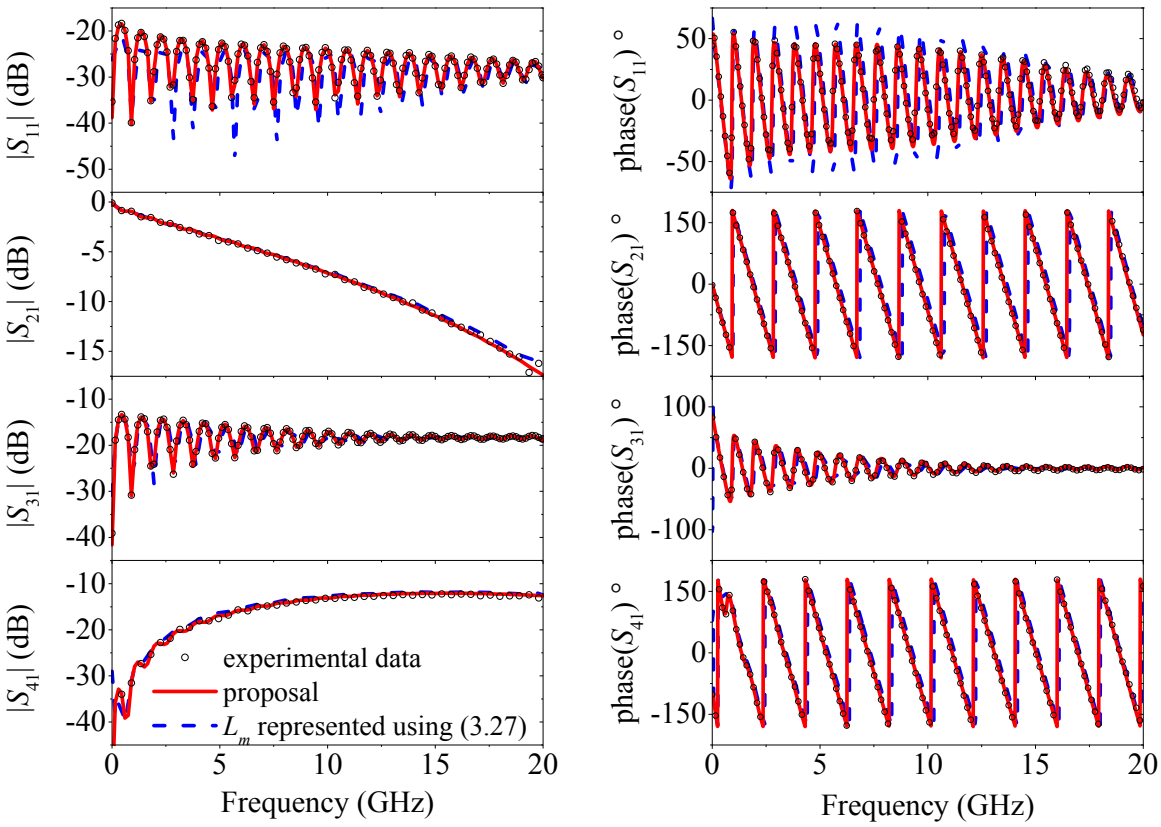


Fig. 4.15 Experimental and simulated single-ended *S*-parameters plotted for confrontation purposes. The length of the homogeneous part of the line is l = 78.7 mm (156 stages were concatenated).

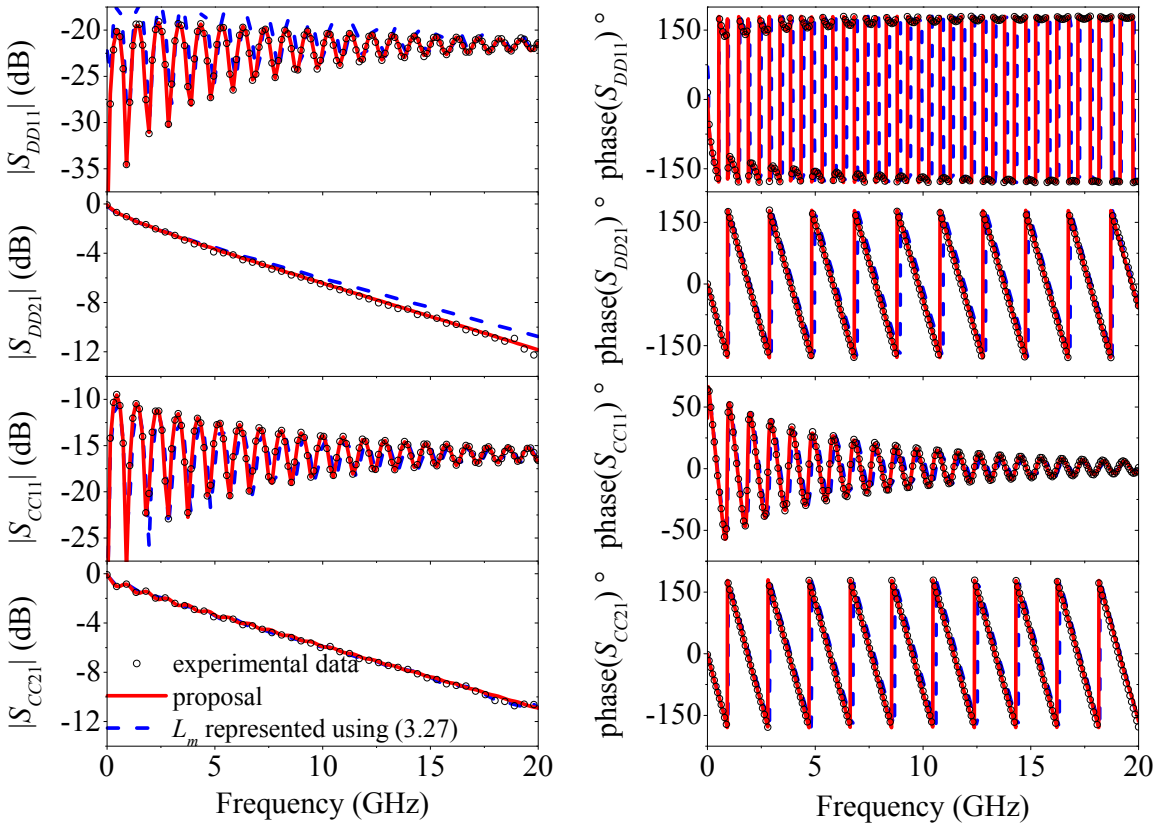


Fig. 4.16 Experimental and simulated mixed-mode *S*-parameters plotted for confrontation purposes, the length of the homogeneous part of the line is l = 78.7 mm (156 stages were concatenated).

4.4 Discussion about Time Domain Simulations using *S*-Parameters

In the industry, the electrical link verification is usually done in the time domain. Thus, the eye mask and bit error rate tests are used to make the decision if the link passes or fails. On the other hand, RF engineers prefer frequency domain measurements using vector network analyzers in order to cover frequency ranges up to hundreds of gigahertz with its inherent advantages (e.g., large signal-to-noise ratios). An additional advantage of data in the frequency domain is that full-wave solvers also provide information about the device under test in this domain that most of the times can be directly compared with measured data. Thus, it is desirable to systematically carry out time domain simulations using models with frequency data for assessing the performance of an interconnection link. For this reason, the quality of the *S*-parameters is of great importance and must fulfill a series of criteria to guarantee the quality of the time domain simulations. In order to analyze the details to be considered when performing these simulations, representations of homogeneous sections of a differential line are analyzed afterwards.

According to [74], there are several criteria to establish the characteristics of an *S*-parameter set to be used for representing a DTL in the *t*-domain, such as: the end/start frequency, the frequency step size, the stability/passivity of the model, if the model is causal or reciprocal, and the accuracy/noise of the data. These criteria will be discussed in detail next.

Frequency Step Size

In the case of the frequency step size (*df*), according to Fourier theory, this must be related to the periodicity (*T*) in the time domain as $T = 1 / df$. This means that no channel with a propagation delay greater than *T* can be accurately modeled by *S*-parameters sampled at a spacing *df*. It follows that for a propagation delay of approximately 0.5 ns and a dielectric constant of 4.3, as in the prototype used here, steps smaller than 2 GHz are required. In our case, the frequency step used in the *S*-parameters set is 10 MHz which would allow the representation of lines presenting a length up to 14.5 m; the prototype used here includes lines with a maximum length of 7.8 cm.

In this regard, the main effect caused by an undersampled *S*-parameters set is the presence of aliasing in the time domain simulations which is not our case.

Start Frequency

It is well known that a start frequency of 0 Hz (DC) is the best choice; however, this is not possible to obtain using currently available test equipment (the characteristic impedance of a line at 0 Hz tends to infinity). A rule of thumb is to select the starting frequency point equal to the frequency step but in general unavailability of low frequency data will have an impact. If the DC value is missing, the response in the time domain is shifted down since the DC Fourier coefficient is half the arithmetic average of the signal. To solve this problem data can be extrapolated to DC; this approach is used in the S-parameters set we are using in the validation process. As can be seen in Fig. 4.17, the response at the end of the DTL we are obtaining does not exhibit the shifting related to not having the DC data when a pulse is injected into it.

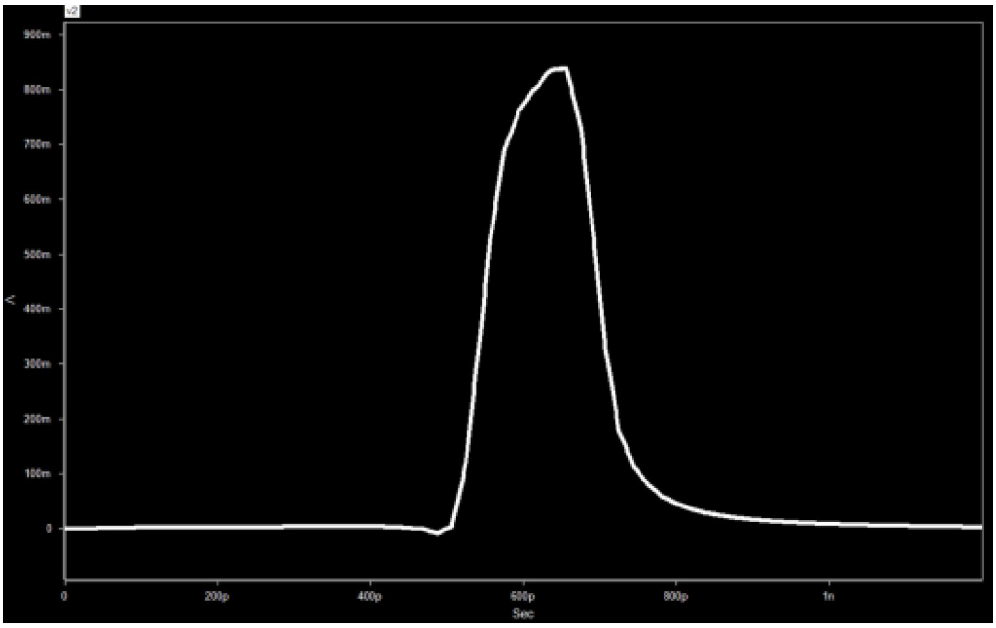


Fig. 4.17 Pulse response of a DTL using the S-parameters obtained by applying the proposal.

Stability/Passivity

Currently, in the literature there exist some approaches to check stability or passivity such as the rational function methodology. However, a simpler test to check stability and passivity is to obtain the impulse response and simulate a long time. If the model is not passive, a ringing associated with convergence and numerical stability problems will be present (see Fig. 4.18). As can be seen in Fig. 4.17, the pulse response finishes before 1 ns. Thus in order to check this criteria in our model, a simulation up to 400 ns was carried out without seeing any stability issue.

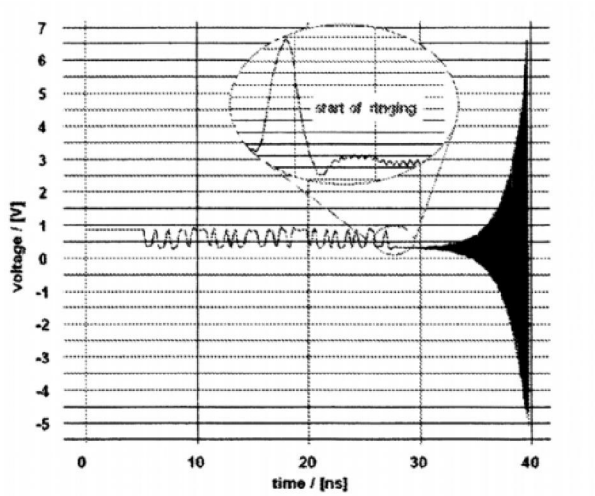


Fig. 4.18 Time domain simulation for a link with a non-passive model [74].

Causality

This is a very important property of any real passive system. In this regard, small causality violations can be found even using measured data directly in time domain simulations. This issue can be explained with the frequency range included in the *S*-parameters. In fact, truncating the frequency response of any channel results in causality violations (e.g. ripples or ringing) which are more pronounced the higher the spectral energy of the signal near the end frequency is. Thus, choosing a proper end frequency is very important to perform time domain simulations using *S*-parameters.

Thus, to analyze the response of the proposal for the homogeneous part of the DTL in the time domain and verify this criteria the model shown in Fig. 4.19 was implemented, where a four-port network containing discreet data in the frequency domain was used. Again, the simulations were performed using Agilent's ADS, which allowed to obtain results in the time domain by applying iFFT. For this purpose, the single ended stimuli shown in Fig. 4.19 were considered since these particular waveforms excite both common and differential modes of the DTL. This can be easily verified when superposition is applied: the waveform in 4.19 is half common mode and half differential mode. Notice in Fig. 4.20 that the waveforms obtained when using the model for L_m considered in this dissertation accurately reproduce the curves obtained when using experimental data for the time domain simulation. In contrast, when the equation (3.29) is used, the corresponding waveforms exhibit a non-causal anticipation. This problem is evident in the time domain; nonetheless, the characterization of L in the frequency domain can also explain this behavior. Since the capacitance and inductance are involved in the dispersion of a non-TEM transmission line, the correct modeling of these parameters is important to ensure the causality property of the models. In this sense, the dispersion is related to the Kramers-Kronig relationships, which must be satisfied to ensure causality [65]. Hence, the incorrect modeling of the inductance results in an incorrect dispersion characterization leading into causality problems for the model of the DTL. Moreover, since SPICE-like simulation tools are standard for high-speed circuit designers, simulations in the time domain were carried out using Synopsis' HSPICE to verify the applicability of the proposed model; in this case, the same results as those obtained when using Agilent's ADS were achieved. Bear in mind, that the simulation in HSPICE was carried out using the data corresponding as in ADS. Thus, even though HSPICE can use the tabular *RLGC* model directly to perform time domain simulations, the data is configured in the Maxwellian format and considers the four parameters as $n \times n$ matrices with non-zero values for R and G outside the main diagonal for n coupled-lines. This means that coupling resistance and conductance elements are needed to define the model in this fashion, which are very difficult to obtain without a field solver. For this reason, a touchstone file that represents the DTL in the frequency domain is used instead to verify the validity of the proposal in HSPICE. Moreover, by using the touchstone

file it is possible to use S-parameters directly in the time domain simulation which is the purpose of this analysis.

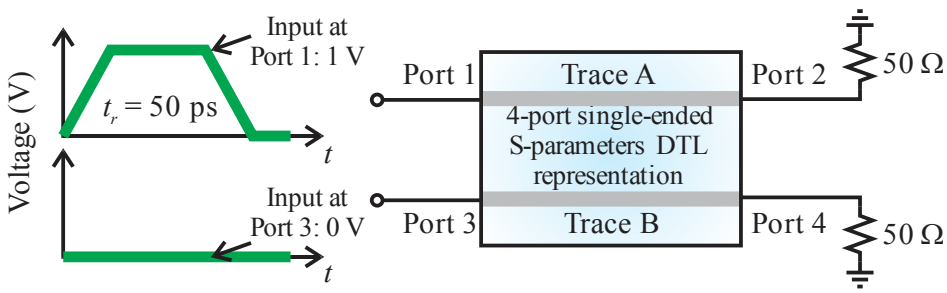


Fig. 4.19 Model implementation to perform time domain simulations from data in the frequency domain.

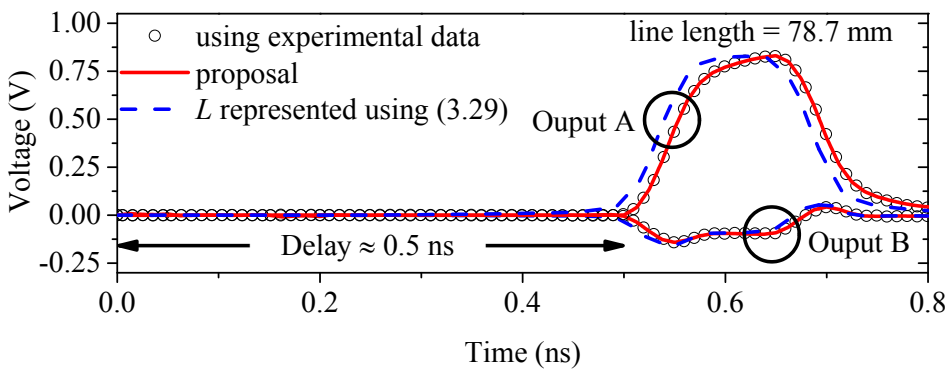


Fig. 4.20 The waveforms compare the results when using experimental data, the proposal, and the typical model for *L*.

Reciprocity

Passive channels without non-reciprocal elements (e.g., ferrites) must show reciprocal *S*-parameters. This means that $S_{ij} = S_{ji}$ where $i \neq j$. Reciprocity offers an *S*-parameters quality evaluation easily. The S-parameter set used for the time domain simulation here exhibits great reciprocity. In [74], it is reported that a good reciprocity is achieved when the difference between forward and reverse parameters is within +/- 0.25 dB; in this work, reciprocity is preserved within 0.05 dB. Fig. 4.21 shows a set of S-parameters obtained from the proposal. As can be seen in this figure, great reciprocity is observed for all the parameters involving return loss, insertion loss, near end crosstalk (FEXT) and far end crosstalk (NEXT).

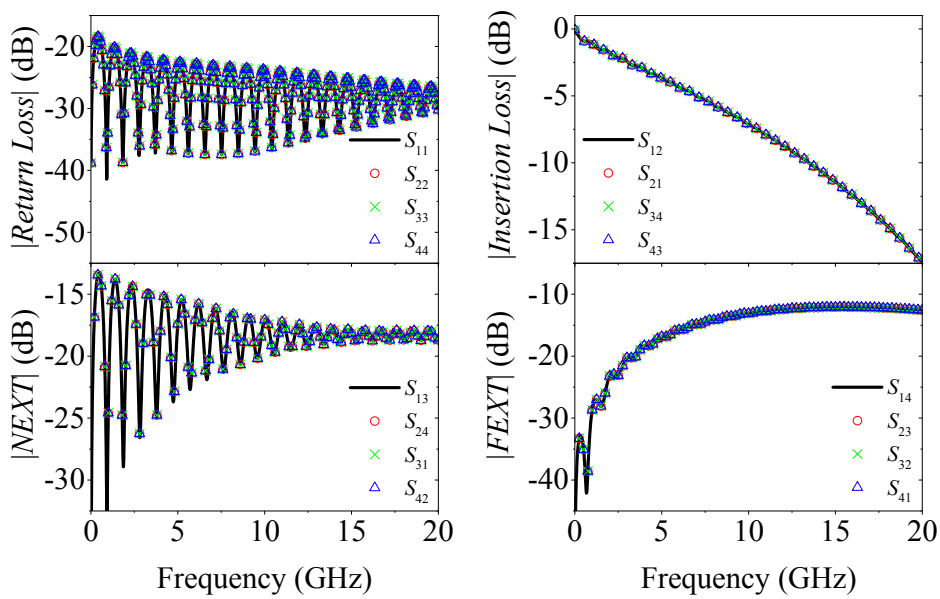


Fig. 4.21 S-parameters obtained from the proposal showing great reciprocity.

Accuracy/Noise

The accuracy of the *S*-parameter measurements is mostly determined by the quality of the calibration process as well as the correct technique to assure contact of the probe tips with the pads of the device under test. In this case, the calibration was carried out just before starting the measurements and verifying that the scratches made by the probe tips were visible but without stressing them.

End Frequency

This criteria was left at the end, since it determines the quality of the *S*-parameters in large degree. In addition, a set of simulations probing this criteria was performed to check the quality of the S-parameters obtained from the proposal.

As is mentioned above, truncating the frequency response of a channel will cause issues when using S-parameters for time domain simulations. For this reason, choosing the correct end frequency value has a very important impact in the quality of these simulations; nevertheless, the decision on what value is the correct is somewhat arbitrary. In this sense, the end frequency value should be high enough to cover the needed frequency content of the signal passing through the channel. It has been found that an end frequency of 4.5 times the inverse of the unit interval of the signal guarantees a coverage of nearly 96% of the spectral power for a channel with perfect transmission. It follows that for a signal period of 200 ps, it is necessary to have frequency data up to 22.5 GHz. On the other hand, commercial circuit simulators like HSPICE or Agilent's ADS require that the end frequency value be the inverse of the fastest transition to be simulated. This means that for a rise or fall time of 50 ps, the end frequency value must be 20 GHz. Thus, in order to

verify this criteria a time domain simulation is carried out using HSPICE varying the end frequency and observe until which minimum value the simulation still being accurate. This simulation uses the circuit depicted in Fig. 4.17, where the time rise and time fall are symmetrical and equal to 50 ps. The pulse width is 100 ps; so, the unit interval is 200 ps for the single ended stimuli applied at port 1. Therefore, it is necessary to have up to 22.5 GHz or 20 GHz to meet requirements defined above. In this sense, HSPICE allows to specify the maximum frequency value used to perform the Inverse Fast Fourier Transform in the transient analysis. Additionally, it is possible to specify the method to extrapolate higher frequency points or to cut off the data as in the case of this simulation. Therefore, a series of simulations were carried out systematically decreasing the end frequency value and not allowing extrapolation to higher values. As can be seen in Fig. 4.22, the proposal can accurately reproduce the response when using measured data with a frequency end of 13.5 GHz. Below this value, the proposed model starts failing. In this case, an end frequency value of 13.5 GHz corresponds to a rise time of approximately 74 ps. As a result, having a good modeling of the device under test may allow to relax this fundamental criteria up to certain extent. Consequently, this analysis can be useful when obtaining experimental data from the equipment without enough bandwidth for the desired simulation.

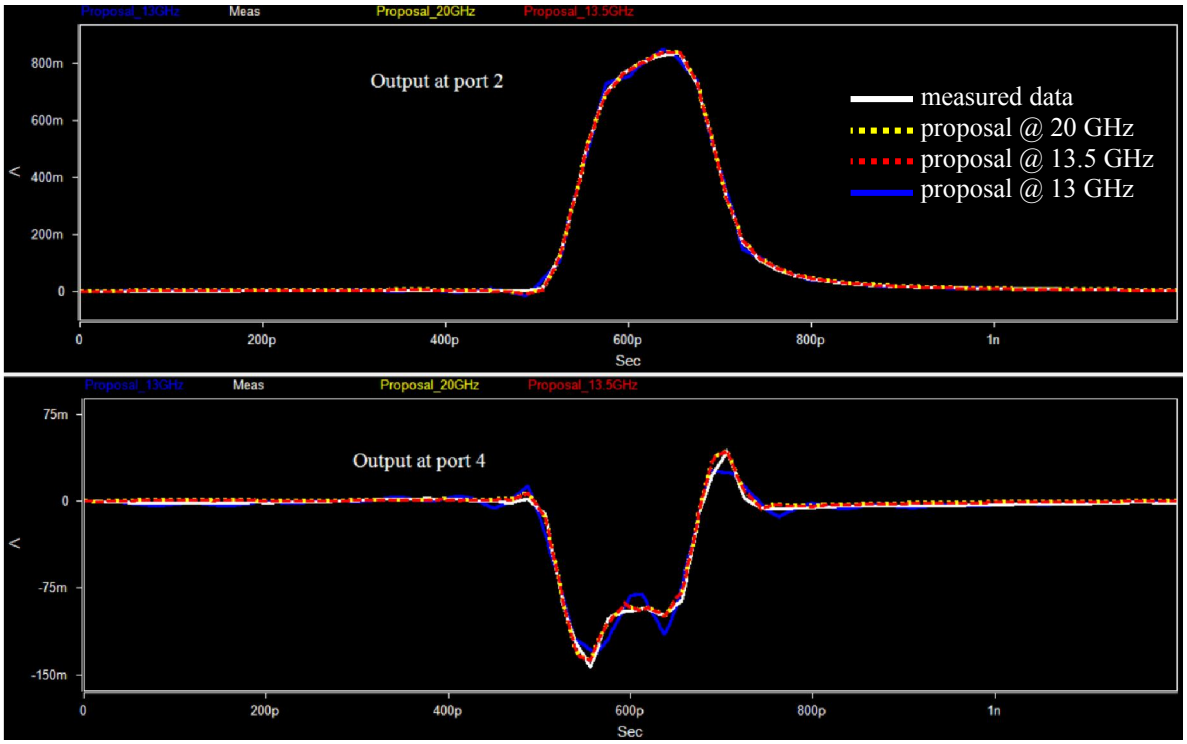


Fig. 4.22 Comparison between the results of the time domain simulation using measured data and the proposal with different end-frequency values.

Finally, as a result of applying the proposed methodology, an accurate modeling of DTLs fabricated on PCB technology using the extracted data and an equivalent circuit for the interconnect has been demonstrated up to 20 GHz, but also in the time domain with a rise time as small as 50 ps. Thus, the proposal represents a valuable tool when characterizing this type of interconnects for either optimization or modeling purposes.

4.5 Conclusions

In this chapter, the topologies proposed in Chapter 3 for the characterization of a differential launch structure as well as the homogeneous part of a DTL were verified and validated with a set of DTLs fabricated on an HDI PCB prototype. In this regard, the quality of the S-parameters used in the time domain simulations were verified. This analysis considers several criteria that must be met in order to obtain reliable time domain simulations. On the other hand, it was also shown that having a good modeling of the device under test allows to perform accurate time domain simulations even when some traditionally established criteria are not fulfilled completely.

Additionally, as can be noticed through the process of validation, the model proposed for the characterization of DTLs relies on the availability of measured data. In this case, microstrip DTLs were analyzed; however, the proposed methodologies can be used to analyze other types of differential transmission lines such as striplines which are very common in modern electronic devices. Therefore, the models proposed show the adaptability to new circumstances.

Finally, the models proposed allow to characterize DTLs up to expected data rates for modern differential buses. Thus, the proposal also helps in the reduction of time and computational costs of analysis of differential buses since most of the times these analysis are made with 3D full wave simulators. Moreover, the proposal also can be used for optimization purposes since an electrical circuit is more intuitive and helpful for circuit designers. Moreover, the results shown in this chapter allow to point out the importance of verifying models for differential interconnects in both time and frequency domains.

Chapter 5

General Conclusions

A detailed analysis allowing physically-based characterization and modeling of on-PCB differential transmission lines in the frequency and time domain was carried out in this thesis. This analysis is based on the systematic processing of experimental data, whereas the representation of each physical effect occurring in the differential transmission line is achieved with distributed models consisting of cascaded circuits containing RLGC lumped elements. As a result of the analysis performed to differential transmission lines, some observations and important conclusions are presented in this final chapter.

5.1 Differential Interconnections versus Noise Rejection Structures

A differential transmission line is used in modern electronic devices to achieve higher data rates since it presents attractive advantages for circuit designers such as excellent common-mode noise rejection characteristics. The importance of this particular feature relies on the fact that in advanced technologies the noise introduced by vias and transistors switching (i.e. SSN) can even let the interconnection channel useless at high frequencies. Bear in mind that special isolation and noise mitigation structures have been developed to prevent the effect of this noise, for instance, EBGs. However, the relatively large size and the use of additional metal layers to form the periodical structures required for implementing EBGs within a PCB is a very expensive alternative. In addition, these periodic structures allow to reject noise only within a narrow band in the frequency domain; so, this alternative is not useful when wide-band communication is required. For this reason, differential transmission lines are preferred in current systems due to its advantages and relative simplicity. In consequence, the modeling of these interconnections is very important for signal integrity engineers. Still, the alternative structures covered in this thesis can have a potential application in the future when the data rates reach high enough values, so, the space required in the prototype may be feasible or when the metal losses in a copper trace let inoperable the interconnection channel.

5.2 Conclusions and Contributions

The main objective of this dissertation is to present physically-based circuit-oriented modeling and characterization techniques for differential interconnects including transitional structures. The models are intended to be used to perform simulations in both frequency and time domains. Thus, in order to achieve this objective, the analysis presented throughout this dissertation takes advantage of the modal decomposition so that each signal

propagation mode can be treated as a separate channel. As a result, existing single-ended approaches could be applied straightforwardly. However, as explained in Chapter 3, additional aspects should be considered when operating a differential interconnect at high frequencies; for instance, the fact that the inductance of the line cannot be represented using previous models and a novel implementation was needed.

In order to develop the modeling methodologies for the differential transmission line, measurements of these interconnects were carried out to allow the computation of the corresponding fundamental parameters as explained in Chapter 3. In this regard, in order to measure differential transmission lines, the use of adapters is needed. Moreover, to carry out reliable high-frequency experiments, probing pads are usually required to allow measurements with coplanar microwave probes. Nevertheless, these adapters introduce parasitics that can be seen as electrical discontinuities which yield mismatch between the probe tips and the transmission line. Therefore, the modeling of a differential terminations like the one presented in Fig. 4.4 is very important to reduce the uncertainty of the data extracted of the differential transmission line as mentioned in Chapter 3 when using single-ended probes. Thus, the corresponding results obtained from the analysis of the transitions could be useful for optimization purposes and to study the sensibility of the parameters of the model to a given de-embedding procedure.

Additionally, in this dissertation it was verified that single-ended approaches for modeling the inductance of a transmission line cannot be applied to the modal representation of a differential transmission line. The additional consideration to be taken into account in this case is the effect of the current distribution on the dispersion characteristics of the line, as well as its dependence on the operating propagation mode. Fig. 3.6 shows how the current is confined depending on the propagation mode. It is important to mention that this effect cannot be neglected for the inductance of a differential transmission line. In contrast, the resistance, the capacitance, and the conductance can still be represented acceptably using traditional models, which is verified in Chapter 4 (Fig. 4.13).

On the other hand, two extra analyses were carried out in this dissertation. Firstly, the analysis of the difference in the impact observed in the eye height for an eye diagram when using differential and common-mode (i.e., single-ended like) signaling. This analysis helps to understand how the common-mode noise is added to the signal and then how it is removed when a differential receiver is part of the interconnection channel. Moreover, this analysis points out the need for a co-design methodology between power and signal delivery networks when differential signaling is not available. In addition, a second analysis performed here is related to verify the quality of the *S*-parameters obtained from the proposal. In this case, the objective of this analysis is to verify that a good modeling in the frequency domain allows to relax the criteria to perform effective and reliable time domain simulations. This is useful particularly when using measured data to perform time domain

analysis since the equipment not always allows measuring up to the desired maximum frequency value.

It is important to remark the fact that the modeling techniques presented in this thesis are based on measurements and equivalent circuit model implementations. Thus, the proposal is appropriated to reduce the time and computational cost of analysis of differential buses avoiding the use of full-wave simulations with its well-known limitations for designing complex circuits. Moreover, the use of an equivalent circuit model helps to understand in a more intuitive way the effect of the parasitics introduced by the interconnection on a signal that is propagated throughout it. In addition, although the validation is carried out with relatively simple structures, it gives important insights into the behavior of differential transmission lines in more complex structures such as packages. Consequently, the analysis presented in this thesis becomes more important these days since modeling techniques for packages are one of the most important areas studied for signal integrity engineers due to the importance of these structures in today's electronic industry.

In accordance to the previous discussion, the contributions of this thesis can be summarized in the next points:

1. The main contribution derived from the analysis presented throughout this thesis is the implementation of a novel formulation for representing a differential transmission line in the frequency and time domains. This approach is the result of the analysis of the current distribution on a differential transmission line depending on the operating propagation mode, obtaining a very accurate representation of the interconnection.

2. The analytical modeling of a differential launch structure which introduces non-desired effects. For this reason, the correct modeling of these structures using the proposal presented here allows to reduce the uncertainty in the extracted data of the device under test. Moreover, the proposal can be used to assess the susceptibility of a device under test to a specific de-embedding procedure.

3. A very important conclusion of this dissertation is the fact that both the frequency and the time domain must be analyzed. As can be seen in Chapter 4 (Fig. 4.15, 4.16 and 4.20), the results showed that the measured data is well represented in the frequency domain using single-ended approaches for the inductance whereas in the time domain these approach is not valid and non-causal results were obtained.

4. The use of 4-port single-ended to mixed-mode *S*-parameters transformation is a very powerful and useful tool to study and analyze differential interconnections. Thus, a reliable way to extract the parameters of the RLGC equivalent circuit

model for the homogeneous part and the simplified LC model for the transition of the differential transmission line is discussed using this approach.

5.3 Future Work

Future research is proposed to overcome the problems in the modeling of differential transmission lines in this dissertation. For this reason, in this final part of the chapter, some research topics are discussed.

In the near future, an analytical methodology to model the inductance in a differential line must be developed. In this thesis, a semi-empirical modeling methodology was presented. Therefore, an important research opportunity is the development of techniques to obtain the corresponding parameters using closed-form expressions.

On the other hand, actual differential interconnections are not planar but have vertical interconnections such as vias. Thus, another research opportunity is to obtain the equivalent circuit model of a differential via pair. As in the case of the planar interconnections analyzed in this dissertation, the current distribution in the barrel of the via may be affected by the propagation mode. In fact, since vias do not have a well-defined return path for the current this effect may be accentuated.

Finally, the needed of a co-design methodology for power and signal integrity brings another research area. Although differential signaling allows to reject common-mode noise, this is not always achieved and some noise remains in the signal. For this reason, most of the times due to the complexity of the routings in current devices, even high-speed differential buses are not allowed to be routed near to very noisy power planes. Thus, it is necessary to verify if the power distribution network meets the specifications in terms of noise in an earlier design stage.

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Appendix

In this appendix, the script used for the time domain simulation in HSPICE described in Fig. 4.19 is detailed.

```
*****************************************************************
.TITLE Simulation used to verify the response of the DTL in the time domain.
* The S-parameters model, which contains the discrete data of the frequency response of the DTL, is defined as:
S1 n1 n2 n3 n4 ref mname=s_model

* 4-port S-parameter model of the DTL, Input Ports: n1, n3 and Output Ports: n2, n4.
* FMAX indicates the maximum frequency value used in the transient analysis and
* HIGHPASS indicates the method to extrapolate higher frequency points; 0: cut off,
* 1: use highest frequency point, 2: perform linear extrapolation using the highest 2
* points and 3: apply the window function to gradually approach the cut-off level (default).
* In this case, the chosen value is 0 in order to verify the End Frequency criteria.

.model s_model S N=4 TSTONEFILE = 'Single_Ended_80_mm.s4p' TYPE=s FMAX=20e9 HIGHPASS=0

.probe

* Probe points to measure the voltage in all the ports.
*************************************
```

```
+       srp=v(1)
+       srl=v(3)
+       v1=v(n1)
+       v2=v(n2)
+       v3=v(n3)
+       v4=v(n4)
*************************************
* Defining the data rate. In this case is the inverse of FMAX.
.param TR = 50p

* Defining the pulse at port 1.
VINn n1 ref pulse (0 1 0nS TR TR '2*TR' 10nS)

* Port terminations. R3in is used to put 0V in Port 3.
R1out n2 ref 50
R2out n4 ref 50
R3in n3 ref 0.00001

********** analysis & control ****************
* This simulation goes up to 2.4 nanoseconds with a step of 1 picosecond.
.TRAN 1PS 2.4NS
.options POST=1 PROBE delmax=1p
 .end
```