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Review

Exploiting magnetic sensing capabilities of Short Split-Drain MAGFETs

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ABSTRACT

The magnetic sensing capabilities of Split-Drain MAGFETs (SD-MAGFETs) with a channel that is a short Hall plate, herein called Short Split-Drain MAGFETs, are analyzed. In addition to the current-lines deflection effect, this paper shows that the magnetoresistance effect also contributes to establish the sensitivity of Short SD-MAGFETs. A relationship between the forces acting on the deflection direction and a model of the Hall angle are developed showing that these effects are favored notoriously when $L/W \leqslant 0.27$. Furthermore, the magnetoresistance effect improves the sensitivity when the channel length is reduced. This allows to design a high-sensitivity SD-MAGFET with a reduced active area. Using the proposed model of the Hall angle with a continuous model of the geometric correction factor, a continuous variation of the Hall angle along the channel for any L/W can be obtained, and a quantitative criterion to establish which range of the L/W values corresponds to a short Hall plate and which one to a long Hall plate can be established. In order to validate the proposed design criteria, a Short SD-MAGFET with $L/W = 0.2$ and $W/L = 10\ \mu m/2\ \mu m$ has been characterized. Sensing capabilities from 90 μT to 27 μT and sensitivities from 15.51% to 59.9% have been experimentally obtained at room temperature and in strong inversion.

Contents

1. Introduction

A Split-Drain MAGFET (SD-MAGFET) is a MOSFET structure able to convert a Magnetic Flux Density (MFD) to a drain current imbalance using galvanomagnetic effects [1,2]. SD-MAGFETs are attractive sensors due to their compatibility with standard CMOS processes and their good linearity with MFD [1,2]. SD-MAGFETs manufactured in standard CMOS processes even with non-rectangular structures [3–10] have achieved sensitivities <10% at room temperature. Analyses of SD-MAGFETs, until now, have considered just the current-lines deflection effect, nevertheless, being its channel a split-contact Hall plate, the current-lines deflection effect [5,11] and the magnetoresistance effect [12,13,11] establish the drain current imbalance and, thus, the sensitivity.

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The SD-MAGFET sensitivity depends on the channel geometry and the bias conditions [14,5–7]. Until now, reported SD-MAGFETs have been optimized considering the ratio between the channel length, L, and channel width, W, of $L/W \geqslant 1$, being L as large as possible [4–7,15–17,8,18]. On the other hand, most of SD-MAGFETs have been characterized with MFDs of units of mT or above [5–7,15,8,18], and some ones with MFDs from hundreds of μT and above [4,19–21].

SD-MAGFETs have been proposed for several applications such as controlling the volume in hearing aids [22], reading magnetically stored information directly [4], developing an IDDQ testing scheme [23,24], monitoring voltage drops in supply lines [25], or monitoring signal integrity [21]. In all these cases, it is desirable to have SD-MAGFETs with a reduced active area in order to be able to use several of these devices in a single chip.

This work investigates the feasibility of using Short SD-MAGFETs, with $L/W < 1$, fully compatible with standard CMOS technology, for sensing MFDs as small as 90 μT. The key to do this is to establish the geometric conditions to favor both the current-lines deflection and the magnetoresistance effects. These effects become more important when the Hall angle increases [1,2].

The rest of this paper is organized as follows: in Section 2, the parameters to characterize MAGFET performance are presented. In Section 3, analytical expressions are developed to establish those L/W ratios that favor the current-lines deflection effect and the magnetoresistance effect. Section 4 shows the design issues of the fabricated Short Split-Drain MAGFET. Section 5 shows the methodology to estimate the magnitude of the MFD experimentally applied. Section 6 shows the followed experimental methodology. In Section 7, the experimental results are presented and discussed. Finally, the conclusions are summarized in Section 8.

2. Performance of a Split-Drain MAGFET

The sensitivity, S, of a SD-MAGFET is defined by Eq. (1). I_{D2} and I_{D1} are the currents in each drain, $I_{D2} - I_{D1}$ is the drain current imbalance denoted as ΔI_D, $I_{D1} + I_{D2}$ is the total drain current and B_z is the intensity of the MFD normal to the channel plane.

$$S = \frac{|I_{D2} - I_{D1}|}{(I_{D1} + I_{D2})B_z} = \frac{|\Delta I_D|}{(I_{D1} + I_{D2})B_z} \tag{1}$$

The output signal of a SD-MAGFET is the drain current imbalance which has a good linearity with the MFD. In this work, both the sensitivity and the drain current imbalance are used to characterize the performance of the proposed Short SD-MAGFET.

Some SD-MAGFETs [3–5] have been characterized using a constant current source connected serially between source and V_{SS} to establish the total drain current. Under this scheme, for certain gate and drain voltages, different source voltages are produced for different W/L ratios. In this work, in order to eliminate the V_{GS} variation, the total drain current is established by the gate and drain voltages and the channel geometry. This scheme allows to compare the results for different geometry MAGFETs at the same bias conditions.

3. Improving sensing capability of a Split-Drain MAGFET

When a n-type Hall plate driving a current $\vec{I}$ is immersed in a magnetic flux density, $\vec{B}_z$, normal to its plane, a bias electric force, $\vec{F}_e$, a Hall electric force, $\vec{F}_{Hn}$, and the magnetic part of the Lorentz force, $\vec{F}_{Lm}$ (see Eq. (2)), act on each carrier with a charge $-q$ moving with a drift velocity $\vec{v}_{dn}$ (see Fig. 1). Where q is the elementary charge.

$$\vec{F}_{Lm} = -q\left[\vec{v}_{dn} \times \vec{B}_z\right] \tag{2}$$

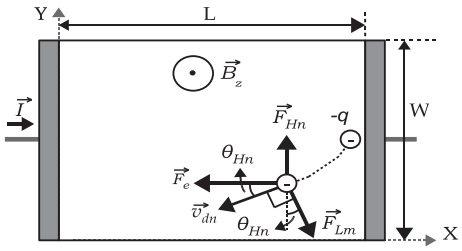


Fig. 1. Forces acting on a carrier and the Hall angle in n-type Hall plate.

Since $\vec{F}_{Lmy}$ is the component of $\vec{F}_{Lm}$ in the deflection direction, if the magnitude of the resulting force in the deflection direction, $\vec{F}_{Lmy} - \vec{F}_{Hn}$, increases, the Hall angle increases, and, thus, the current-lines deflection and the magnetoresistance effects are favored. Because of this, the geometric conditions to increase the Hall angle are analyzed.

3.1. Forces acting on the deflection direction

The geometry effect is introduced through the geometric correction factor, G, which varies along a Hall plate. G is defined as the ratio between the Hall voltage obtained by action of F_{Hn} in a real Hall plate, V_{Hn}, and one, $V_{H\infty}$, obtained in an ideal Hall plate where $F_{Hn} = F_{Lmy}$ along a Hall plate [2,5]. Then, if W is the width of the Hall plate, G can be expressed as:

$$G(x) = \frac{V_{Hn}(x)}{V_{H\infty}} = \frac{W \cdot F_{Hn}/(-q)}{W \cdot F_{Lmy}/(-q)} = \frac{F_{Hn}}{F_{Lmy}} \tag{3}$$

From Eq. (3), when the L/W ratio decreases, the F_{Hn}/F_{Lmy} ratio decreases [5], and, therefore, the magnitude of the resulting force in the deflection direction increases.

3.2. Continuous model of the Hall angle

The deflection angle of the current lines with respect to the longitudinal direction, the Hall angle, θ_{Hn}, is established by the forces acting on carriers (see Fig. 1). According to the reported expression for θ_{Hn} given in [1,2], $\theta_{Hn} < 3°$ for $B_z \leqslant 1$ T with $\mu_n \leqslant 500\ \text{cm}^2/\text{V s}$. Therefore, the longitudinal component of $\vec{F}_{Lm}$ can be neglected. Then, using Eq. (3), the Hall angle can be defined as:

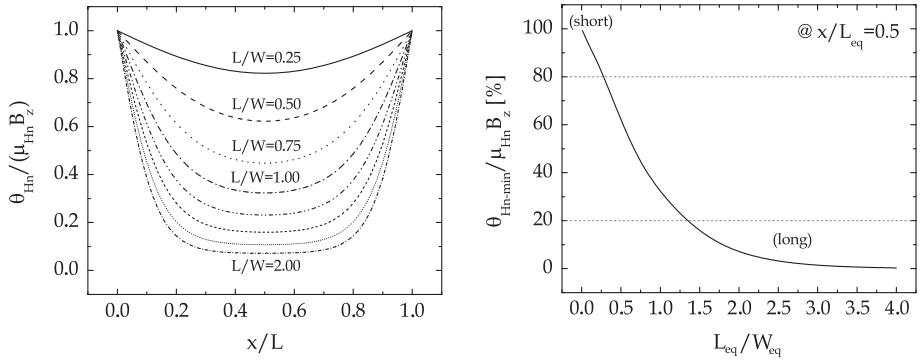
$$\tan\theta_{Hn} = \frac{F_{Lmy} - F_{Hn}}{F_e} = (1 - G(x))\frac{F_{Lmy}}{F_e} \tag{4}$$

Using Eq. (2) and Fig. 1, $F_{Lmy} = q\, v_{dn} B_z \cos\theta_{Hn}$.$\vec{F}_e$ is generated by the bias electric field, $\vec{E}_e$, ($\vec{F}_e = -q\vec{E}_e$) that can be related to the x-component of the drift velocity as $\vec{E}_e = -\vec{v}_{dnx}/\mu_{Hn}$. Where $\mu_{Hn} = r_{Hn} \cdot \mu_n$ is the Hall mobility, r_{Hn} is the Hall scattering factor and μ_n is the carrier mobility. Then, according to Fig. 1 and using the previous definitions, F_e can be expressed as $F_e = q\, v_{dn} \cos\theta_{Hn}/\mu_{Hn}$. Replacing the previous expressions of F_e and F_{Lmy} in Eq. (4), the Hall angle is defined as:

$$\tan\theta_{Hn} = (1 - G(x))\mu_{Hn} B_z \tag{5}$$

Eq. (3) is coherent with Eq. (5). When the L/W ratio decreases, the F_{Hn}/F_{Lmy} ratio also decreases (see Eq. (3)) which means that the magnitude of the resulting force acting on each carrier in the deflection sense increases, and hence, the magnitude of θ_{Hn} increases (see Eq. (5)).

Using the continuous model of G reported in [5], Eq. (5) is a continuous model of the Hall angle at L/W and all along the channel length. This is a significant improvement with respect to the model reported in the literature [1,2] since the proposed model allows to analyze the impact of the channel geometry on the deflection



(a) Along the channel length (b) Minimum value of θ_{Hn}

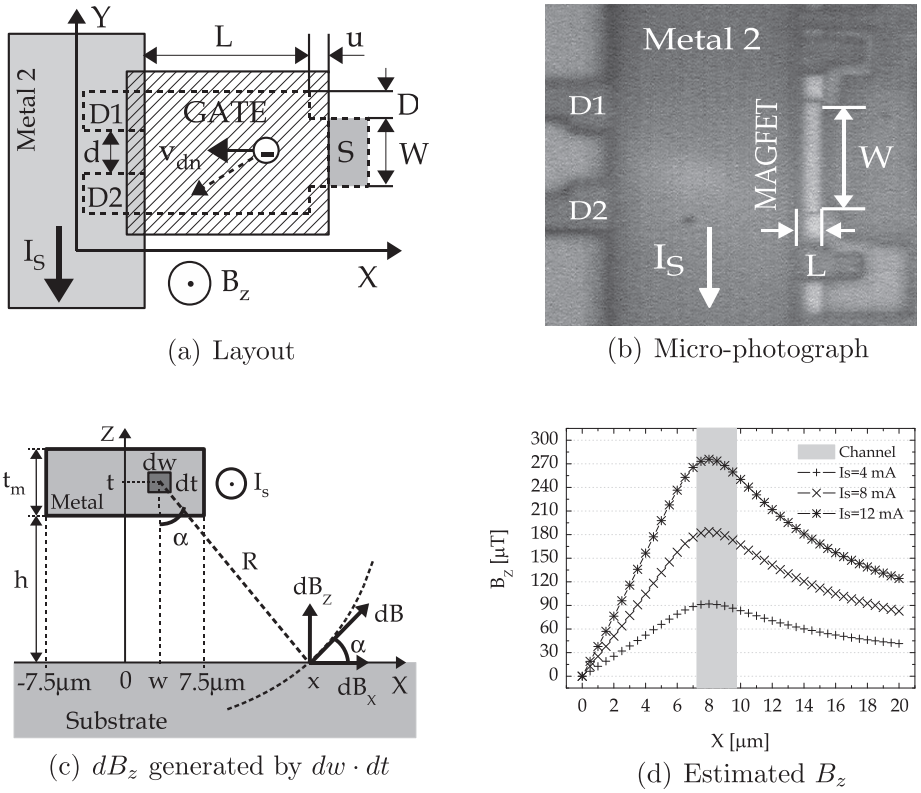
Fig. 2. Variation of the Hall angle for different values of *L*/*W*.

angle. Using the model of $G(x)$ reported in [5], the continuous variation of the Hall angle with respect to its maximum value ($\theta_{Hn}/(\mu_{Hn}B_z)$) along a Hall plate is shown in Fig. 2a for different *L*/*W* ratios. Fig. 2b shows the variation of the minimum value of the Hall angle, $\theta_{Hn}(x/L = 0.5)$, with *L*/*W* ratio.

In this work, a Hall plate with $L/W \geqslant 1.36$ is considered as long for a reduction of θ_{Hn} greater than 80% (see Fig. 2b). In a similar way, a Hall plate with $L/W \leqslant 0.27$ is considered as short for a reduction of θ_{Hn} less than 20% (see Fig. 2b). In this last case, the Hall angle maintains close to its maximum value which favors the current-lines deflection and the magnetoresistance effects [1,2].

4. Short Split-Drain MAGFET design

According to Section 3, the *L*/*W* ratio should be ⩽0.27. In addition, it has to be considered that due to the magnetoresistance effect, a CMOS split-contact Hall plate increases its resolution when its length decreases [12]. For a SD-MAGFET as Fig. 3a shows, if *u* increases, the equivalent length of channel increases, and, thus, the *L*/*W* ratio increases which would decrease the impact of the effects of interest in the sensitivity. Inversely, when *W* increases, the *L*/*W* ratio decreases with the impact of the effects of interest in the sensitivity would increase. With constant $W + 2D$, when *d* increases, the sensitivity caused by the current-lines deflection effect [5] and the one caused by the magnetoresistance effect decreases [12]. Under the same condition, if *D* increases, the sensitivity caused by the current-lines deflection effect [5] and by the magnetoresistance effect [12] does not significantly vary when $D \leqslant 15$ μm. Nevertheless, the equivalent width of the channel increases when *D* increases, which reduces the *L*/*W* ratio increasing the Hall angle (see Fig. 2b). As a result, *u*, *d* and should be as short as possible but *D* should be >0 to reduce the *L*/*W* ratio but as small as possible to have an adequate area overhead.



(a) Layout (b) Micro-photograph

(c) dB_z generated by $dw \cdot dt$ (d) Estimated B_z

Fig. 3. Experimental conditions.

To validate the proposed criteria design for SD-MAGFETs, an *n*-type Short SD-MAGFET with $L/W = 0.2$, $L = 2\ \mu m$, $W = 10\ \mu m$, $u = 0.4\ \mu m$, $d = 0.6\ \mu m$ and $D = 0.5\ \mu m$ (see Fig. 3a) has been designed and fabricated using AMS 0.35 μm CMOS technology. In order to reduce the effect of process variation, L was chosen five times greater than the minimum channel length allowed by the technology. The geometric parameters u, d and D are designed with minimum values allowed by the design rules. A micro-photograph of the fabricated Short SD-MAGFET is shown in Fig. 3b.

5. Estimation of the applied magnetic flux density

The magnetic flux density (MFD) used to characterize the fabricated SD-MAGFET is produced by a DC current, I_s, flowing through an interconnection (metal 2) of 15 μm in width (see Fig. 3a and b). This metal can be approximated as infinite wires with an infinitesimal transversal section $dw \cdot dt$ (see Fig. 3c). Using the Biot-Savart law, for a point on the surface of the substrate at a distance x from the symmetry axis of the transversal section of the interconnection (see Fig. 3c), the intensity of the MFD, dB_z, normal to the channel plane produced by the current flowing through each section $dw{\cdot}dt$ is estimated by Eq. (6), where w_m is the metal width.

$$dB_z(x) = \frac{\mu_0}{2\pi}\left(\frac{I_s}{w_m t_m}\,dw\,dt\right)\frac{x-w}{(x-w)^2+t^2} \tag{6}$$

Then, the total MFD, B_z, at the same point x, is estimated integrating dB_z over the section $w_m \cdot t_m$:

$$B_z(x) = \int_h^{h+t_m}\int_{-w_m/2}^{w_m/2} dB_z(x) \tag{7}$$

Fig. 3d shows $B_z(x)$ for x values from 0 μm to 20 μm. For metal 2 in the used technology, $t_m = 0.64\ \mu m$ and $h = 2.5\ \mu m$ (see Fig. 3c). Experimentally, the intensities of I_s were of 4 mA, 8 mA and 12 mA. As the channel length of the manufactured Short SD-MAGFET is 2 μm, in agreement with the layout shown in Fig. 3a, the intensities of the MFD in the channel are the values within the gray region shown in Fig. 3d, that is to say from 90 μT to 275 μT.

6. Experimental methodology

Measurements were obtained using an *Agilent B1500A* SPA. The current I_s was varied from −12 mA to 12 mA in 4 mA steps. Fig. 3a shows the positive sense of I_s and the corresponding sense of the normal magnetic flux density on the side of interest of the metal *2*. The intensities of the MFD, B_z, normal to the MAGFET's channel plane on the surface of the substrate for these current intensities are shown in Fig. 3d. Then, intensities of MFDs of 90 μT, 180 μT and 275 μT, were generated on the channel of the SD-MAGFET.

For fixed gate and drain voltages, the current drain imbalance, $I_{D2} - I_{D1}$, as a function of I_s, were measured using the *Agilent B1500A* SPA. Each measured point (see Fig. 4) was obtained taking 640 samples. One set of measurement was obtained sweeping I_s as shown in Fig. 4. In order to enhance accuracy ten sets of measured data were obtained.

Three steps were followed. In the first step, the measured data were saved with the *Agilent B1500A*, and a linear regression defined as $y_i = m_i I_s + b_{0i}$ was obtained for each set of measurements. As Fig. 4 shows, when I_s does not generate a MFD, B_z, that is to say $I_s = 0$, the value of $I_{D2} - I_{D1}$ is not zero but b_{0i}. This value of drain current imbalance represents the offset of the magnetic sensor caused mainly by mismatch between the two drains and between the cables and test probes used to contact both drains. In the second step, the effect of the offset was eliminated (see Fig. 4). After the second step, each linear regression has an equation as $y_i = m_i I_s$. In the third step, an average slope, m_{av}, was obtained for all the regression lines. m_{av} establishes the sensor's resolution.

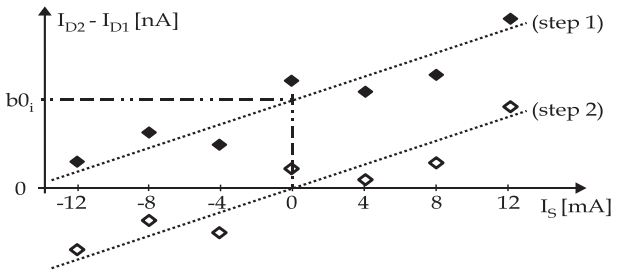


Fig. 4. Experimental methodology: steps 1 and 2.

7. Experimental results

For an *n*-MOS transistor in the technology used, the maximum drain and gate voltage is 3.3 V, the parameter of the mobility is $U0 = 475.8$ ($VTHO = 0.49$ V). Considering this, Gate voltages, V_G, of 1.6 V, 2.4 V and 3.2 V were applied. The same values were also considered for drain voltages, V_D. The total drain current had intensities from 150 mA to 1.15 mA. The magnetic flux densities and the values of drain current imbalance have been obtained according to the experimental methodology given in Section 6. This allows to obtain the total deflected drain current and the sensitivity of the MAGFET (see Eq. (1)).

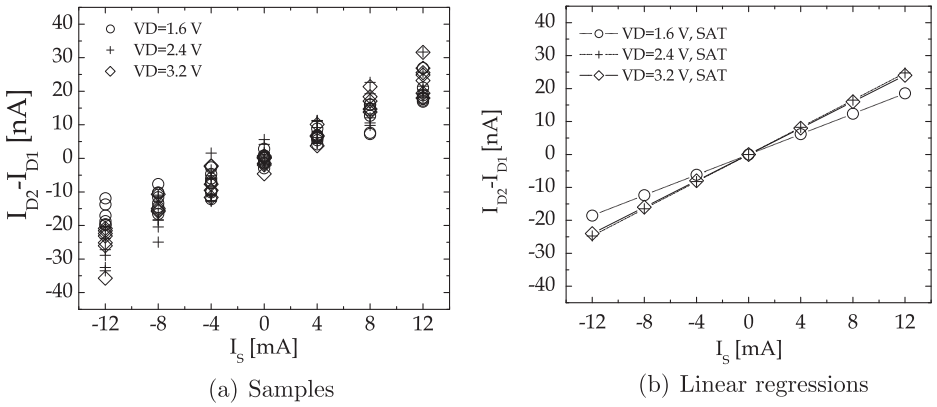


Fig. 5. Drain current imbalance with $V_G = 1.6$ V.

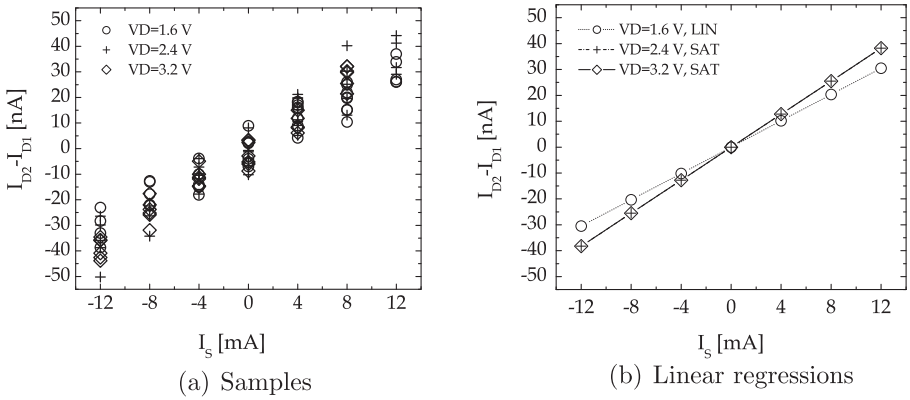


Fig. 6. Drain current imbalance with V_G = 2.4 V.

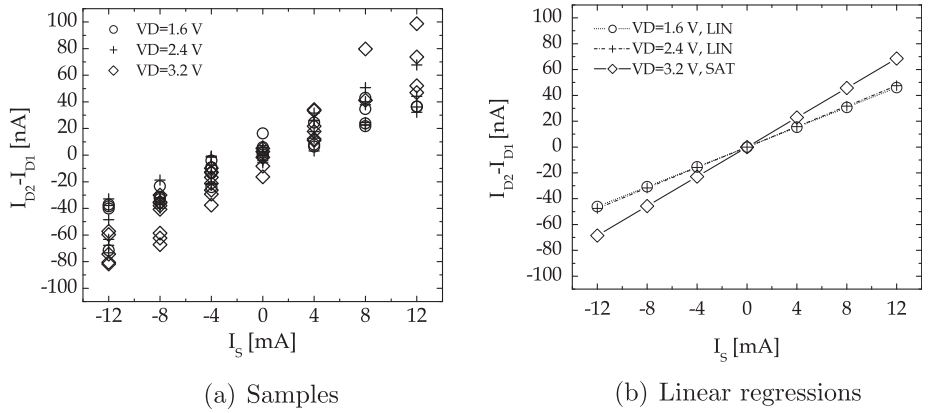


Fig. 7. Drain current imbalance with V_G = 3.2 V.

7.1. Drain current imbalance

Fig. 5 shows the results obtained using V_G = 1.6 V for different V_D. The device is in saturation in all cases. All samples (see Section 6) for each considered V_D are shown in Fig. 5a. There are no significant differences between the $I_{D2} - I_{D1}$ values for V_D = 2.4 V and for V_D = 3.2 V, but they are higher in magnitude than those obtained for V_D = 1.6 V (see Fig. 5b).

Applying V_G = 2.4 V (see Fig. 6), when the device goes from the linear (V_D = 1.6 V) to the saturation region (V_D = 2.4 V and V_D = 3.2 V), the drain current imbalance, $I_{D2} - I_{D1}$, increases noticeable. Being in saturation, there is no significant difference between the values of $I_{D2} - I_{D1}$ for V_D = 2.4 V and for V_D = 3.2 V (see Fig. 6b).

Fig. 7 shows the results obtained with V_G = 3.2 V. Being in the linear region (V_D = 1.6 V and V_D = 2.4 V), the drain current imbalance $I_{D2} - I_{D1}$ does not vary significantly with the drain voltage, V_D. However, going from the linear to the saturation region, an increase in the values of $I_{D2} - I_{D1}$ appears (see Fig. 7b).

Organizing the obtained data in a different way, Fig. 8 allows to better observe some facts. The drain current imbalance, $I_{D2} - I_{D1}$, increases significantly when the gate voltage, V_G, also increases. This behavior is independent of the operation region of the Short SD-MAGFET. When V_G increases, the total drain current increases, and, therefore, $I_{D2} - I_{D1}$ increases.

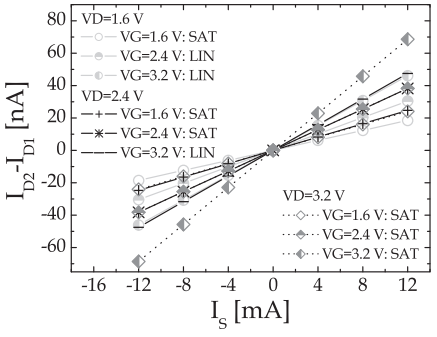


Fig. 8. Drain current imbalance with all V_D and all V_G.

7.2. Performance

The resolution and the sensitivity, S, of the fabricated Short SD-MAGFET were obtained (see Fig. 9). The resolution varies from 67.4 μA/T to 249.5 μA/T (see Fig. 9a), and S varies from 15.51% to 59.9% as Fig. 9b shows. According to the reported models of the sensitivity considering only the current-lines deflection effect [5,9], S < 10%. Hence, the higher sensitivities obtained with the fabricated Short SD-MAGFET are associated to the magnetoresistance effect. When the gate voltage increases, the total drain current and the carrier concentration in the channel increase, and thus, the Coulomb scattering increases which reduces the magnitude of the Hall angle [2]. Then, the drain current imbalance and the resolution increases in less proportion than the increment of the total drain current. Because of this, the ratio between the drain current imbalance and the total drain current decreases, and, as a result, the sensitivity decreases.

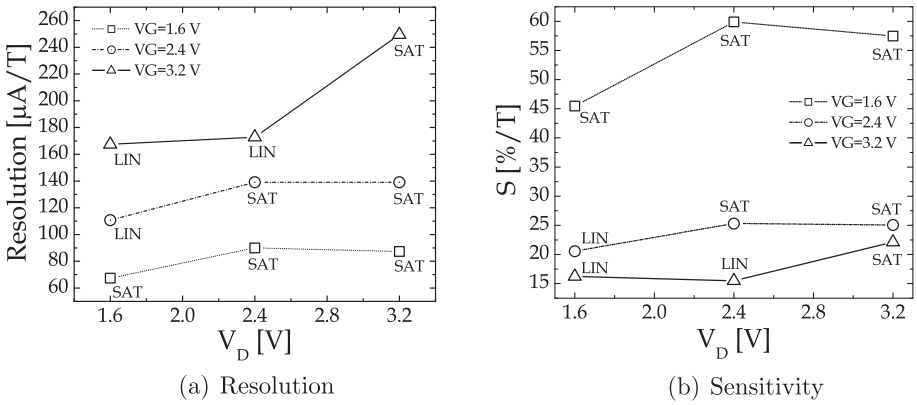


Fig. 9. Performance of the manufactured Short Split-Drain MAGFET.

7.3. Discussion

The drain current imbalance, the resolution and the sensitivity experimentally obtained for the fabricated Short SD-MAGFET are higher than those obtained with reported SD-MAGFETs manufactured with a standard CMOS process at room temperature and in strong inversion [4–8,3,9,**?**]. Higher sensitivities than the ones obtained in this work are reported in [7] for SD-MAGFET operating in the sub-threshold region. If the gate voltage would decrease, the sensitivity of the manufactured Short SD-MAGFET proposed in this work would also increase as it is suggested in [7]. An SD-MAGFET with sensitivities of up to 100% is proposed in [26] but its structure is not compatible with a standard CMOS process. On the other hand, the drain current imbalance, the resolution and the sensitivity increases noticeably when the Short SD-MAGFET passes from the linear to the saturation region because, in the saturation region, the magnetoresistance effect is much greater than in the linear region in a SD-MAGFET [11].

The fabricated Short SD-MAGFET is able to measure a MFD as small as 90 μT. Moreover, since it has high sensitivity and resolution using a small active area, the total area would decrease to achieve the same performance in applications as those reported in [4,17].

8. Conclusions

Design criteria of Short Split-Drain MAGFETs in order to favor the current-lines deflection effect and the magnetoresistance effect to improve the drain current imbalance, the sensitivity and the resolution have been presented. This has been possible establishing a new relationship between the forces acting in the deflection direction and developing a model of the Hall angle including the impact of the geometry. According to this, the current-lines deflection effect and the magnetoresistance effect are significantly favored when $L/W < 0.27$. Considering that the resolution caused by the magnetoresistance effect increases when the channel length is reduced, a high-sensitivity Short Split-Drain MAGFET can be obtained with a small active area. This is verified with a Short Split-Drain MAGFET with $L/W = 0.2$, $L = 2$ μm and $W = 10$ μm which is able to measure magnetic flux densities as low as 90 μT, making it adequate for critical area applications in CMOS integrated circuits. The fabricated CMOS Short Split-Drain MAGFET has sensitivities from 15.51% to 59.9% measured at room temperature and working in a strong inversion. These values are much higher than those obtained with CMOS Split-Drain MAGFETs with two or three drains and even with non-rectangular Split-Drain MAGFETs reported until now. The increase of the sensitivity is mainly associated to the magnetoresistance effect.

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References

[1] Baltes HP, Popović RS. Integrated semiconductor magnetic field sensors. Proc IEEE 1986;74(8):1107–32.
[2] Popović RS. Hall effect devices: magnetic sensors and characterization of semiconductors. Adam Hilger; 1991.
[3] Kub FJ, Scott CS. Multiple-gate split-drain MOSFET magnetic-field sensing device and amplifier. In: Technical digest, international electron devices meeting; 1992. p. 517–20.
[4] Rohrer S et al. A MAGFET sensor array for digital magnetic signal reading. In: Proc. tenth annual IEEE international ASIC conference and exhibit; 1997. p. 308–10.
[5] von Kluge JWA, Langheinrich WA. An analytical model of MAGFET sensitivity including secondary effects using a continuous description of the geometric correction factor G. IEEE Trans Electron Dev 1999;46(1):89–95.
[6] Rubio C, Bota S, Macfas JG, Samitier J. Modelling, design and test of a monolithic integrated magnetic sensor in a digital CMOS technology using a switched current interface system. Analog Integr Circ Signal Process 2001;29:115–26.
[7] Rodríguez-Torres R, Gutiérrez-Domínguez E, Klima R, Selberherr S. Analysis of split-drain MAGFETs. IEEE Trans Electron Dev 2004;51(12):2237–45.
[8] Young-Jae M, Soo-Won K. A CMOS TDC-based digital magnetic Hall sensor using the self temperature compensation. In: IEEE custom integrated circuit conference; 2008. p. 329–32.
[9] Yunruo Y, Dazhong Z, Qing G. Sector split-drain magnetic field-effect transistor based on standard CMOS technology. Sensors Actuat A: Phys 2005;121(2):347–51.
[10] Qing G, Dazhong Z, Yunruo Y. CMOS magnetic sensor integrated circuit with sectorial MAGFET. Sensors Actuat A: Phys 2006;126(1):154–8.
[11] Dobrovolsky VN, Krolevets AN. Theory of magnetic-field-sensitive metal–oxide-semiconductor field-effect transistors. J Appl Phys 1999;85(3):1956–60.
[12] von Kluge JWA. Analysis of split-current magnetic field sensitive resistors. Sensors Actuat A: Phys 2001;93(2):103–8.
[13] Sugiyama Y, Soga H, Tacano M, Baltes H. Highly sensisitive split-contact magnetoresistor with AlAs/GaAs superlattice structures. IEEE Trans Electron Dev 1989;36(9):1639–43.
[14] Lau J, Ko PK, Chan PCH. Modelling of split-drain magnetic field-effect transistor (MAGFET). Sensors Actuat A: Phys 1995;49:155–62.
[15] Pesić-Brdanin T, Janković N, Pantić D. SPICE MAGFET model and its application for simulation of magnetically controlled oscillator. In: Proc 26th international conference on microelectronics, MIEL 2008; 2008. p. 503–6.
[16] Donoval M, Daricek M, Stopjakova V, Marek J. On-chip integration of magnetic force sensing current monitors. In: Proc of the 2008 11th IEEE workshop on design and diagnostics of electronic circuits and systems, DDECS'08; 2008. p. 1–4.
[17] Castaldo FC, Mognon VR, dos Reis Filho CA. Magnetically-coupled current sensors using CMOS split-drain transistors. In: IEEE power electronics specialists conference; 2008. p. 4777–80.
[18] Yosry E et al. Compact model of dual-drain MAGFETs simulation. Int J Electron Commun Comput Eng 2009;1(2):112–6.
[19] Li ZQ, Sun XW. A CMOS magnetic latch with extremely high resolution. In: International electron device meeting, IEDM'02, digest; 2002. p. 909–12.
[20] Li ZQ, Sun XW. Weak magnetic field pattern detection by CMOS magnetic latch. IEEE Electron Dev Lett 2003;24(10):652–4.

[21] Gutiérrez-Domínguez EA, Torres-Ríos E, Torres-Torres R. Magnetic sensing as signal integrity monitoring in integrated circuits. In: Proc. 35th European solid-state device research conference, ESSDERC 2005; 2005. p. 277–80.
[22] Kaulberg T, Bogason G. Position detection with the use of MAGFETs. In: Proc. IEEE instrumentation and measurement technology conference, IMTC/95; 1995. p. 158–62.
[23] Kim H, Walker DMH, Colby D. A practical built-in current sensor for IDDQ testing. In: Proc. IEEE international test conference, ITC 2001; 2001. p. 405–14.
[24] Xue B, Walker DMH. Built-in current sensor for IDDQ test. In: Proc. 2004 IEEE international workshop on current and defect based testing, DBT 2004; 2004. p. 3–9.
[25] Xue B, Walker DMH. I_{DDQ} test using built-in current sensing of supply line voltage drop. In: Proc. IEEE international test conference, ITC 2005; 2005. p. 954–63.
[26] Kordalski W et al. Bulletin of the polish academy of sciences. Tech Sci 2007;55(3):325–9.