Efficient Dithering in MASH Sigma-Delta Modulators for Fractional Frequency Synthesizers

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***Abstract*—The digital multistage-noise-shaping (MASH) $\Sigma\Delta$ modulators used in fractional frequency synthesizers are prone to spur tone generation in their output spectrum. In this paper, the state of the art on spur-tone-magnitude reduction is used to demonstrate that an M-bit MASH architecture dithered by a simple M-bit *linear feedback shift register (LFSR)* can be as effective as more sophisticated topologies if the dither signal is properly added. A comparison between the existent digital $\Sigma\Delta$ modulators used in fractional synthesizers is presented to demonstrate that the MASH architecture has the best tradeoff between complexity and quantization noise shaping, but they present spur tones. The objective of this paper was to significantly decrease the area of the circuit used to reduce the spur tone magnitude for these MASH topologies. The analysis is validated with a theoretical study of the paths where the dither signal can be added. Experimental results of a digital M-bit MASH 1-1-1 $\Sigma\Delta$ modulator with the proposed way to add the LFSR dither are presented to make a hardware comparison.**

***Index Terms*—Fractional, frequency synthesizers, phase noise, Sigma-Delta, spur tones.**

I. Introduction

FRACTIONAL FREQUENCY SYNTHESIZERS using $\Sigma\Delta$ modulation are a good solution to integrate a frequency synthesizer with the fine step resolution and the high spectral purity that diverse communication protocols impose. In these frequency synthesizers, the fractional frequency step resolution is obtained by changing the division modulus factor with the output sequence from a digital $\Sigma\Delta$ modulator [1].

In order to achieve a high performance and to have the required spectral purity, attention must be paid to the digital $\Sigma\Delta$ modulator since it increases the complexity and cost of the circuit. This is because $\Sigma\Delta$ modulation affects the synthesizer's total phase noise figure. As the input for the digital modulator is a constant, the spur tones from the quantization error in the digital $\Sigma\Delta$ modulator affect the phase noise even more. Therefore, usually, high-cost digital $\Sigma\Delta$ architectures must be selected in order to avoid the spur tones and to accomplish the phase noise specifications.

In this paper, a deep insight into spur tone magnitude reduction techniques for MASH digital $\Sigma\Delta$ modulators is presented. The contribution of this work relies on the use of closed-form equations [2]–[4] to characterize the digital $\Sigma\Delta$ modulator periodicity when a dither signal from an LFSR is added as a least significant bit (LSB). The effects of adding the dither signal in different paths within the modulator are expressed in the equations, and the results are compared. It is also mathematically demonstrated that a pseudorandom generator with a very long repeating sequence will not reduce the spur tone magnitude if it is not added in a path that disables the periodicity in the digital modulator. On the other hand, the equations are used to demonstrate that a very simple dither generator (which was obtained from a small-sized LFSR) can be as effective as a more cumbersome $\Sigma\Delta$ topology if added in a path that disables the periodicity.

This paper is organized as follows: In Section II, a comparison of digital $\Sigma\Delta$ modulator architectures for fractional frequency synthesizers is presented, and it is concluded that a multistage-noise-shaping (MASH) architecture has the best tradeoff between complexity and noise shaping (which justifies the great amount of research work for this architecture). In Section III, the most relevant spur tone magnitude reduction techniques for MASH modulators are analyzed to see their advantages and drawbacks. In Section IV, the state-of-the-art theory on spur tone disabling is used to demonstrate that a very simple dither generator is effective to decrease the spur tone magnitude for the frequencies of interest in fractional synthesizers. Section V presents the experimental results of a third-order digital $\Sigma\Delta$ modulator, and a comparison is done to show that the simple dither generator can be as effective as an architecture that uses more resources. Finally, in Section VI, the conclusions of this work are given.

II. $\Sigma\Delta$ Modulators for Fractional Synthesizers

To avoid the spur tones in the total phase noise figure, the $\Sigma\Delta$ modulator must be of high order and must have enough quantization levels. Contrary to this, for fractional synthesizers, the $\Sigma\Delta$ modulator's order must be equal or less than the synthesizer order; otherwise, the phase noise figure will significantly be affected [5]. Many architectures have been proposed to accomplish this restriction. Here, this paper compares the most important to show that the MASH architecture has the best tradeoff for complexity and performance. The simulations for every architecture were realized in Matlab-Simulink for a sample frequency of 25 MHz. The reference frequency in fractional synthesizers is the sample frequency for the digital $\Sigma\Delta$ modulator

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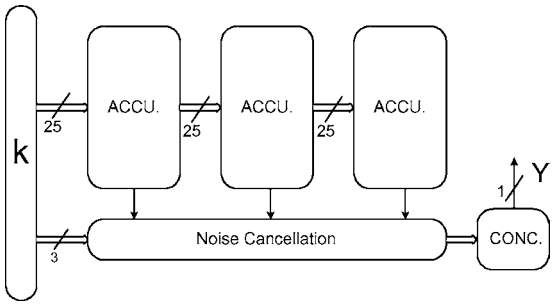

Fig. 1. Digital $\Sigma\Delta$ modulator hybrid architecture.

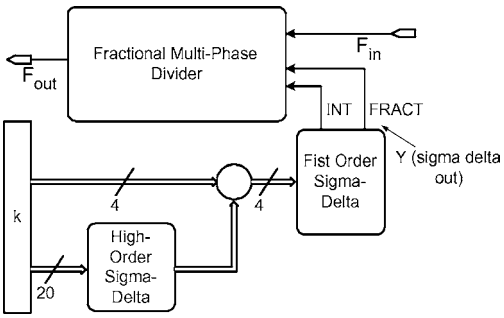

Fig. 2. Multiphase divider with hybrid digital $\Sigma\Delta$ modulator.

and is within this range. In general, we have classified these architectures into three main groups:

A. Hybrid Architectures

The resolution in a $\Sigma\Delta$ modulator can be increased with hybrid topologies. The architecture presented in [6] is built by a *MASH* architecture and a concentrator (another digital $\Sigma\Delta$ modulator), as shown in Fig. 1.

The concentrator is used to convert the multibit output (from the MASH architecture) into a single-bit output. In this way, high-order modulation is obtained, and the synthesizer order restriction is accomplished. Although the input word length is large (more than 24 bits), it is well known that a single-bit output makes it more difficult to avoid the spur tones in the $\Sigma\Delta$ modulator spectrum [7], [8]. This limits the benefits of the architecture.

Another hybrid architecture has been presented in [9], where the multiphase fractional division is proposed. For this technique, the programmable divider selects between 16 signals with different phases to achieve a fractional division. To avoid the spur tones and to increase the resolution, a long input word (24-bit) is separated. The 20 LSBs are processed by a high-order digital $\Sigma\Delta$ modulator, as shown in Fig. 2.

The high-order $\Sigma\Delta$ modulator makes the quantization noise randomized enough, and finally, a first-order digital $\Sigma\Delta$ modulator produces the output sequence that controls the multiphase frequency divider. Unfortunately, to make the output sequence random enough to avoid spur tones, the high-order $\Sigma\Delta$ modulator must be at least of sixth order, and the multiphase frequency divider needs to be robust to ensure an accurate delay between phases. The hybrid architectures appear to reduce the spur tones but at the high cost of increasing the hardware.

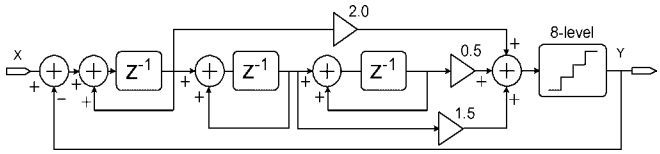

Fig. 3. Single-loop digital $\Sigma\Delta$ modulator.

B. Loop Architectures

Single-Loop Architectures: Single-loop architectures can be designed to reduce the quantization noise pushed to high frequencies. Fig. 3 shows a block-level model of the single-loop digital $\Sigma\Delta$ modulator proposed in [10].

The noise-shaping transfer function of this single-loop architecture is

$$H_n(z) = \frac{(1-z^{-1})^3}{1 - z^{-1} + 0.5z^{-2} - 0.1z^{-3}}. \quad (1)$$

The advantage of this $\Sigma\Delta$ modulator is the suppressed quantization noise for high frequencies due to the poles into the noise-shaping function of (1). The multibit quantizer in this single-loop architecture makes the output appear more random, and the spur tones are less prominent. Nevertheless, in [10], a pseudorandom signal with a 24-bit linear feedback shift register (*LFSR*) is added to disable the tones. All the advantages are at the cost of increased complexity to realize the forward loops and the increased in-band noise (although it will be filtered by the fractional synthesizer loop). The stability of the digital modulator depends on the loop coefficients, which also limit the input dynamic range.

Multiloop Architectures: Several multiloop digital $\Sigma\Delta$ architectures have been proposed [11], [12]. The goal in these architectures is to obtain a high-order modulator to avoid the spur tones in the output *power spectral density (PSD)*. At the same time, the noise-shaping transfer function must not increase the low-frequency phase noise figure of the frequency synthesizer. These multiloop architectures use, in general, multipliers to add coefficients in the loop to avoid instability. In [12], a fourth-order digital $\Sigma\Delta$ modulator with four loops, as shown in Fig. 4, is proposed. Every loop consists of an accumulator, an adder, and two multipliers to obtain the scaling coefficients from a multibit quantizer.

The disadvantage is the great complexity to achieve a multiloop architecture, and the coefficients to avoid instability may limit the input dynamic range. To overcome this problem, another architecture is proposed in [13] to increase the input dynamic range and to reduce the high-frequency-shaped noise. For that topology, the zeros in the noise transfer function are moved to a value that is a multiple of the minimum fractional division step, similar to the noise transfer function in (2) for a specific design in [13]

$$H_n(z) = 1 - \left(3 - \frac{612}{2^{16}}z^{-1}\right) + \left(3 - \frac{612}{2^{16}}z^{-2}\right) - z^{-3}. \quad (2)$$

This noise transfer function is a modified version of a third-order MASH noise transfer function with an increased complexity. To disable the spur tones on this architecture, a dither signal is added at the quantizer input, as shown in the model

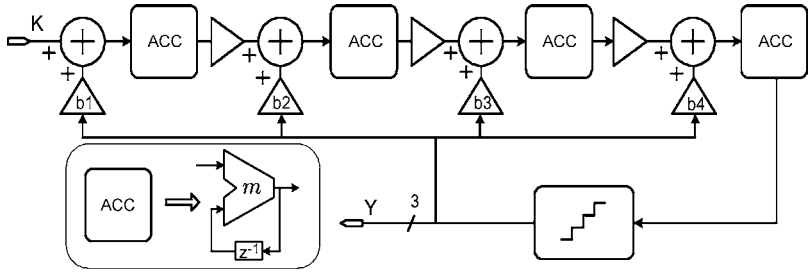

Fig. 4. Fourth-order multiloop digital $\Sigma\Delta$ architecture.

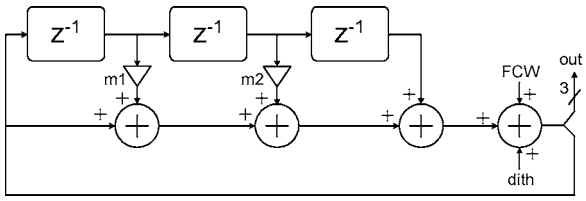

Fig. 5. Digital $\Sigma\Delta$ multiloop architecture with modified coefficients.

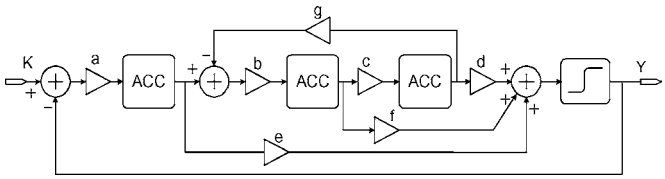

Fig. 6. Digital $\Sigma\Delta$ Chebyshev modulator.

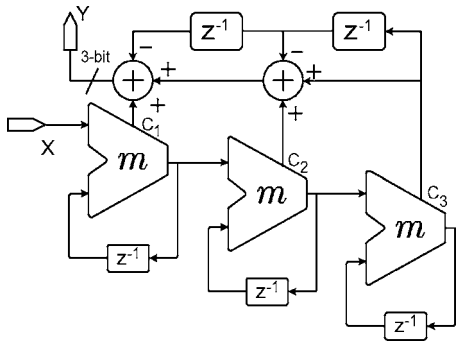

Fig. 7. Digital MASH $\Sigma\Delta$ modulator.

presented in [13] (see Fig. 5); the dither signal is obtained from a 20-bit *LFSR*, increasing the complexity even more.

Chebyshev Loop: As mentioned for the previous architectures, the reduction in the noise-shaped quantization noise is at the cost of increased noise for low frequencies, and there must be a tradeoff. The architecture shown in Fig. 6 has a Chebyshev noise transfer function and has a better compromise [14].

The noise transfer function of this architecture is

$$N(z) = \frac{z^3 - 3z^2 + 3^z - 1}{(1 - abf)z^3 - (3 + abcd + abf)z^2 + 3z - 1}. \quad (3)$$

This transfer function has the best noise shaping, as will be shown in the next section. Again, the disadvantages in this architecture are the increased hardware and the one-bit quantizer at the output, which makes the spur tones to appear.

C. MASH Architectures

The MASH architectures [15], [16] have the simplest configuration, because they only require adders and registers to be implemented. The MASH $\Sigma\Delta$ modulation uses accumulators in a cascade configuration, and the quantized output of each stage is processed by a noise cancellation logic, as shown in Fig. 7.

Since, for digital MASH architectures, the noise cancellation logic is perfect, the quantization noise is only that of the last accumulator (with a shaping order equal to the modulator's order). Furthermore, unlike most architectures, the signal transfer function does not affect the input. For a constant input, it is not of a concern, but for *frequency synthesizers used as modulators, it is a very valuable characteristic*, because the division modulus factor is time dependent. This architecture is inherently stable, and the dynamic range consists of all the input quantization levels. Moreover, as will be demonstrated in the next section, the noise transfer function has the same high-frequency behavior as some multiloop architectures. Thus, the only disadvantage is the high probability for this architecture to generate spur tones because of the periodic behavior at the output. In this paper, this disadvantage is eliminated in a more efficient way.

D. Comparison Between Architectures

Table I compares the different $\Sigma\Delta$ architectures, when used in a fractional synthesizer, with the normalized loop filter cutoff frequency $(f_c/f_{\rm ref})$, the spur tone magnitude, and the dither characteristic (if used). It is clear that the hybrid, multiloop, and Chebyshev architectures do not need a dither signal to avoid the spur tones, and the loop filter cutoff frequency can be relatively large. This is at the cost of significant increase in the hardware to design the $\Sigma\Delta$ modulator. It can be seen in Table I that, for some single-loop and multiloop architectures, a dither signal is added (as an LSB from an LFSR with more than 24 bits), but they still present spur tones. On the other hand, the MASH modulator has a simpler architecture with only adders and registers, but it is necessary to add a dither signal. Because of this drawback, for fractional synthesizers with MASH modulators, a low-frequency loop filter in the synthesizer is used to reduce the spur tones (see $f_c/f_{\rm ref}$ in Table I).

The noise-shaping figures of the architectures reviewed in this section are presented in Fig. 8. It is clear that the best noise shaping from all the architectures is the $\Sigma\Delta$ Chebyshev, because it reduces the high-frequency-shaped noise. The multiloop and single-loop architectures have an improvement in the noise-shaping reduction, but again the hardware is increased. The MASH architecture has a similar noise-shaping function (even compared with the multiloop architecture), but the most

TABLE I
$\Sigma\Delta$ ARCHITECTURE COMPARISON

Publication	f_c/f_{ref}	$\Sigma\Delta$	$\Sigma\Delta$ Order	Synt. order	Dither	Spurs
[10]	$40e3/8e6 = 0.005$	Single-Loop	3	4	2^{24} LFSR	-80dB@200KHz
[11] , [12]	$30e3/13e6 = 0.023$	Multi-Loop	4	5	No dither	-70dB@300KHz
[13]	$200e3/13e6 = 0.0153$	Multi-Loop	3	4	2^{10} Off-Chip LFSR	No
[6]	$100e3/5e6 = 0.02$	Hybrid	≥ 4	5	No Dither	-70dB@10MHz
[9]	$50e3/16e6 = 0.0031$	Hybrid	≥ 6	3	No Dither	No
[14]	$200e3/18.75e6 = 0.0106$	Chebyshev	3	5	No Dither	No
[16]	$35e3/26e6 = 0.00135$	MASH	3	4	Off-Chip Dither	No

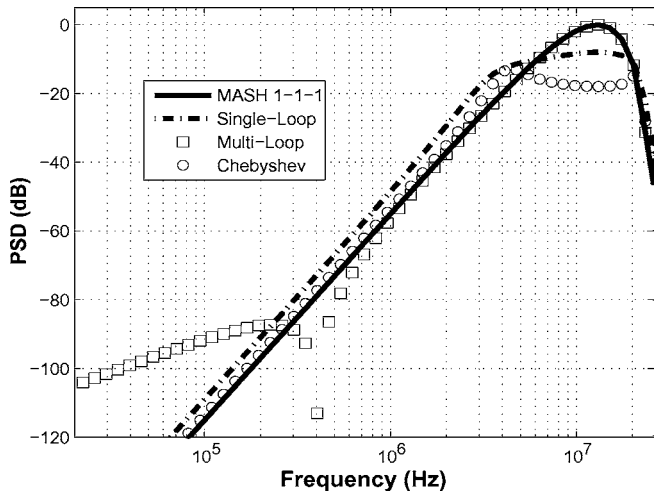

Fig. 8. Noise-shaping comparison of digital $\Sigma\Delta$ modulators.

important advantage is the significant reduction in the hardware, compared with the other topologies.

The only disadvantage of the MASH architecture is the spur tones that are present due to the great simplicity of the architecture. In this paper, it is proposed to add a pseudorandom sequence for MASH architectures in a more efficient way.

III. SPUR TONE REDUCTION IN MASH MODULATORS

In the previous section, it was concluded that the MASH modulators are the most simple digital $\Sigma\Delta$ modulators and have very similar noise-shaping figures, compared with more sophisticated architectures, but they may present spur tones. Some works in literature that have reduced the spur tones in the MASH architecture are listed in the next sections to make a comparison.

Prime Modulus Quantizer: To reduce the spur tone magnitude, a high-resolution digital MASH $\Sigma\Delta$ modulator can be used (increasing the hardware), where it is necessary to set a sort of initial conditions, as empirically demonstrated by Borkowski and Kostamovaara in [17] and [18]. This was later mathematically demonstrated by Hosseini and Kennedy [3], with the estimation of the sequence length of an lth-order MASH architecture. It was also demonstrated that the sequence length is equal to the quantization level M, if M is a prime number. This design consideration reduces the spur tone magnitude, but the prime modulus quantizer is more complicated than a power of two quantizer. Another disadvantage is the need to ensure the zero initial conditions for the quantization errors in the digital modulator.

Output Feedback: Liu *et al.* [19] proposed a novel topology to randomize the output sequence of a MASH modulator. The technique takes the output of the digital MASH architecture and processes it into another digital accumulator; the accumulator output substitutes the carry in of the second stage. The technique should not be used for a non-dc input as the $\Sigma\Delta$ filters the input signal; the filtering also depends on the resolution of the modulator. Furthermore, as the extra accumulator feeds back the output sequence, the dither is correlated to the input signal.

Modified Error Feedback Modulator (MEFM): Hosseini and Kennedy [2], [4] created a theory to ensure a maximum sequence length in MASH architectures with a modified accumulator, having a feedback loop. With this theory, all the semi-empirical works previously presented can be explained. Nevertheless, for the *MEFM* MASH modulators to have a maximal-length sequence, every accumulator needs an extra M-bit adder. In addition, an output filter to compensate the feedback paths in the modulator must be instantiated at the MASH output. Under these conditions, the MASH architecture has as much hardware as the single-loop architecture presented in Section II.

Shaped Additive LFSR Dither: Adding a pseudorandom signal at the modulator's *input LSB* is one of the first techniques to reduce the spur tone magnitude for any digital $\Sigma\Delta$ modulator. The basic idea is to use a very long pseudorandom generator to make the quantization error appear more randomized. The problem with this way of reducing the spur tone magnitude is not only the modification to the input signal but also the increased quantization noise for very low frequencies in the output spectrum. This drawback was later solved by introducing a shaped dithered signal by an analog $\Sigma\Delta$ modulator with an input dc value [20]. In addition, in that work, it was proposed to add the dither signal into the MASH accumulator stages in order to obtain a shaped dither.

To compare these mentioned techniques, we show the simulations of a 4-bit digital MASH $\Sigma\Delta$ modulator in Fig. 9. The simulations were run with the same parameters of the last section but with a 9-MHz sinusoidal input value. For this low-resolution digital MASH, the feedback dithering technique [19] presents spur tones, even when the input signal is not a constant value. For these dynamic simulations, dithering has the same performance as that in the undithered case. At this point, the MEFM is a good technique but considerably increases the hardware.

In this paper, the different forms to add a pseudorandom sequence from an *LFSR* in MASH topologies are explored. It is demonstrated that the *LFSR* size can be reduced, and the spur tone reduction is as effective as more complex techniques but at a lesser extent.

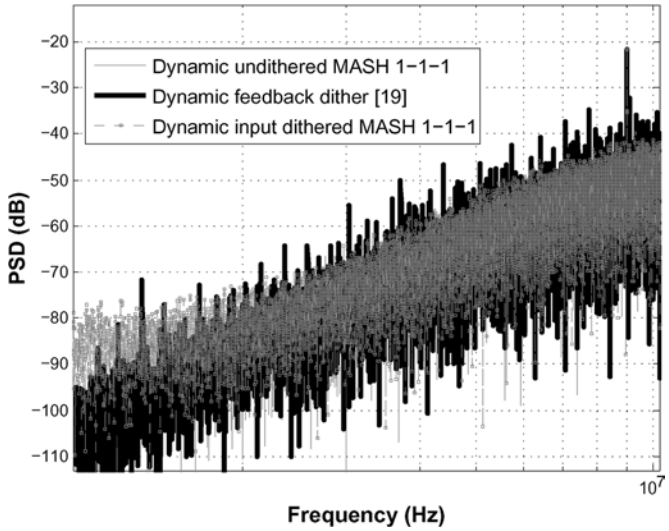

Fig. 9. Comparison of state-of-the-art spur tone reduction techniques.

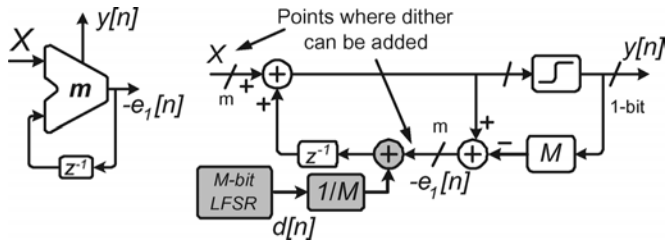

Fig. 10. Digital accumulator model.

IV. Dithering MASH ΣΔ Modulators With LFSRs

The research presented in this section deals with the addition of a dither signal coming from a pseudorandom generator (an LFSR) into MASH architectures. Although the substitution of the LSB into the digital MASH modulators is not an addition, the only way to obtain a closed-form expression to estimate their periodicity is by approximating this action as an addition. Moreover, the theory proposed by Hosseini and Kennedy [2], [3] is used in this work to propose an efficient way to add the dither signal from a small-sized LFSR and not from a very large one, as it was done before.

A. Dither With LFSR in a Digital Accumulator

Fig. 10 shows the block-level model of an M-bit digital accumulator, which is the main block of the digital ΣΔ MASH modulators. The access nodes where the dither signal can be added are at the accumulator's input, adder's output, and after the delay. If the dither signal is added at the input of the accumulator, then the traditional LFSR input dither is obtained. If the dither signal is added before or after the delay signal (see Fig. 10), the accumulator's output $Y(z)$ can be expressed as

$$Y(z) \approx X(z) + \frac{1}{M} z^{-1} D(z) + (1 - z^{-1}) E_1(z) \qquad (4)$$

where $X(z)$ is the input signal, $E_1(z)$ is the quantization error, and $D(z)$ is the dither signal.

By substituting the LSB in this way, the dither signal does not affect the input signal $X(z)$. To estimate the periodicity of the digital accumulator for this case, the output error sequence can be calculated as

$$\begin{aligned} e_1[n] &= \left(x[n] + \frac{1}{M} d[n] + e_1[n-1] \right) \bmod M \\ e_1[n-1] &= \left(x[n-1] + \frac{1}{M} d[n-1] + e_1[n-2] \right) \bmod M. \end{aligned} \qquad (5)$$

Then, for a constant input $x[n] = X$, the error signal can be written as

$$e_1[n] = \left(nX + \frac{1}{M} \sum_{k=1}^{n} d[k] + e_1[0] \right) \bmod M \qquad (6)$$

for the quantization error to be periodic, i.e., $e_1[n] = e_1[n+N]$, and

$$\left(NX + \frac{1}{M} \sum_{k=1}^{N} d[k] \right) \bmod M = 0. \qquad (7)$$

To estimate the period of the quantization error N, when the dither signal is added with an LFSR, we take as a premise that this pseudorandom generator has the same number of ones and zeroes [21]. Thus

$$\sum_{k=1}^{N} d[k] = \frac{N}{2} = \frac{KM}{2} \qquad (8)$$

where it is supposed that the dither signal (for the M-bit accumulator) comes from an M-bit LFSR. Then, if $N = KM$, where K is an entire number representing the periodic characteristic of the LFSR, we can write

$$\left(NX + \frac{K}{2} \right) \bmod M = 0 \qquad (9)$$

as $K/2$ can be an entire number for every K power of two; then, the value $(NX + K/2)$ is divisible by M for several values of X, and the dither signal from the M-bit LFSR does not have any effect on the digital accumulator.

Fig. 11 shows the approximated power spectrum from a Matlab-Simulink simulation of an 8-bit accumulator with $X = 128$ for three cases: 1) when the accumulator is not dithered; 2) when the dither is added as in Fig. 10 with an 8-bit LFSR; and 3) when the dither is added with a digital wideband white noise source. It is noticeable that the dither does not randomize the output sequence, even when the dither generator is ideal, which is the case of a very large LFSR. We can conclude from this analysis that increasing the size of the LFSR will not improve the spur tone magnitude reduction. Therefore, (8) is a good approximation in this analysis.

B. Dither in MASH

If two or more accumulators are cascaded, the MASH architecture is obtained. This architecture can be used in fractional synthesizers. When a dither signal is introduced, the quantization noise is filtered by the frequency synthesizer loop.

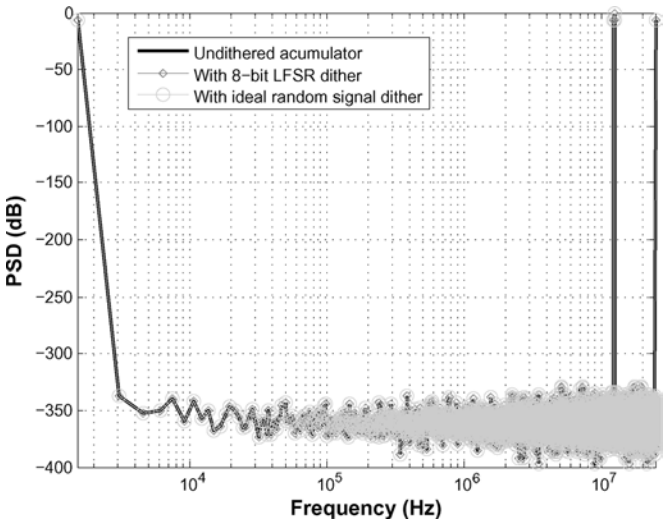

Fig. 11. PSD of a dithered digital accumulator.

However, it is necessary to reduce it if better performance is desired. This can be achieved by introducing the dither signal in the internal nodes of the MASH modulator [20]. In addition, for fractional synthesizers, it is important to *maintain the input signal unchanged*.

In a third-order MASH modulator, the dither can be shaped if the LSB at the input of the third accumulator is substituted by the pseudorandom signal, as it is modeled in Fig. 12. The 3-bit output signal for this case is

$$Y(z) = X(z) + \frac{1}{M}(1-z^{-1})^3 D(z) + (1-z^{-1})^3 E_3(z). \quad (10)$$

The dither signal $D(z)$ now is shaped by the third-order function of the MASH. In order to estimate the period N of the quantization errors in the MASH modulator of Fig. 12, we can write

$$e_1[j] = (jX + e_1[0]) \bmod M \quad (11)$$

$$e_2[k] = \left[\sum_{j=1}^{k} (jX + e_1[0]) \bmod M + e_2[0]\right] \bmod M \quad (12)$$

$$e_2[k] = \left(\frac{k(k+1)}{2}X + e_1[0] + e_2[0]\right) \bmod M \quad (13)$$

and similar to the case of the dithered accumulator, the quantization error in the dithered third stage of the MASH 1-1-1 is

$$e_3[n] = \left[\sum_{k=1}^{n} \left(e_2[k] + \frac{1}{M}d[k] + e_3[0]\right)\right] \bmod M \quad (14)$$

for the quantization error to be periodic, i.e., $e_3[n] = e_3[n+N]$, and using (12)–(14)

$$\left(\frac{N(N+1)(N+2)}{3\cdot 2}X + \frac{1}{M}\sum_{k=1}^{N} d[k]\right) \bmod M = 0 \quad (15)$$

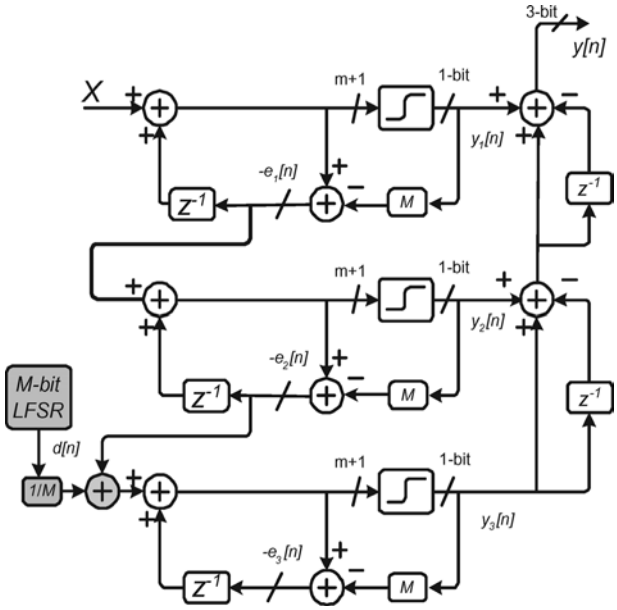

Fig. 12. Dithering the MASH 1-1-1 in the third stage.

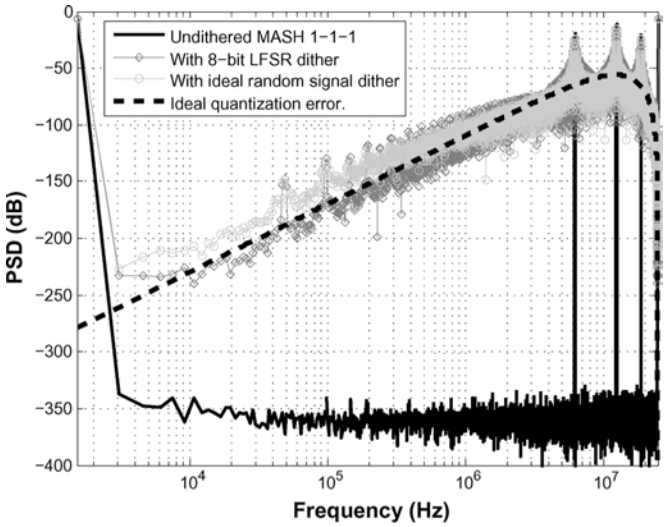

Fig. 13. MASH 1-1-1 output spectrum with dither in the third stage.

if the premise for the LFSRs is used as before, then the last equation can be written as

$$\left(\frac{N(N+1)(N+2)}{3\cdot 2}X + \frac{1}{M}\frac{KM}{2}\right) \bmod M = 0. \quad (16)$$

In this equation, as $K/2$ can be an entire number for every K power of two, the value $(N(N+1)(N+2)X)/3\cdot 2 + K/2)$ is divisible by M for several values of X. Therefore, for this dither topology, the dither signal from a very large LFSR does not reduce the quantization spur tone magnitude.

To prove this, the approximated power spectrum of an 8-bit MASH 1-1-1 modulator from a Matlab simulation is shown again in Fig. 13 for the following cases: when the dither is not added, when the dither is added as in Fig. 12 with an 8-bit LFSR, and with an ideal wideband white noise source.

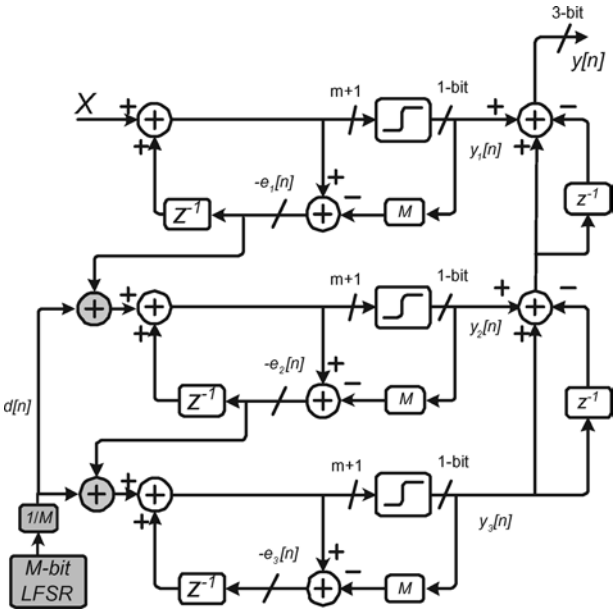

Fig. 14. Proposed solution for dithering the MASH 1-1-1.

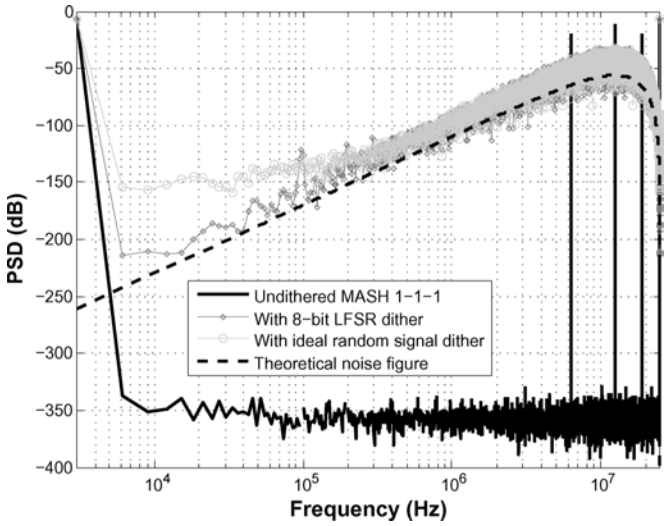

Fig. 15. Efficiently dithered MASH 1-1-1 output spectrum.

From the figure, it can be seen that the spur tone magnitude is the same for the three cases. This proves the theory developed in the last section, i.e., increasing the size of the LFSR will not improve the spur tone magnitude reduction.

C. Effective LFSR Dither for the MASH Modulator

It was demonstrated that, if the dither signal from a pseudorandom generator is added at the input of the third stage (to reduce the low-frequency quantization noise), it will not reduce the spur tone magnitude, regardless if the LFSR sequence length is very large. In spite of this, if the pseudorandom sequence is added in a different path, it can reduce the spur tone magnitude with a very simple pseudorandom generator.

The idea in this analysis is to disable the periodicity of the MASH modulator output sequence. There are several paths where the dither signal can be added, but the selected path must have a tradeoff between the periodicity disabling and low-frequency noise increase. In this research, the best path to add a pseudorandom sequence in a MASH 1-1-1 is shown in Fig. 14. This can be achieved by only substituting the LSB at the input of the last two stages by the signal coming from an M-bit LFSR. This will not add more hardware to the modulator.

The quantization errors for this case are

$$e_2[k] = \left[\frac{k(k+1)}{2} X + \frac{1}{M} \sum_{j=1}^{k} d[j] + e_1[0] + e_2[0] \right] \bmod M \tag{17}$$

$$e_3[n] = \left[\frac{n(n+1)(n+2)}{3 \cdot 2} X + \frac{1}{M} \sum_{k=1}^{n} \sum_{j=1}^{k} d[j] + \sum_{k=1}^{n} d[k] + e_1[0] + e_2[0] + e_3[0] \right] \bmod M \tag{18}$$

for the quantization error to be periodic, i.e., $e_3[n] = e_3[n+N]$, and we can write

$$\left[\frac{N(N+1)(N+2)}{3 \cdot 2} X + \frac{1}{M} \sum_{k=1}^{N} \sum_{j=1}^{k} d[j] + \sum_{k=1}^{N} d[k] \right] \bmod M = 0. \tag{19}$$

Now, the double summation cannot be approximated as an entire number that is divisible by M, because, for every k value, the $d[j]$ values will not be uniformly distributed. With this way of adding the dither signal, the quantization error period N does not depend on the input value X. When the dither signal is added as it is proposed, the 3-bit output after the noise cancellation logic can be written as

$$Y(z) = X(z) + \frac{1}{M} D(z) \left((1 - z^{-1}) + (1 - z^{-1})^2 \right) + (1 - z^{-1})^3 E_3(z). \tag{20}$$

Fig. 15 shows the approximated output PSD of the 8-bit simulated MASH 1-1-1 modulator for three cases: 1) when the modulator is not dithered; 2) when a dither signal from a simple 8-bit LFSR is added as in Fig. 14; and 3) when an ideal wideband white noise source is added as the dither signal in the same figure. It can be seen that the 8-bit LFSR dither is enough to reduce the spur tones at high frequencies, although some low-frequency components increase the noise (but they can be filtered by the frequency synthesizer, as demonstrated in Fig. 16).

If the sequence length of the pseudorandom generator is increased up to an ideal random signal (see Fig. 15), the dither noise is shaped, and the low-frequency noise increases. Nevertheless, the high-frequency spur tone magnitude is the same as that for the 8-bit LFSR case.

The advantages in adding a dither signal in this way is the noise-shaping function for the dither signal with *no additional components* but only the substitution of the LSBs at the indicated nodes. In addition, a very simple M-bit LFSR can be used

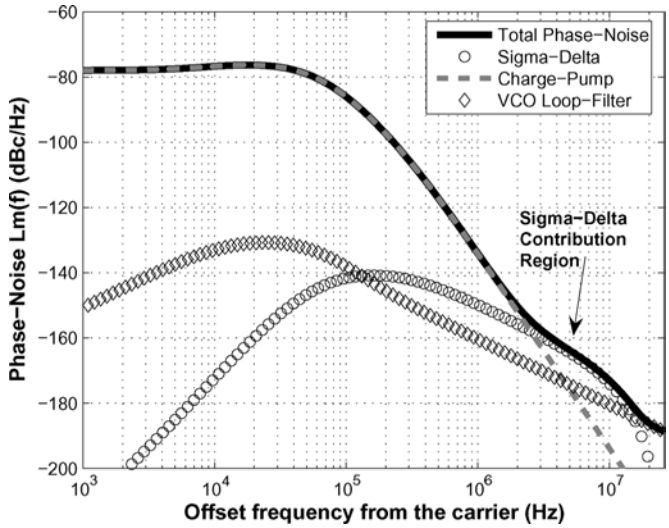

Fig. 16. $\Sigma\Delta$ modulator contribution to phase noise in a fractional synthesizer.

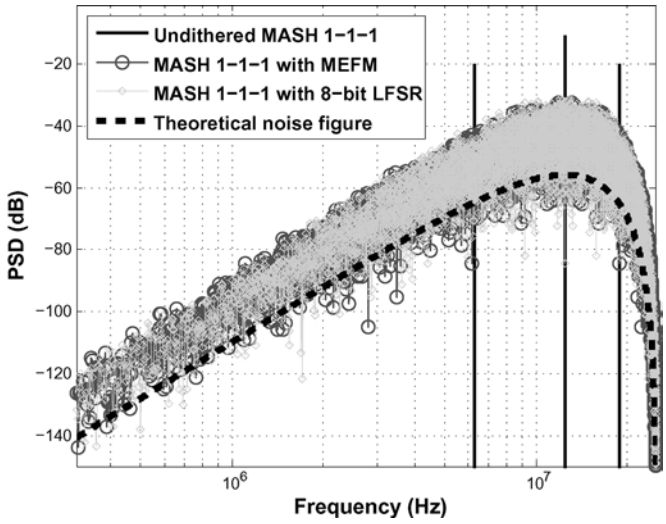

Fig. 18. Measurement results from the digital modulator for $X = 128$.

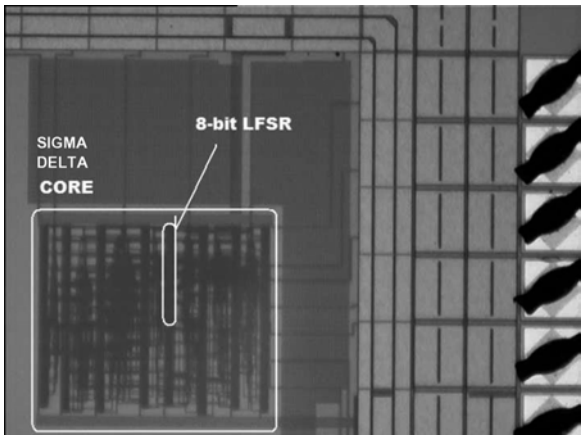

Fig. 17. Microphotograph of the fabricated digital $\Sigma\Delta$ modulator.

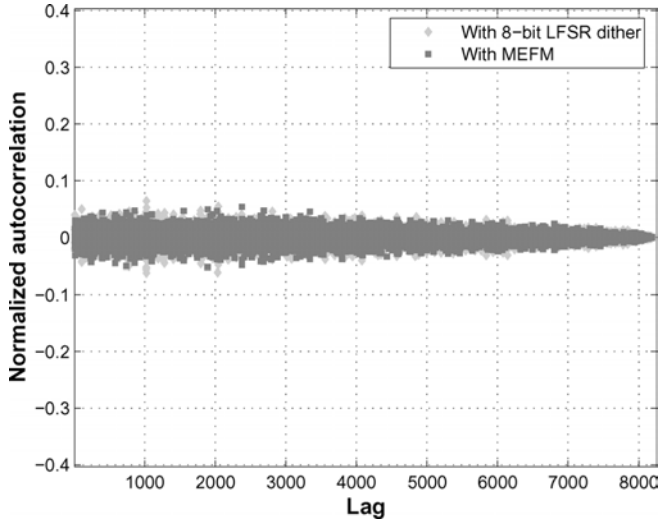

Fig. 19. Comparison of output autocorrelation sequences.

to reduce the spur tone magnitude for the high frequencies offset from the carrier (which are the components affecting the total fractional synthesizer phase noise). Another advantage among the previous techniques is that the constant modulated signal is not affected by the dither addition, and there is no need for a postfilter stage.

V. Experimental Results

In order to demonstrate the advantages of the proposed dither addition, a third-order digital MASH $\Sigma\Delta$ modulator was fabricated in a 0.35-μm CMOS process, and it is shown in Fig. 17. The MASH 1-1-1 has an 8-bit resolution in each accumulator, and the dither generator is a simple 8-bit LFSR. The output from this very simple dither generator is applied to the MASH modulator, as proposed in Section IV-C, and the data were obtained with a logic analyzer HP 1663 A.

Fig. 18 shows a comparison of the measured PSD of the fabricated MASH modulator when it is not dithered, when the dither is added with an 8-bit LFSR, and with a simulation in Matlab for the MEFM MASH [4]. The sample frequency is 25 MHz with the critical constant input value $X = 128$, and the power spectrums are compared to the theoretical quantization error. The spur tone magnitude reduction at high frequencies is the same for the MEFM and the simple M-bit LFSR dither. As the noise increase (due to the noise shaping) for low frequencies can be eliminated by the fractional synthesizer, the 8-bit LFSR proposed dither is as effective as the MEFM structure but is much less complicated.

The autocorrelation sequence is the best form to explore the periodicity of a discrete sequence, and it was calculated for a 2^{13} output sequence for the measured data and a simulated MASH 1-1-1 MEFM. Fig. 19 shows a detailed view of the autocorrelation sequences; it can be seen that both of them have very similar characteristics, which means that they have the same periodic behavior.

The MASH 1-1-1 MEFM [4] is used to compare the 8-bit LFSR dither addition as it is the most effective spur tone magnitude reduction up to now. It has been proven that the simple 8-bit LFSR is enough to reduce the spur tone magnitude if it is added in the indicated nodes, which disable the MASH periodicity. The only difference between the simple dither addition and the MASH MEFM structure is the hardware budget. Table II makes a coarse comparison of the hardware used for both spur

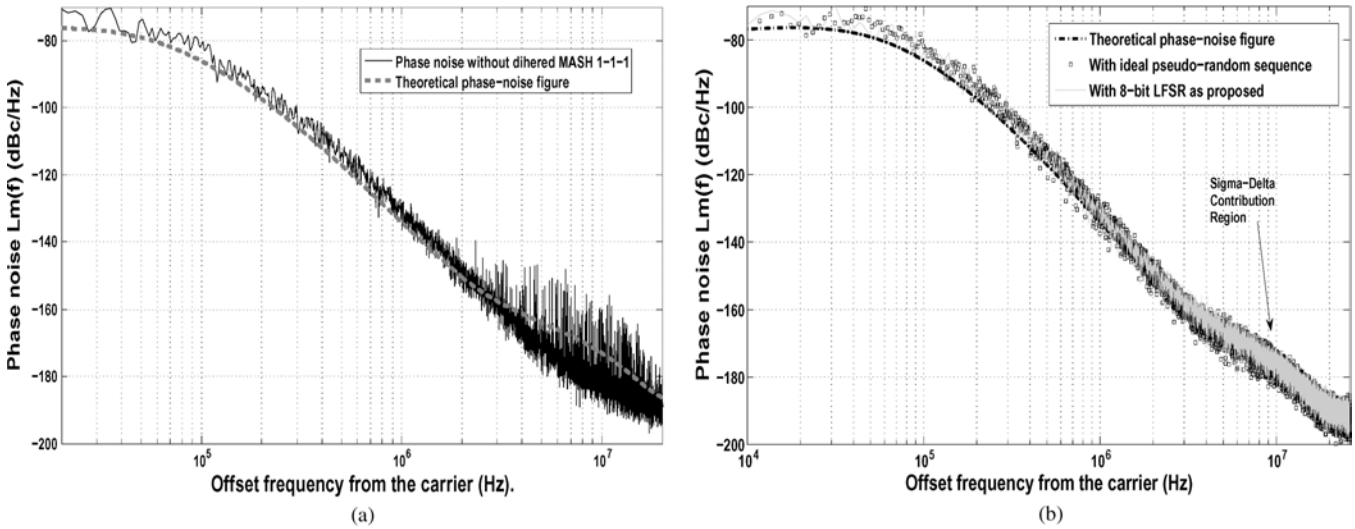

Fig. 20. Simulation results from the fractional synthesizer behavioral model. (a) Phase noise without dither. (b) Phase noise with dither from an 8-bit LFSR.

TABLE II
$\Sigma\Delta$ HARDWARE COMPARISON

Architecture	Number of gates	Normalized Hardware	Power @25MHz
Undithered MASH 1-1-1	420	100%	3.6mW
MEFM MASH 1-1-1	640	152%	N.A.
M-bit LFSR dither	460	109%	3.61mW

TABLE III
FRACTIONAL-N FREQUENCY SYNTHESIZER'S CHARACTERISTICS

Synthesizer	$4rd$ order	Tuning	$(1.47-1.87)GHz$
$\Sigma\Delta$ modulator	MASH 1-1-1	F_{ref}	$26MHz$
$\Sigma\Delta$ output bits	4	f_c	$\approx 100KHz$

tone reduction strategies, taking into account only the number of gates used for each one. The number of gates was obtained from the Matlab simulations for the MEFM and the proposed dither technique.

The simple 8-bit LFSR dithering increases the number of gates by less than 10%. With this little increase in the number of gates, the layout area could slightly increase due to the routing. With the MEFM strategy, the gate number increases by about 50%; this increase in the number of gates will strongly impact the chip area and power consumption. In addition, in Table II, the measured power consumption of the architectures is compared. The power increase with the 8-bit LFSR dither is minimum.

To characterize the effectiveness of the simple 8-bit LFSR dither, a fractional synthesizer (with the parameters shown in Table III) was simulated with behavioral models in VerilogA [22]. The simulation includes the three major noise sources in the fractional synthesizer: 1) the noise from the charge pump; 2) the noise from the VCO and loop filter; and 3) the noise from the quantization error in the digital $\Sigma\Delta$ modulator. A transient simulation was run, and the output from the fractional synthesizer is processed in Matlab to obtain the approximated output spectrum with a *Welch* algorithm.

Fig. 20(a) shows the synthesizer's output phase noise from the behavioral simulation for the case when no dither is added. The phase noise was obtained from a 2^{24} sample sequence using the windowed method and compared to an analytical prediction [23]. Around the region where the $\Sigma\Delta$ modulator dominates the output phase noise, it can be seen how the spur tones degrade the phase noise up to $+20$ dB.

When the 8-bit LFSR, which is used as dither generator, is activated, the spur tones are well disabled, as shown in Fig. 20(b). In the same figure, the phase noise from a simulation with an ideal dithered signal (which is simulated with an ideal wideband white noise source) is plotted to demonstrate that the simple 8-bit LFSR is enough to randomize the fractional synthesizer for the frequencies of interest in the phase noise figure. Regardless of the dither signal being shaped, the noise levels are not significant, and the simple dither generator is as effective as that in more sophisticated architectures but has much lower area and, therefore, cost.

VI. CONCLUSION

It has been demonstrated that a simple M-bit LFSR in an M-bit MASH architecture reduces the spur tone magnitude as effectively as more complicated state-of-the-art MASH spur reduction techniques. The theoretical study on this paper has also used the state-of-the-art theory on maximum-sequence-length MASH modulators [3] to demonstrate that increasing the size of an LFSR as much as possible will not improve the spur tone reduction, even if the dither signal is added in a path that totally shapes the dither signal.

The explored paths, to add the dither signal, make the quantization noise increase for low-frequency values, but these components are filtered by the fractional synthesizer. Therefore, the simple M-bit LFSR dither signal makes it possible to barely increase the number of gates of the MASH modulators and the circuit cost. Another advantage is that the signal transfer function is not affected by simple dither addition, and there is no need to filter the signal from the MASH modulator when the fractional synthesizer is not used with a constant input signal.

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