Designing Adaptive Conditioning Electronics for Smart Sensing

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***Abstract*—This paper presents a robust digitally programmable CMOS analogue processor designed for sensor output conditioning in embedded applications. In addition, system adaptability allows for correction of the deviations in circuit operation due to ageing, mismatch or environmental effects, lending a smart nature to the devices. In order to tune the free parameters of the system, two training strategies based on perturbative algorithms are compared. The processor performance is validated by adjusting the response of an angular position sensor and the insensitivity to parameter mismatch is demonstrated through high-level simulations based on Monte Carlo electrical simulation data.**

***Index Terms*—Adaptive signal processing, intelligent sensors, mixed analog-digital integrated circuits.**

I. Introduction

TODAY'S sensor market is advanced towards the so called *smart sensors*, that is, integrated sensor systems that contain on a single chip the sensing, interfacing, signal processing and intelligence (self-testing, self-identification, and self-adaptation) functions [1]. For the realization of these smart sensor systems, CMOS is the most suitable technology due to the capability of cointegration of sensors and sensor electronics, both analogue and digital. Therefore, at present, research challenges are focused on the implementation of low cost high performance CMOS smart sensors. Furthermore, if these smart sensors target the ever-increasing wireless sensor network (WSN) market, low-voltage low-power electronic circuits are required to maximize the lifetime of the battery operated systems.

To standardize the sensor output response, the transfer function from the sensor input to the electrical output should be the same for all sensors of the same type. However, due to process variations, properties vary from device to device and so do transfer characteristics. Therefore, calibration is mandatory to achieve a precise relation between the electrical output and the physical signal being measured. Accurate sensors are usually more expensive than uncalibrated sensors because the calibration process is individually carried out for each device, pushing up production costs. Alternatively, automation of calibration is possible provided that the smart sensor contains a digitally programmable calibration function. This not only reduces costs and minimizes calibration time at factory, but also allows the customer to perform recalibration if necessary [2].

There are several methods for calibrating linearity errors in the sensor transfer characteristic, such as piecewise-linear interpolation, lookup table-based linearization and electronic implementation of the inverse function of the sensor curve [3]–[6]. Another option is the use of Artificial Neural Networks (ANNs), which, for linearization purposes, are made up of only a small number of programmable neurons or processing units. As a result, ANNs constitute a flexible solution at a low cost in terms of area, power consumption and computational complexity, thus being a valuable choice for adaptive sensor processing in embedded applications.

This paper presents a CMOS digitally programmable analogue processor which consists of basic current-mode processing units arranged in a multilayer perceptron configuration, a well known type of ANN suitable for small application-specific circuits because of the reduced set of arithmetical operations that it can perform [7], [8]. The proposed conditioning circuit provides a robust method to linearize an output sensor response while it can also compensate for deviations in the sensor transfer function due to ageing and cross-sensitivity to temperature [9]. In its design, as the proposed calibration technique is based on analogue signal processing, sensitivity to process parameter mismatches becomes a major issue [10]. Furthermore, performance of classical learning algorithms used in ANNs is degraded by nonidealities in the operation of the arithmetic blocks [11]. Therefore, a careful design of the ASIC and specific layout techniques to reduce transistor mismatch are essential. The feasibility of the proposed approach is demonstrated through an example: the output of a giant magneto-resistive (GMR) sensor is linearized through the proposed conditioning circuitry and its robustness to mismatches is confirmed through high-level system operation simulations based on electrical simulation data.

This paper is structured as follows. Section II presents the design of the basic building blocks which make up the adaptive conditioning circuit, as well as the complete perceptron processing architecture. Two different system training strategies for

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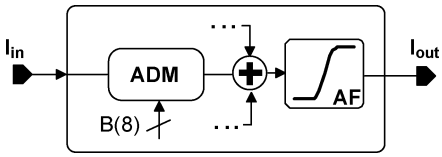

Fig. 1. Basic current mode processing unit.

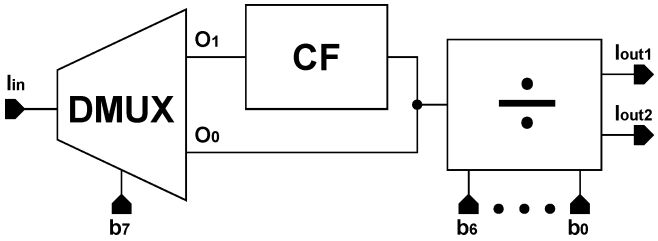

Fig. 2. Mixed A/D full multiplier.

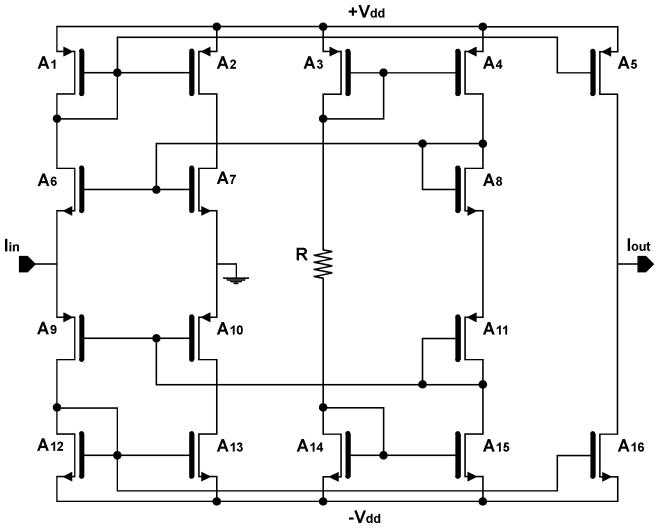

Fig. 3. Sign circuit. Class AB noninverting current follower (CF).

the calculation of calibration parameters are presented and compared in Section III. Then, in Section IV, the proposed conditioning circuit is validated by linearizing the output response of a GMR sensor and the circuit robustness to mismatches is demonstrated by using high-level models for Monte Carlo simulations. Finally, conclusions are drawn in Section V.

II. CMOS Conditioning Circuit

Distributed monitoring systems are more and more used in industrial process control, health care, environmental analysis and many other application domains. However, battery-operated portable embedded systems demand low power consumption and high processing speed. This is not easy to achieve with the voltage-mode approach in analogue signal processing due to the progressive reduction of bias voltages in submicron technologies. Furthermore, analogue processors based on ANNs consist of a number of unit cells and minimizing the area consumption of the basic processing unit leads to a considerable area reduction of the whole system. To design small, fast and power saving processors compatible with low bias voltage, the analogue current mode approach appears to be the best choice [12].

Another issue to consider in the design of the basic ANN analogue processing unit is the necessity of accuracy in order to ensure robust operation of the processor. Accuracy, in turn, is limited by mismatches between transistors. Unfortunately, the design and layout techniques to improve transistor matching directly impact on the area, power consumption, and operational speed of the system [13]. Thus, a careful design is mandatory to achieve good performance.

Programmable coefficients must be stored in on-chip memories to confer adaptability to the system and allow for automatic calibration of the smart sensor. Analogue memories are not reliable enough, as low accuracy stems from mismatch and offsets. In contrast, digital register-based memories exhibit immunity to noise and to interference. Furthermore, their quiescent power consumption is negligible, which is a very convenient feature in our target application. Processing the signals in the analogue domain while storing and applying the programmable coefficients in the digital form thereby, takes advantage of both the analogue and the digital approaches.

Taking all these issues into account, a complete ANN-based CMOS conditioning circuit based on the analogue-digital current-mode processing unit shown in Fig. 1 has been designed using a standard 0.35 μm–3.3 V CMOS process. Its basic components are: a set of linear analogue-digital full multipliers (ADM), which multiply their corresponding input current by a set of digital weighting values; and an activation function (AF) circuit, that generates the processor unit output by performing a nonlinear operation with the weighted sum of the input currents. The description and implementation of these main blocks and of the multilayer perceptron configuration constituting the complete conditioning circuit are described in the following.

A. Multiplier

Processor adaptability is achieved by using a mixed-mode programmable multiplier. The use of this cell to implement adaptive processors was presented in [14] and [15], where promising results were obtained in practical applications. The required resolution depends on the minimum accuracy needed to solve the problem. Usually, data classification tasks require lower resolution than continuous function estimation tasks [16]. In our case, an 8-bit weight representation provides satisfactory accuracy, as will be shown next.

The proposed 8-bit ADM is depicted in Fig. 2. It is composed of an input 1-to-2 analogue demultiplexer (DMUX), a current follower (CF) and a 7-bit digitally programmable current ladder ($\div$). The 8-bit digital weight controls the direction and amount of current flowing through each of the outputs. The sign bit (b_7) selects the output current direction, forcing the current to flow through the current follower (Fig. 3) when b_7 is high. The current ladder is an NMOS programmable structure based on the classical R-2R current ladder [17], as shown in Fig. 4. The input current I_0 is divided into two currents $I_{out1} = \Delta I_0$ and $I_{out2} = (1-\Delta)I_0$, where the division factor Δ is controlled by

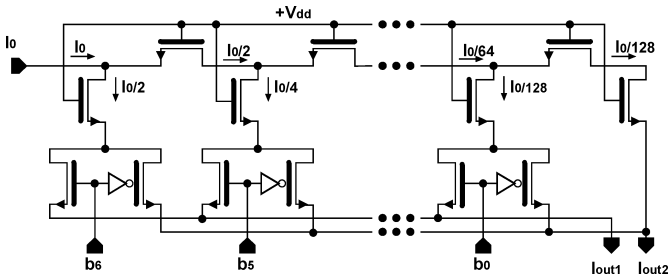

Fig. 4. Current ladder (÷).

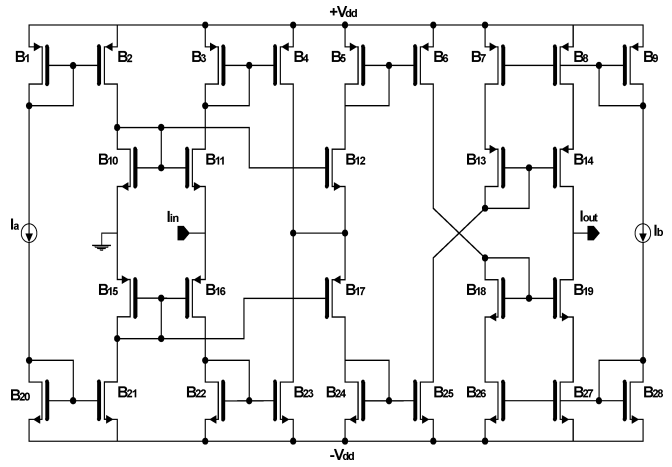

Fig. 5. Activation function circuit.

the digital word $\mathrm{B}(7) = \{b_6, b_5, \ldots, b_0\}$ and its value is given by

$$\Delta = \frac{1}{2^n}\left(\sum_{j=0}^{n-1} b_j 2^j\right) \quad \text{with n} = 7. \tag{1}$$

In this work, I_{out1} is the signal to be processed, whereas I_{out2} is driven to ground. Provided that all transistors which work in the ON state (triode region) have the same gate voltage V_{dd}, the linear MOS current division principle [18] is applicable to this structure and, therefore, the quotients I_{out1}/I_{in} and I_{out2}/I_{in} are inherently linear. Then, the ideal output current of the whole ADM is given by

$$I_{out1} = wI_{in} \quad \wedge \quad w = (-1)^{b_7}\frac{1}{2^7}\left(\sum_{j=0}^{6} b_j 2^j\right). \tag{2}$$

To ensure good device matching, current divider transistor sizes were selected $(\mathrm{W/L}) = (5\ \mu\mathrm{m}/2\ \mu\mathrm{m})$.

B. Activation Function

A processor with nonlinear features can be applied in a wider variety of problems than a linear processor. Thus, the AF circuit in the proposed processing architecture consists of a class AB current amplifier (Fig. 5) implementing a sigmoid circuit with a bias current $I_a = 25\ \mu\mathrm{A}$ (for $I_{in} = 0$). Note that the current I_b (right side of the schematic) limits the maximum absolute value of the output current to a predetermined value, fixed to 50 μA, providing the nonlinear operation.

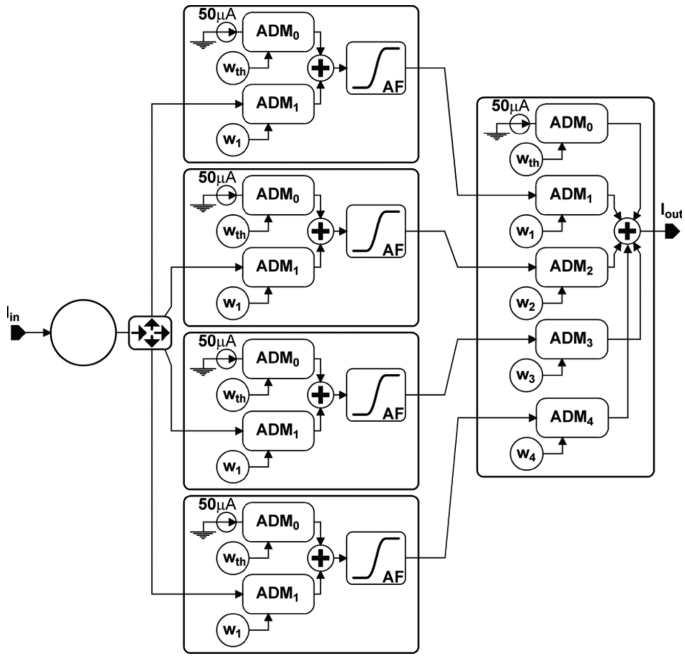

Fig. 6. ANN conditioning circuit: 1-4-1 perceptron-based architecture.

C. Processing Architecture

Fig. 6 shows the complete conditioning circuit based on the former presented basic building blocks. It consists of five perceptrons in two layers, in a 1-4-1 configuration. ADM circuits provide programmability through digital weights $W = \mathrm{B}(8)$, offering the required accuracy to achieve good system performance. The input signal is replicated and driven to the inputs of the four processors in the first processing layer. Here, each of the mixed analogue-digital multipliers weights the input current by a digital value w_i. This weighted current, added to an additional term which corresponds to the weighted limiting 50 μA current, is carried out to the input of the activation function circuit. The output processor combines the different currents from the four processors in the last layer, plus an additional bias value, giving the conditioning circuit output. The operation of the system can be adjusted by setting the appropriate weight values in the registers.

III. Perceptron Operation and Training Algorithms

As just seen, perceptrons are processing units that operate weighting and accumulating input signals, providing a nonlinear output. The perceptron weights are the free parameters used to adjust the system transfer function to match the target response. In order to select the proper weight values, a training algorithm is needed. In this work, the operation of the conditioning circuit is tuned using algorithms based on parameter perturbation: although weight tuning techniques based on error backpropagation algorithms work properly in the presence of some circuit nonidealities [11], [19], perturbative algorithms present higher robustness to circuit mismatches and offsets at a lower complexity cost.

These algorithms change the value of a set of weights $W = [w_{ij}]$ in the network with small random $[pert_{ij}]$ weight perturbations

$$W' = W + [pert_{ij}] \tag{3}$$

evaluating the root mean square error (RMSE) achieved in the system transfer function when the perturbation is added

$$E(W') = rms(\sum_k (o_k - f(W')) \tag{4}$$

where o_k are the target network outputs for each input pattern k, and $f(W')$ is the conditioning transfer function using the perturbed weights. If the resulting value $E(W')$ is smaller than the previous error $E(W)$, modified weights W' are kept; otherwise, weights W remain unchanged. This process is repeated until the system reaches the desired performance.

In this work, two different perturbation strategies have been tested: parallel and single-parameter perturbation. For each case, we present a study of the range of perturbation values versus the minimum RMSE achieved for a conditioning circuit applied to extend the linear span of a sensor, limiting the training process to 400 successive iterations as a practical tradeoff between calculation time and accuracy. Results are obtained by averaging ten complete training process samples for each one of the possible perturbation ranges and training strategies.

A. Parallel Perturbation

In this learning approach, the full digital weight set of the conditioning circuit is modified in parallel and the RMSE of the output is calculated for the new weight configuration. Fig. 7(a) shows the normalized RMSE (RMSE of the processed output compared to the RMSE of the raw sensor) as a function of the maximum number of parameter bits that can be modified. It can be seen that the RMSE increases exponentially with the number of bits that can be modified, thus reducing the weight training performance.

B. Single-Parameter Perturbation

In this perturbation strategy, the output RMSE is calculated after modifying only one randomly selected weight. Fig. 7(b) shows the normalized RMSE as a function of the maximum number of bits that can be perturbed. In this case, the achieved RMSE remains almost constant for perturbations up to 6 bits.

By comparing Fig. 7(a) and (b), both training techniques provide similar results for variations up to 4 bits. Therefore, due to its lower complexity, single-parameter algorithm is a better choice for hardware implementation, since only a perturbation from 1 to 6 bits must be calculated per iteration, as opposed to the set of N 1-to-3 bit perturbations required for the parallel perturbation algorithm, in a conditioning circuit with N parameters.

In addition, by using a single-parameter perturbation algorithm the system can double the linear range of the sensor in less than the selected limit of 400 iterations, assuming a maximum error of 1° in the angle estimation. Fig. 8 shows the evolution of the RMSE for two single-parameter perturbation training cases [perturbing two bits, see Fig. 7(b)]. Weight is updated only when the new RMSE decreases. In the single-parameter perturbation algorithm, the convergence time is limited by the weight updating time (weight selection, perturbation, error estimation and comparison to previous error) and not by the mixed-mode perceptron operation.

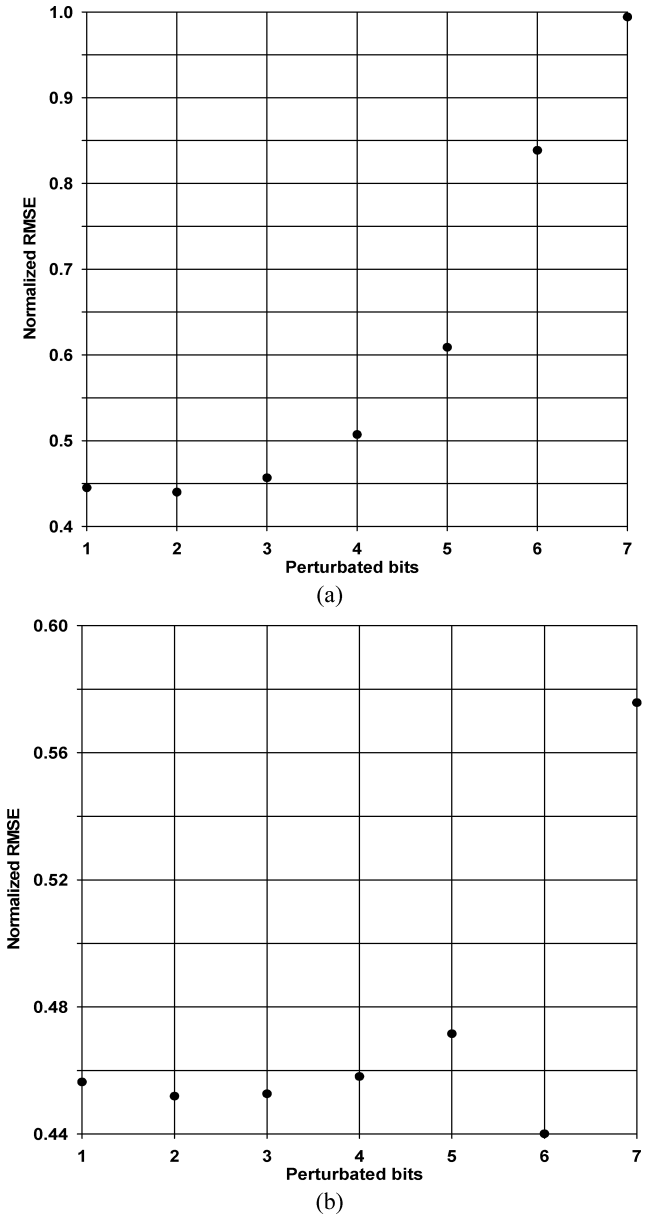

Fig. 7. (a) Parallel and (b) single-parameter training algorithms: RMSE versus number of bits perturbed.

IV. Results

The ANN-based conditioning circuit of Fig. 6 has been designed in a standard 0.35 μm–3.3 V CMOS process. Fig. 9 shows the 8-bit full multiplier output for several digital words, i.e., for different current scaling ratios, as a function of the input current. The simulated and ideal AF response, as well as their difference ($I_{out} - I_{ideal}$), are shown in Fig. 10. Note that, as expected, the output is limited to ± 50 μA, and so will the currents to be driven to the next layer of processors.

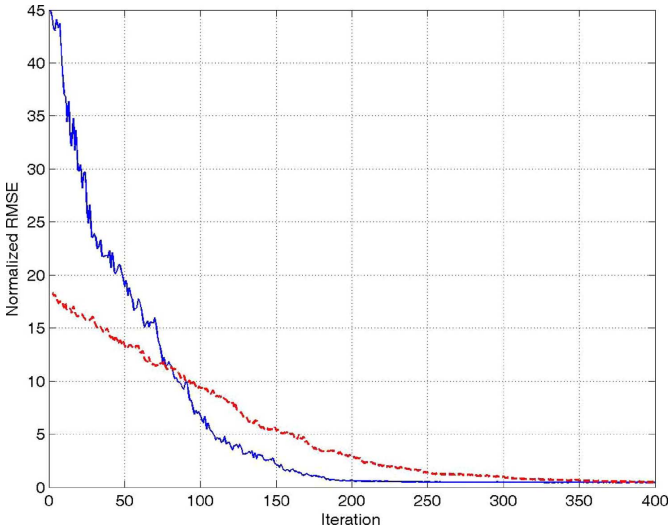

Fig. 8. Evolution of RMSE for two different single perturbation training cases.

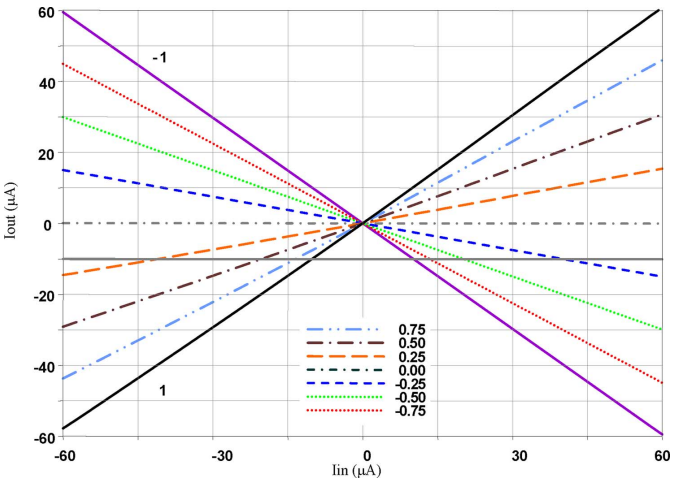

Fig. 9. Mixed multiplier output for several digital operands.

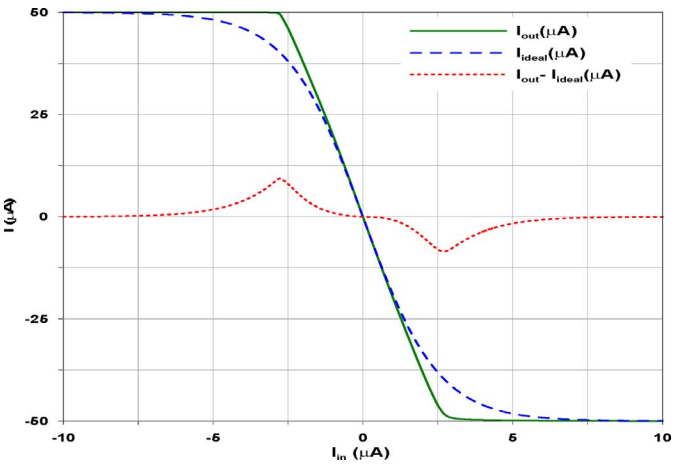

Fig. 10. Simulated (solid line), ideal (dashed) activation functions and the difference between them ($\mathrm{I}_{out} - \mathrm{I}_{ideal}$) (dotted).

The whole processing architecture, including digital memories, takes up an active area of 0.25 mm^2. The maximum operation power consumption is 10.8 mW and the leakage power

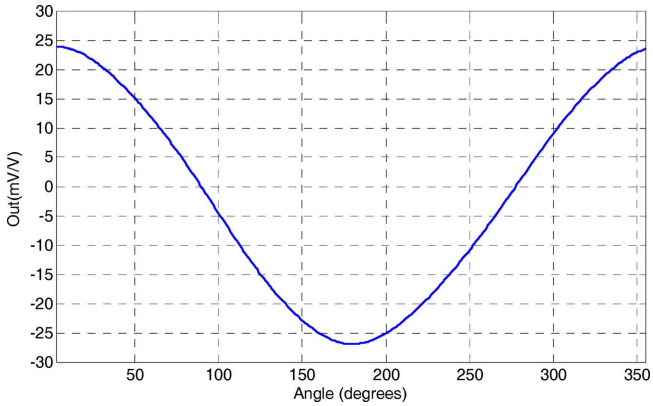

Fig. 11. GMR output behavior into a magnetic field.

consumption in quiescent state, lower than 104 nW, is only due to the memory registers. To verify its performance and robustness to circuit mismatches, the proposed CMOS conditioning architecture is employed to compensate the nonlinearity in the response of a giant magneto-resistive sensor (GMR) [20] meant for angular position measurements [21], [22]. Fig. 11 shows the output of the GMR as a function of its orientation into a magnetic field. It presents a sinusoidal dependence with the angular position, which is only linear in the center of the 0–180 and 180–360 degree ranges. Consequently, by compensating the nonidealities of the sensor behavior it is possible to extend its linear range, thus improving a subsequent analogue-to-digital conversion.

A. *Compensation Circuit*

Output linearization is simulated using the proposed unit elements arranged in the architecture shown in Fig. 6.

Patterns consist of 175 GMR output measurements collected in the 180°–355° range. Data are divided in two datasets: 10% of the patterns are used during the verification stage and the rest of them are used in the tuning or calibration process. The goal is to extend the span where the error is smaller than 1°. Using the standard circuit electric models (without mismatch effects), and a single-parameter perturbation algorithm, the sensor compensated span is 125% higher than the raw output, as shown in Fig. 12.

B. *Effects of Mismatch*

To study the effects of mismatch on the adaptive conditioning circuit, process (batch-to-batch) and mismatch (per instance) Monte Carlo (MC) statistical variations for netlist parameters at nominal temperature (27 °C) were carried out according to the manufacturer's specifications [23]. However, as these simulations are quite time-consuming and computationally intensive, they were performed individually for each building block. Therefore, based on MC electrical simulation data, both the ADM and AF circuits were numerically modeled in Matlab at a system level. High-level simulations were then carried out to study mismatch effects on the whole processing architecture in a more efficient way.

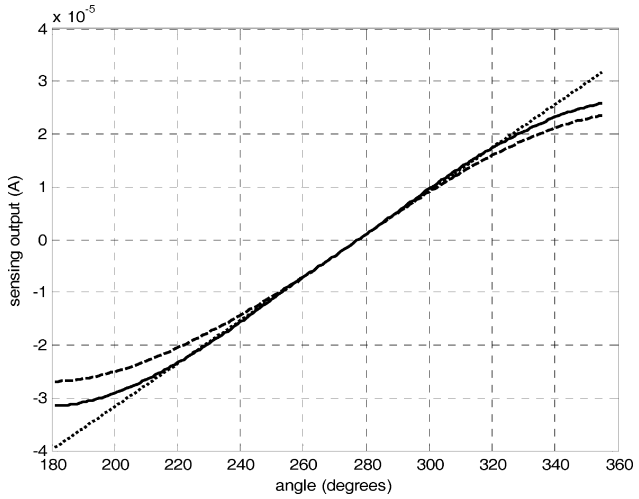

Fig. 12. GMR behavior (dashed line) compared to ideal linear output (dots) and compensated output (continuous).

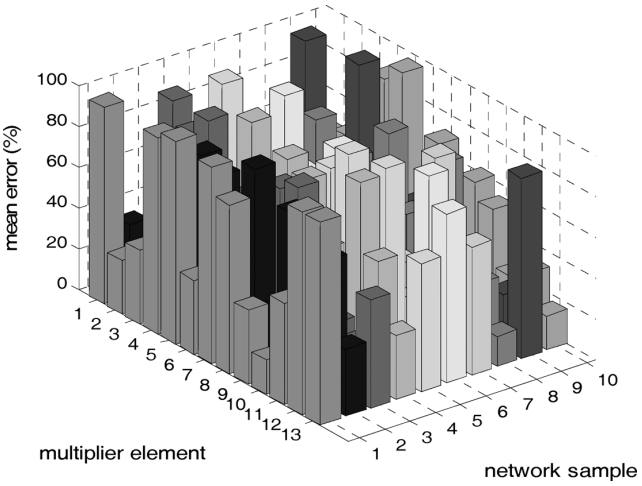

Fig. 13. Mean error for the mismatching-dependent multipliers.

From Monte Carlo simulation results, the 8-bit ADM operation can be modeled by

$$I_{out1} = \alpha\ w\, I_{in} + \beta\ I_{in} + \gamma w + \delta \tag{5}$$

where w is the programmable weight, I_{in} is the input current and the coefficients α, β, γ, and δ represent the mismatch effects, which will differ from one multiplier to another. Fig. 13 shows the mean error in the output current of 13 multiplier ADM cells (see Fig. 6) due to mismatches, considering 10 different mismatch-dependent case samples. Therefore, each multiplier in the processing architecture, as can be seen in Fig. 13, is affected by mismatches in a different way. Though the mean error is very high for some samples, this does not affect the correct processing of the sensor output, as will be shown in the following.

As for the AF sigmoid circuit, a polynomial approximation fails to fit the nonlinear function properly due to its complexity. For this reason, the high-level circuit operation is modeled by means of a lookup table. Fig. 14 shows the mean error in the

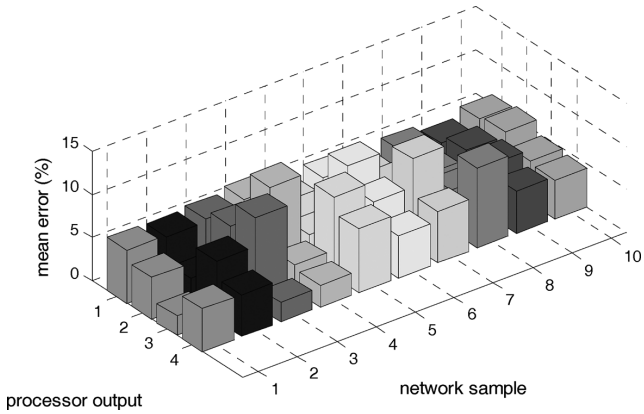

Fig. 14. Mean error for the mismatching-dependent activation functions.

TABLE I
LINEAR GMR SENSOR RANGES

Simulation #	Angle (min)	Angle (max)	Improvement
Basic sensor	251	304	----------
Mismatch Case #1	215	331	119%
Mismatch Case #2	215	331	119%
Mismatch Case #3	216	323	102%
Mismatch Case #4	214	323	106%
Mismatch Case #5	214	329	117%
Mismatch Case #6	214	323	106%
Mismatch Case #7	211	323	111%
Mismatch Case #8	206	324	122%
Mismatch Case #9	214	323	106%
Mismatch Case #10	214	322	104%
Mean Results	**216**	**322**	**100%**

output current of four AF circuits (see Fig. 6) caused by mismatches, also considering ten different mismatch-dependent case samples. Again, as shown in the figure, each AF circuit in the processing architecture is affected by mismatches in a different way.

Finally, these data were used to perform high-level simulations of the whole adaptive conditioning circuit affected by mismatching considering the previously studied practical case of linearizing the output response of a giant magneto-resistive sensor. Table I shows the ranges where the error remains lower than 1° for the raw sensor output and the linearized span achieved for ten different mismatch case simulations for the complete processing circuit. Results show that the sensor compensated span is at least 100% higher than the raw output, even taking into account mismatch effects. Therefore, adaptive circuits based on mixed-mode perceptron processors work properly in sensor preprocessing electronics because of their adaptability and thus their ability to counteract mismatch effects. In summary, the proposed processor is very appropriate for implementing almost-analogue interfaces in integrated sensors due to its compactness, robustness and low bias voltage.

V. CONCLUSION

This paper presents two CMOS current-mode circuit elements designed for adaptive sensor processing in small embedded applications: a mixed analogue-digital multiplier and a sigmoid circuit. By properly combining several of these electronic blocks, it is possible to calibrate the output response

of real sensors. The processing elements can be programmed by changing the digital parameters included in the mixed-mode multipliers. In this way, automation of the calibration process is possible. A proper parameter selection is achieved by using perturbative algorithms. Our study shows that a single-weight perturbation training scheme achieves better results than parallel perturbation training, at a lower electronic complexity.

To evaluate the robustness of the proposed architecture to mismatch, the basic building blocks were modeled on the basis of Monte Carlo simulations. These models were used to study the effects of mismatching on the whole processing system through high-level simulations in Matlab.

The simulation results were applied to linearize the response of a GMR sensor and the insensitivity to parameter mismatch was demonstrated. Circuit programmability allows for compensation of deviations in system performance or temperature drifts [9], with a significant increase in the sensor linearity for a maximum error of 1° in the angular position estimation. Results show the utility of the proposed solution in sensor applications where an accurate and temperature-independent behavior is required, as in automotive applications [22].

Due to the small size (0.25 mm^2 active area), reduced maximum operation power consumption (10.8 mW), negligible quiescent power consumption (less than 105 nW) and digital tunability, the proposed adaptive circuit is very appropriate for automatic calibration of integrated sensors, lending a "smart" nature to the devices.

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