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LETTER TO THE EDITOR

Symbolic analysis of (MO)(I)CCI(II)(III)-based analog circuits

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SUMMARY

New nullor-based models are introduced to describe the behavior of the first generation current conveyor (CCI), second generation current conveyor (CCII), third generation current conveyor (CCIII), their inverting equivalents (ICCI(II)(III)), and/or their multiple output topologies (MO(I)CCI(II)(III)). These nullor equivalents include only grounded resistors to improve the formulation of equations in symbolic nodal analysis. In this manner, it is highlighted the usefulness of the proposed models to calculate analytical expressions in MO(I)CCI(II)(III)-based analog circuits. Copyright © 2009 John Wiley & Sons, Ltd.

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KEY WORDS: current conveyor; nodal analysis; nullor; symbolic analysis; universal filter

1. INTRODUCTION

The nullor is quite useful for the development of analysis, synthesis, and design procedures [1], because it allows us to model the behavior of any active device [2, 3]. For instance, among the plethora of active devices, the current conveyor (CC) is a universal one [3, 4], whose derivations are known as first generation CC (CCI) [5–7], second generation CC (CCII) [8–13], and third generation CC (CCIII) [14, 15]. These three kinds of CCs have been designed to provide tunable characteristics [16, 17], and also they have their inverting topologies [18, 19]. In particular, the positive-type CCII (CCII+) can be evolved to design the current feedback opamp (CFOA) [20]. Furthermore, CCs are suitable to design active filters [21–39], simulated inductances [40–43], gyrators [44], and impedances [45, 46]. Besides, their parasitic effects must be taken into account to improve circuit performances [47]. CFOAs also provide advantages in active filter design [48–50].

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By modeling the behavior of analog circuits using nullors, some circuit transformations can be performed [51–54]. On the other hand, symbolic analysis can be applied to calculate analytical expressions of analog circuits [55–82]. For instance, in [68] it was shown the application of symbolic analysis to CCII-based circuits using nullors by applying graph methods [69]. Furthermore, in this work new nullor-based equivalents are introduced for the CCI(II)(III)s, their inverting equivalents ICCI(II)(III)s, and their multiple output equivalents MO(I)CCI(II)(III)s. All these equivalents consist of nullors with grounded resistances in order to improve the formulation of equations in symbolic nodal analysis (NA) [70–76], because floating resistances require more computational work since they have four entries [68], while grounded ones have only one entry in NA. Henceforth, this paper introduces new (MO)(I)CCI(II)(III)s models to enhance the calculation of analytical expressions.

2. NULLOR-BASED EQUIVALENTS

This section introduces new nullor-based equivalents of the (MO)(I)CCI(II)(III)s and CFOA by including its parasitic resistance at the terminal X (Rx), in order to perform symbolic NA. Although there can be different nullor-based equivalents of CCs, it is desirable to generate models with grounded passive elements because they have only one entry in the NA formulation, while floating ones have four entries. Therefore, in Figure 1 are shown the nullor-based equivalents of: (a) positive-type CCI (CCI+), (b) negative-type CCI (CCI−), (c) inverted CCI+ (ICCI+), (d) inverted CCI− (ICCI−), and (e) multiple-outputs ICCI (MOICCI).

In Figure 2 are shown the nullor-based equivalents of: (a) positive-type CCII (CCII+), (b) negative-type CCII (CCII−), (c) inverted CCII+ (ICCII+), (d) inverted CCII− (ICCII−), and (e) multiple-output CCII (MOCCII).

The CCIII is not a very popular topology in the literature founded until this moment. Besides, in Figure 3 are shown the nullor-based equivalents of: (a) positive-type CCIII (CCIII+), (b) negative-type CCIII (CCIII−), (c) inverted CCIII+ (ICCIII+), (d) inverted CCIII− (ICCIII−), and (e) multiple-outputs ICCIII (MOICCIII).

By cascading the CCII+ with a voltage follower (VF [83]), one gets the nullor-based equivalent of the CFOA, as shown in Figure 4.

3. SYMBOLIC NA

The formulation and solution of the system of equations describing the behavior of an analog circuit are the main computer tasks in symbolic analysis [55–63]. Using nullors, one is able to formulate a system of equations by only applying NA [72–76], because all non-NA compatible elements can be transformed as NA compatible ones [73]. Further, the solution can be performed by applying determinant decision diagrams [64, 65].

In order to verify the usefulness of the proposed nullor-based equivalents, this section shows the symbolic NA applied to CC-based circuits. It is worthy to mention that in [68] one can find only the nullor equivalent of the CCII+; however, that model does not include Rx and generates four entries for each floating (two) resistor. On the other hand, the nullor equivalent proposed herein in Figure 2(a) is quite appropriate for NA because it generates only two entries and includes Rx.

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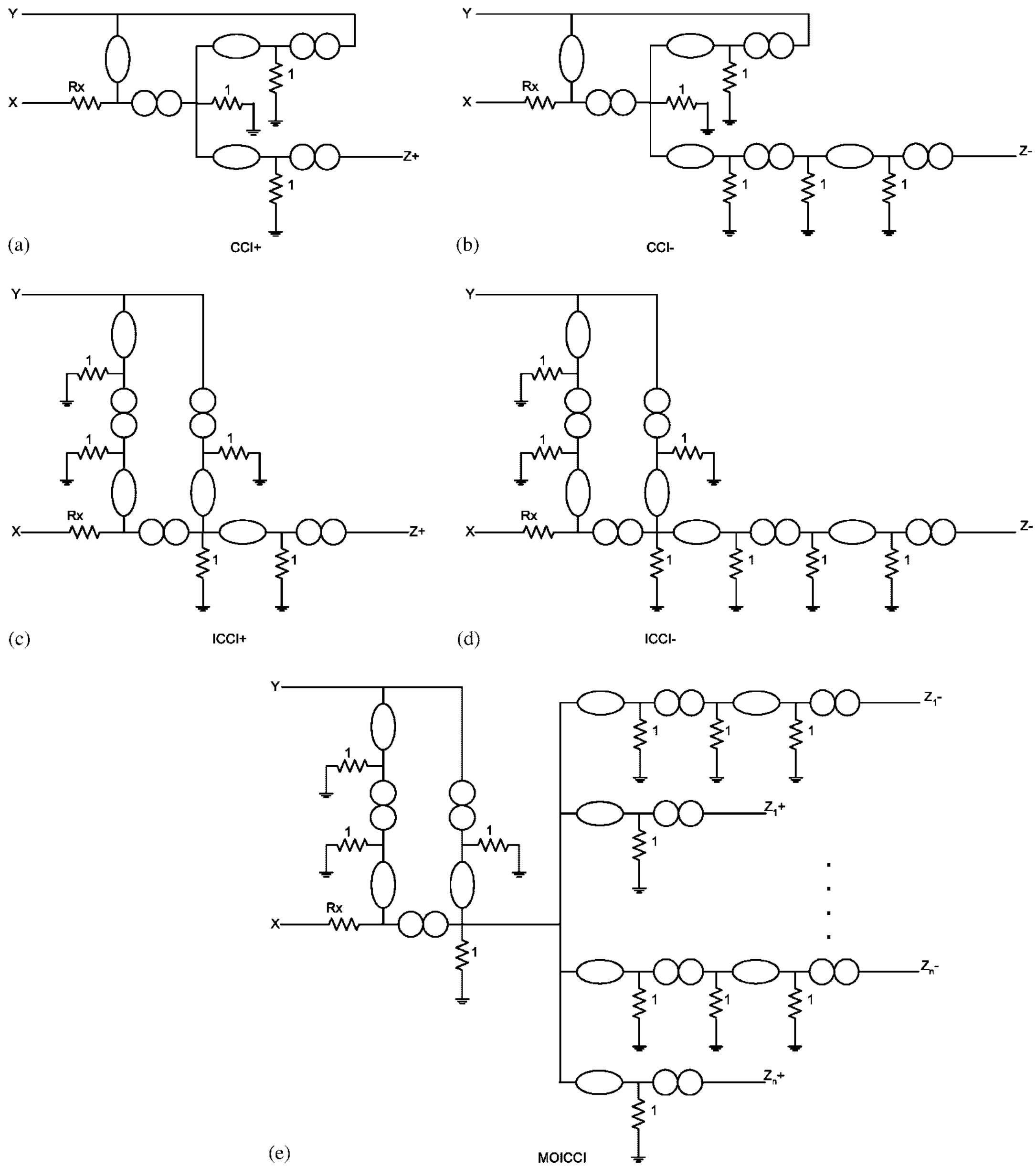

Figure 1. Nullor equivalents: (a) CCI+; (b) CCI−; (c) ICCI+; (d) ICCI−; and (e) MOICCI.

The ($\mathbf{i}=\mathbf{Yv}$) NA-formulation of nullor circuits has been presented in [72–75], and it has been improved in [76] by exploiting the properties of the nullator and norator [84]. Let us consider the dual-output CCII-based current-mode universal filter shown in Figure 5 [85]. Its nullor equivalent

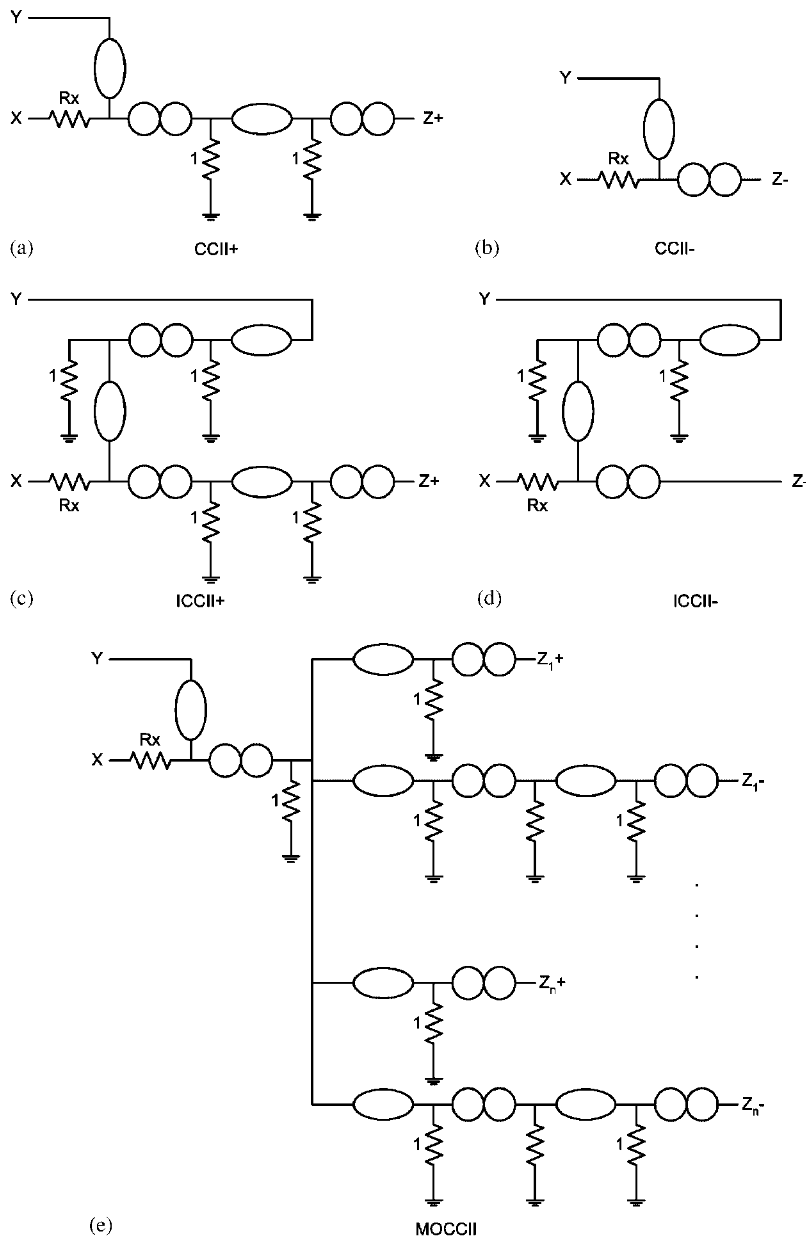

Figure 2. Nullor equivalents: (a) CCII+; (b) CCII−; (c) ICCII+; (d) ICCII−; and (e) MOCCII.

is shown in Figure 6. By applying the symbolic NA-method [76], the formulation is given by Equation (1) and the current relationships are given by Equation (2). By setting: $I_1 = \text{Iin}$ and $I_2 = I_3 = 0$, one obtains a low-pass (LP), with $I_2 = \text{Iin}$ and $I_1 = I_3 = 0$, a band-pass (BP), with

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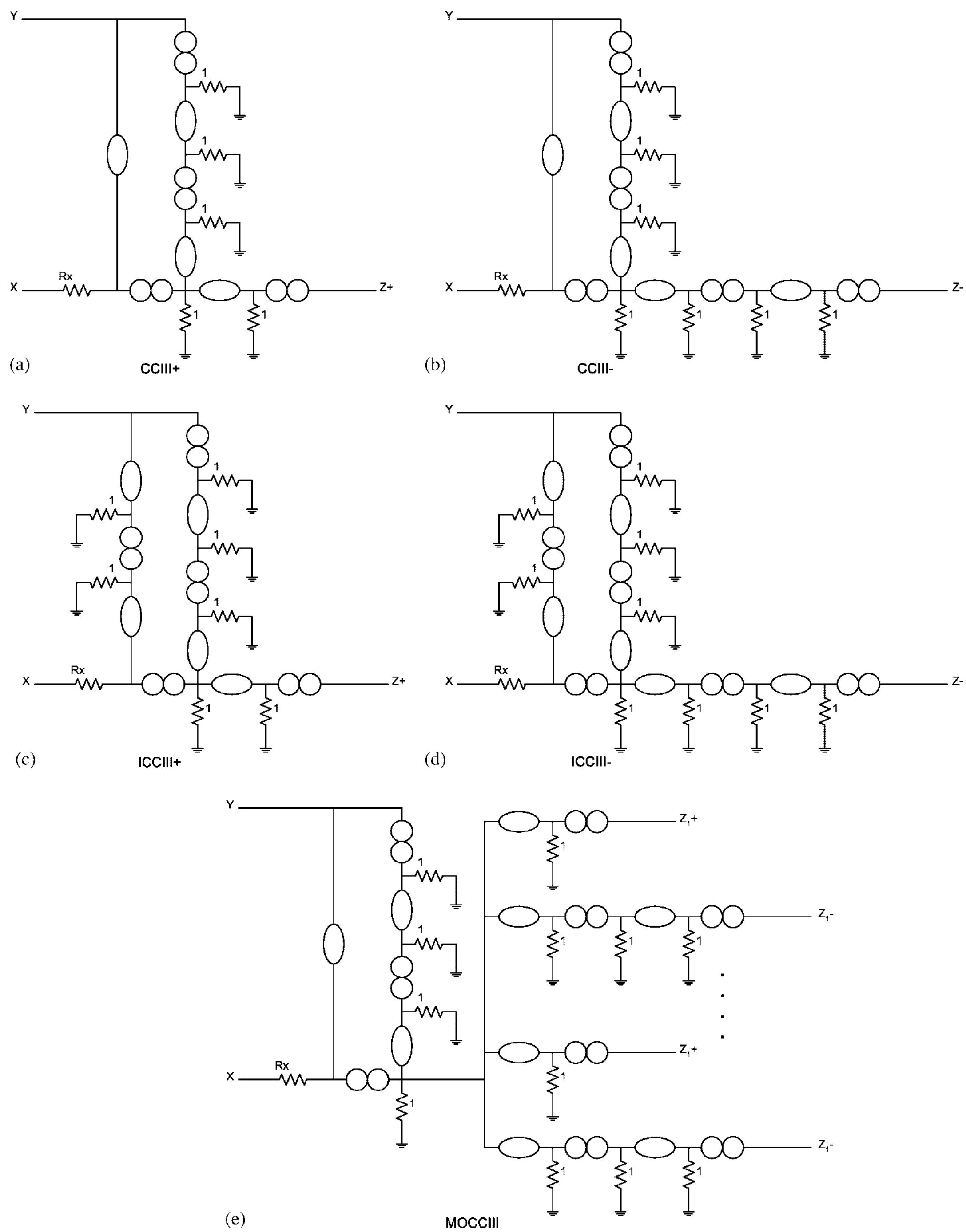

Figure 3. Nullor equivalents: (a) CCIII+; (b) CCIII−; (c) ICCIII+; (d) ICCIII−; and (e) MOICCIII.

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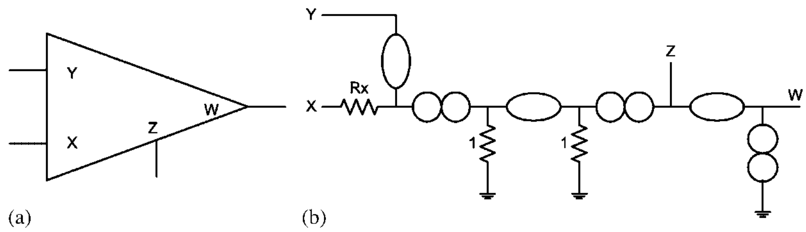

Figure 4. Nullor equivalent of the CFOA.

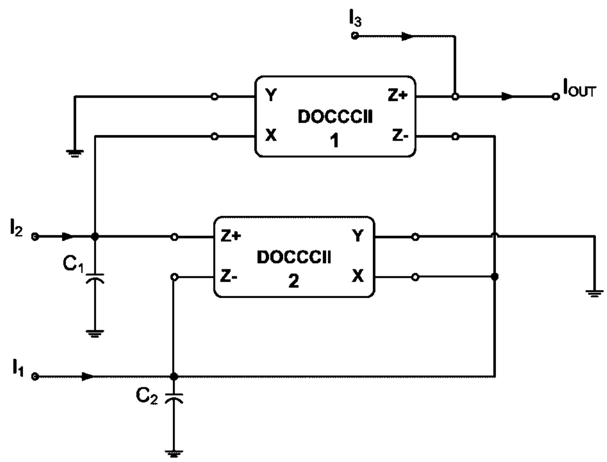

Figure 5. Current-mode DOCCII-based universal filter.

$-I_1 = I_2 = I_3 = \text{Iin}$, a high-pass (HP), and with $I_2 = I_3 = \text{Iin}$ and $I_1 = 0$, a Notch response.

$$\begin{bmatrix} I_1 \\ I_2 \\ 0 \\ I_3 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} sC_2+g_{x2} & 0 & 0 & 1 & 0 & 1 & 0 \\ 0 & sC_1+g_{x1} & 0 & 0 & 1 & 0 & 0 \\ 0 & -g_{x1} & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & g_L \\ 0 & 0 & 1 & 1 & 0 & 0 & 0 \\ -g_{x2} & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_{3,4,5} \\ v_{6,7} \\ v_{8,9,10} \\ v_{11,12} \\ v_o \end{bmatrix} \tag{1}$$

$$I_{\text{out}} = \frac{(s^2 Rx_1 Rx_2 C_1 C_2 + sRx_2 C_2 + 1) I_3 - (sRx_2 C_2) I_2 + I_1}{s^2 Rx_1 Rx_2 C_1 C_2 + sRx_2 C_2 + 1} \tag{2}$$

From Equation (2), the center or cut-off frequency is given by Equation (3), where for a frequency response of 2 MHz: $C_1 = C_2 = 200\,\text{pF}$ and $Rx_1 = Rx_2 = 419.63\,\Omega$. In Figure 7 are shown the LP, BP, HP and Notch responses in dashed line. When more parasitic elements are included, the

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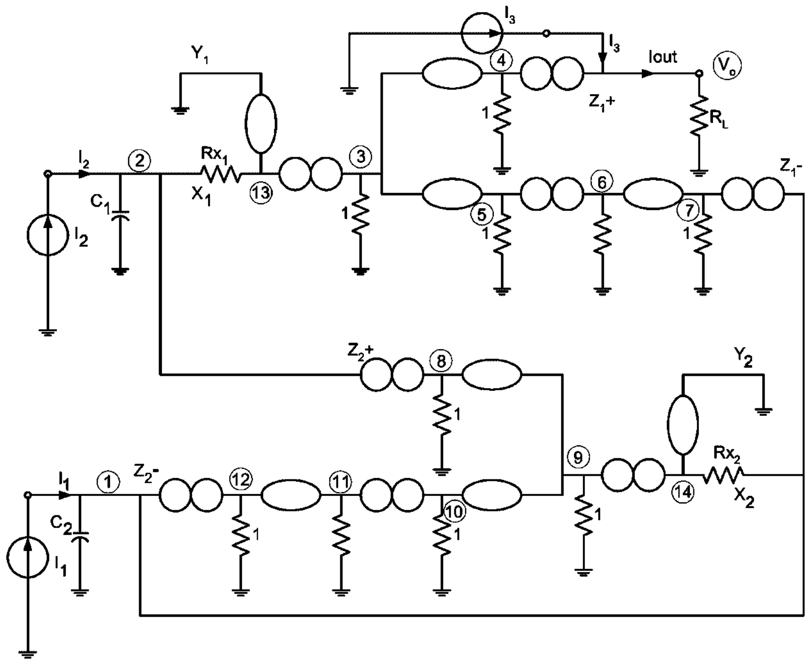

Figure 6. Nullor equivalent of Figure 5.

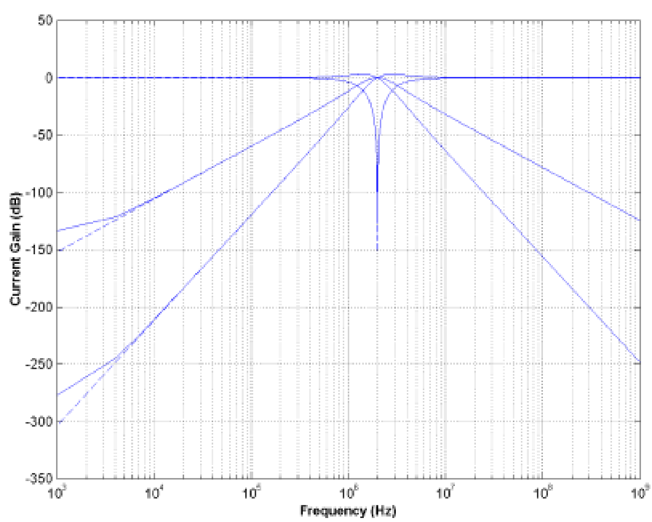

Figure 7. Responses of the filter including Rx (dashed lines), and including Rx, $Rz+$, and $Rz-$ (solid line).

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symbolic expressions grow and the simulation results may be degraded. For instance, by adding $Rz+=704.38\,\mathrm{k}\Omega$ and $Rz-=697.95\,\mathrm{k}\Omega$, the LP, BP, HP, and Notch responses are in solid line in Figure 7.

$$\omega_o = \sqrt{\frac{1}{Rx_1 Rx_2 C_1 C_2}} \tag{3}$$

As shown in [86], parasitic impedances, e.g. Rx, play an important role in filter performances. As a result, the proposed (MO)(I)CCI(II)(III) nullor equivalents are quite useful to compute symbolic expressions by applying NA.

4. CONCLUSIONS

New (MO)(I)CCI(II)(III) models have been introduced consisting of nullors and only grounded resistances. The proposed nullor equivalents allow to an integrated circuit designer to include parasitic elements, and from Section 3 it can be concluded that they are quite suitable to compute analytical expressions of CC-based analog circuits.

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