Analog Integr Circ Sig Process (2012) 71:221–230
DOI 10.1007/s10470-011-9693-7

A design-oriented methodology for accurate modeling of on-chip interconnects

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Received: 22 December 2010 / Revised: 19 February 2011 / Accepted: 7 July 2011 / Published online: 20 July 2011
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Abstract An accurate modeling methodology for typical on-chip interconnects used in the design of high frequency digital, analog, and mixed signal systems is presented. The methodology includes the parameter extraction procedure, the equivalent circuit model selection, and mainly the determination of the minimum number of sections required in the equivalent circuit for accurate representing interconnects of certain lengths within specific frequency ranges while considering the frequency-dependent nature of the associated parameters. The modeling procedure is applied to interconnection lines up to 35 GHz obtaining good simulation-experiment correlations. In order to verify the accuracy of the obtained models in the design of integrated circuits (IC), several ring oscillators using interconnection lines with different lengths are designed and fabricated in Austriamicrosystems 0.35 μm CMOS process. The average error between the experimental and simulated operating frequency of the ring oscillators is reduced up to 2% when the interconnections are represented by the equivalent circuit model obtained by applying the proposed methodology.

Keywords *ABCD* matrix · De-embedding procedure · Interconnection lines · Lumped equivalent circuit · Distributed equivalent circuit · Modeling · *S*-parameters · *VLSI* circuits

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1 Introduction

On-chip interconnections play a key role in determining the performance of high frequency analog, digital, and mixed signal electronic systems, especially with the continuous downscaling of the fabrication technologies, which has pushed the operating frequency of the integrated systems within the gigahertz (GHz) range. Due to this increase in frequency, the global interconnections (e.g. power supply, clock, control signals, etc.) are taking more importance on influencing the operation of current and future electronic systems. Therefore, an accurate modeling (electrical representation) and characterization (parameter extraction) of the interconnection lines used in this type of systems represent an important research area [1].

Due to the continuous down scaling of the technology and increase of operating frequency, the resistance and the inductance associated with the metal lines as well as the conductance and the capacitance associated with the intermetal dielectric (IMD) have taken importance in limiting the performance of on-chip interconnections. Therefore, in current and future high-speed integrated circuit (IC) which exhibit sub-nanosecond switching, it is necessary to consider *RC*, *RLC*, or *RLGC* equivalent circuit models for representing the delay and losses associated with practical high-speed interconnections [1, 2]. In fact, in several works of the state-of-the-art, the interconnection lines are represented by means of a distributed equivalent circuit model including the total resistance, inductance, and capacitance associated with the interconnection line. In these existing interconnect models, the per-unit-length resistance (R_l), inductance (L_l), and capacitance (C_l) associated with an interconnection line are obtained from analytical expressions and technology parameters provided by the foundry [1–3]. However, the values for R_l, L_l, and C_l are assumed

to be constant with frequency, which is fundamentally incorrect within the GHz frequency range.

In order to take into consideration the frequency dependence of the interconnect parameters and the effects that become apparent at high frequencies, the approaches in [4–6] carry out the parameter extraction directly from *S*-parameter measurements. However, this procedure has been rarely used in practical IC circuit designs since many designers assume that within the frequency ranges their ICs work it is feasible to neglect the frequency dependence of the *RLC* parameters. So, one of the contributions of our proposal is encouraging designers to use experimentally implemented interconnect representations even though many authors are still assuming frequency independent for the *RLC* parameters associated with on-chip interconnects [2].

In the design of complex integrated systems, another aspect that must be taken into account by the circuits designer is the trade-off between the accuracy of the equivalent circuit model used to represent an interconnection line and the computation time required to carry out the corresponding simulations. In several works, the interconnection lines have been represented by a distributed equivalent circuit model implemented with *n* sections (e.g. 20 sections as shown in [7]). Obviously, using a large value for *n* allows to accurately represent an interconnection up to higher frequencies than in the case of using a small value for *n*; unfortunately, this also increases the simulation time, which is considerably higher in the design of IC containing thousand of interconnections. Therefore, the determination of the number of sections in which the equivalent circuit model has to be divided for properly representing a line of a given length and operating up to a given frequency is very important; however, the procedure to determine the number of sections is not clearly stated in the previous approaches.

The main contribution of our proposal is the establishment of a methodology that allows circuit designers to perform an accurate representation of the interconnection lines used in high complex analog, digital and mixed signal systems. This methodology (developed from *S*-parameter measurements) includes the parameter extraction procedure, the equivalent circuit model selection, and mainly the determination of the minimum number of sections required in the equivalent circuit for accurate representing interconnects of certain lengths within specific frequency ranges while considering the frequency-dependent nature of the associated parameters. The paper is organized as follows: Sect. 2 presents the on-chip interconnection line structure. Section 3 shows the parameter extraction procedure. The interconnection line modeling is presented in Sect. 4. Section 5 shows the application of the modeling methodology in the design of ICs. Finally, Sect. 6 shows the conclusion of this work.

2 On-chip interconnection line structure

In today's IC design, one of the most used structures is the microstrip line. In general, there are two ways to implement a microstrip line on a silicon IC substrate [8]. In the first one, a microstrip line lies on top of a SiO_2 layer that in turns lies on silicon substrate and the backside metallization acts as the ground plane. In the second case, the microstrip line lies on top of one of the IMD SiO_2 and a metal grid underneath works as the ground or return path plane. This work is focused in the later case, and the lines used for the corresponding analysis are fabricated in Austriamicrosystems 0.35 μm process.

Figure 1 shows a simplified microstrip line implemented in the Metal 4 level that lies on top of the inter-metal dielectric level-4 (IMD4), where *w*, *t* and *l* are the width, thickness, and length of the interconnection, respectively; *h* and *gnd* are the thicknesses of the IMD and the ground plane, respectively. The nomenclature "Metal [*x*] over Metal [*y*], $w = [\ z]$ μm" will refer to a microstrip line implemented in the Metal *x* level, using the Metal *y* level as a ground plane, and a conductor width of *z* μm. Table 1 shows the thickness for different metal and IMD levels available in Austriamicrosystems 0.35 μm process technology.

In order to carry out the parameter extraction associated with an interconnection line, two test structures are designed as shown in Fig. 2. These test structures (which are required for the de-embedding procedure used in this work) consist of a microstrip interconnection line implemented as described in Fig. 1 with a width $w = 2$ μm, and different lengths ($l = 400$ μm and $l = 1{,}000$ μm). The ground plane is constructed with horizontal and vertical crossed lines forming small slots (6 × 12 μm) in the Metal *y* level. Notice that these slots are smaller than the wavelength λ within the analyzed frequency range; thus, this grid is sufficiently small

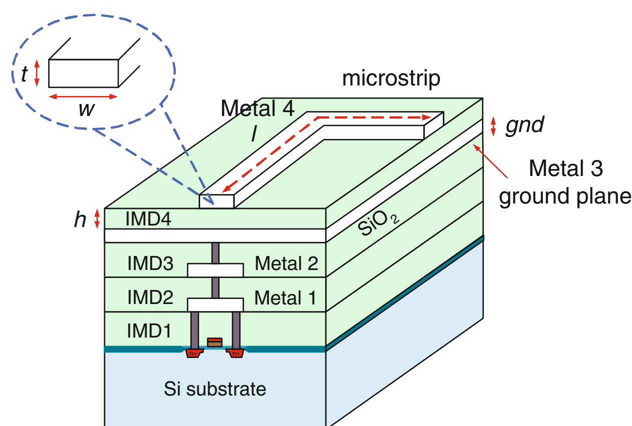

Fig. 1 Simplified structure of a typical on-chip microstrip interconnection

Table 1 Austriamicrosystems 0.35 μm process parameters

Parameter	Thickness (nm)	Parameter	Oxide thickness (nm)
Metal 4	925	IMD4	1000
Metal 3	640	IMD3	1000
Metal 2	640	IMD2	1000
Metal 1	665	IMD1	645

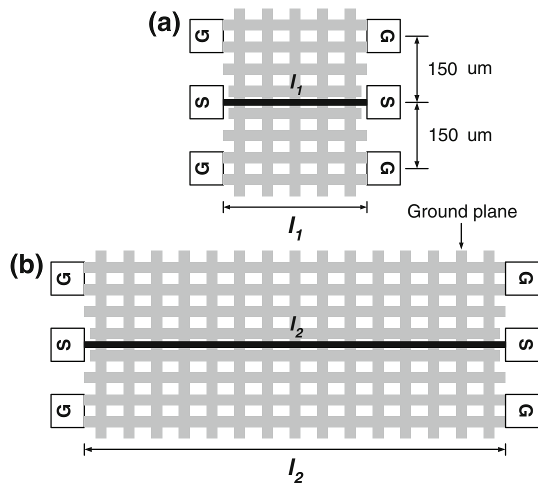

Fig. 2 Microstrip interconnection line structure: **a** *short line* $l = 400$ μm, **b** *long line* $l = 1{,}000$ μm

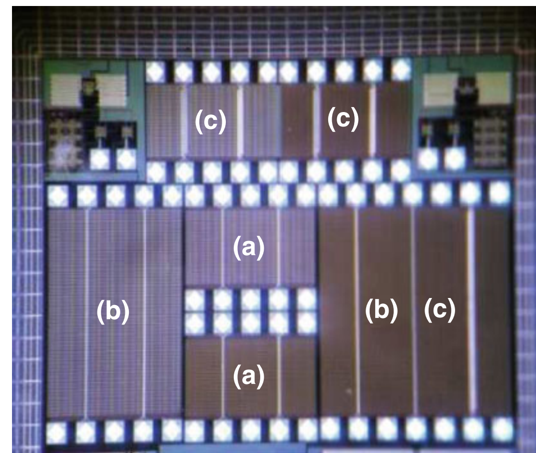

Fig. 3 Photograph of fabricated microstrip lines: *a short line* $l = 400$ μm, *b long line* $l = 1{,}000$ μm, *c* other test structures

to be considered as a solid metal plane for the minimum studied wavelength ($\lambda = 8.5$ mm) [9].

Access to the microstrip lines is provided by 95 × 95 μm^2 signal pads constructed in the Metal 4 level. Beside each signal pad, 95 × 95 μm^2 pads are used to contact the ground plane using ground-signal-ground (GSG) device probes of 150 μm pitch. It is important to mention that the values of the characteristic impedance Z_C and propagation constant γ associated with an interconnection line are directly related to the width and thickness of the metal layer; therefore, the previously described experiments should be repeated for groups of lines with different Z_C and γ (i.e. changing with and thicknesses). Figure 3 shows a photograph of some of the fabricated lines.

3 Interconnection line parameter extraction procedure

In order to perform the extraction of the R_l, L_l, and C_l parameters associated with the interconnection lines described in the previous section, the corresponding *S*-parameters were measured from 0.01 to 35 GHz using an HP8510C vector network analyzer (VNA) with semi-rigid cables and the corresponding GSG coplanar probes described above (device probes). The VNA system was previously calibrated up to the probe tips by using an impedance-standard-substrate (ISS) provided by the probe manufacturer and the line-reflect-match (LRM) procedure.

As previously mentioned, GSG pads are indispensable to access the device under test (DUT). Hence, a de-embedding procedure is required to eliminate the parasitic contribution introduced by the associated pad-to-line discontinuities. Fortunately, for practical purposes the fundamental parameters Z_C and γ (per-unit-length) do not vary from line to line as long as the materials and cross section of the lines is the same, which allows to remove the effect of the pad parasitics using measurements of two lines. From this assumption, Z_C and γ of the fabricated lines are determined applying the de-embedding procedure reported in [9] to two lines with the same characteristics but different lengths (e.g. 400 and 1,000 μm). Figure 4 shows the extracted Z_C and γ for the fabricated interconnection line (Metal 4 over Metal 3, $w = 2$ μm); notice the smooth and physically expected resulting curves when plotting the obtained data versus frequency which is one indicatives of an adequate de-embedding procedure.

After determining Z_C and γ, the values for the R_l, L_l, C_l parameters associated with the interconnection line can be directly obtained from [4, 5]:

$$R_l = Re(\gamma Z_C) \quad (1)$$

$$L_l = \frac{Im(\gamma Z_C)}{2\pi f} \quad (2)$$

$$C_l = \frac{Im(\gamma / Z_C)}{2\pi f} \quad (3)$$

where the following equations are used:

$$\gamma Z_C = R_l + j2\pi f L_l \quad (4)$$

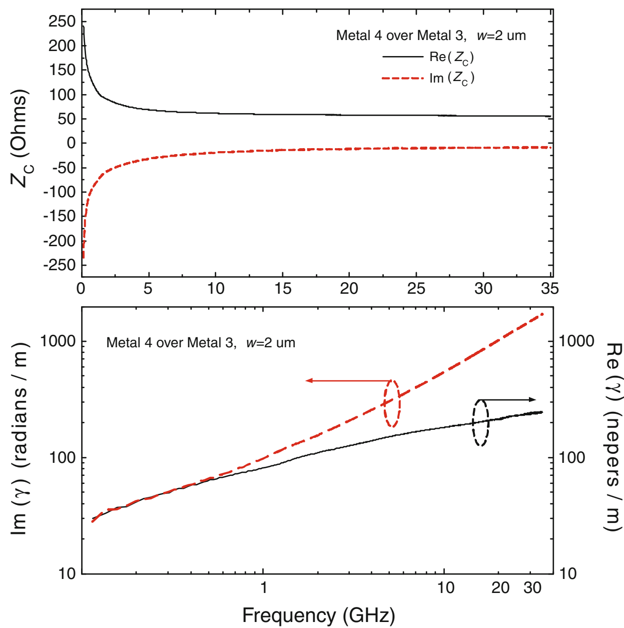

Fig. 4 Experimental characteristic impedance and propagation constant for the fabricated microstrip line Metal 4 over Metal 3, $w = 2$ μm

$$\frac{\gamma}{Z_C} = G_l + j2\pi f C_l \tag{5}$$

Figure 5 shows the obtained values for R_l, L_l, and C_l for the fabricated interconnection line (Metal 4 over Metal 3, $w = 2$ μm) up to 35 GHz. From this figure it is possible to observe the frequency dependence of the R_l, L_l, and C_l parameters obtained from S-parameter measurements. Since the resistance is mainly related to the metal losses, this parameter exhibits an increase with frequency owing to the skin effect [5, 10]. The inductance parameter is also associated with the metal line and the ground plane structure; and the corresponding curve drops with frequency to preserve causality (i.e. the energy stored by the equivalent inductance of the structure decreases when the energy associated with the resistive effect increases). Finally, for the case of the capacitance, the corresponding curve is approximately constant since the permittivity of the dielectric only suffers a relatively small change within the analyzed frequency range.

In Fig. 5, the dotted lines represent the values for R_l, L_l, and C_l obtained by using:

$$R_l = R_0 + \sqrt{f} R_s \tag{6}$$

$$L_l = L_\infty + \frac{R_s}{2\pi\sqrt{f}} \tag{7}$$

$$C_l \approx C_0 \tag{8}$$

where R_0 and R_s are the per-unit-length dc resistance and skin effect resistance, respectively; while, L_∞ is the

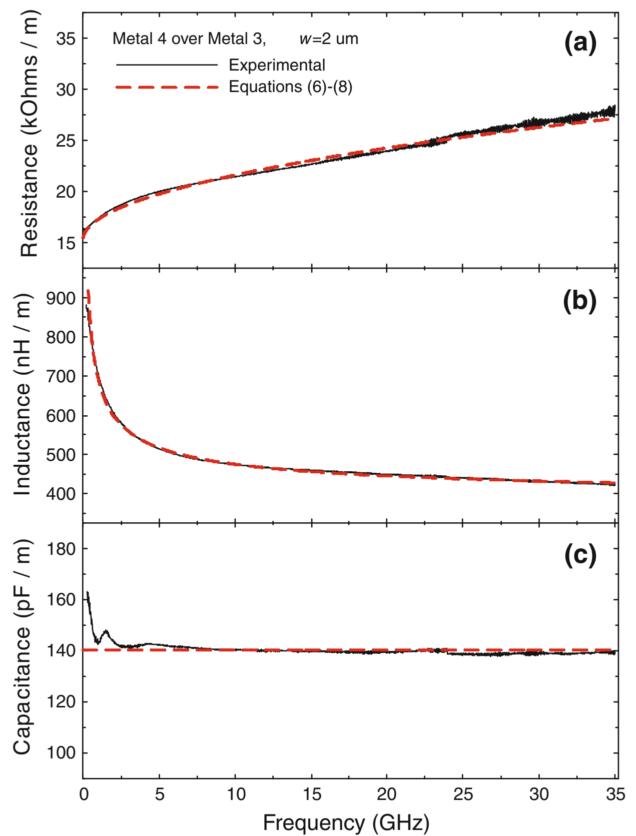

Fig. 5 **a** Resistance, **b** inductance, and **c** capacitance per-unit-length for the fabricated microstrip line Metal 4 over Metal 3, $w = 2$ μm

per-unit-length inductance at high frequencies [11]. For the case of the C_l, the dependence of this parameter with frequency and conductivity is typically quite weak; therefore, the values for C_l can be approximated by the per-unit-length dc capacitance C_0 assuming perfect conductors [12].

Now, the values for R_l, L_l, and C_l obtained from the Eqs. 6–8 can be incorporated into a simulation environment (e.g. eldo, hspice, etc.) to determine the values of total resistance (R_T), total inductance (L_T), and total capacitance (C_T) for an interconnection line of a certain length at a given frequency.

4 Interconnection line modeling

An interconnection line can be modeled using either a lumped or a distributed electrical equivalent circuit which allows to accurately represent the delay and losses associated with the line. As explained later, the selection between a lumped and a distributed model strongly depends on the line length and the operating frequency. For the case of the distributed model, the corresponding implementation is carried out by assuming that the interconnection line can be represented by means of n stages connected in cascaded

configuration. Therefore, the determination of the optimal model and the value for n for accurate representation of interconnection lines of certain lengths within specific frequency range is desirable. This determination is carried out by correlating experimentally determined data with equivalent circuit simulations corresponding to lines of different lengths.

In order to perform the simulation-experiment correlations, the S-parameter data associated with interconnection lines of certain lengths are obtained by applying the Transmission Line Theory [13].

The $ABCD$-parameter matrix associated with a uniform transmission line is given by:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh(\gamma l_i) & Z_C \sinh(\gamma l_i) \\ \frac{1}{Z_C}\sinh(\gamma l_i) & \cosh(\gamma l_i) \end{bmatrix} \quad (9)$$

where the subscript i is used to distinguish between the parameters of lines with different lengths. Thus, once that the experimental Z_C and γ have been determined, the $ABCD$ parameters of a line with arbitrary length l_i can be obtained by using (9) and the corresponding S-parameters are directly obtained using a two-port network parameter conversion [13]. In this work, these obtained S-parameters are assumed to be the experimental data associated with an homogeneous section of line with a given length. Thus, the obtained equivalent circuit models are compared with these data to verify the corresponding accuracy.

As previously stated, on-chip interconnects can be represented by means of *RC*, *LC*, *RLC lumped* or *distributed* equivalent circuits. Therefore, in order to verify the accuracy of the previously mentioned model approaches, several simulation-experiment comparisons are carried out. For the moment, it will be assumed that $n = 6$ sections are sufficient to represent the *distributed* nature of an interconnection line with $l = 1{,}000$ μm within the measured frequency range. Thus, using this value, the validity of the *RC* and *LC* models is verified.

Figure 6 shows the experimental and simulated return and insertion losses ($|S_{11}|$ and $|S_{21}|$, respectively) for an interconnection line with $l = 1{,}000$ μm up to 35 GHz. As can be seen, the *RC distributed* equivalent model is not adequate to simultaneously represent the return and insertion losses beyond a relatively low frequency. Now, for the case of the *LC distributed* model, a considerable deviation of the curves associated with the *LC* model from the experimentally determined data can be observed. Hence, it is obvious that a combination of the *RC* and *LC* models (i.e. an *RLC* equivalent circuit model) is indispensable in order to accurately represent the interconnection lines under study.

Now, the frequency ranges of validity for the *RLC lumped* and *RLC distributed* equivalent circuit models as well as the criteria for the determination of the minimum number sections (required in a *distributed* model) are presented.

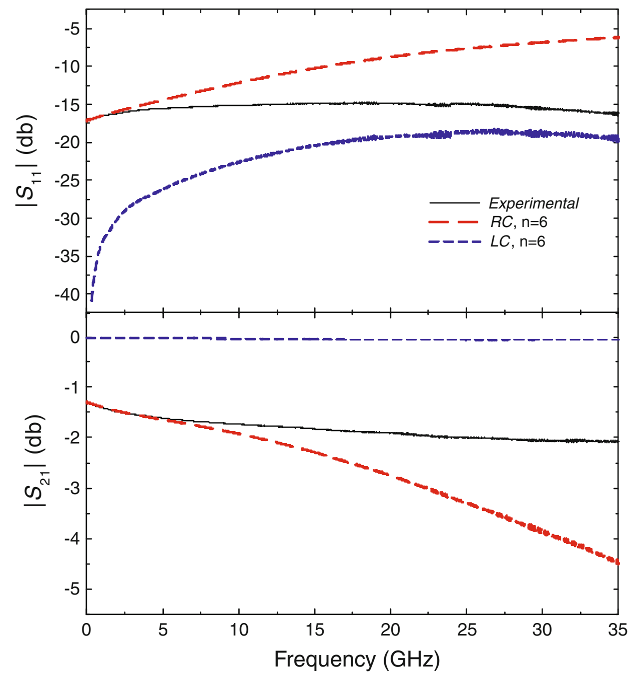

Fig. 6 Experimental return and insertion losses compared with simulated data using *RC* and *LC* distributed equivalent circuit models for the line with $l = 1{,}000$ μm

Figure 7 shows the experimental and simulated insertion losses for an interconnection line with length $l = 1{,}000$ μm. In this figure the corresponding simulated data are obtained using an *RLC lumped* and *RLC distributed* equivalent circuit model implemented with 2, 4, and 6 sections. Notice the large discrepancy between the experimental and the simulated data obtained using an *RLC lumped* equivalent circuit; more precisely, when the interconnection line is modeled by an *RLC lumped* equivalent circuit, the corresponding insertion losses are accurately represented up to about 4 GHz. This frequency limit is determined when the difference between the experimental and simulated $|S_{21}|$ is 1% as shown in the inset of Fig. 7. Now, when the interconnection line is modeled by an *RLC distributed* equivalent circuit implemented with 2, 4, and 6 sections, the corresponding $|S_{21}|$ and $\angle S_{21}$ parameters are accurately represented up to 8, 17, and 30 GHz, respectively by using the previously mentioned criteria. Then, as previously shown, the $|S_{11}|$ and $|S_{21}|$ parameters associated with an interconnection line of a certain length can be accurately represented at higher frequencies using an *RLC distributed* equivalent circuit model implemented with a greater number of sections.

Now, in order to establish the boundary between the *RLC lumped* and the *RLC distributed* model regions, and to verify the accuracy of the *distributed* models using

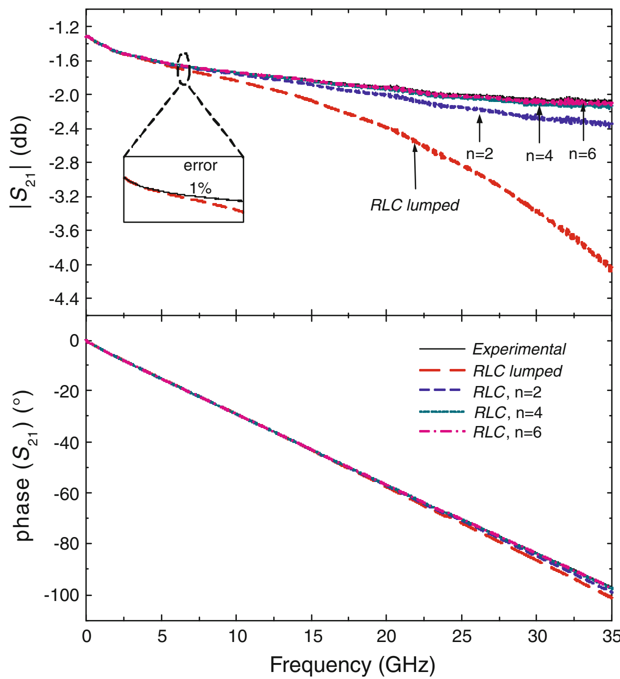

Fig. 7 Experimental insertion loss compared with simulated data using *RLC lumped* and *RLC distributed* (2, 4, and 6 sections) equivalent circuit models for the line with $l = 1{,}000$ μm

different number of sections, a set of interconnection lines with $l = 100$, 200, 400, 1500, 2000, 2500, and 3000 μm are analyzed.

As expected, the corresponding $|S_{21}|$ and $\angle S_{21}$ parameters associated with long interconnection lines are larger than for short and moderately long lines. Hence, in this case the circuit designer must decide if it is feasible to use a long interconnection line, or it is necessary to segment the line and use buffers [14]. In an homogeneous interconnection line, the length (l) for which the line can be considered as short enough to be represented by means of a simple *lumped* equivalent circuit model is inversely proportional to the phase constant β. To write this relation as an equation, a proportionality constant (Δ) has to be included, which yields: $l = \Delta/\beta$. To express this equation in a more intuitive way, β is written in terms of the L_lC_l elements and the frequency ($\beta = 2\pi f\sqrt{L_lC_l}$), which yields [15]:

$$l = \frac{\Delta}{2\pi f\sqrt{L_lC_l}} \tag{10}$$

where Δ is an arbitrary constant (dependent on the acceptable error for the S-parameters) typically set to 0.25.

Indeed, based on the results obtained by applying the simulation-experiment procedure described in this section to a set of interconnection lines with different lengths, it has been shown that the boundaries of the *RLC distributed* equivalent circuit model regions are proportional to the number of sections n and the value of Δ. This is logical since the bigger n is the longer the line that can be represented by an n-stage model at a given frequency; mathematically this is expressed as:

$$l = \frac{n\Delta}{2\pi f\sqrt{L_lC_l}} \tag{11}$$

Figure 8 shows the combination of l and f for which the studied interconnection lines can be represented by an *RLC lumped* model and when can be represented by an *RLC distributed* equivalent circuit model implemented with $n = 2$, 4, 6, 8, 10, and 12 sections. In this figure, the experimental data are obtained using the simulation procedure and error criterion previously established, whereas the theoretical curves are obtained using equation (11). Notice that this equation allows predicting the maximum length of a line which can be accurately represented by an *RLC lumped* equivalent circuit model (i.e. $n = 1$) at a given frequency. However, when n increases by sectionalizing the *RLC* model, this length also increases as it has been previously discussed. This fact is reflected in Eq. 11, which predicts that by sectionalizing the model in n stages the length of the line that can be accurately represented increases by a factor of n with respect to the corresponding *lumped* model at a given frequency.

The information shown in Fig. 8 can be interpreted by the circuit designers as follows. As an example, consider an interconnection line with $l = 1{,}000$ μm; this line can be modeled by an *RLC lumped* equivalent circuit only up to about 4.4 GHz as can be seen in Fig. 8. Now, if the same interconnection is modeled by an *RLC distributed* equivalent circuit implemented with 2 sections, the delay and losses associated with the line can be accurately represented up to 9.3 GHz. Finally, when the same *RLC distributed* equivalent circuit is implemented with 4 sections, the interconnection line under study can be adequately represented up to 20.1 GHz.

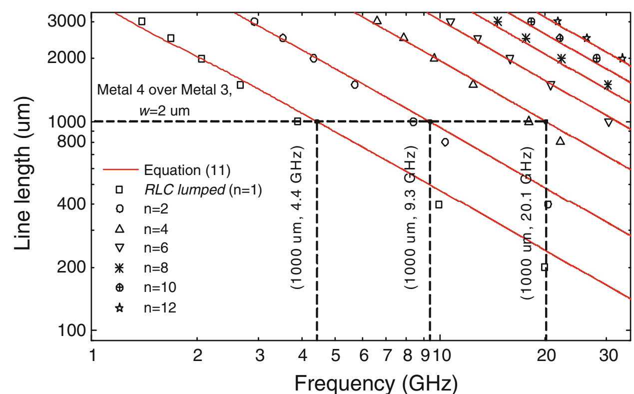

Fig. 8 *RLC lumped* and *RLC distributed* equivalent circuit model regions using 2, 4, 6, 8, 10 and 12 sections for interconnection lines Metal 4 over Metal 3, $w = 2$ μm

Now, the simulation-experiment procedure (previously described) is applied to an interconnection line implemented in the Metal 4 level using the Metal 1 as a ground plane (Metal 4 over Metal 1, $w = 2$ μm). Thus, according to the information shown in Fig. 9, an interconnection line with $l = 1{,}000$ μm can be represented by an *RLC lumped* equivalent circuit up to about 5.5 GHz. Now, when the interconnection line under study is modeled by an *RLC distributed* equivalent circuit implemented with 2 sections, the line can be adequately represented up to 10.3 GHz. Finally, if the same *RLC distributed* equivalent circuit is implemented with 4 sections, the delay and losses associated with the interconnection line can be accurately represented up to 21.2 GHz.

Notice the good correlation between the experimental data and the theoretical curves obtained using the proposed equation; hence, a plot of this type provides important information to analytically determine the minimum number of sections required in an equivalent circuit model for accurate representation of interconnections given the maximum operating frequency. In consequence, the equivalent circuit model used to represent the interconnection lines in the simulations of complex systems can be simplified saving computation time.

5 Design case study

Nowadays, the design of microprocessors that perform many functions at high speed and consuming low power is very important for the implementation of multimedia equipment (e.g. computers, cell phones, video games, video cameras, audio players, etc.). In a high performance microprocessor, a large number of functions are carried out in a synchronous digital way; therefore, the incorporation of a synchronization system responsible for generating and distributing the clock signal (to all points where the signal is required in the microprocessor) is indispensable.

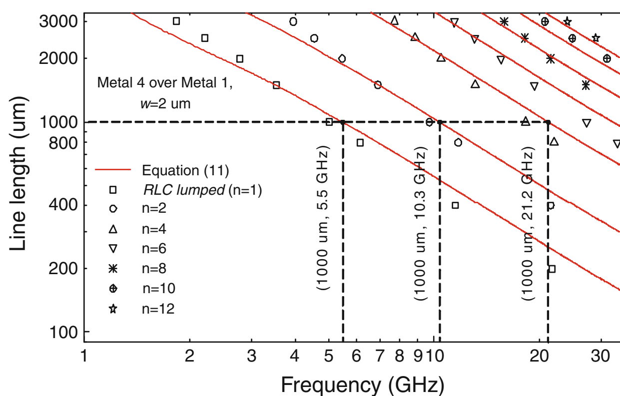

Fig. 9 *RLC lumped* and *RLC distributed* equivalent circuit model regions using 2, 4, 6, 8, 10 and 12 sections for interconnection lines Metal 4 over Metal 1, $w = 2$ μm

In current microprocessors, the clock signal is generated at a single point and distributed throughout the IC using a global synchronization system. However, due to the continuous down scaling of the technology, the increase in area of the ICs and operating frequency, and the physical limitations of the interconnection materials; the use of global systems is declining. Therefore, the local synchronization systems implemented by interconnecting and coupling oscillators (resonant and no-resonant) represent an attractive alternative to solve the problems associated with global systems [16–18]. In the design of either global or local synchronization systems, the interconnection lines play a key role in the generation and distribution of the clock signal; hence, the modeling and characterization of interconnection lines used in the implementation of these systems are very important.

In order to show the applicability of the proposed interconnection line modeling methodology in the design of synchronization blocks, the design and fabrication of several ring oscillators using interconnection lines with $w = 2$ μm and $l = 70$, 1000, 1500, 2000, and 3000 μm. (lengths typically used in this systems) are carried out. The oscillators are designed and fabricated using an Austriamicrosystems 0.35 μm process, a power supply of 3.3 V, and the Metal 4 level for the interconnection lines.

An oscillator is a feedback circuit which generates by itself (i.e. without excitation) a periodic signal at frequency *f*. A ring oscillator is a feedback circuit implemented by *N* gain stages in a close loop which generates a periodic signal if and only if the oscillation criteria (Barkhausen criteria) are satisfied [19]. The operating frequency in a ring oscillator is given by:

$$f = \frac{1}{2Nt_d} \tag{12}$$

where N and t_d are the number and delay of the gain stages, respectively.

Figure 10 shows the schematic and a photograph of a ring oscillator implemented by three gain stages which are connected using long interconnection lines (length in the order on millimeters). Now, the operating frequency of this oscillator is given by:

$$f = \frac{1}{2Nt_d + 2Nt_l} \tag{13}$$

where t_l is the delay associated with the interconnection line. The operating frequency of the ring oscillator is directly related to the delay associated with the gain stages and the interconnection lines. This feature of the ring oscillators allows to verify the accuracy of the equivalent circuit models obtained using the proposed interconnection line modeling methodology.

As can be observed in Fig. 10, meander interconnection lines are used in the implementation of the ring oscillators. In [20], an analysis of the impact of the bends in the interconnection lines is presented. The experimental results obtained in [20] show a variation of 0.03 db between the *S*-parameters associated with interconnection lines ($l = 300$ μm) with 45° and 90° bends at 20 GHz. Based on these results, it is evident that there is an impact of the bends in the *S*-parameters of very short lines. However, interconnection lines with lengths in the order of millimeters are used in the design application presented in this section. The magnitude of the S_{11} and S_{12} parameters associated with these interconnections is considerably much larger than the magnitude of the variation generated by the bends; for this reason, the impact of the bends is not significant in the performance of the meander interconnects used in the implementation of the ring oscillators.

The operating frequency is obtained through simulations and measurements of the implemented ring oscillators. For the case of the simulations, the interconnection lines used in the implementation of the oscillator are replaced by the obtained equivalent circuit models; then, the corresponding simulations are performed in the Mentor Graphics environment. The on-chip measurements were performed using an Advantest R3265A series spectrum analyzer (SA) with a semi-rigid cable and the corresponding on-chip one point probes. Figures 11 and 12 show the simulated transient response and the measured output spectrum for a three-stage ring oscillator using long interconnection lines, respectively.

Figure 13 shows the experimental and simulated operating frequency for the implemented three-stage ring oscillators varying the length of the interconnection lines. In this figure, the corresponding simulated data are obtained considering the parasitic effects associated with the gain stages while the interconnection lines are represented by the equivalent circuit models obtained by applying the proposed methodology. The Post Layout (*P. Layout*) simulations also consider the parasitic effects associated with the gain stages; in this case, however, the interconnection lines are represented by the equivalent circuit model provided by the parameter extraction tool from Mentor Graphics software. Whereas that, the *Experimental* data denotes the measurement results which are used as a reference to carry out the corresponding comparison with the simulated data. The deviation of the simulated from the experimental data allows to determine which one of the models is the most accurate and appropriate to represent an interconnection line. Thus, the error parameter can be defined as $\frac{(\text{Simulation} - \text{experimental})*100}{\text{experimental}}$.

From Fig. 13, notice the large discrepancy between the *Experimental* and the *P. Layout* simulation data; more precisely, when the interconnection lines are represented by the equivalent circuit model provided by the parameter extraction software, the average error is 20%. It is important to note that the accuracy between the *Experimental* and the *P. Layout* simulation data only depends on the equivalent circuit model generated by the extraction tool; this tool automatically generates a distributed equivalent circuit which only takes into account the resistance associated with the metal lines and the capacitance associated with the IMD. In fact, the parameter extraction tool uses data provided by the chip manufacturer which commonly provide nominal values for the material properties obtained at fixed frequencies (in some cases even at dc). As can be observed in Fig. 13, the *P. Layout* simulated operating frequency of the ring oscillators is lower than the

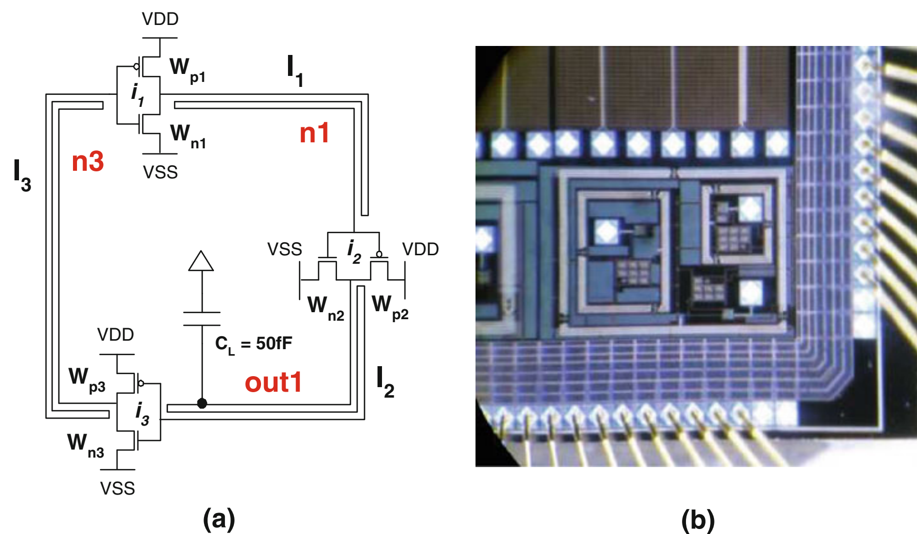

Fig. 10 Three-stage ring oscillator: **a** schematic, **b** photograph

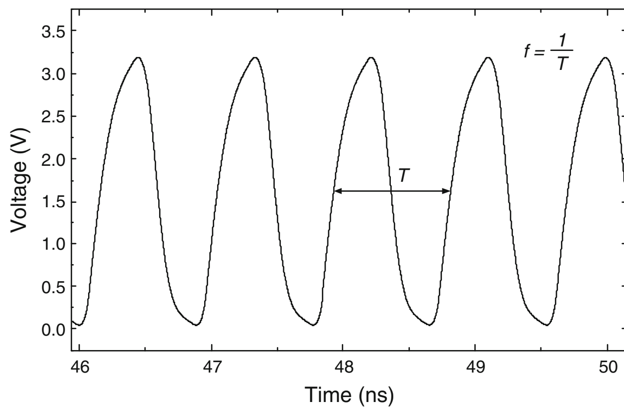

Fig. 11 Simulated transient response for a three-stage ring oscillator using long interconnection lines

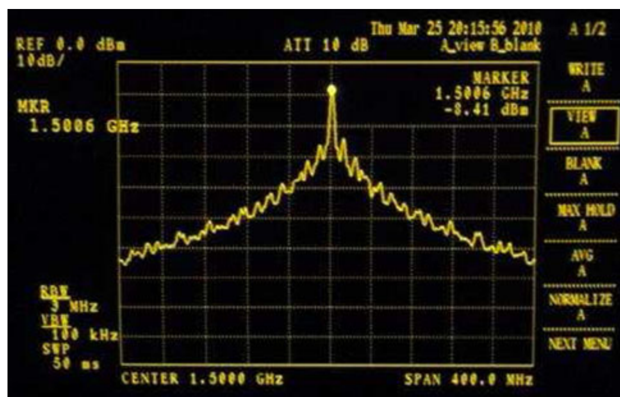

Fig. 12 Measured output spectrum for a three-stage ring oscillator using long interconnection lines

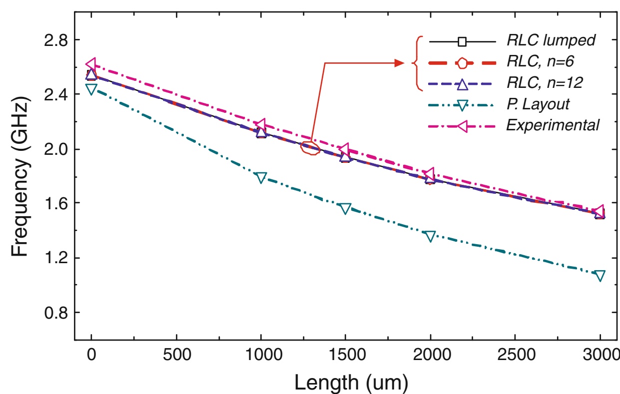

Fig. 13 Experimental operating frequency for three-stage ring oscillators compared with simulated data using *RLC lumped* and *RLC distributed* ($n = 6$ and 12 sections) equivalent circuit models

Experimental data; this is mainly because the equivalent circuit model provided by the extraction tool used in the post layout simulations is overestimating the delay associated with the interconnection lines.

Now, observe the good correlation between the experimental and the simulated data obtained using the *RLC lumped* and *RLC distributed* equivalent circuits implemented with 6 and 12 sections; thus, when the interconnection lines are represented by these equivalent circuits, the average error is 2%. It is important to mention that in these simulations the information associated with an interconnection line fabricated in the Metal 4 level using the Metal 1 as a ground plane is used; this is because in the design of ICs, the power and ground lines located in the lowest metal levels provide a virtual reference plane for the interconnection lines [9].

Notice that the simulated data obtained using the *RLC lumped* and *RLC distributed* equivalent circuits implemented with 6 and 12 sections show the same average error. In order to explain these results, consider the experimental operating frequency for the implemented three-stage ring oscillator using interconnection lines with $l = 1{,}000\ \mu m$ which is =2.2 GHz. According to the results obtained in Sect. 4 (specifically the information shown in Fig. 9), at this operating frequency, an interconnection line with $l = 1{,}000\ \mu m$ can be accurately represented by an *RLC lumped* equivalent circuit; for this reason, when the interconnection line is represented by an *RLC distributed* equivalent circuit implemented with a greater number of sections, the error percentage remains constant. Obviously, the use of an equivalent circuit implemented with a minimum number of sections reduces the computation time required to perform the corresponding simulations which is considerable high, especially in the design of systems with a large number of interconnects.

6 Conclusion

An accurate modeling methodology for typical on-chip interconnects used in the design of high frequency analog, digital, and mixed signal systems has been presented. This methodology developed from experimental data allows circuit designers to perform the parameter extraction, the equivalent circuit model selection, and analytical determination of the minimum number of sections required in the electrical equivalent circuit for accurate representing interconnects of certain lengths within specific frequency ranges.

It was demonstrated that an accurate representation of the interconnection lines used in the design and implementation of an IC is carried out by applying the proposed modeling methodology.

This methodology can be used by circuit designers to perform accurate representations of any type of interconnections used in current and future IC applications fabricated in different technologies.

References

1. Ismail, Y. I., Friedman, E. G., & Neves, J. L. (2000). Equivalent Elmore delay for RLC trees. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 19*(1), 83–97.
2. Chen, T. C., Pan, S. R., & Chang, Y. W. (2004). Timing modelling and optimization under the transmission line model. *IEEE Transactions on Very Large Scale Integration* (*VLSI*) *Systems, 12*(1), 28–41.
3. Salim-Maza, M., Aguirre-Hernandez, M., & Linares-Aranda, M. (2005). Fused timing analytical model for repeater insertion and optimization. In *Proceedings of the 48th Midwest symposium on circuits and systems, 2005*, Vol. 1, pp. 720–723.
4. Eo, Y., & Eisenstadt, W. R. (1993). High-speed VLSI interconnect modeling based on S-parameter measurements. *IEEE Transactions on Components*, *Hybrids*, *and Manufacturing Technology, 16*(5), 555–562.
5. Eisenstadt, W. R., & Eo, Y. (1992). S-parameter-based IC interconnect transmission line characterization. *IEEE Transactions on Components, Hybrids, and Manufacturing Technology, 15*(4), 483–490.
6. Hegazy, H. M. (2005). RLC parasitic extraction and circuit model optimization for Cu/SiO_2-90 nm inductance structures. In *Proceedings of the European gallium arsenide and other semiconductor application symposium, EGAAS 2005*, Vol. 1, pp. 685–688.
7. Goren, D., Zelikson, M., Galambos, T. C., Gordin, et al. (2002). An interconnect-aware methodology for analog and mixed signal design, based on high bandwidth (over 40 GHz) on-chip transmission line approach. In *Proceedings of the design, automation and test in Europe conference and exhibition, 2002*, Vol. 1, pp. 804–811.
8. Rehman, A. (2007). Microstrip design in a silicon technology using closed form analytical expressions. *High Frequency Electronics, 6*(4), 18–28.
9. Mangan, A. M., Voinigescu, S. P., Ming-Ta, Y., & Tazlauanu M. (2006). De-embedding transmission line measurements for accurate modeling of IC designs. *IEEE Transactions on Electron Devices, 53*(2), 235–241.
10. Barger, A., Goren, D., & Kolodny, A. (2004). Design and modelling of network on chip interconnects using transmission lines. In *Proceedings of the 2004 11th IEEE international conference on electronics, circuits and systems, ICECS 2004*, Vol. 1, pp. 403–406.
11. Zhang, J., et al. (2010). Causal RLGC(f) models for transmission lines from measured S-parameters. *IEEE Transactions on Electromagnetic Compatibility, 52*(1), 189–198.
12. Marks, R. B., & Williams, D. F. (1991). Characteristic impedance determination using propagation constant measurement. *IEEE Microwave and Guided Wave Letters, 1*6, 141–143.
13. Pozar, D. M. (1998). *Microwave engineering*. New York, NY: Wiley.
14. Nalamalpu, A., & Burleson, W. (2000). Repeater insertion in deep sub-micron CMOS: Ramp-based analytical model and placement sensitivity analysis. In *Proceedings of the 2000 IEEE international symposium on circuits and systems, ISCAS 2000*, Geneva, Vol. 3, pp. 766–769.
15. Johnson, H., & Graham, M. (2003). *High-speed signal propagation*: *Advanced black magic*. Upper Saddle River, NJ: Prentice Hall.
16. Wood, J., et al. (2001). Rotary traveling-wave oscillator arrays: A new clock technology. *IEEE Journal of Solid-State Circuits, 36*(11), 1654–1664.
17. O'Mahony, F., et al. (2003). A 10-GHz global clock distribution using coupled standing-wave oscillators. *IEEE J. Solid-State Circuits, 38*(11), 1813–1820.
18. Salim-Maza, M. (2005). Generación y Distribución de Señal de Reloj para Sistemas en Chip utilizando Anillos Interconectados Acoplados. Ph.D. dissertation, Instituto Nacional de Astrofísica, Óptica, y Electrónica (INAOE), Puebla, México, June 2005.
19. Razavi, B. (2001). *Design of analog CMOS integrated circuits*. New York, NY: McGraw-Hill.
20. Shi, X., et al. (2005). RF equivalent-circuit model of interconnect bends based on S-parameter measurements. *Microwave and Optical Technology Letters, 45*(2), 170–173.

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