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Low-voltage differential voltage follower for WTA and fully differential applications

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Abstract: A low-voltage differential version of a high performance voltage follower is presented. The proposed circuit is very compact, and symmetric with respect to the input devices. Both differential input devices are enhanced by local shunt feedback, increasing the gain and, thus, reducing the output resistance for higher precision. The circuit has proved useful as a winner-take-all (WTA) circuit. It also features operation as a fully differential amplifier with low supply voltage requirements close to a transistor's threshold voltage. Experimental results verifying the operation of the proposed structure are provided.

Keywords: analog CMOS integrated circuits, winner-take-all (WTA) analog circuits

Classification: Integrated circuits

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1 Introduction

Winner-take-all (WTA) circuits have become fundamental in many systems that require minimum (MIN) and maximum (MAX) operations. Some applications of these types of operation include non linear analog systems such as data acquisition, function synthesis and precision rectifiers. In this type of circuits a given set of inputs are available, in which the input with the highest or lowest level, depending on the operation being performed, defines the output signal.

2 Conventional WTA

Fig. 1 a shows a basic current-mode WTA consisting of two inputs [1]. Consider the initial condition where $I_1 = I_2$, if transistors M1a and M2a are identical their gate-source voltages are also the same, thus $V_1 = V_2$. Under these conditions the current in both transistors is I_c, and M1c and M2c have the current $I_1 = I_2$. Therefore, the output exhibits a voltage $V_c = V_{GSM1c,2c}$. Now consider the case where I_1 increases, this causes the gate-source voltage of M1c to increase. Due to the fact that the gate terminals of M1c and M2c are connected, V_{GSM2c} also increases; although the current I_2 is not increasing; hence the drain-source voltage of M2c tends to decreases to compensate this effect, forcing the operation into triode. Consequently, the output voltage adopts the gate-source voltage of the input transistor with the larger input current, corresponding to the expression:

$$V_c = \sqrt{\frac{I_i^{\max}}{K(W/L)}} - V_T \tag{1}$$

Where $K = (\mu C_{ox})/2$, W/L represents the dimensions of the transistor and V_T is the threshold voltage. Note that the minimum supply requirement is that of two gate-source voltages and a drain-source saturation voltage.

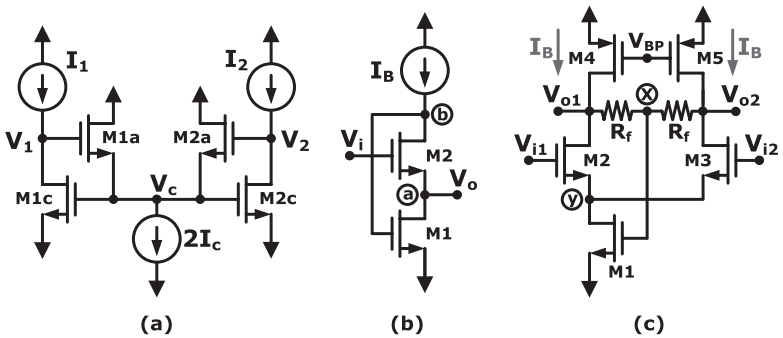

Fig. 1. a) Conventional WTA [1], b) Flipped voltage follower (FVF) [2], and c) proposed symmetrical differential FVF (SDFVF).

3 Symmetric differential voltage follower as WTA

As mentioned previously, the WTA follows the input signal with the dominant voltage level, thus the proposed circuit is based on a high performance

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voltage follower denominated Flipped Voltage Follower (FVF) [2], and shown in Fig. 1 b. Note that transistor M2 has a constant biasing current I_B, which produces a constant voltage V_{GS2}, reflecting variations in V_i at node a level shifted by V_{GS2}. Additionally, M1 can sink large currents, offering a very low impedance at this node of approximately $1/(g_{m1}g_{m2}r_{o2})$.

The proposed circuit is shown in Fig. 1 c. It consists of two FVF's, where M1 offers shunt feedback for both M2 and M3. The resistors R_f avoid the necessity of connecting the gate of M1 directly to the drain of the differential transistors as in the FVF. This permits the architecture to have different voltage levels at the drain of M2 and M3, which also results in moderate gain as explained later. M1 behaves as a current sensing transistor for both M2 and M3, offering a symmetric current-sinking capability to both of the input transistors. Thus, it is denominated the "Symmetric Differential FVF" or SDFVF. The SDFVF presents an enhanced output resistance of $1/(2g_{m1}g_{m2,3}r_{o2,3})$. When large differential signals are present, node y reflects the voltage variations of the minimum of the input voltages, with a constant dc level shift of V_{GS} of the corresponding input transistor. Under this condition, the other input transistor obtains a gate-source voltage larger than the required to operate with a current I_B, forcing it to go into triode region with a small V_{DS}. At this point, this transistor presents a resistance of R_{triode}, whereas the other transistor combined with M1 present a much lower resistance as described for the FVF, thus, controlling the voltage at node y.

In addition, this structure also offers moderate gain at the output voltages V_{o1} and V_{o2} when small signals are present at the inputs, and both M2 and M3 operate in saturation, the output voltages V_{o1} and V_{o2} present moderate gain, operating as a fully differential amplifier. In such case, common-mode output voltages are mounted on a DC level of value $V_{GSM1} - V_{ss}$. Under these conditions no current flows across the resistors R_f, thus M1 operates as a diode connected transistor adjusting V_{GSM1} to sink the current provided by M4 and M5. The small-signal gain is defined by $g_{m1,2}(r_{o4,5}||r_{o2,3}||R_f)$, and node x behaves as a signal ground, maintaining the voltage V_{GSM1} required to have $2I_B$. For small signal applications this circuit operates similar to the conventional fully differential (FD) amplifier reported in [3] with reduced supply voltage. The conventional FD in [3] requires a gate-source voltage and two drain-source voltages, whereas the proposed requires a gate-source voltage and one drain-source saturation voltage.

4 Experimental results

To validate the proposed structure, the conventional and proposed structures were assembled on a breadboard using commercial transistor arrays ALD06 and ALD07 (NMOS and PMOS). Their parameters are: for $\beta = \mu C_{ox}(W/L)$; $\beta_{NMOS} = 480\,\mu A/V^2$, $\beta_{PMOS} = 220\,\mu A/V^2$, $\lambda_{NMOS,PMOS} = 0.05\,V^{-1}$, $|V_{T(NMOS,PMOS)}| = 0.7\,V$, $\gamma = 0.3\,\sqrt{V}$. The circuits were tested with a biasing current $I_B = 50\,\mu A$, resistances $R_f = 100\,k\Omega$ and a load capac-

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itance of 140 pF on each of the differential outputs. Fig. 2 shows the WTA operation of the circuits in Fig. 1 a and 1 c, where the conventional WTA has a supply voltage of $V_{dd} - V_{ss} = 3.5\,V$ and the proposed SDFVF has $V_{dd} - V_{ss} = 2.5\,V$. Two different input signals were used for the SDFVF, a sine waveform $V_{i1} = 1\,V_{pp}$ at 10 kHz and $V_{i2} = 1\,V_{pp}$ at 100 kHz. These signals were also used to generate linear currents I_1 and I_2 for the conventional WTA using independent PMOS FVF's with sensing resistors of 5 kΩ. Observe that the output voltage V_y in the SDFVF follows accurately the minimum of the input signals whereas voltage V_c in the conventional WTA presents a distortion due to the quadratic terms of the current-voltage relation of transistors M1c and M2c. Fig. 3 shows the transient response of the circuits in Fig. 1 c and the conventional FD in [3] using a supply voltage of $V_{dd} - V_{ss} = 3\,V$. The circuits were tested in a conventional inverting configuration with feedback and input resistors of 100 kΩ. An input signal of

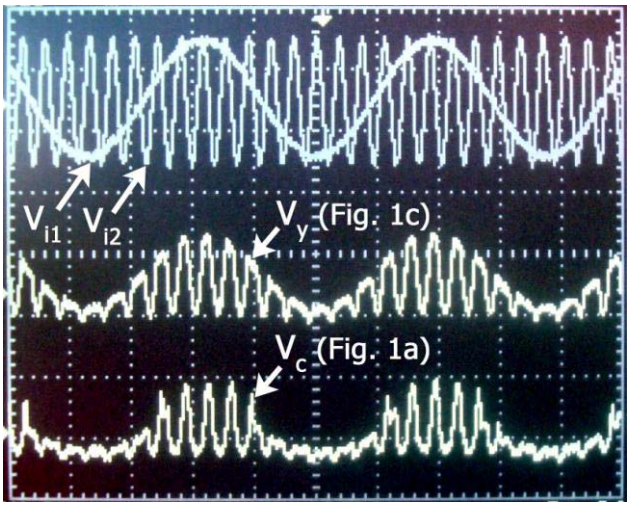

Fig. 2. Output voltage of the conventional WTA and the proposed SDFVF operating as a WTA with sine input signals $V_{i1} = 1\,V_{pp}$ at 10 kHz and $V_{i2} = 1\,V_{pp}$ at 100 kHz.

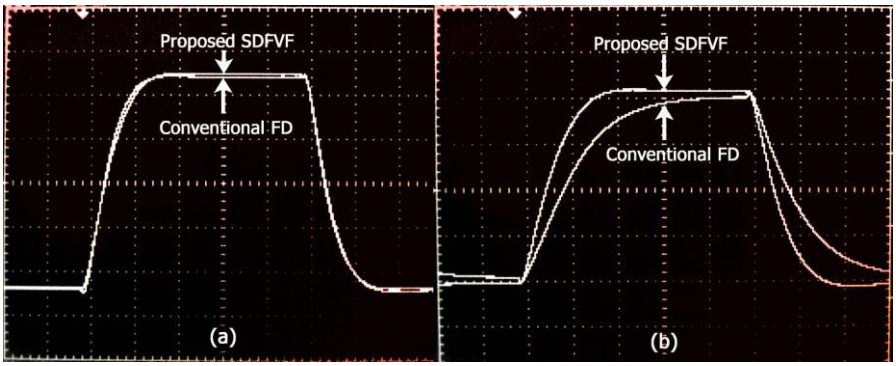

Fig. 3. Transient response of the conventional FD and proposed SDFVF with a $V_i = 1.2\,V_{pp}$ at 40 kHz using a supply voltage of a) 3 V and b) Using 1.4 V.

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$V_i = 1.2\,V_{pp}$ at 40 kHz was used. Observe that the signal from the conventional FD is not able to follow the input signal, showing that transistors have been forced out of saturation, whereas the proposed structure maintains its operation.

5 Conclusion

A high performance differential voltage follower for WTA application was discussed. The operation was demonstrated experimentally with high precision. Also, results from experimental measurement of the circuit as a fully-differential amplifier with low power supply were presented.

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