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HfO_2 nanoparticles embedded within a SOG-based oxide matrix as charge trapping layer for SOHOS-type memory applications

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ABSTRACT

In this work, HfO_2 nanoparticles (np-HfO_2) are embedded within an amorphous Spin-On Glass (SOG)-based oxide matrix and used as charge-trapping layer for memory applications. Following specific thermal treatments, the np-HfO_2 act as charge storage nodes able to retain charge injected after applying a constant gate voltage. A Silicon-Oxide-High-k-Oxide-Silicon (SOHOS)-type memory has been fabricated with the high-k charge-trapping layer containing 5, 10 and 15% of np-HfO_2 concentration within the SOG-oxide matrix. The memory's charge trapping characteristics are quantized by measuring the flat-band voltage (Vfb) shift of SOHOS capacitors after charge injection and then correlated to np-HfO_2 concentration. Since a large memory window has been obtained for our SOHOS memory, the relatively easy injection/annihilation (programming/erasing) of charge injected through the substrate opens the possibility to use this material as an effective charge-trapping layer. A very small injected charge density of 1×10^{-6} C/cm^2 shifts Vfb by 100 mV without needing to overstress the dielectric by hot-carrier injection, a usual method in SOHOS memories. In conclusion, using a simple spin-coating method for the charge-trapping layer, wide current memory windows have been obtained in SOHOS-memories and their charge-trapping characteristics are quantized and correlated to the np-HfO_2. concentration.

1. Introduction

As the need for increased Non-Volatile Memory (NVM) performance approaches the physical limits offered by conventional materials, research on new materials/architectures for memory applications has been constantly sought in order to meet the stringer specifications imposed on these devices [1,2]. Among the current memory technologies available (still dominated by the floating gate flash technology), the Silicon-Oxide-Nitride-Oxide-Silicon (SONOS)-memory, or floating trap memory, is one attractive candidate to realize flash-memory vertical scaling [3,4]. In a floating gate device, the charge is stored in the polysilicon floating gate as free carriers having a continuous spatial distribution in the conduction band, while the SONOS memory stores charge in spatially isolated deep level traps within the nitride oxide [5–7]. Also, in a SONOS-memory it is possible to both increase its programming speed and to lower its operating voltage by reducing the tunnel oxide thickness [8]. However, this seriously degrades the charge retention capability of the device so that the SOHOS (Silicon-Oxide-High-κ-Oxide-Silicon) flash memory has emerged as a way to increase its charge retention by replacing the silicon nitride with a higher dielectric constant material as charge trapping layer [9]. Because of the higher dielectric constant, the electric field across the tunneling oxide is enhanced thus enabling a greater injection of charge from the silicon into the trapping layer and also, enables the use of thicker oxide tunnel layers so that the levels of leakage current tunneling back to the substrate are decreased as well, the combined effect being that of better charge injection/retention characteristics. Besides the conduction mechanisms used for charge injection, quite important for effective programming of these devices [10], several high-k materials have been explored for SOHOS-type memories, they include Al_2O_3 [11–14], HfO_2 [15–17], HfAlO [18–20] and many other materials that are currently under research and which are important to enhance the performance of memory devices based on charge trapping phenomena.

Aiming to increase the charge-based programming/erasing capacity of SOHOS-type memory devices, this work study the ability of np-HfO_2 (embedded within a SOG-oxide matrix) to act as charge trap centers in a Metal-Oxide-High-k-Oxide-Silicon (MOHOS) capacitor structure. We quantize the general charge trapping capacity of the high-k layer in MOHOS devices by measuring the shift in their flat band voltage (ΔVfb) after programming/erasing operations and we correlate our results to the concentration of np-HfO_2 within the oxide matrix. Since the np-HfO_2 based trapping layer shows a large memory window itself for charge trapping, we then exploit this characteristic in order to inject just enough charge at the memory device (under low-electric field substrate injection conditions) and a steady increase/decrease in ΔVfb is obtained during programming/erasing operations. We show that ΔVfb

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is dependent on both the applied gate voltage and the np-HfO_2 concentration. On the other hand, given that the programming/erasing speed operations are usually flat-band/threshold voltage (Vfb/Vth) shift vs time plots and that they are measured in terms of the applied gate voltage, having thinner oxide stacks (including all blocking/trapping/tunneling oxides) would increase the current density being injected to the trapping layer and thus, a lower operating voltage would be needed to shift Vfb/Vth in any particular direction. This effect could be mistakenly interpreted as a higher efficiency of the high-k layer to trap charge since lower operating voltages are needed. By integrating the injected gate current density Jg with time, we are able to quantize the effective density of charge being injected at the memory device:

$$Q_{inj} = \int_0^t J_g dt. \quad (1)$$

Where J_g is gate leakage current density and t is time, while the units for Q_{inj} are C/cm^2. This measurement can be applied to other memory devices having oxide structures with different gate areas and blocking/trapping oxide thicknesses (different leakage current densities) and thus, we would be able to measure the intrinsic capacity of the whole oxide stack for programming/erasing operations in a more realistic way, that is, dependent only on the injected charge density and independent of gate area and oxide stack thickness. Finally, after chemically oxidizing the silicon surface (in order to get an ultra-thin tunneling oxide), the charge trapping layer based on np-HfO_2 can be easily deposited atop the oxidized silicon surface by the sol–gel spin coating method, which is also used for deposition of the thicker blocking oxide. Therefore, the fabrication cost of the MOHOS-memory is dramatically reduced since film formation with the sol–gel spin coating is a simple method in comparison with atomic layer deposition (ALD), physical vapor deposition (PVD), or chemical vapor deposition (CVD) and the sol–gel materials used to develop both the blocking and charge trapping layers are economic and readily available.

2. Experimental

For all experiments, we used silicate-type SOG materials (from Filmtronics, Corp., 15A), N-type silicon wafers (100) with resistivity of 5–10 Ω·cm, and np-HfO_2 having granular diameter around 100 nm (99.9% purity from American Elements). Standard RCA-cleaning procedures (to eliminate organic/metallic silicon surface contaminants) were applied to all wafers and then dipped in HF solutions so that HF-last surfaces were obtained. The oxide stack fabrication was realized sequentially thus obtaining 1) an ultra-thin direct-tunneling chemical oxide SiO_x, 2) a high-k trapping oxide based on np-HfO_2 and 3) a thick blocking SOG-based oxide SiO_2. The thin tunneling oxide SiO_x was obtained by immersion of the HF-last silicon wafers into H_2O_2 at 75 °C by 16 min so that a thin chemical oxide (2.4 nm) was developed at the silicon surface. The np-HfO_2 charge trapping layer was obtained by preparing a np-HfO_2:H_2O:CH_3COOH:SOG solution in which the concentration ratios of np-HfO_2 to SOG were 5, 10 and 15%. The solute concentration was measured with an analytical balance AG285 from Mettler-Toledo. These np-HfO_2 were then hydrolyzed in the SOG solutions and subjected to water bath (baine marie, 80 °C, 2 h) treatments in order to obtain homogeneous solution mixtures. The final np-HfO_2:SOG solutions were directly applied on the wafers' surfaces and spinned at 7000 rpm by 20 s. After np-HfO_2:SOG application, all films were initially baked at 200 °C (10 min in N_2 ambient) in order to evaporate most of the organic solvents. A second thermal treatment of 800 °C (30 min in N_2) was also performed within a quartz furnace so that better film densification and solvent removal could be obtained after this curing process. The SiO_2 blocking oxide was also formed by direct deposition of a silicate SOG solution on the wafer surface and spinned at 7000 rpm by 20 s. This last film was also baked at 200 °C (10 min in N_2) and 1000 °C (30 min in N_2) so that the former oxide films are covered with this thicker blocking oxide. The thicknesses for all oxide films were measured with a Gaertner ellipsometer L117 and a Tencor alpha-step equipment. The average thickness for the blocking and trapping oxide layers is 130 and 120 nm respectively. For electrical C–V and I–V characterization, all oxide films were metalized with 1 μm of aluminum by evaporation and unless otherwise stated, a gate capacitor area of 13.34e–4 cm^2 was used for all MOS devices. Following metallization, a last thermal treatment (450 °C in forming gas ambient, 5% $H_2 + 95\%N_2$) was applied to half of the samples in order to compare the charge retention ability of the whole oxide stack after passivation of all dangling bonds with a H_2-based annealing. It is important to mention that all memory characteristics presented in this work were only obtained for the H_2-annealed samples so that this last thermal treatment is very important in order to obtain reproducible I–V, C–V and memory performance characteristics. The final memory device is then composed of a Metal/Oxide/High-k/Oxide/Silicon or MOHOS structure. All films' chemical compositional analysis was obtained by Fourier-Transform InfraRed (FTIR) spectrum measurements in absorbance mode with a Bruker Vector-22 system. Finally, C–V and I–V measurements were done by using a Keihtley Model 82-DOS Simultaneous C–V system and an HP 4156B Semiconductor Parameter Analyzer respectively.

3. Results

Fig. 1 shows a schematic of the fabricated sample and the idealized energy band diagram in (a) and (b) respectively. The energy conduction and valence band offsets of the HfO_2 material with respect to SiO_2 show a moderate energy barrier for electrons and holes respectively [21,22], thus limiting the applied electric field to lower values in order to avoid leakage of carriers out of the HfO_2 trapping layer via a Fowler–Nordheim (F–N) or other conduction mechanism. This is important since the injection of carriers (for both programming/erasing steps at the trapping layer) from the silicon substrate is usually done via a moderate gate electric field and hot carrier injection (HCI) mechanism both applied simultaneously to a SONOS/SOHOS structure.

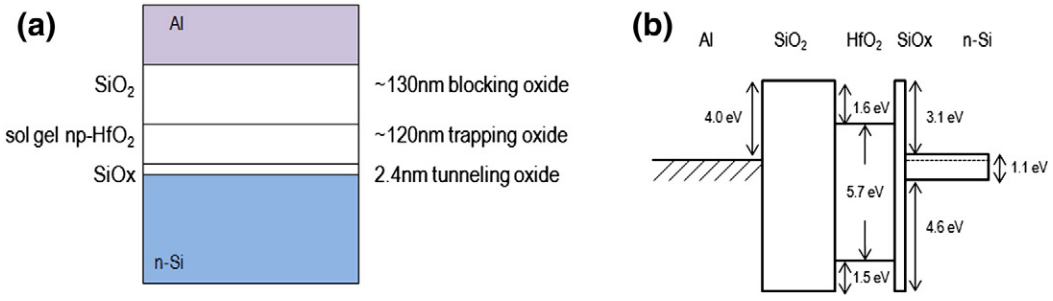

Fig. 1. (a) Schematic of the MOHOS memory containing the blocking/trapping/tunneling oxides. (b) Idealized energy band diagram for the memory structure shown in (a). The energy conduction and valence band-offsets are also shown for reference.

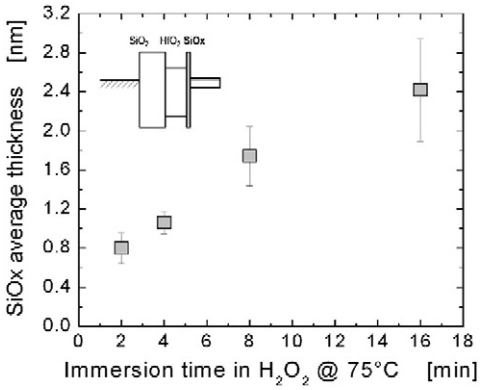

Fig. 2. Average thickness of ultra-thin chemical oxide SiOx with immersion time in hot H_2O_2. A chemical oxide with ~2.4 nm is used as the tunneling oxide and its location within the memory structure is highlighted in the inset.

In some cases, channel hot electron injection (programming condition), and band-to-band tunneling induced hot hole injection (erasing condition) are used [22–24]. Trapping of charge via HCI could decrease the general reliability of a Metal-Oxide-Semiconductor Field-Effect Transistor MOSFET device [25–27] and likewise, the reliability of a FET-based memory device after overstressing the charge trapping layer with this mechanism. In this work, we are able to inject electronic charge to the np-HfO_2 trapping layer after applying a small gate electric field only (without using any HCI mechanism) so that a memory device with enhanced reliability is expected. Fig. 2 shows the average thickness of the chemical oxide (SiO_x) grown after immersion of HF-last silicon wafers into hot H_2O_2 from 2 to 16 min. The average SiOx thickness is obtained after measuring 10 different spots on the chemically-oxidized wafers by ellipsometry and for each immersion time while the bars show the maximum/minimum oxide thickness values. In our memory structure we have used a tunneling oxide of ~2.4 nm, which is grown after 16 min of immersion within H_2O_2. The inset highlights the location of this ultra-thin tunneling oxide SiO_x within the memory structure. Fig. 3(a) shows that by adding only 6.6% of np-HfO_2 into SOG, the electrical accumulation capacitance (Cox) of MOS structures is increased by ~8.6 times as compared to the same SOG-based oxide without np-HfO_2 addition (having both the same area and oxide thickness). In the same figure, the top inset shows the FTIR absorption spectra for SOG-based oxides in which np-HfO_2 concentration of 5, 10 and 15% has been introduced. There, we notice that by increasing the Hf content in the prepared solutions, there is a corresponding increase in the magnitude of the absorption peak related to the Hf-O chemical bond (as shown by the arrow) and which is found at 752 cm^{-1} [28]. The bottom inset highlights the location of the trapping oxide layer within the memory structure. It is important to state that the C–V and I–V characteristics present in Fig. 3(a–b) are obtained from capacitor structures having only the np-HfO_2 charge trapping layer deposited atop the silicon substrate (including a thin interfacial tunneling oxide), so there is no blocking oxide layer present at this stage. The purpose is to electrically test the charge trapping and blocking oxide layers independently. In Fig. 3(b), we notice that after stressing the charge trapping layer with a continuous gate voltage up to Vg = 8 V, the first stressing test (sweep 1, applied to several samples having two different gate areas), shows a high-conduction state for the gate current whereas a second stressing test (sweep 2, applied to the former samples) initially develops a low-conduction state for gate current, then an increase in gate current by a different conduction mechanism and finally, electrical breakdown which again increases the gate current to a high-conduction state. Therefore, the np-HfO_2 oxide is able to develop a resistance switching mechanism in which a large window for charge conduction (around 6 orders of magnitude between the OFF and ON state) is obtained. Since there is a large conductivity window present in this material, we will use this large window to inject electronic charge into it in order to modulate the Vfb of MOS structures during programming/erasing operations, instead of forcing the np-HfO_2 to modulate its conduction state from OFF to ON conditions. The inset in this figure highlights the location of the trapping layer within the memory structure as well. Fig. 4(a–b) shows the C–V and I–V characteristics of only the thicker blocking oxide layer respectively. In Fig. 4(a), the C–V characteristics of non-diluted or 100% SOG-based oxide are compared against those of a high-quality thermally grown oxide and SOG-oxides that were diluted in deionized water by 50% and 33% as well. This way, several SOG-based oxides thinner than 130 nm can be electrically tested by C–V and I–V measurements. The C–V characteristics show an increase in Cox as the oxide gets thinner and a low dispersion in both Cox and Vfb for each set of samples is also shown. Obtaining a low Cox/Vfb dispersion is indication of a good uniformity in both the oxide thickness throughout the silicon surface and charge density within the oxide as well. Fig. 4(b) shows the I–V characteristics for 100%, 50% and 33% SOG-based oxides, having an oxide thickness of 130, 33 and 20 nm respectively. We notice that even for the thinner oxides, the electrical conduction processes developed within all dielectrics are quite restrained for both the inversion and accumulation regimes (within the gate voltage applied). These oxides have very low gate current densities so that, along with C–V measurements, it is demonstrated that the blocking oxide layer presents an electrical quality high enough [29] to act as a blocking barrier for injected charge carriers

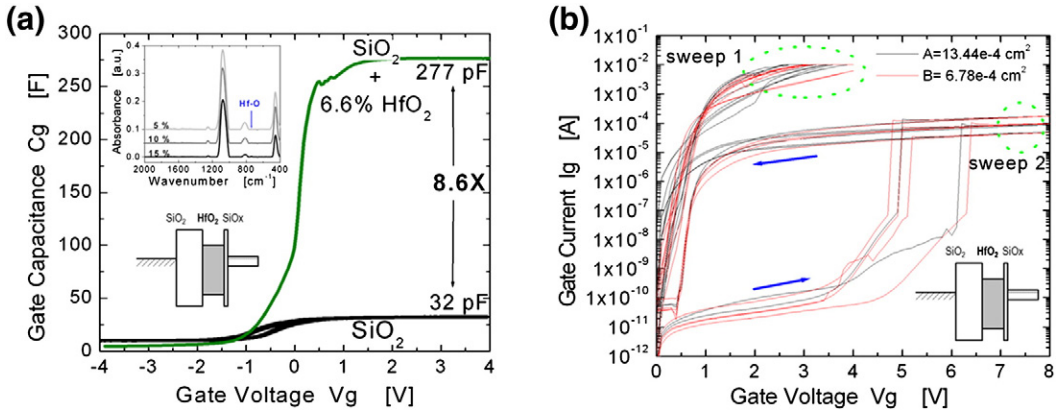

Fig. 3. (a) C–V characteristics for SOG-based oxides without/with HfO_2 nanoparticles. Addition of 6.6% np-HfO_2 within the SOG-oxide matrix increases its dielectric constant by ~8.6×. The top inset shows FTIR absorption spectra for oxides with a np-HfO_2 concentration of 5%, 10% and 15%. The absorption peak for the Hf-O chemical bond is found at 752 cm^{-1} and increases with respect to np-HfO_2 concentration. The bottom inset highlights the location of the charge trapping layer based on np-HfO_2 within the memory structure. (b) I–V characteristics for the trapping layer based on np-HfO_2. After two gate voltage sweeps, resistance memory effects having a large memory window are observed for the trapping layer and this conductivity window will be used for trapping of charge. The inset highlights the location of the trapping layer within the memory structure.

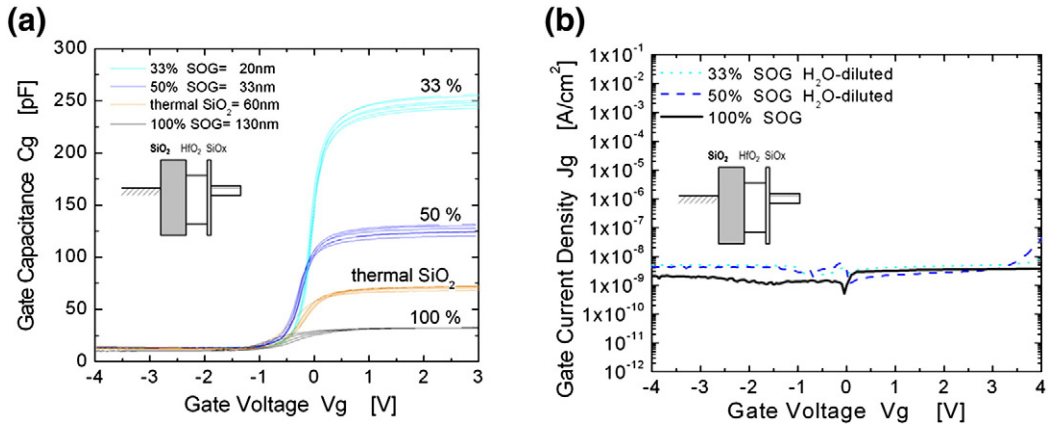

Fig. 4. (a) C–V characteristics of the SOG-based blocking oxide SiO_2. Low Cox/Vfb dispersion is observed for all SOG-based oxides and their characteristics are even comparable to those presented by a thermally grown oxide, thus confirming the high quality of the blocking oxide. The inset highlights the location of the blocking oxide within the memory structure. (b) J–V characteristics of the SOG-based oxides showing negligible gate leakage current for all polarization conditions, showing again a high capacity of the SOG-based blocking oxide to retain the charge being trapped at the np-HfO_2 trapping layer after injection. The inset highlights the location of the blocking oxide within the memory structure.

within the proposed memory structure. In both figures, the inset highlights the location of this blocking oxide within the memory structure.

From this point on, all the electrical testing is applied to the complete memory structure having the blocking/trapping/tunneling oxide layers. Fig. 5(a) shows the I–V data for the MOHOS memory structure in which the trapping oxide layer has np-HfO_2 concentration of 5%, 10% and 15%. Initially, a very low conduction state is shown under accumulation up to Vg = 4 V, then a different conduction mechanism increases the current flow steeply until breakdown is reached at about 5.3 V and these same characteristics appear for all memory samples. Once Vg = 10 V, we measure the gate current back to 0 V and we confirm that the memory structure remains at the high conduction state, thus limiting the gate voltage range that can be applied to the trapping layer for charge injection to Vg<5 V (we use V1 and V2 as stressing voltages for that purpose). Fig. 5(b) shows the C–V data for the same memory structures before breakdown. Even though their Vfb is shifted towards negative values (indicative of a large density of positive charge within the oxide stack), there is a correspondent increase in Cox with np-HfO_2 concentration. An increase in the inversion capacitance (Cinv) for each concentration is also shown. This last feature could hinder proper Vfb calculation after C–V measurement but we have tried to minimize the error by obtaining Vfb from at least 10 different devices having similar C–V characteristics and even to obtain Vfb after differentiating the initial C^{-2} vs. Vg curve and finding Vfb at the maximum slope of the left flank [30]. The Vfb data presented in Fig. 5(b) is the average result of all measured devices after using at least two different methods to obtain Vfb.

Fig. 6(a–b) shows the Vfb shift in MOHOS devices after injecting substrate electrons (programming condition) and substrate holes (erasing condition) with time. We notice greater Vfb shift for devices having greater np-HfO_2 concentration. Because of a higher dielectric constant, the electric field across the tunneling oxide is enhanced thus enabling greater injection of charge from the silicon into the trapping layer. We can see that the level of positive/negative Vfb shift is dependent on the programming/erasing time for all conditions. In Fig. 6(b), we notice that for the np-HfO_2 with 10% concentration, the erasing condition does not recover the Vfb shift completely, and this effect can be due to the existence of deep trap levels within the np-HfO_2 trapping layer thus making harder to annihilate the initially trapped electrons. Fig. 7(a–b) shows that by doubling the Vg applied to the memory structures, largest Vfb shifts are obtained. During programming operation and for a np-HfO_2 concentration of 15%, a very fast injection of electrons (time of 1 s) is able to shift Vfb up to 75 mV whereas a longer time for electron injection (time of 300 s) shifts Vfb up to almost 200 mV. Although Vfb shift is lower for 10% and 5% concentrations, doubling Vg produce enough energy for the injected electrons to shift Vfb even for the 5% concentration, which was not the case for Vg = 2 V. During erasing condition, hole trapping shifts Vfb to negative values.

Up to now, we have obtained the memory performance of MOHOS structures by applying a constant gate voltage and measuring their Vfb shift with respect to their programming/erasing times. However, since having thinner memory oxide stacks (scaled devices) would increase the charge density being injected to the trapping layer,

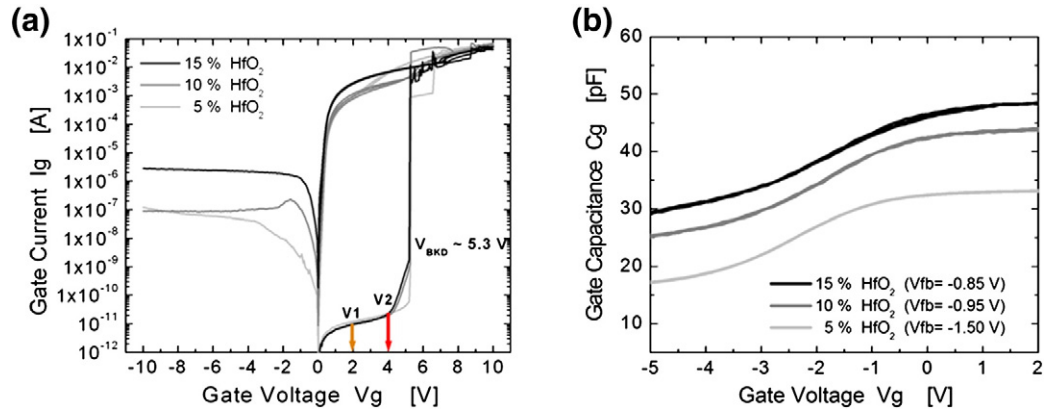

Fig. 5. (a) I–V characteristics for a MOHOS memory with different concentrations of np-HfO_2 as trapping layer. Since breakdown occurs at Vg ~ 5.3 V, electron injection into the trapping layer is done at V1 and V2. (b) C–V characteristics for the same MOHOS memory before breakdown. Although Vfb has been largely shifted towards negative values, there is a corresponding increase in Cox with np-HfO_2 concentration.

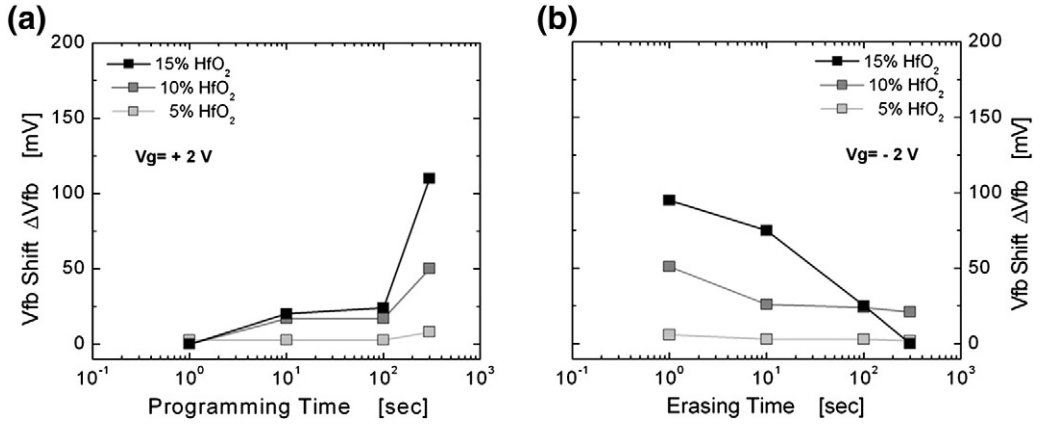

Fig. 6. (a) Vfb shift vs. programming time (electron injection) for a MOHOS-memory with different concentrations of np-HfO_2 as trapping layer. Vfb shift is greatly increased with programming time for the greater np-HfO_2 concentration at Vg = +2 V. (b) Vfb shift vs. erasing time (hole injection and/or electron annihilation) for the same MOHOS-memory. A complete Vfb recovery is observed for the memory having greater np-HfO_2 concentration at Vg = −2 V.

shift of Vfb/Vth to any particular direction could be done using lower operating voltages and/or reduced programming/erasing speeds and this could be mistakenly interpreted as a higher efficiency of the high-k layer to trap charge. By integrating the injected gate current density Jg with time, see Eq. (1), we are able to quantize the effective density of charge being injected at the memory device, Qinj. Figs. 8–9 show the ability of our MOHOS devices to shift Vfb during programming/erasing conditions after charge injection using V1 and V2. Figs. 8(a)–9(a) show that the memory structures having the largest np-HfO_2 concentration shift Vfb to larger values because they trap more injected charge. From both figures, our devices shift Vfb up to 100/200 mV after trapping extremely small Qinj values of 1×10^{-6}/3×10^{-5} C/cm^2 respectively. Trapping layers having lower np-HfO_2 concentrations are unable to inject large Qinj values, thus trapping less charge and ultimately, reducing Vfb shift. Figs. 8(b)–9(b) show Vfb recovery of the MOHOS devices after hole injection. It is clear that a trapping layer having a larger np-HfO_2 concentration is able to shift Vfb more efficiently after using the same hole injection density. In other words, there is a steeper Vfb recovery slope for the device having a 15% concentration of np-HfO_2 as compared to the others. For these figures, a very small Qinj ~ 10^{-6} C/cm^2 is enough to recover all or most of the initially shifted Vfb.

4. Discussion

Considering the large conductivity window between the LOW/HIGH conduction states (OFF/ON conditions) of about 9 orders of magnitude shown in Fig. 5(a), we think that there is plenty of room to inject large densities of electronic charge at the trapping oxide layer in order to properly modulate Vfb/Vth in memory devices without needing to overstress the stacked oxide using any HCI mechanism. Under this high conduction state, we also measure the gate current flow in inversion (from Vg = 0 to −10 V) so that we could obtain the complete picture of electronic conduction for this memory structure. After breakdown, the electronic conduction properties of the memory devices are quite similar to those of a metal/semiconductor rectifying contact, which makes sense if one considers the existence of a conductive filament path connecting both the silicon substrate to the aluminum metal gate. On the other hand, during electrical operation of our memory devices, we think that Vfb shifts because of electron/hole trapping mechanisms at the np-HfO_2 trapping layer. By looking at the idealized energy band diagram of Fig. 1(b), we notice that the conduction/valence band offsets of HfO_2 to silicon substrate are 1.5 and 3.1 eV respectively. During programming condition, electrons accumulate at the substrate's surface and they gain enough energy from the applied gate voltage Vg enabling them to cross the tunneling oxide's energy barrier with energies well below 3.1 eV (the tunneling oxide is thin enough and electrons can tunnel directly) and be trapped at the np-HfO_2 trapping layer, thus shifting Vfb to positive values. During erasing conditions, a negative gate voltage inverts the silicon surface thus increasing the hole density and because of the electric field, these holes are trapped at the np-HfO_2 layer (where they could annihilate some already trapped electrons), thus shifting Vfb to negative values. The former process would occur after the holes are able to tunnel through the thin tunneling oxide and

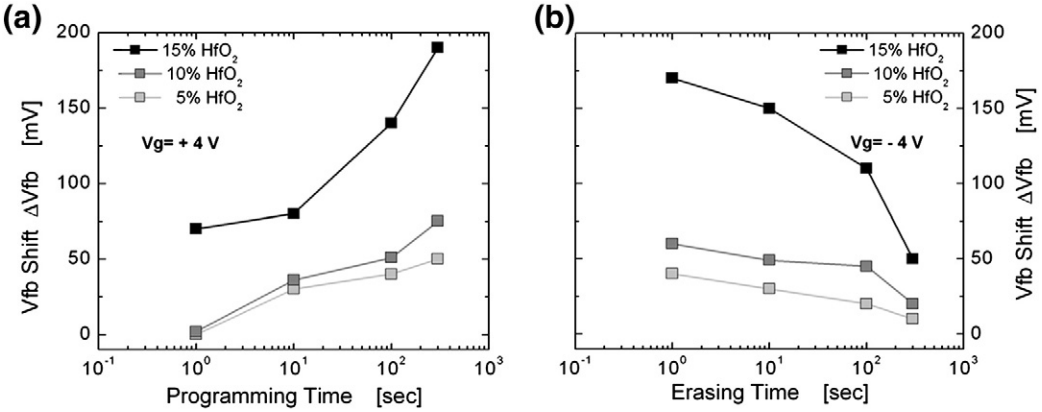

Fig. 7. (a) Vfb shift vs. programming time for a MOHOS-memory with different concentrations of np-HfO_2 as trapping layer. With Vg = +4 V, doubling the voltage or electric field applied to the gate enhances Vfb shift during electron injection. (b) Vfb shift vs. erasing time for a MOHOS-memory with different concentrations of np-HfO_2 as trapping layer. With Vg = -4 V, doubling the voltage or electric field applied to the gate enhances Vfb recovery during hole injection and/or electron annihilation as well.

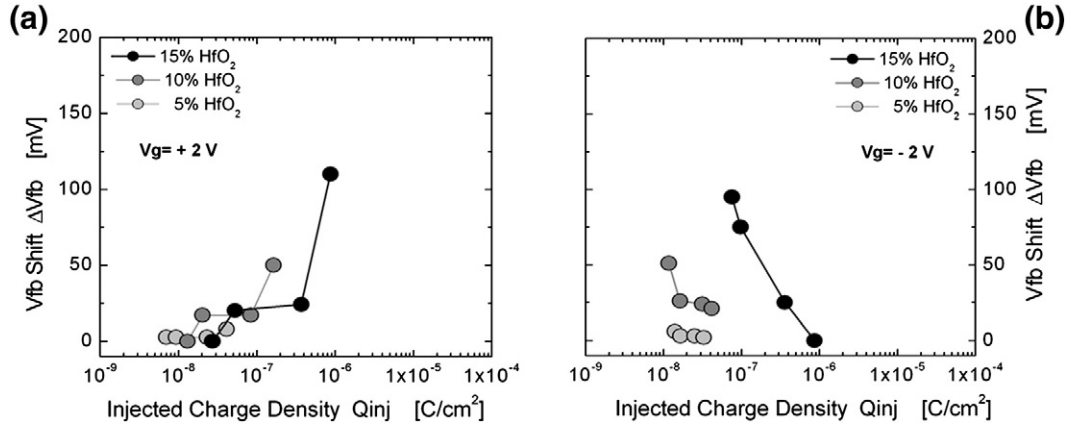

Fig. 8. (a) Vfb shift vs. injected charge density Qinj (at Vg = +2 V) for a MOHOS-memory with different concentrations of np-HfO_2 as trapping layer. The memory structure having the largest np-HfO_2 concentration is able to trap more injected charge and thus, shift Vfb to larger values. (b) Vfb shift vs. injected charge density Qinj (at Vg = −2 V) for a MOHOS-memory with different concentrations of np-HfO_2 as trapping layer. The memory structure having the largest np-HfO_2 concentration is able to fully recover Vfb by using larger Qinj. In both cases, a small charge density of ~10^{-6} C/cm^2 is enough to completely shift/recover Vfb.

also have enough energy, well below 3.1 eV (valence band offset), to be trapped at the np-HfO_2 trapping layer.

Even though the programming/erasing times are rather slow in our MOHOS-type memories, we have shown that after injecting very small charge densities $Qinj \ll 1\times10^{-4}$ C/cm^2 into the gate oxides (without using any HCI mechanism), proper modulation of Vfb can be achieved and reliability of these devices is expected to increase. In order to reduce the programming/erasing times, ways for increasing the density of injected charge Qinj must be sought whether by increasing the applied gate electric field, the dielectric constant of the charge-trapping layer or even by reducing the physical thickness of the tunneling oxide or the trapping layer itself. In the end, the best solution will be that having the best performance/reliability compromise since the former characteristics are all interrelated. Also, the use of metallic nanoparticles (np) embedded within an oxide matrix must be done carefully in order to avoid possible migration/diffusion of these highly reactive nanoparticles towards the bottom/top materials, thus degrading the performance of the memory devices. With this in mind, it is highly recommended to use low thermal-budgets as possible or even gate-last fabrication approaches in order to keep all metallic nanoparticles within the boundaries of the charge-trapping layer. Finally, by plotting the Vfb shift data of Figs. 6–7 using Qinj instead of programming/erasing times, we are able to measure the intrinsic capacity of the whole oxide stack for programming/erasing operations being only dependent with the injected charge density and independent of gate area and oxide stack thickness. This can be useful for comparison of scaled memory devices based on trapping of injected charge.

5. Conclusions

Using np-HfO_2 as a charge-trapping layer in MOHOS memory devices has been demonstrated. By increasing the volume concentration ratio of np-HfO_2 to SOG, the dielectric constant of the charge-trapping oxide is increased, thus enhancing the electric field across the tunneling oxide and enabling greater injection of charge from the silicon substrate. A large conductivity window has been obtained for the charge-trapping layer, which is used to inject electronic charge into it and shift the Vfb of MOHOS structures during programming/erasing operations. It is shown that a larger injection of charge is obtained for memory structures having greater concentration of np-HfO_2, and the initially shifted Vfb is then recovered after applying a gate voltage with reverse polarity, indicative of good endurance characteristics. Charge injection is done without using any Hot-Carrier Injection mechanism, quite important in order to enhance the overall reliability of a memory device. By using Qinj instead of programming/erasing times, we are able to measure the intrinsic capacity of the whole oxide stack for memory operations being only dependent with the injected charge density and independent of gate area and oxide stack thickness. We believe this procedure can be useful to compare the basic performance of scaled memory devices (having smaller gate areas and thinner oxide stacks) during charge injection routines.

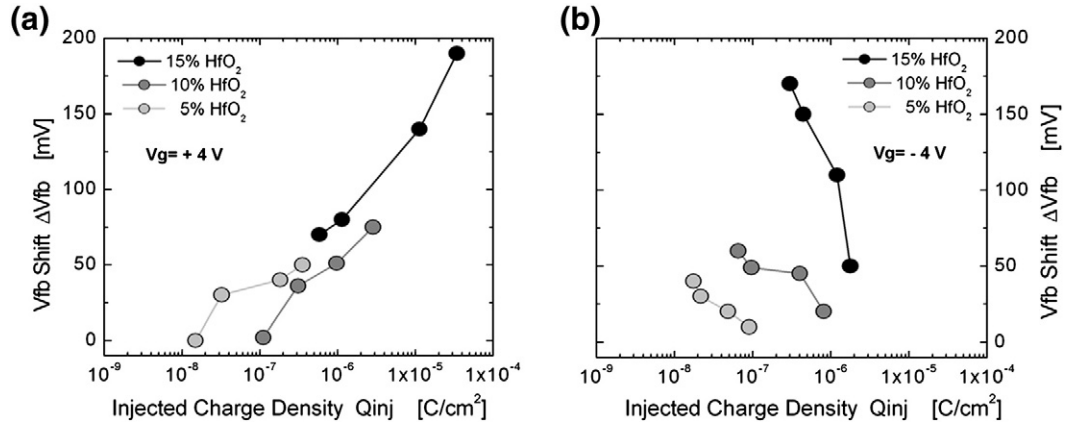

Fig. 9. (a) Vfb shift vs. injected charge density Qinj (at Vg = +4 V) for a MOHOS-memory with different concentrations of np-HfO_2 as trapping layer. The memory structure having the largest np-HfO_2 concentration is able to trap more injected charge and thus, shift Vfb to larger values. (b) Vfb shift vs. injected charge density Qinj (at Vg = −4 V) for a MOHOS-memory with different concentrations of np-HfO_2 as trapping layer. The memory structure having the largest np-HfO_2 concentration is able to recover Vfb more efficiently (using the same Qinj) as compared to other np-HfO_2 concentrations.

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