Journal of Non-Crystalline Solids 358 (2012) 2340–2343

Contents lists available at SciVerse ScienceDirect

Journal of Non-Crystalline Solids

journal homepage: www.elsevier.com/locate/jnoncrysol

Ambipolar a-SiGe:H thin-film transistors fabricated at 200 °C

Miguel Dominguez *, Pedro Rosales, Alfonso Torres, Mario Moreno, Joel Molina, Francisco De la Hidalga, Carlos Zuniga, Wilfrido Calleja

National Institute for Astrophysics, Optics and Electronics (INAOE), Electronics Department, Luis Enrique Erro No. 1, Puebla, Z.P. 72840, Mexico

ARTICLE INFO

Article history:
Received 10 August 2011
Received in revised form 26 November 2011
Available online 5 January 2012

Keywords:
Thin-film transistor;
Hydrogenated amorphous silicon–germanium;
Spin-On Glass

ABSTRACT

In this paper, we study the ambipolar behavior of a-SiGe:H thin-film transistors fabricated at 200 °C. A sub-threshold slope and an on/off current ratio of 0.34 V/DEC and 10^5, respectively, were measured for the n-type region, whereas values of 0.15 V/DEC and 10^4 for were measured for the p-type region. We also obtained the characteristic energies for the deep localized states of the a-SiGe:H film, the flat-band voltages, and threshold voltages among other device parameters for the ambipolar thin-film transistors.

1. Introduction

Thin film transistors (TFTs) are being widely used in active matrix liquid crystal displays (AMLCD). For this application, the use of complementary devices, n- and p-type transistors, is attractive since this technology allows for the implementation of efficient digital circuits. Although complementary metal oxide semiconductor (CMOS) logic circuits, based on separated n- and p-type doped deposited layers, are currently under development [1], the use of ambipolar TFTs, operating as either p- or n-type transistors, can simplify the design and reduce the cost for the fabrication of the complementary logic circuits. Hydrogenated amorphous silicon (a-Si:H) has been typically used as the active layer of TFTs. However, due to the preference for unipolar operation (n-type), polycrystalline silicon and other microcrystalline materials have been proposed for such applications. Nevertheless, the polycrystalline materials are deposited at temperatures above 450 °C [2,3]. This makes mandatory the use of expensive substrates which leads to a more expensive fabrication process. The fabrication of ambipolar transistors calls for both, the formation of source and drain ohmic contacts (metal–semiconductor interface), and the use of a high-quality gate insulator (insulator–semiconductor interface) [4–6]. The electrical parameters of the TFTs depend directly on the quality of the insulator–semiconductor interface [7]. In order to achieve a high quality interface, we use Spin-on Glass (SOG) as the gate insulator and a-SiGe:H as the active layer on our inverted staggered TFTs.

In this paper, we study the ambipolar behavior and characteristics of a-SiGe:H thin-film transistors fabricated at 200 °C. From the electrical characterization of the fabricated devices, we obtained the characteristic energies for the deep localized states of the a-SiGe:H film, and also other figures of merit and parameters such as the flat-band voltages (Vfb) and threshold voltages (V_T) of the TFTs.

2. Experiment

The fabricated TFTs used the inverted staggered structure; the process flow and cross section of the TFT structure are shown in Fig. 1. The simplified process flow is as follows: first, a 200 nm-thick Aluminum layer is e-gun evaporated and patterned as a bottom gate above the previously oxidized silicon substrate (Fig. 1a). Next, 160 ± 5 nm-thick of SOG diluted with 2-propanol and cured at 200 °C is used as the gate insulator (Fig. 1b). The refractive index of the SOG film was very close to that shown by thermally grown SiO_2 (1.46). The calculated dielectric constant was approximately 4.03 ± 0.05, which is also close to the value presented by thermally grown SiO_2 [8]; additionally, we observed an insulator breakdown field approximately of 4.5 MV/cm. Later, a 100 ± 4 nm-thick undoped a-SiGe:H and 40 ± 4 nm-thick n-type a-Ge:H films (Fig. 1c) were deposited using low frequency (110 kHz) plasma-enhanced chemical vapor deposition (LF PECVD) at 200 °C, pressure of 0.6 Torr and an RF power of 300 W. After that, 300 nm-thick Aluminum was e-gun evaporated and patterned to form the source and drain electrodes (Fig. 1d). Then, the n-type a-Ge:H film was etched using reactive ion etching (RIE) to self-align and to form the source and drain regions (Fig. 1e). Finally, a passivation 160 ± 5 nm-thick layer of SOG, diluted with 2-propanol and cured at 200 °C, was deposited (Fig. 1f). The

* Corresponding author.
E-mail address: mdominguez@inaoep.mx (M. Dominguez).

0022-3093/$ – see front matter © 2011 Elsevier B.V. All rights reserved.
doi:10.1016/j.jnoncrysol.2011.12.051

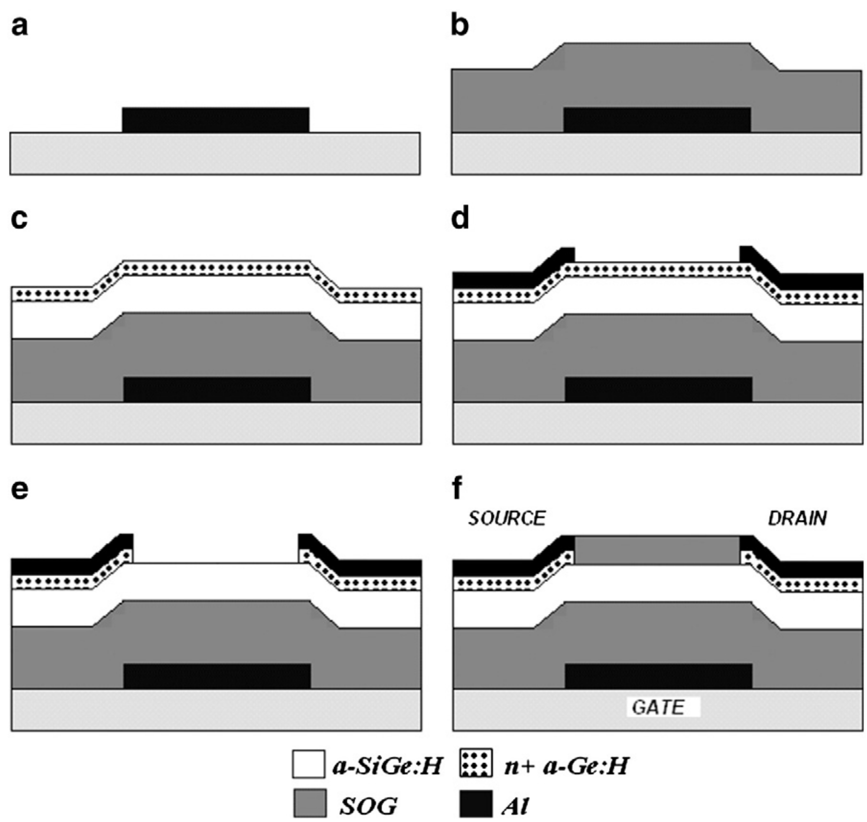

Fig. 1. Process flow and cross section of the inverted staggered a-SiGe:H TFTs, using SOG as passivation and gate insulator films (not to scale).

differences in the thickness of the films are due to process variations reflected in our pilot samples.

3. Results

The electrical characterization of the devices was conducted using the *HP 4156B Semiconductor Parameter Analyzer*. All the measurements were done under dark conditions. Fig. 2 shows the transfer characteristics of the ambipolar a-SiGe:H TFT with a width/length ratio W/L = 70 μm/75 μm.

As can be seen in Fig. 2, for positive gate bias the transfer characteristic shows an n-type TFT behavior, whereas for negative gate bias shows a p-type TFT behavior. From this figure we calculated the subthreshold slopes S at Vds = Vgs, resulting in 0.34 ± 0.023 V/DEC for the n-type region and 0.15 ± 0.024 V/DEC for the p-type region. On the other hand, the on/off-current ratio was 10^5 for the n-type and 10^4 for the p-type region. The off-current for both regions was approximately 2 pA at 0 V.

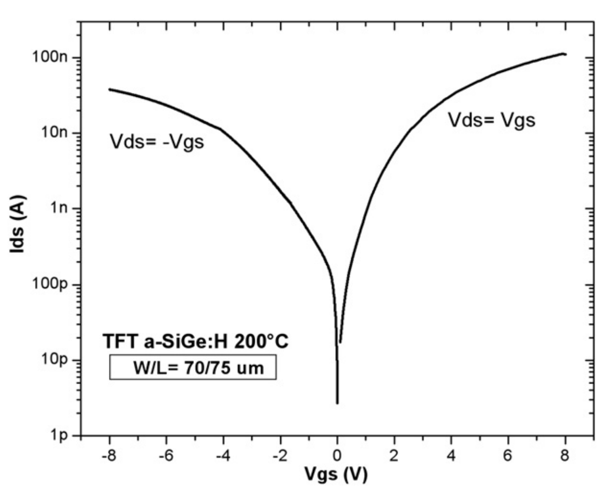

Fig. 2. Transfer characteristic of the ambipolar a-SiGe:H TFT.

Several models have been reported in the literature in order to characterize the ambipolar behavior of the TFTs from the transfer and output characteristics [4–6]. In the sake of simplicity, we use the method proposed by [4] to obtain the most important parameters of the ambipolar TFTs. This model consists in the calculation and plotting of the parameter M, which is the ratio of the Ids current (at Vds = Vgs) to the transconductance (Eq. 1) for both, n-type and p-type regions of the TFT. Two tangential lines are drawn to the M curve, one in the regime below threshold (L1), and another above the threshold regime (L2) (Fig. 3). The intercepts of L1 and L2 with the Vgs axis are equal to the flat-band voltage and V_T, respectively. From the slope (S1) of L1, we can obtain the characteristic energies of deep states, E_{A2} from the n-type region and E_{D2} from the p-type region (Eq. 2).

$$M = \mathrm{Ids}/(\mathrm{dIds}/\mathrm{dVgs}) \tag{1}$$

$$E_{A2}, E_{D2} = KT/2S1 \tag{2}$$

Where K is the Boltzmann's constant and T is the temperature in Kelvin.

The V_T and flat-band voltage values, calculated from Fig. 3, are 1.58 ± 0.04 and 0.21 ± 0.04 V for n-type region and −1.46 ± 0.04 and −0.08 ± 0.04 V for p-type region, respectively.

It is well know that the Density of States (DOS) determines the electrical properties of the amorphous materials. Numerous experimental techniques have been applied for the investigation of intrinsic and extrinsic defects states, leading to two models [9–11]. In one of them DOS is composed of acceptor-like states (near the conduction

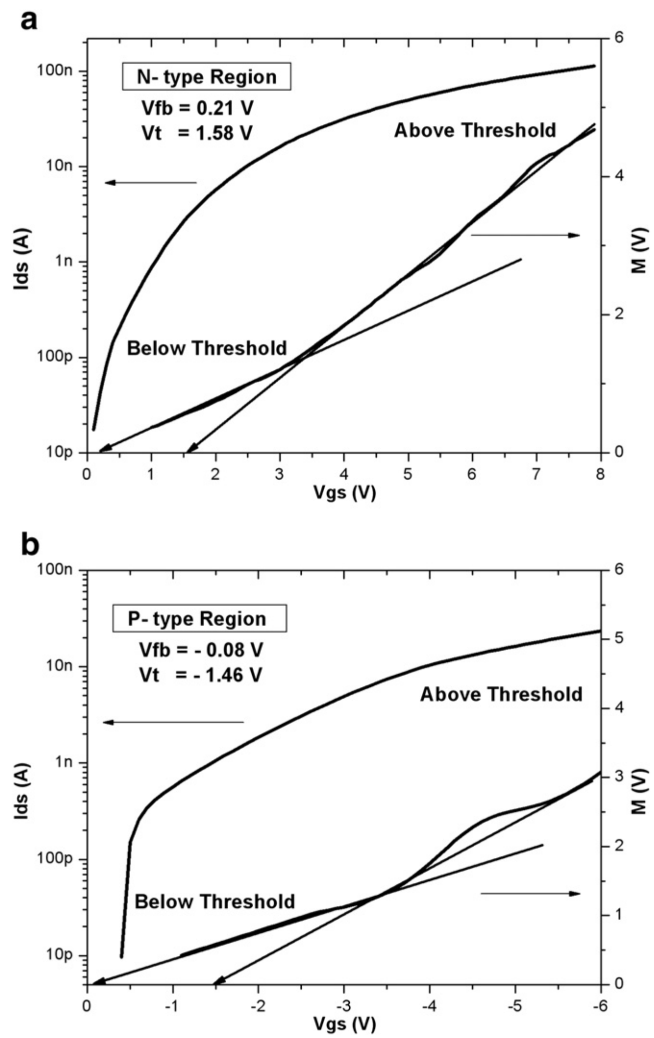

Fig. 3. Ids and M curves for the (a) n-type and (b) p-type regions.

band) given by the sum of a first term (tail states), a second term (deep states), and donor-like states (near the valence band) given by the sum of the third term (tail states) and the fourth term (deep states). A numerical approximation of the DOS distribution g(E) is given by [10]:

$$g(E) = g_{A1}\exp(E/E_{A1}) + g_{A2}\exp(E/E_{A2}) + g_{D1}\exp(-E/E_{D1}) + g_{D2}\exp(-E/E_{D2}) \quad (3)$$

Where g_{A1} and g_{A2}, are the minimum Density of States tail-acceptor and deep-acceptor states, respectively, and g_{D1} and g_{D2} are the minimum Density of States of tail-donor and deep-donor states, respectively. While E_{A1} and E_{A2}, are the characteristic energies of tail-acceptor and deep-acceptor states, respectively, and E_{D1} and E_{D2} are the characteristic energies of tail-donor and deep-donor states, respectively.

Then, using the S1 extracted from Fig. 3 and Eq. (2), the values of E_{A2} and E_{D2} are equal to 35 ± 3.36 and 72 ± 4.33 meV. Table 1 summarizes results of the electrical measurements. The differences in the calculated values are due to process variations and error estimates by the analysis software Origin.

Table 1
Parameters of a-SiGe:H TFTs.

Parameter	p-Type region	n-Type region
V_T	− 1.46 ± 0.04 V	1.58 ± 0.04 V
Vfb	− 0.08 ± 0.04 V	0.21 ± 0.04 V
|Vt − Vfb|	1.38 ± 0.08 V	1.37 ± 0.08 V
ΔVfb	0.29 ± 0.08 V	
E_{D2}, E_{A2}	72 ± 4.33 meV	35 ± 3.36 meV
S	0.15 ± 0.024 V/DEC	0.34 ± 0.023 V/DEC

4. Discussion

As can be seen, the values of V_T and subthreshold slopes reported here are lower than those reported in [4,12,13]. These low values are most probably a result of the use of SOG as the gate insulator, which improves the insulator–semiconductor interface. Since the ambipolar characteristics are strongly related to the high quality of the insulator–semiconductor interface, our result agrees with previous published results in the literature, where the ambipolar behavior has been observed only in devices with a gate insulator based on SiO_2 [4–6]. Then, we can infer that the inherent fixed positive charge in an SiNx insulator may prevent the formation of a p-channel in the device when the gate voltage is biased negatively.

The characteristic energies of deep localized states for a-SiGe:H films are lower than those presented by a-Si:H films [4,11]. This is because the a-SiGe:H film has a higher DOS due to the incorporation of Ge.

As expected, the flat-band voltages are lower than the threshold voltages for each region. The difference in flat-band voltages, for the n-type and p-type regions, is due to the trapping and detrapping of charge carriers between the a-SiGe:H film and the SOG insulator [14]. Electrons are trapped in the n-type region and holes are trapped in the p-type region. Thus, the flat-band voltage for the n-type region is more positive than that observed for the p-type region.

5. Conclusions

The ambipolar characteristics of a-SiGe:H thin-film transistors fabricated at 200 °C were obtained. For positive gate bias the transfer characteristic showed an n-type TFT behavior and for negative gate bias showed a p-type TFT behavior. The very low subthreshold slope obtained for both regions is an improvement for TFTs fabricated at low temperatures. The use of SOG as the gate insulator also improved the insulator–semiconductor interface. The characteristic energies of deep localized states for the a-SiGe:H film are lower than those presented by a-Si:H because the a-SiGe:H film has a higher DOS due to the incorporation of Ge. Therefore, the preparation of higher quality a-SiGe:H films needs a further investigation.

Acknowledgment

The authors want to thank all personnel of the laboratory of microelectronics at INAOE and to the CONACYT for the scholarship No. 160547.

References

[1] O. Moustapha, A. Abramov, D. Daineka, M. Oudwan, Y. Bonnassieux, P. Roca i Cabarrocas, Phys. Status Solidi C 7 (3–4) (2010) 1140.
[2] J.T. Lin, K.D. Huang, S.F. Hu, Semicond. Sci. Technol. 23 (2008) 075007.
[3] K. Shimizu, J. Zhang, J. Lee, J. Hanna, Mater. Res. Soc. Symp. Proc. 762 (2003) A20–A25.
[4] B. Wu, C. Hao, T. Wu, M. Chen, M. Jow, H. Chen, IEEE Trans. Electron. Devices 36 (12) (1989) 2903.
[5] G. Neudeck, H. Bare, K. Chung, IEEE Trans. Electron. 2 (1987) 344 Devices ED-34.
[6] H. Pfleiderer, IEEE Trans. Electron. 1 (1986) 145 Devices ED-33.
[7] M. Oudwan, O. Moustapha, A. Abramov, D. Daineka, Y. Bonnassieux, P. Roca I Cabarrocas, Phys. Status Solidi A 207 (5) (2010) 1245.
[8] M. Dominguez, P. Rosales, A. Torres, J. Molina, M. Moreno, F. De la Hidalga, C. Zuñiga, W. Calleja, Proc. IEEE Electronics, Robotics and Automotive Mechanics Conference, 741, 2010.

[9] PISCES User's Manual, Silvaco International, November (2002).
[10] Y. Hamakawa, Amorphous Semiconductor, Amsterdam: North Holland, 1982, p. 119.
[11] K. Lee, M. Shur, T. Fjeldly, T. Ytterdal, Semiconductor Device Modeling for VLSI, Prentice hall, New Jersey, 1993, pp. 494–528.
[12] J.J. Huang, C.J. Liu, H.C. Lin, C.J. Tsai, Y.P. Chen, G.R. Hu, C.C. Lee, J. Phys. D: Appl. Phys. 41 (2008) 245502.
[13] Jaehyun Moon, Yong-Hae Kim, Dong-Jin Park, Choong-Heui Chung, Seung-Youl Kang, Jin-Ho Lee, Solid State Electron. 54 (2010) 1326.
[14] G. Neudeck, K. Chung, H. Bare, IEEE Trans. Electron. 4 (1987) 866 Devices ED-34.