Return Loss and Crosstalk Mitigation in Coupled Vias for Modern High-Speed Packaging

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ABSTRACT: A method for mitigating the return loss and crosstalk corresponding to coupled vias is presented in this article. The method is based on selecting the proper dimensions for the antipad holes related to vias as well as the most adequate distribution of the ground vias, which allows to simultaneously reducing impedance mismatch and undesirable via coupling. The usefulness of the method is demonstrated by improving the performance of a 2 $\times$ 3 array of six signal vias. As a result, return loss levels below -45 dB and crosstalk levels below -40 dB are obtained in the 0–50 GHz frequency range. © 2011 Wiley Periodicals, Inc. Int J RF and Microwave CAE 22:224–234, 2012.

Keywords: coupled vias; physics-based circuit model; return loss; crosstalk; high-speed interconnects

1. INTRODUCTION

Modern electronic packaging involves the design of high-speed and low-power interconnects in compact spaces to take advantage of advanced integrated circuit technologies. As a result, packaging approaches based on very fine pitch traces, low-loss dielectric materials, and via structures are being developed as a promissory solution to the problems related to current and future electronic systems [1]. In fact, these packaging approaches must allow the implementation of chip-to-chip links, which must be capable of transmitting digital signals with very short rise/fall times at data rates that are higher than those presented in conventional packages and printed circuit boards (PCBs). Furthermore, transmitting this type of signals represents a challenge because of the signal degradation and distortion introduced by the chip-to-chip link, as the frequency increases. Unfortunately, although vias play a key role in the development of reliable links, these structures are responsible for severe signal integrity problems such as impedance mismatch, crosstalk, mode conversion, and electromagnetic interference [2]. For this reason, much research effort is being dedicated to modeling [3–5] and reducing [6–8] the undesirable effects introduced by via structures in multilayer packages and PCBs. In particular, return loss and crosstalk mitigation in vias is mandatory in modern packaging technologies to avoid signal degradation because of reflections and parasitic coupling.

Nowadays, a common practice for designing PCBs and advanced packages is using full-wave numerical methods to analyze coupled vias by applying the Foldy-Lax approach [9–11]. Although this approach is faster than commercial full-wave simulators, it still requires considerable simulation time, which may be prohibitive in early design stages. Furthermore, simultaneously minimizing the return loss and crosstalk in coupled vias is very hard to achieve based on full-wave approaches due to the difficulty of correlating the geometry and dimensions of these structures with the corresponding electrical properties. Nevertheless, despite these inconveniences, using full-wave solvers as the main tool for analyzing return loss and crosstalk effects in modern packaging is still a common practice, leading to the development of optimization approaches [12]. Alternatively, impedance matching techniques and equivalent circuit models can be used as described in Refs. 13 and 14. Nonetheless, these techniques are restricted to single-ended vias and Ref. 13 may be not suitable for practical applications due to the difficulty of fabricating ellipse-shaped antipad holes. Another problem occurring in PCB and package interconnects is the propagation of parallel-plate waves (PPW) in the cavities formed by the planes in multilayered structures. This problem has been solved by strategically placing ground (GND) vias, which allows reducing crosstalk

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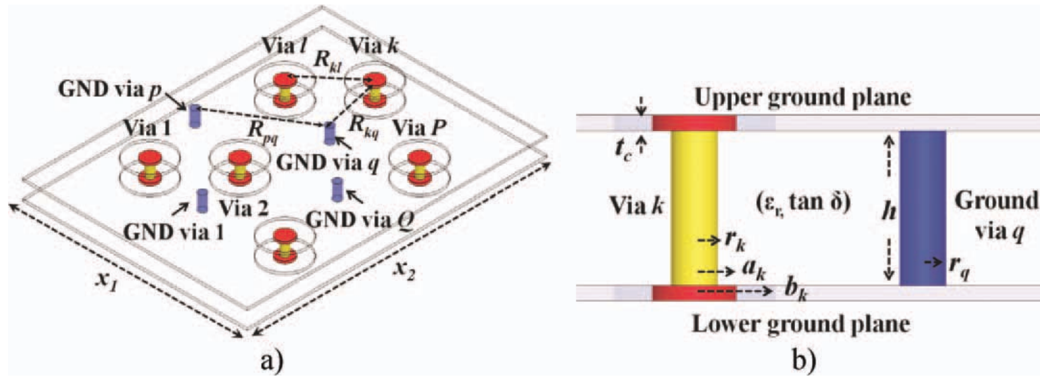

Figure 1 *P* signal vias and *Q* GND vias inside a cavity formed by a parallel-plane pair and the corresponding dimensions: (a) perspective view and (b) lateral view. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com.]

effects due to parasitic PPW propagation [7]. However, the number of necessary GND vias as well as the impact on the corresponding electrical performance is not provided.

Thus, as there is a lack of proposals for mitigating the return loss and crosstalk associated with coupled vias in a systematic and easy way, we propose a method for mitigating these effects in coupled vias. In this regard, we propose a simple and accurate circuit model based on the one reported in Ref. 15 for representing signal vias sharing many GND vias. Furthermore, closed-form expressions for calculating the corresponding circuit parameters are developed. Afterward, a rigorous analysis of the simplified circuit model is carried out to establish the necessary conditions to simultaneously minimize the return loss and crosstalk. These conditions are used to develop a method based on a systematic design of the antipad holes related to vias as well as the corresponding distribution of the GND vias, which leads to minimizing the impedance mismatch and the parasitic coupling. Finally, the proposed method is applied to improve the return loss and crosstalk corresponding to a 2 × 3 array of six signal vias. Results show that the proper design of the antipad holes and the distribution of the GND vias is an effective technique to reduce return loss and crosstalk effects at high frequencies.

2. CIRCUIT MODELING FOR COUPLED VIAS

Vias are widely used to interconnect devices located at different layers in a package and therefore present a multilayer nature. However, to simplify the analysis presented here, we consider the case where vias are embedded between two metal layers, that is, vias crossing a single cavity. The case for vias crossing several metal layers can also be obtained using the proposed technique by sectionalizing the structure and applying cascading concepts. Figure 1a shows *P* signal vias (i.e., used as signal paths) and *Q* GND vias inside a cavity formed by a rectangular parallel-plane pair with dimensions x_1 and x_2. Notice that R_{kl} is the distance separating vias *k* and *l*, R_{kq} is the distance between via *k* and GND via *q*, whereas R_{pq} is the distance separating GND vias *p* and *q*. In addition, Figure 1b shows a side view of Figure 1a, where the barrel, pad, and antipad hole radii corresponding to via *k* are denoted as r_k, a_k, and b_k, respectively, whereas r_q is the radius of the barrel associated with GND via *q*. In this structure, the metal planes present a thickness t_c and are separated by a dielectric layer with a thickness *h*. The dielectric material presents a relative permittivity ε_r, and a loss tangent tan δ.

Before starting with the analysis, it is important to point out the fact that various equivalent circuit models have been reported to simplify the analysis and design of vias in high-speed interconnects. In this regard, one of the main contributions is the development of physics-based models, such as those proposed in Refs. 15–17. Because the circuit elements in these models are associated with physical effects occurring in the structure, there is a correlation between the geometry and disposition of vias with the corresponding electrical properties. This is an important characteristic for a model, because this allows to implement representations that are scalable. A model of this type is presented in this section for coupled vias crossing a single cavity.

A. Circuit Model Topology

Taking into account that the typical dimensions of vias are within the order of micrometers (μm) for modern packaging applications, *h*, r_k, a_k, b_k, R_{kl}, R_{kq}, and R_{pq} can be considered as electrically small in the frequency range of some tens of gigahertz. On the other hand, if signal vias are located away from the edges, and the package has a high count of GND vias, the cavity resonances are small, or even, negligible [8]. In this way, the boundaries due to the finite size of the cavity disappear, and the waves propagating along the cavity are not reflected. Thus, vias can be assumed to be embedded into a circular parallel-plate cavity with infinity radius. Under these conditions, vias in Figure 1a can be modeled using the circuit model depicted in Figure 2, which is a simplified version of the circuit model proposed in Ref. 15.

In the model of Figure 2, each via can be regarded as a two-port π-network coupled to several two-port π-

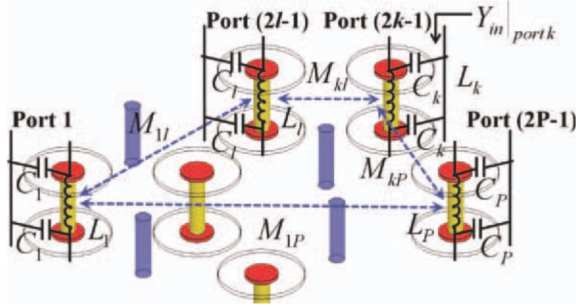

Figure 2 Simplified physics-based circuit model corresponding to vias in Figure 1a. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com.]

networks that represent other vias. For vias within the μm range, the capacitances due to high-order modes (C_v^1) and the zero-order propagating mode (C_v^0) proposed in Ref. 15 can be neglected due to that these are smaller than shunt capacitances. Hence, the capacitance C_k (k =1, 2..., P) is used to model the total electric field distribution around the via k, and this can be calculated as:

$$C_k = C_k^{\mathrm{P}} + C_k^{\mathrm{B}} + C_k^{\mathrm{C}} \tag{1}$$

In this case, C_k^{P} and C_k^{B} are the pad-to-plane and the barrel-to-plane capacitances, respectively, and these are associated with the electric field distribution corresponding to high-order transversal magnetic (TM) modes around the via k, whereas C_k^{C} is the coaxial capacitance component which is due to the coaxial transversal electromagnetic (TEM) mode at the antipad hole. All these capacitances can be calculated using the following expressions [15]:

$$C_k^{\mathrm{P}} = \frac{j4\varepsilon_{\mathrm{r}}\varepsilon_0\pi^2 a_k}{h\ln(b_k/a_k)} \sum_{n=1,3,5\ldots}^{2N-1} [F_n(a_k) - F_n(r_k)] \tag{2}$$

$$C_k^{\mathrm{B}} = \frac{j4\varepsilon_{\mathrm{r}}\varepsilon_0\pi^2 a_k}{h\ln(b_k/a_k)} \sum_{n=1,3,5\ldots}^{2N-1} F_n(r_k) \tag{3}$$

$$C_k^{\mathrm{C}} = \frac{2\pi\varepsilon_{\mathrm{r}}\varepsilon_0 t_{\mathrm{c}}}{\ln(b_k/a_k)} \tag{4}$$

where the functions $F_n(a_k)$ and $F_n(r_k)$ are defined, respectively, as:

$$F_n(a_k) = \frac{W_{10}(k_n a_k, k_n r_k)[W_{10}(k_n\rho_k, k_n b_k) - W_{10}(k_n\rho_k, k_n a_k)]}{k_n(1+\delta_{n0})W_{10}(k_n\rho_k, k_n r_k)} \tag{5}$$

$$F_n(r_k) = \frac{W_{10}(k_n r_k, k_n r_k)[W_{10}(k_n\rho_k, k_n b_k) - W_{10}(k_n\rho_k, k_n r_k)]}{k_n(1+\delta_{n0})W_{10}(k_n\rho_k, k_n r_k)} \tag{6}$$

In these equations, ρ_k is an auxiliary parameter which defines a circular virtual boundary around via k that is used to include the significant TM modes in the capacitance calculation, $k_n = \sqrt{k_0^2\mu_0\varepsilon_0\varepsilon_r - \left(\frac{n\pi}{h}\right)^2}$ is the radial wavenumber, n is the mode number, δ_{n0} is the Kronecker delta, and $W_{10}(x, y)$ is an auxiliary function defined as the determinant of the zero and first Bessel functions, $J_0(y)$ and $J_1(x)$, and the zero and first second-order Hankel functions, $H_0^{(2)}(y)$ and $H_1^{(2)}(x)$:

$$W_{10}(x,y) = \begin{vmatrix} J_1(x) & J_0(y) \\ H_1^{(2)}(x) & H_0^{(2)}(y) \end{vmatrix} \tag{7}$$

In the case of vias without pads (i.e., when $a_k = r_k$), the pad-to-plane capacitance C_k^{P} is negligible. Therefore, C_k is reduced to the sum of the capacitances expressed in eqs. (3) and (4).

On the other hand, because h, R_{kl}, R_{kq}, and R_{pq} are features electrically short, all high-order TM waves are evanescent and well-confined inside the boundary defined by ρ_k. Therefore, the inductance L_k (k =1, 2..., P) can be used to represent the total magnetic field distribution around the via k, whereas the mutual inductance M_{kl} can be used to model the coupling between the via k and the via l due to the propagation of the zero-order TM mode in the parallel-plane pair. In this case, L_k can be computed as:

$$L_k = 2L_k^{\mathrm{P}} + L_k^{\mathrm{V}} \tag{8}$$

where L_k^{P} is the inductance due to the coaxial TEM mode at the antipad hole of the via k, and this can be found using the expression for the per-unit-length inductance of a coaxial transmission line:

$$L_k^{\mathrm{P}} = \frac{\mu_0 t_{\mathrm{c}} \ln(b_k/a_k)}{2\pi} \tag{9}$$

and L_k^{V} is an equivalent inductance which takes into account the inductance due to the via k as well as the spatial distribution of Q GND vias around it. To illustrate how L_k^{V} and M_{kl} are calculated, consider the via k and the via l sharing Q GND vias as depicted in Figure 3. Notice that the currents I_k and I_l are injected at the upper ports ($2k - 1$) and ($2l - 1$), respectively, and these currents travel along the barrels of the via k and the via l,

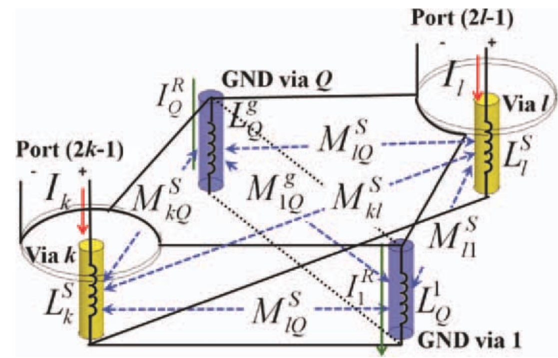

Figure 3 Two signal vias sharing Q GND vias and the related self and mutual inductances. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com.]

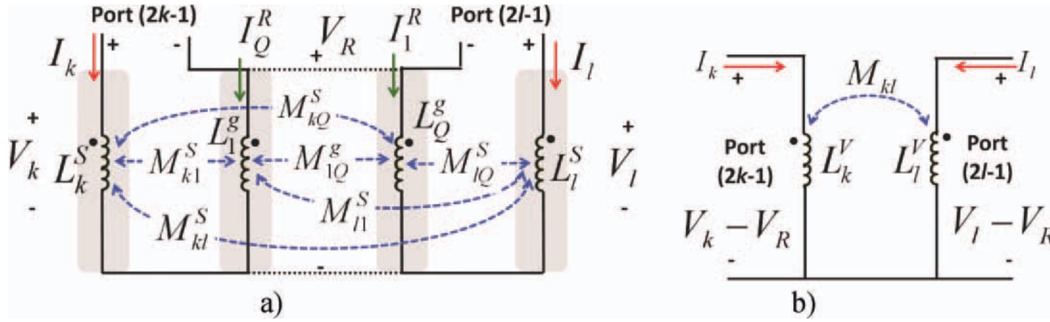

Figure 4 (a) Circuit model for two vias sharing Q GND vias and (b) combination of Q GND vias and two vias into two self inductances and one mutual inductance. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com.]

originating the inductances L_k^{S} and L_l^{S} as well as the mutual inductance M_{kl}^{S}. If vias are located away from the edges of the cavity, the following closed-form expressions can be used to find L_k^{S}, L_l^{S}, and M_{kl}^{S} [18]:

$$L_{k,l}^{\mathrm{S}} = \frac{\mu_0 h}{2\pi}\left[\ln\left(\frac{x_1+x_2}{4(r_{k,l})}\right) - 0.75\right] \tag{10}$$

$$M_{kl}^{\mathrm{S}} = \frac{\mu d}{2\pi}\left[\ln\left(\frac{x_1+x_2}{4(R_{kl}+r_l)}\right) - 0.75\right] \tag{11}$$

Due to the fact that GND vias provide a low-impedance return path for the injected currents at the upper ports, these currents return throughout the GND vias originating the inductances $L_{\mathrm{q}}^{\mathrm{g}}$ ($q = 1, 2, \ldots, Q$), the mutual inductances M_{kq}^{S} (between via k and the GND vias), the mutual inductances M_{lq}^{S} (between via l and the GND vias), and the mutual inductances M_{pq}^{g} (between GND vias). Replacing r_k by r_q in eq. (10) and R_{kl} by R_{kq}, R_{lq}, and R_{pq} in eq. (12), $L_{\mathrm{q}}^{\mathrm{g}}$, M_{kq}^{S}, M_{lq}^{S}, and M_{pq}^{g} can be calculated. Continuing with the analysis, the circuit in Figure 3 can be rearranged as shown in Figure 4a, which indicates that the voltages across the inductances associated with the GND vias are the same (marked as V_{R} in the figure). Therefore, the currents and voltages at the defined inductances can be related through the following matrix equation:

$$j\omega\begin{bmatrix} I_k \\ I_l \\ I_1^R \\ \vdots \\ I_Q^R \end{bmatrix} = \begin{bmatrix} B_{11}^{kl} & B_{12}^{kl} & B_{13}^{kl} & \ldots & B_{1(Q+2)}^{kl} \\ B_{21}^{kl} & B_{22}^{kl} & B_{23}^{kl} & \ldots & B_{2(Q+2)}^{kl} \\ B_{31}^{kl} & B_{32}^{kl} & B_{33}^{kl} & \ldots & B_{3(Q+2)}^{kl} \\ \vdots & \vdots & \vdots & \ldots & \vdots \\ B_{(Q+2)1}^{kl} & B_{(Q+2)2}^{kl} & B_{(Q+2)3}^{kl} & \ldots & B_{(Q+2)(Q+2)}^{kl} \end{bmatrix}\begin{bmatrix} V_k \\ V_l \\ V_R \\ \vdots \\ V_R \end{bmatrix} \tag{12}$$

where the matrix $\mathbf{B}^{kl}$ is given as:

$$\mathbf{B}^{kl} = \begin{bmatrix} L_k^{\mathrm{S}} & M_{kl}^{\mathrm{S}} & M_{k1}^{\mathrm{S}} & M_{k2}^{\mathrm{S}} & \ldots & M_{kQ}^{\mathrm{S}} \\ M_{kl}^{\mathrm{S}} & L_l^{\mathrm{S}} & M_{l1}^{\mathrm{S}} & M_{l2}^{\mathrm{S}} & \ldots & M_{lQ}^{\mathrm{S}} \\ M_{k1}^{\mathrm{S}} & M_{l1}^{\mathrm{S}} & L_1^{\mathrm{g}} & M_{l2}^{\mathrm{g}} & \ldots & M_{lQ}^{\mathrm{g}} \\ M_{k2}^{\mathrm{S}} & M_{l2}^{\mathrm{S}} & M_{l2}^{\mathrm{g}} & L_2^{\mathrm{g}} & \ldots & M_{l2}^{\mathrm{g}} \\ \vdots & \vdots & \vdots & \vdots & \ldots & \vdots \\ M_{kQ}^{\mathrm{S}} & M_{lQ}^{\mathrm{S}} & M_{lQ}^{\mathrm{g}} & M_{2Q}^{\mathrm{g}} & \ldots & L_Q^{\mathrm{g}} \end{bmatrix}^{-1} \tag{13}$$

Because the voltage is the same for every GND via and the total current flowing through the GND vias is the return current, that is, $I_R = \sum_{i=0}^{Q} I_i^R = -(I_k + I_l)$, eq. (12) can be simplified to:

$$j\omega\begin{bmatrix} I_k \\ I_l \\ I_R \end{bmatrix} = \begin{bmatrix} B_{11}^{kl} & B_{12}^{kl} & \sum_{j=3}^{Q+2} B_{1j}^{k} \\ B_{21}^{kl} & B_{22}^{kl} & \sum_{j=2}^{Q+2} B_{1j}^{kl} \\ \sum_{j=3}^{Q+2} B_{j1}^{kl} & \sum_{j=3}^{Q+2} B_{j2}^{kl} & \sum_{i=3}^{Q+2}\sum_{j=3}^{Q+2} B_{ij}^{k} \end{bmatrix}\begin{bmatrix} V_k \\ V_l \\ V_R \end{bmatrix} \tag{14}$$

By inverting the 3 × 3 matrix in eq. (14), eq. (12) can be rewritten as:

$$\begin{bmatrix} V_k \\ V_l \\ V_R \end{bmatrix} = j\omega\begin{bmatrix} L_{eq_11}^{kl} & L_{eq_12}^{kl} & L_{eq_13}^{kl} \\ L_{eq_21}^{kl} & L_{eq_22}^{kl} & L_{eq_23}^{kl} \\ L_{eq_31}^{kl} & L_{eq_32}^{kl} & L_{eq_33}^{kl} \end{bmatrix}\begin{bmatrix} I_k \\ I_l \\ I_R \end{bmatrix} \tag{15}$$

where

$$\begin{bmatrix} L_{eq_11}^{kl} & L_{eq_12}^{kl} & L_{eq_13}^{kl} \\ L_{eq_21}^{kl} & L_{eq_22}^{kl} & L_{eq_23}^{kl} \\ L_{eq_31}^{kl} & L_{eq_32}^{kl} & L_{eq_33}^{kl} \end{bmatrix} = \begin{bmatrix} B_{11}^{kl} & B_{12}^{kl} & \sum_{j=3}^{Q+2} B_{1j}^{k} \\ B_{21}^{kl} & B_{22}^{kl} & \sum_{j=2}^{Q+2} B_{1j}^{kl} \\ \sum_{j=3}^{Q+2} B_{j1}^{kl} & \sum_{j=3}^{Q+2} B_{j2}^{kl} & \sum_{i=3}^{Q+2}\sum_{j=3}^{Q+2} B_{ij}^{k} \end{bmatrix}^{-1} \tag{16}$$

In this way, the contributions of the Q GND vias that share the return current are combined, and the $(Q + 2) \times (Q + 2)$ inductance matrix in eq. (13) is transformed into a

3×3 equivalent inductance matrix in eq. (16). Thus, the circuit in Figure 4a can be simplified to the circuit depicted in Figure 4b. Consequently, eq. (15) can be reduced to:

$$\begin{bmatrix} V_k - V_R \\ V_l - V_R \end{bmatrix} = j\omega \begin{bmatrix} L_k^{\rm V} & M_{kl} \\ M_{kl} & L_l^{\rm V} \end{bmatrix} \begin{bmatrix} I_k \\ I_l \end{bmatrix} \tag{17}$$

where

$$L_k^{\rm V} = L_{eq_11}^{kl} + L_{eq_33}^{kl} - L_{eq_31}^{kl} - L_{eq_13}^{kl} \tag{18}$$

$$L_l^{\rm V} = L_{eq_22}^{kl} + L_{eq_33}^{kl} - L_{eq_23}^{kl} - L_{eq_32}^{kl} \tag{19}$$

$$M_{kl} = L_{eq_12}^{kl} + L_{eq_33}^{kl} - L_{eq_32}^{kl} - L_{eq_13}^{kl} \tag{20}$$

In this case, $L_k^{\rm V}$, $L_l^{\rm V}$, and M_{kl} denote the equivalent self inductance associated with the via k, the equivalent self inductance associated with the via l, and the equivalent mutual inductance between the via k and the via l, respectively. For the case of vias without pads, the inductance given in eq. (9) must be calculated replacing a_k by r_k As mentioned before, circuit models for multilayer vias can be obtained using the circuit model for a single cavity in Figure 2 considering that multilayer vias are composed by many cascaded cavities.

3. CONDITIONS FOR MINIMIZING THE RETURN LOSS AND CROSSTALK

The circuit model developed in the previous section provides means of relating geometry parameters with electrical properties. This fact allows finding the necessary conditions for analytically minimizing the return loss and crosstalk. In accordance with Figure 2, the return loss at the upper port corresponding to the via k can be written as:

$$S_{(2k-1)(2k-1)} = \frac{\left(1/Y_{\rm in}|_{{\rm port}k}\right) - Z_0}{\left(1/Y_{\rm in}|_{{\rm port}k}\right) + Z_0} \tag{21}$$

where $Y_{\rm in}|_{{\rm port}\ k}$ is the input admittance seen at port $2k - 1$ when an impedance $Z_{\rm L}$ is connected at the port $2k$, whereas Z_0 is the reference impedance associated with the network ports. The input admittance $Y_{\rm in}|_{{\rm port}\ k}$ can be found by shorting the remaining ports in Figure 2. Therefore, when a current is injected at the port $2k - 1$, it returns throughout the inductances associated with the remaining vias. Considering $Z_{\rm L} = Z_0$, the circuit model in Figure 2 can be simplified into a two-port network (using a similar procedure as that described in Section 2) as shown in Figure 5. In this case, L_k^e is the effective inductance seen at port $2k - 1$ given as:

$$L_k^e = L_{eq_11}^{k} + L_{eq_22}^{k} - L_{eq_21}^{k} - L_{eq_12}^{k} \tag{22}$$

where the elements L_{eqij}^k are determined using the following equations:

$$\begin{bmatrix} L_{eq_11}^k & L_{eq_12}^k \\ L_{eq_21}^k & L_{eq_22}^k \end{bmatrix} = \begin{bmatrix} B_{11}^k & \sum_{j=2}^{\rm P} B_{1j}^k \\ \sum_{j=2}^{\rm P} B_{j1}^k & \sum_{i=2}^{\rm P}\sum_{j=2}^{\rm P} B_{ij}^k \end{bmatrix}^{-1} \tag{23}$$

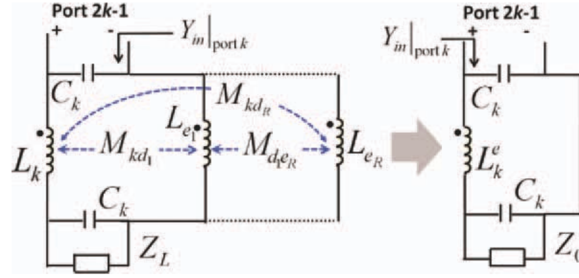

Figure 5 Circuit model for calculating the input impedance $Y_{\rm in}|_{{\rm port}\ k}$ at port $2k - 1$ and the corresponding simplification. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com.]

$$\mathbf{B^k} = \begin{bmatrix} L_k & M_{kd_1} & M_{kd_2} & \dots & M_{kd_{\rm R}} \\ M_{d_1k} & L_{d_1} & M_{d_1e_1} & \dots & M_{d_1e_{\rm R}} \\ M_{d_2k} & M_{e_1d_1} & L_{d_2} & \dots & M_{d_2e_{\rm R}} \\ \vdots & \vdots & \vdots & \dots & \vdots \\ M_{d_Rk} & M_{e_Rd_1} & M_{e_Rd_2} & \dots & L_{d_R} \end{bmatrix}^{-1} \tag{24}$$

In this case, $\mathbf{B^k}$ is a $P \times P$ matrix with subindexes defined as $\{d_1,\ldots, d_R\} = \{e_1,\ldots, e_R\} \in \{1,2,\ldots,P\} - \{k\}$. Taking into consideration that the port impedance Z_0 is purely real, accordingly to Figure 5 the input admittance $Y_{\rm in}|_{{\rm port}\ k}$ is found to be:

$$Y_{\rm in}|_{{\rm port}k} = j\omega C_k + \frac{(1/Z_0) + j\omega C_k}{1 - \omega^2 C_k L_k^e + j\omega L_k^e (1/Z_0)} \tag{25}$$

Then, substituting eq. (25) into eq. (21) and after several mathematical manipulations, the magnitude of the return loss corresponding to the via k can be expressed as:

$$\left|S_{(2k-1)(2k-1)}\right| = \sqrt{1 - \frac{4\left(b_4^k\omega^4 + b_2^k\omega^2 + 1\right)}{\left(b_4^k\omega^4 + b_2^k\omega^2 + 2\right)^2 + \left(a_5^k\omega^5 + a_3^k\omega^3 + a_1^k\omega\right)_k^2}} \tag{26}$$

where

$$b_4^k = \left(L_k^e C_k\right)^2 \tag{27}$$

$$b_2^k = L_k^e\left(L_k^e/Z_0^2 - 2C_k\right) \tag{28}$$

$$a_1^k = Z_0\left(2C_k - L_k^e/Z_0^2\right) \tag{29}$$

$$a_3^k = Z_0 L_k^e\left(L_k^e C_k/Z_0^2 - 3C_k^2\right) \tag{30}$$

$$a_5^k = Z_0\left(L_k^e\right)^2 C_k^3 \tag{31}$$

From eq. (26), it is clear that the return loss at via k vanishes at all frequencies if the following condition is satisfied:

$$\frac{4\left(b_4^k\omega^4 + b_2^k\omega^2 + 1\right)}{\left(b_4^k\omega^4 + b_2^k\omega^2 + 2\right)^2 + \left(a_5^k\omega^5 + a_3^k\omega^3 + a_1^k\omega\right)^2} = 1 \tag{32}$$

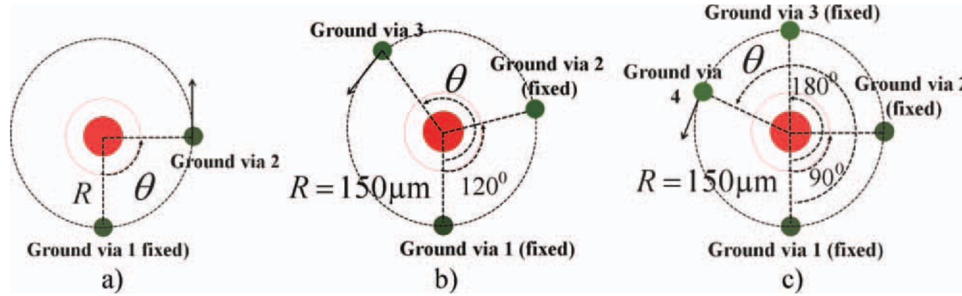

Figure 6 Test structures to investigate the impact of the number of GND vias and the corresponding spatial distribution in the value of L_k: (a) two GND vias, (b) three GND vias, and (c) four GND vias. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com.]

Bearing in mind that vias in modern packaging present dimensions within the μm range, the coefficients in eqs. (27) and (28) can be ignored, because C_k and L_k^e present values of femtofarads (fF) and picohenries (pH), respectively. Thus, the condition for zero return loss at via k in eq. (32) can be rewritten as:

$$a_5^k\omega^5 + a_3^k\omega^3 + a_1^k\omega = 0 \tag{33}$$

Notice that eq. (33) is satisfied at all frequencies, if coefficients in eqs. (29)–(31) are equal to zero. Obviously, this is the ideal case, when C_k and L_k^e are equal to zero, which is not possible in practice due to the parasitics associated with the via k. Although eqs. (29)–(31) cannot be set to zero simultaneously, an acceptable reduction in the return loss is obtained, when eq. (29) is equated to zero. In this case, the well-known impedance matching equation is obtained [13, 14]:

$$\sqrt{L_k^e/2C_k} = Z_0 \tag{34}$$

The left member in eq. (34) can be seen as the equivalent impedance Z_k^e related to via k including coupling effects. When Z_k^e is equal to Z_0, impedance matching is achieved and the return loss of the via k is minimized in a determined bandwidth. Nevertheless, for high-speed packaging applications, this bandwidth may not be enough to avoid signal distortion due to reflection noise. This is because digital signals with very short rise/fall times have a wide spectrum with high-frequency harmonics. Consequently, the return loss has to be minimized in a wide bandwidth to avoid distortion due to high-frequency harmonics. From eq. (33), it is clear that the bandwidth where return loss is minimized can be extended, if coefficients in eqs. (30) and (31) are reduced as much as possible, while eq. (34) is fulfilled. Because eqs. (30) and (31) depend on L_k^e, these coefficients can be minimized if L_k^e is reduced. Hence, impedance matching as well as minimization of L_k^e must be simultaneously carried out to extend the bandwidth where return loss is mitigated.

Finally, the condition for minimizing the crosstalk effect in coupled vias can be derived using Figure 2. In accordance with this figure, the magnitude of the near-end crosstalk (NEXT) between the signal via k and the signal via l is given as:

$$\left|S_{(2k-1)(2l-1)}\right| = \frac{\omega M_{kl}}{2Z_0} \tag{35}$$

From eq. (35), it is clear that the magnitude of NEXT between the via k and the via l vanishes at all frequencies, if the mutual inductances M_{kl} are equal to zero. Unfortunately, due to the fact that in practice M_{kl} is different from zero; crosstalk mitigation is carried out by reducing M_{kl} as much as possible.

4. METHOD DESCRIPTION

As previously mentioned, return loss and crosstalk can be mitigated, if impedance matching and minimization of L_k^e and M_{kl} are simultaneously achieved. As C_k, L_k^e, and M_{kl} depend on the geometric features of vias as well as on the material properties, impedance matching and the minimization of L_k^e and M_{kl} can be performed for particular materials by systematically selecting an appropriate geometry for the vias as well as the number of GND vias. In other words, the design parameters are ε_r, tan δ, h, r_k, r_q, a_k, b_k, t_c, R_{kl}, R_{kq}, R_{pq}, and Q. Ideally, any parameter related to geometry can be changed to obtain the adequate values for C_k, L_k^e, and M_{kl}. However, there are limited features of the geometry corresponding to the vias that can be easily changed. For instance, h determines the height of the cavity and therefore the height for vias and GND vias is the same, R_{kl} is determined by the pitch in the escape routing area of ball-grid-array packages, a_k is regulated by the dimensions of the solder balls, and r_k and r_q values are restricted by the manufacturing process. Thus, the parameters that can be easily changed are b_k, R_{kq}, R_{pq} and Q (which are related to the antipad holes and the GND via distribution).

From eqs. (2)–(4), it is clear that C_k can be set to a desired value by changing b_k. Thus, C_k can be reduced/increased, if b_k is increased/reduced. On the other hand, in accordance with eqs. (22)–(24), L_k^e depends on the values corresponding to L_k and M_{kl}, and therefore, L_k^e depends on b_k, R_{kq}, R_{pq}, and Q. From eq. (8), it is clear that L_k includes the effect of L_k^{P} and L_k^{V}, and because L_k^{P} is

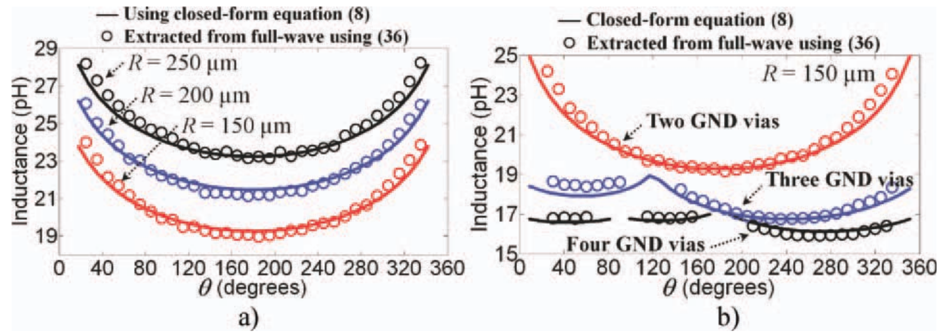

Figure 7 L_k versus θ and R for the test structures shown in: (a) Figure 6a and (b) Figures 6b and 6c. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com.]

inversely proportional to C_k as can be seen in eq. (9), the only way to reduce L_k^e is by means of reducing L_k^V (which depends on R_{kq}, R_{pq}, and Q). Now, to investigate how the GND via distribution affects the value corresponding to L_k and therefore L_k^e, consider the via k with two GND vias disposed in a circle with a radius R as shown Figure 6a, where the via l is placed far away from the via k. The corresponding dimensions for h, a_k, b_k, r_k, and r_q are 30, 54, 104, 26, and 26 μm, respectively. The material properties for this structure are $\varepsilon_r = 3.4$ and $\tan\delta = 0.02$, both at 1 GHz. Notice that the GND via 1 is fixed, whereas location of the GND via 2 depends on the angle θ. Closed-form equations provided in Section 2 were used to calculate L_k as a function of θ and R. Additionally, L_k was determined using full-wave simulations to assess the accuracy of the developed closed-form expressions. In this case, L_k is extracted from simulation results using the following expression:

$$L_k = \frac{1/\mathrm{Im}(Y_{21})}{2\pi f_r} \tag{36}$$

where Y_{21} is the admittance parameter from port 1 to port 2 (these ports are located at the top and bottom antipad holes of the via k) and f_r is the frequency at which Y_{21} is calculated. L_k as a function of θ is plotted in Figure 7a for $R = 250$, 200, and 150 μm, respectively. As can be seen, eq. (8) predicts very well the value of L_k extracted from full-wave simulations with $f_r = 1$ GHz). In this case, L_k decreases as θ increases, because the mutual inductance between GND vias 1 and 2 decreases. Thus, when the two GND vias are on opposite sides (i.e., θ = 180°) L_k is minimized. On the other hand, when R decreases the mutual inductance between the signal via and the two GND vias increases, decreasing L_k. Because L_k^e needs to be minimized to extend the bandwidth where the return loss effect is mitigated, Figure 7a suggests that GND vias need to be placed in opposite sides and close to the signal via as much as possible to minimize L_k^e. To corroborate this fact, consider the same structure in Figure 6a but now with three and four GND vias disposed in a circle with a radius $R = 150$ μm, which is shown in Figures 6b and 6c. Figure 7b shows L_k calculated using eq. (8) and extracted from full-wave simulations. As can be seen, excellent agreement between the two approaches is achieved. Notice that the curve corresponding to L_k for three GND vias presents a discontinuity from 90 to 150°. This is because at these angles, GND vias 2 and 3 intersect between them, and therefore, this angle range was excluded from the L_k calculation. A similar situation occurs for the curve corresponding to L_k for four GND vias. In accordance with Figure 7, by adding extra-GND vias at opposite sides, L_k is considerably reduced. If GND vias cannot be placed at opposite sides due to either design or layout restrictions, these must be placed away from each other as much as possible to reduce the mutual inductance between GND vias.

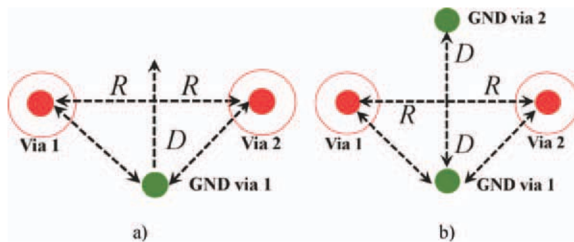

Figure 8 Test structures to investigate the impact of the number of GND vias and the corresponding spatial distribution in the value of M_{kl}: (a) one GND via and (b) two GND. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com.]

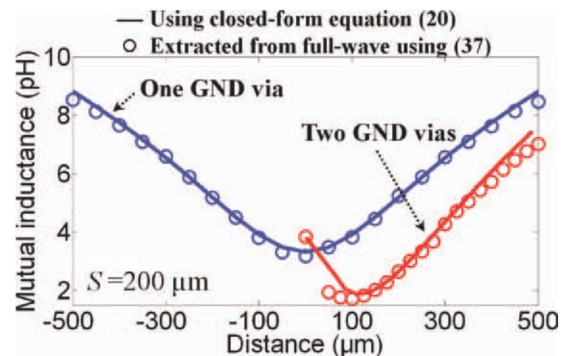

Figure 9 M_{kl} versus D for the test structures in Figure 8a and Figure 8b. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com.]

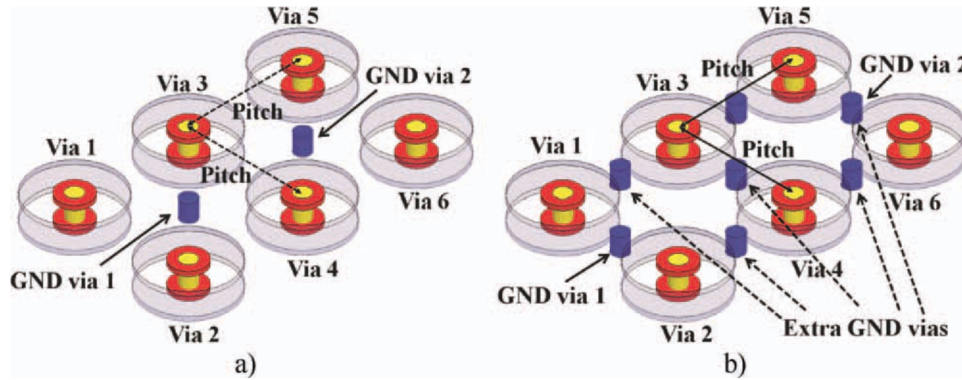

Figure 10 Six signal vias disposed in a 2 × 3 array with (a) two GND vias and (b) seven GND vias. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com.]

Additionally, the number and distribution of GND vias between via k and via l determine the value corresponding to M_{kl} in accordance with eq. (20). Thus, to investigate how the distribution of GND vias can be used to minimize M_{kl}, consider two vias with one GND via placed as shown Figure 8a and two vias with two GND vias located as shown in Figure 8b. The parameters h, a_k, b_k, r_k, and r_q for these structures are the same as those shown in Figure 6a, with $R = 200$ μm. In the case of the analysis based on Figure 8a, the distance D is varied from -500 to 500 μm, whereas D in Figure 8b is varied from 0 to 500 μm. M_{kl} between the two vias, in both cases, was calculated using eq. (20). Additionally, to assess the accuracy of eq. (20), M_{kl} was extracted from full-wave simulations using:

$$M_{kl} = \frac{Z_0 \mathrm{Im}(S_{kl})}{\pi f_r} \tag{37}$$

where the port k and port l are located at the top of the via k and the top of the via l, respectively, and f_r is the frequency at which S_{21} is computed. Figure 9 shows M_{kl} as a function of D. As can be noticed, closed-form eq. (20) predicts very well the value of M_{kl} extracted from full-wave simulations. According to Figure 9, one GND via placed between the two vias reduces M_{kl}. Furthermore, adding extra-GND vias close to both vias reduces M_{kl}. Thus, double benefit is obtained when GND vias distribution is carefully designed, because minimization of L_k^e and M_{kl} can be simultaneously carried out.

Based on the previous results and on the fact that the antipad holes and the GND via distribution are the features that can be easily modified to achieve impedance matching as well as the minimization of L_k^e and M_{kl}, a systematic method for finding the geometry which simultaneously provides return loss and crosstalk mitigation can be resumed in the following steps:

1. Considering that the geometry features related to vias h, r_k, r_q, a_k, t_c, R_{kl}, and Q are fixed parameters, calculate C_k, L_k^e, and M_{kl} using eqs. (1), (22), and (20), respectively; determine also b_k that satisfies impedance matching (notice that M_{kl} are independent of b_k). The resulting values are called b_k*, C_k*, L_k^e*, and M_{kl}*.
2. Determine the return loss and crosstalk using eqs. (26) and (35) with C_k*, L_k^e*, and M_{kl}*. If the level of return loss and crosstalk is satisfactory within the desired bandwidth go to Step 4, otherwise go to Step 3.
3. Add extra-GND vias (distant from each other) around vias to reduce L_k^e, and M_{kl}. Afterward, calculate C_k, L_k^e, and M_{kl} using eqs. (1), (22), and (20), respectively; determine the new value of b_k* that satisfies eq. (34).

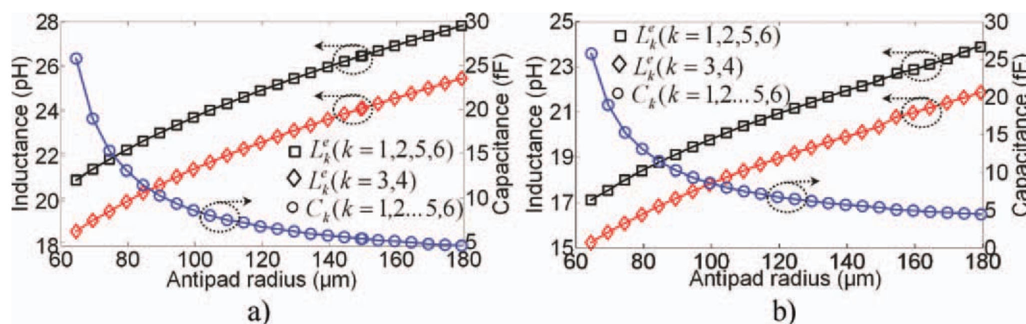

Figure 11 C_k and L_k^e corresponding to vias depicted in (a) Figure 10a and (b) Figure 10b. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com.]

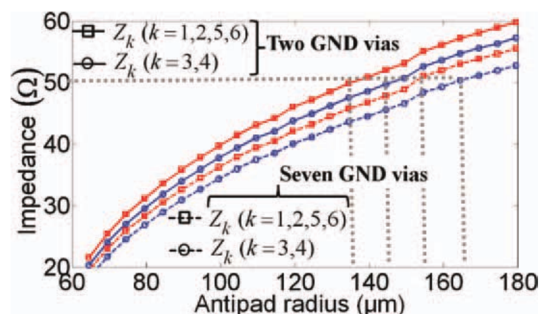

Figure 12 Equivalent impedance Z_k^e corresponding to vias depicted in Figure 10. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com.]

Modify the old values for C_k* and L_k^e* with the new values and go to Step 2.

4. Perform a full-wave simulation of the optimized geometry (h, r_k, r_q, a_k, b_k*, t_c, and Q) to verify the results. Taking into consideration that b_k* can be an approximated value, fine tuning may be required to determine final values.

5. EXAMPLE AND DISCUSSION

To demonstrate the concepts discussed throughout this article, the return loss and crosstalk mitigation corresponding to a 2 × 3 array of six vias (as shown in Fig. 10a) was carried out by applying the method described in the previous section. The dimensions h, r_k, r_q, a_k, t_c, and R_{kl} are 30, 26, 26, 54, 15, and 400 μm for k = 1, 2,…, 6, respectively. Regarding to material properties, the dielectric material presents a dielectric constant $\varepsilon_r = 3.4$ and loss tangent $\tan\delta = 0.02$ (both at 1 GHz), whereas copper is used for the GND planes. These vias are intended to transmit high-speed signals in a 50-Ω system (i.e., $Z_0 = 50$ Ω) and the following specifications are given: return loss <−40 dB and crosstalk <−30 dB, both in the 0–50 GHz range.

First, L_k^e, C_k, and M_{kl} corresponding to vias in Figure 10a were calculated for b_k within 64–180 μm range (see Fig. 11a). As can be seen in Figure 10a, C_k is reduced if b_k is increased, whereas L_k^e increases when b_k increases (due to the pad inductance L_k^{P} which depends on b_k). Also, notice that L_k^e for vias located at the center (k = 3,4) is lower than L_k^e for vias located at the corner edges (k = 1, 2, 5, and 6). This is because the vias at the center have the GND vias closer than vias at the corner edges, and therefore, L_k^e is smaller. On the other hand, because M_{kl} is included in L_k^e, and this value is independent of b_k, these values are not plotted (consider the value corresponding to M_{12} = 6.8 pH as an example). The equivalent impedance Z_k^e for each via was calculated using eq. (34) and thus, b_k* to obtain impedance matching was determined. From Figure 12, notice that b_k* = 135 μm for vias located at the corner edges and b_k* = 145 μm for vias located at the center. Afterward, return loss and crosstalk for each via were determined using eqs. (26) and (35). In this case, specifications are not fulfilled.

Because the return loss and crosstalk specifications are not fulfilled, five GND vias were added to the vias in Figure 10a, as shown in Figure 10b. In this case, L_k^e and C_k are plotted in Figure 10b and as can be seen, L_k^e is reduced with respect to L_k^e plotted in Figure 10a; in addition, M_{12} was reduced from 6.8 to 2.5 pH. Afterward, Z_k^e for the signal vias with seven GND vias was calculated and plotted in Figure 12. As can be seen, for signal vias with seven GND vias, the new values for the antipad radius at which impedance matching is achieved are: (1) b_k* = 155 μm for vias located at the corner and (2) b_k* = 165 μm for vias located at the center. Again using eqs. (26) and (35), return loss and crosstalk were calculated, and at this time, the specifications are fulfilled.

As a final step, 3D models for vias with two and seven GND vias using the optimized geometry were implemented and simulated in Ansoft's HFSS 11 within the 0–50 GHz frequency range to corroborate previous results. Additionally, a 3D model for vias with two GND vias and b_k = 50 μm was simulated. The magnitude of the return loss for vias in the corner edges as well as the return loss for vias in center is plotted in Figure 13. As can be noticed, the return loss for vias with two GND vias and b_k = 50 μm is higher than the return loss for vias with two GND vias and b_k* = 135 and 145 μm, because impedance matching is achieved in the second case. On the other hand, although vias with two GND vias and b_k* = 135 and 145 μm significantly reduce the return loss, the vias with seven vias (b_k* = 155 and 165 μm) provide a better performance compared with the first one. This is

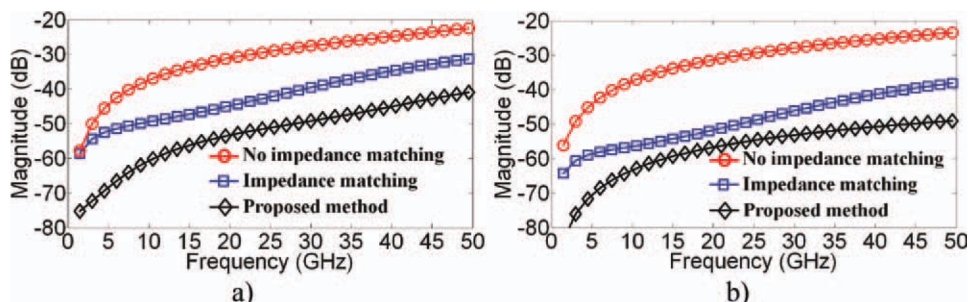

Figure 13 Magnitude of the return loss corresponding to (a) vias at the edge corners and (b) vias at center of the array. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com.]

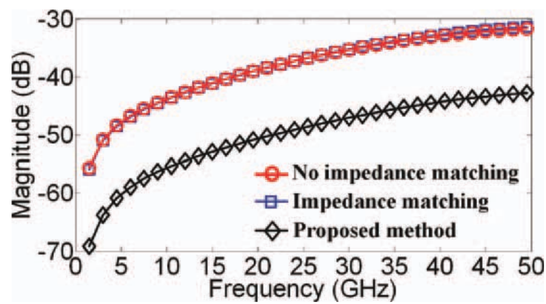

Figure 14 Magnitude of NEXT between vias 1 and 3. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com.]

because L_k^e was reduced using additional GND vias, and therefore, better matching impedance is achieved in a wider frequency range than for the case with signal vias with two GND vias. The results for the latter case are: reflection-loss lower than -40 dB for vias at the corner edges and -50 dB for vias at the center; both in 0–50 GHz frequency.

Finally, the magnitude of NEXT between via 3 (located at the center of the array) and via 1 (located at the left corner) is plotted in Figure 14. Although vias with two GND vias and $b_k* = 135$ and 145 μm reduce the return loss by impedance matching NEXT is not reduced. Conversely, for vias with seven GND vias and $b_k* = 155$ and 165 μm, the return loss as well as NEXT are reduced about 10 dB compared to vias with two GND vias. This is because by adding GND vias close to signal vias, the value corresponding to M_{12} and the impedance mismatch are reduced at high frequencies.

6. CONCLUSIONS

A method for mitigating the return loss and crosstalk in coupled vias has been presented. For this purpose, a simply physics-based circuit model was developed to represent coupled vias inside a cavity and the corresponding GND via distribution to establish the necessary conditions for simultaneously mitigating the return loss and crosstalk effects. From the analysis presented in Section 3, it is clear that the bandwidth where return loss and crosstalk is mitigated can be extended by means of reducing the effective inductance value seen at each via as well as by reducing the mutual inductance between vias in addition to impedance matching. As it was demonstrated, reduction of the effective value seen at each via and mutual inductance between vias can be simultaneously performed by adding GND vias.

The proposed method was applied to a 2 × 3 via array to improve its performance. The results show that a careful design of the antipad holes as well as the GND via distribution in coupled vias is a powerful technique to reduce the return loss and crosstalk at high frequencies. Finally, the method can be extended to arbitrary number of vias bearing in mind that the height and the distance between them are electrically short. Because the method is based on closed-form equations, this can be used in early design stages of chip-to-chip links to optimize the electrical performance in a fast and straightforward way.

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