Modeling and Parameter Extraction of Test Fixtures for MOSFET On-Wafer Measurements up to 60 GHz

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ABSTRACT: We present a circuit model and parameter determination methodology for test fixtures used for on-wafer S-parameter measurements on CMOS devices. The model incorporates the frequency dependence of the series resistances and inductances due to the skin effect occurring in the metal pads. Physically based representations for this effect allow for excellent theory-experiment correlations for different dummy structures, as well as when de-embedding transistor measurements up to 60 GHz. © 2012 Wiley Periodicals, Inc. Int J RF and Microwave CAE 23:655–661, 2013.

Keywords: RF-measurements; S-parameters; test fixtures; equivalent circuit modeling; CMOS devices

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I. INTRODUCTION

The characterization and modeling of microwave devices require high-frequency on-wafer measurements. In this case, to make a connection with the probe tips and to apply the RF stimulus to the device under test (DUT), a test fixture is necessary. This introduces considerable parasitic effects between the calibrated reference plane and the DUT, which have a high impact on the quality of the RF measurements. Generally, the parasitic effects of the test fixture are removed from the experimental data using a de-embedding procedure. This is based on the separate measurement of a set of dummy structures (e.g., open, short and through dummies) and then removing the corresponding effects from a complete structure, that is, including the DUT [1–3]. Therefore, the efficiency of these methods is linked to the quality of test fixtures used for the characterization of microwave devices [4].

Additionally, it is important to mention that when measuring dummy structures (e.g., open circuited dummies), substantial noise may be present at high frequencies as measurement uncertainty increases as the impedance of the measured structure becomes higher [5, 6]. Thus, understanding the physical origin of the parasitics for a more complete knowledge of the influence of the test structures on the measurements is needed. This is especially important to define the frequency range up to where the test fixture is practical, to optimize the layout design of the pads, and to evaluate the sensitivity of specific DUT model parameters to a particular de-embedding method.

Approaches such as modeling the probe pads, interconnections, and DUT in a cascade configuration have been proposed, and these aim at identifying and removing the parasitic effects from raw measurements [7]. However, the origin of the parasitics or their relation to the embedding network layout is not possible using these techniques. The relation with the physical structure is more evident when the unwanted effects of the test fixtures are modeled separating their influence in impedance (Z) and admittance (Y) blocks, a methodology which in turn has allowed for a deeper understanding of these high frequency effects through the development of equivalent circuit models [8, 9].

Nevertheless, most of these models consist of frequency independent circuit elements, and the modeling of crucial high frequency effects, such as the skin effect, which significantly affects the series resistive and inductive elements in the models for on-wafer pad structures, tend to produce very large ladder circuits [10], increasing the complexity of the extraction methodologies.

To overcome these limitations, this article presents how the skin effect can be satisfactorily incorporated into the modeling of test fixtures in an RF-CMOS process, showing the convenience of including this important high frequency effect. A simple extraction methodology based on transmission-line concepts was developed, and the

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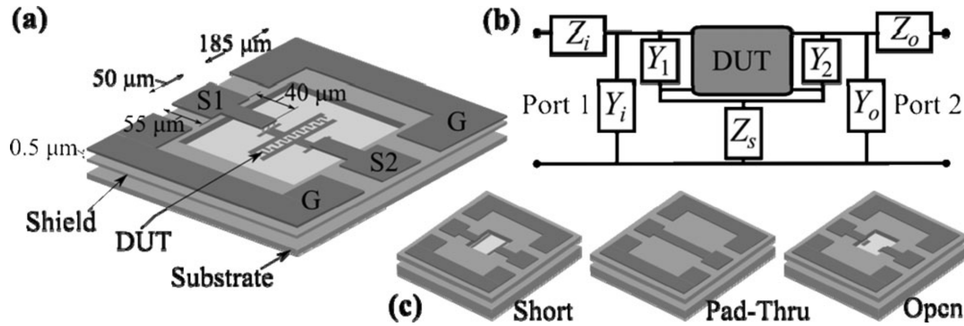

Figure 1 (a) Sketch of a DUT embedded in a test fixture, (b) corresponding circuit model consisting of generic impedance and admittance blocks, and (c) associated dummy structures for de-embedding purposes.

resulting model was used in the de-embedding of an RF-NMOS, obtaining a significant improvement in modeling the high frequency range up to 60 GHz, over a typical approach consisting of frequency independent circuit elements.

II. GENERIC MODEL FOR A SHIELDED TEST STRUCTURE

When using coplanar microprobes to measure on-wafer S-parameters, it is a common practice to shield the pads from the substrate; this allows to neglect the negative influence of the pad coupling through the substrate. As can be seen in Figure 1a, this is achieved using a metal layer that leaves a window to interconnect the pads with the DUT. In this case, the test structure including the DUT can be represented by the circuit shown in Figure 1b, which considers the corresponding parasitic effects using generic impedance and admittance blocks. In this case, Z_i and Z_o include the series parasitics associated with the pads and the lines interconnecting the test fixture with the DUT; Y_i and Y_o take into account the electrical coupling from the signal pads to the ground pads and the shield plane; Y_1 and Y_2 are used to represent the shunt parasitics occurring at the test-fixture-to-DUT interface; and finally Z_S is associated with the interconnections between the DUT and the ground pads.

Before developing a model based on *RLGC* parameters for the test fixture, the admittances and impedances in the model of Figure 1b have to be determined as a function of *f*. For this purpose, the dummy structures illustrated in Figure 1c, are used. The corresponding equivalent circuits for these structures are shown in Figure 2.

First, the series elements Z_i, Z_o, and Z_S are obtained from the measurements performed on the short structure. Here, $1/Y_i >> Z_S$ and $1/Y_o >> Z_S$ were assumed; in this case:

$$z_i = z_{11_{Sh}} - z_{12_{Sh}} \tag{1}$$

$$z_o = z_{22_{Sh}} - z_{12_{Sh}} \tag{2}$$

$$z_S = z_{12_{Sh}} \tag{3}$$

where the S-parameters associated with the short structure were converted to *Z*-parameters and are labeled with sub-index *Sh*.

Once the series impedances (i.e., Z_i and Z_o) have been determined, their effect can be removed from the experimental S-parameters corresponding to the Pad-Thru structure using simple two-port network parameter transformations. The resulting parameters are sub-indexed with *Th** and can be related to the model in solid lines in Figure 2b; thus, Y_i and Y_o can be obtained from the Y_{Th*}-parameters using:

$$Y_i = Y_{11_{Th*}} + Y_{12_{Th*}} \tag{4}$$

$$Y_o = Y_{22_{Th*}} + Y_{21_{Th*}} \tag{5}$$

Notice in Figure 2b that Z_{th} represents the line interconnecting the port-1 to port-2 signal pads, and its calculation is not necessary within the present analysis. Afterward, Z_i, Z_o, Y_i, and Y_o are removed from the S-parameters associated with the Open structure, yielding the model shown in solid lines in Figure 2c. Thus, from the corresponding Z-parameters, Y_1 and Y_2 can be determined as

$$Y_1 = Z_{11_{Op*}} - Z_S \tag{6}$$

$$Y_2 = Z_{22_{Op*}} - Z_S \tag{7}$$

where the subindex *Op** is used to denote the Z-parameters of the model in solid lines in Figure 2c.

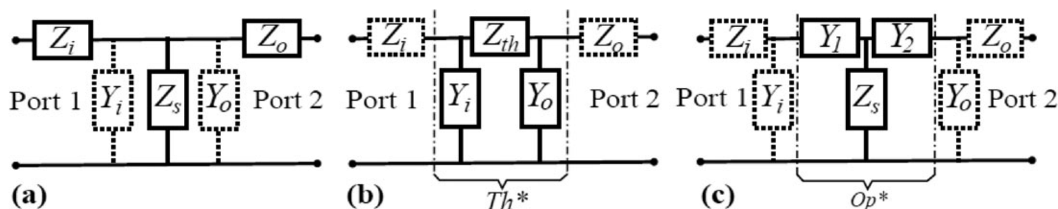

Figure 2 Models for the (a) Short, (b) Pad-Thru, and (c) Open dummy structures.

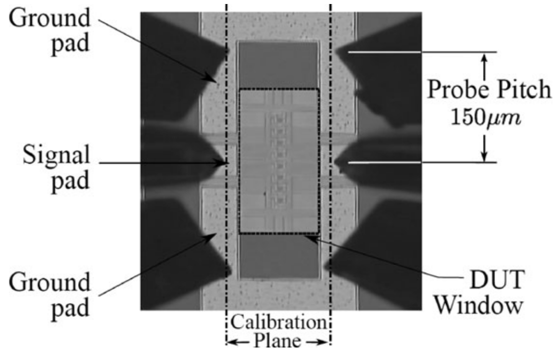

Figure 3 Micrograph detailing the fabricated test-fixture including a DUT and showing the probes used to perform the S-parameter measurements. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com.]

Once all the elements in the model shown in Figure 1b have been determined, *RLGC* parameters can be used to represent the variation of these impedances and admittances as a function of f. This is explained hereafter.

III. FABRICATED PROTOTYPES AND MEASUREMENTS

In order to validate the extraction and modeling methodology, the structures shown in Figure 1c were fabricated on a 90 nm RFCMOS process. All these structures present a ground shield implemented in the bottom metal layer available in the process (i.e., level-1 metal), which is connected to the ground pads of the test fixture to correctly establish the ground reference. These pads, as well as those for the signals at port-1 and port-2, are made of aluminum at the level-3 metal. Furthermore, the pads are configured for ground-signal-ground (GSG) coplanar RF probes with a 150 μm pitch, as shown in Figure 3. This figure illustrates the test fixture including a DUT. All the experimental data used throughout this article correspond to on-wafer two-port S-parameter measurements performed on the previously described structures up to $f =$ 60 GHz using a previously calibrated vector network analyzer. These measurements were performed applying a signal power of -20 dBm at each port.

IV. EQUIVALENT CIRCUIT MODELING

The methodology proposed here to obtain the equivalent circuit representation for the series and shunt parasitics is illustrated for the case of Z_S and the blocks at the left of the DUT (i.e., at port-1 in Fig. 1b), as the parameters associated to Port 2 can be obtained in a similar way by applying the same methodology using the corresponding experimental data. Before starting to explain the equivalent circuit for the test structure, it is important to remark the fact that for the maximum frequency analyzed in this article (i.e., 60 GHz) the corresponding wavelength, within the structure, is $\sim$4.9 mm, which is very large in comparison to the maximum length occurring in the structure ($\sim$90 μm). This allows to neglect the distributed nature of the pad, which is observed at much higher frequencies, and a lumped circuit such as that shown in Figure 4 results adequate.

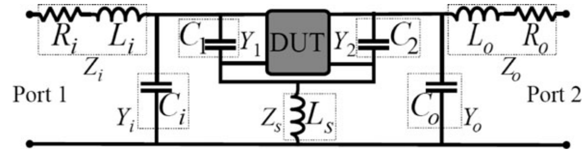

Figure 4 Equivalent circuit model for the test fixture using *RLGC* elements.

In Figure 1b, Z_i includes the series effects of the pads and lines used to reach the DUT. These effects are related to the finite resistivity of the metal used to form the pads and the inductance associated with the current loop formed by the signal pads and the return path. Therefore, Z_i can be modeled as shown in Figure 4 by using an equivalent resistance and inductance R_i and L_i, respectively. The value of these parameters depends on material and geometrical factors, but it is important to take into account that R_i and L_i are also strongly dependent on f due to the confinement of the current in the surface of a metal because of the skin effect, which is noticeable within the gigahertz range. This is neglected in previous approaches for modeling RF probing pads [10–13], either limiting the frequency range of validity of the model [13], or requiring the use of multiple resistances and inductances [10].

Two equations that accurately represent f-dependent R_i and L_i, including the skin effect are [14]:

$$R_i = R_{LFi} + K_i\sqrt{f} \tag{8}$$

$$L_i = L_{HFi} + \frac{K_i}{2\pi\sqrt{f}} \tag{9}$$

where R_{LFi}, L_{HFi}, and K_i are independent of f. Thus, considering equations (8), (9), and $Z_i = R_i + j2\pi f L_i$, R_{LFi}, and K_i can be determined by performing a linear regression of the experimental $\mathrm{Re}(Z_i)$ versus $\sqrt{f}$ data, whereas L_{HFi} can be obtained from the slope of a linear regression of the $\frac{\mathrm{Im}(Z_i)}{\sqrt{f}}$ versus $2\pi\sqrt{f}$ data. The extraction of these parameters is shown in Figure 5a and b for f >15 GHz as

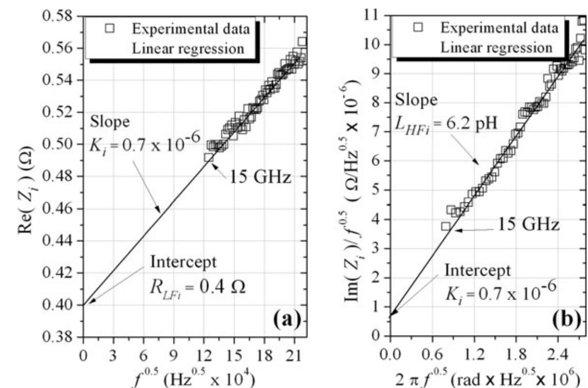

Figure 5 Linear regressions used to determine R_{LFi}, K_i, and L_{HFi}.

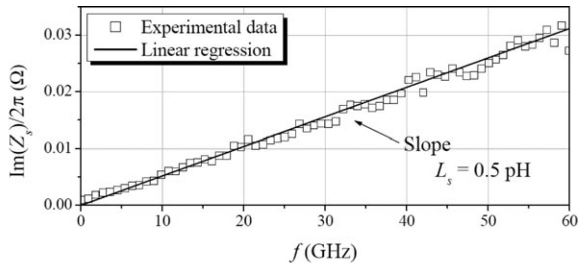

Figure 6 Linear regression used to determine L_S.

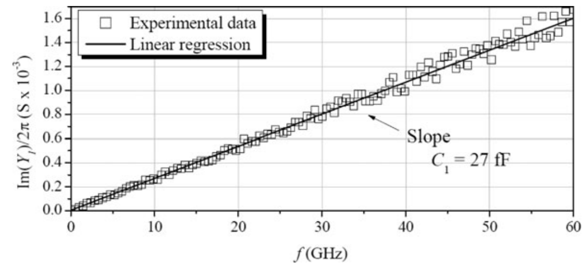

Figure 8 Linear regression used to determine C_1.

the frequency dependent nature of $|Z_i|$ is only observed beyond the frequency at which the skin depth is as small as the pad thickness. For the case of the studied pads, made of aluminum, this occurs approximately at $f = 14$ GHz, as at this frequency $\delta \approx 700$ nm (i.e., the metal pad thickness). Observe that K_i can be consistently obtained using a regression based either on (8) or (9); this is due to the fact that K_i accounts for the reduction of the cross-sectional area where the current is flowing through the pads (i.e., the skin effect), which impacts both R_i and L_i equally.

At this point, it is convenient to mention that Z_i and Z_o are associated with the series parasitics occurring at the input and output ports, including the corresponding signal and ground paths. However, a fraction of the series parasitics are present at both ports; for instance, those related to the thin vias used to interconnect the DUT reference terminal to ground. This effect is represented by means of Z_S, which can be modeled by means of an inductance (L_S). In contrast to L_i and L_o, L_S can be considered as independent of f due to the relatively small size of the vias used as vertical interconnects; thus, the impact of skin effect is not important for Z_S at the frequencies of interest in this article. Hence, assuming $Z_S \sim j2\pi f L_S$, L_S is directly obtained from the slope of the $\mathrm{Im}(Z_S)/2\pi$ versus f curve. The determination of this parameter is shown in Figure 6.

The shunt admittances, Y_i and Y_o include the capacitive effect occurring between the signal pad and the return path formed by the ground pads and the ground shield. In practice, the associated capacitors present losses because of the finite value of the loss tangent of the field oxide. For f up to some tens of gigahertz, however, the impact of these losses on Y_i is small and a single capacitance (C_i) can be used to represent the shunt admittance. Moreover, C_i presents an approximately constant value with f as long as the silicon substrate effects are negligible. So, C_i can be easily determined from a regression of the $\mathrm{Im}(Y_i)/2\pi$ versus f curve, as shown in Figure 7.

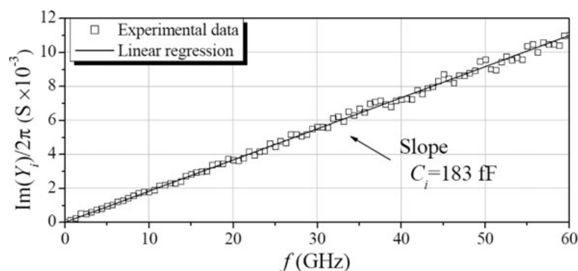

Figure 7 Linear regression used to determine C_i.

Finally, the admittances Y_1 and Y_2 are associated with small capacitances at the test-fixture-to-DUT transition. For the case of Y_1, a capacitance C_1 is used to represent this effect and can be determined from the slope of a linear regression of the $\mathrm{Im}(Y_1)/2\pi$ versus f experimental data, as shown in Figure 8.

V. MODEL VERIFICATION

In order to point out the advantages of using the proposed model and parameter extraction methodology, the model in Figure 4 was implemented in Agilent's ADS circuit simulator for two cases: using f-independent series elements (the corresponding model is referred to as FIM), and using (8) and (9) to represent the f dependent nature of the series resistances and inductances of the structure (i.e., FDM model). Then, a comparison involving S_{11} and S_{22} is performed as S_{12} and S_{21} present a magnitude below -30 dB within the measured f-range because of the excellent isolation between ports in the fabricated test fixture. It is important to point out the fact that even though many circuit simulators are readily available for including frequency dependent elements, this type of effect can be implemented in SPICE using arrays of frequency independent elements [15].

As shown in Figure 9, the two studied models acceptably reproduce the experimental S_{11} and S_{22} measured data from the Open structure within the whole analyzed f-range. The relatively good model-experiment correlation obtained when using FIM is due to the fact that the shunt elements are dominant for the Open structure, and their impact on the f-dependent series elements on the measured S-parameters is small.

In contrast, the dominant effects in the short structure are those associated with the series elements, which are f-dependent. Thus, notice in Figure 10 that FIM fails to represent the experimental S_{11} and S_{22} data for f >30 GHz. In fact, beyond this frequency, R_i and R_o substantially differ from their corresponding values at low frequencies (i.e., R_{LFi} and R_{LFo}, respectively) and considering their f-dependent nature it becomes mandatory to obtain realistic simulation results. In this regard, extracting the associated parameters using the proposed methodology yields excellent results at least up to $f = 60$ GHz, as shown in Figure 10.

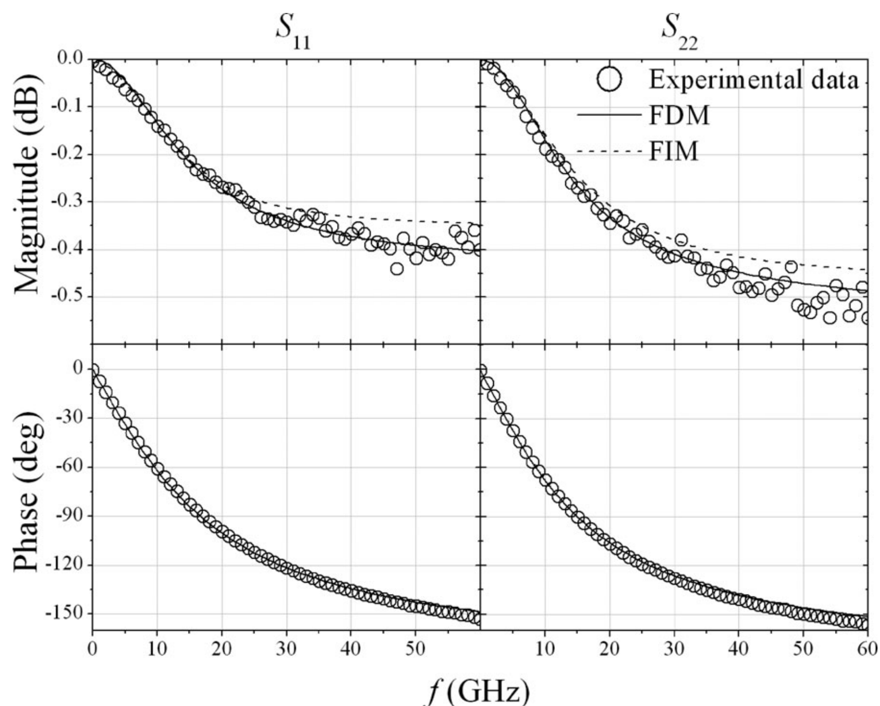

Figure 9 Comparison between simulated and experimental data corresponding to the open structure when using the models that consider *f*-independent (FIM) and *f*-dependent (FDM) series elements.

Notice also in Figures. 9 and 10 that the experimental data corresponding to the dummy structures includes considerable noise beyond 30 GHz, which is inherent to reflective structures fabricated in CMOS processes. In consequence, these noisy data may introduce errors when applying the de-embedding procedure. For this reason, when an appropriate representation of the dummy structure is achieved using equivalent circuit models, these models can be used instead of directly using the noisy data corresponding to the dummy structure; this allows to reduce the noise observed in the final de-embedded data.

VI. DEVICE MODELING APPLICATION

The models discussed in Section IV were used here to de-embed measurements performed on a common source/bulk RF-nMOSFET fabricated on a p-type Si substrate and embedded between the same type of pads studied in previous sections. This device consists of 64 gate fingers,

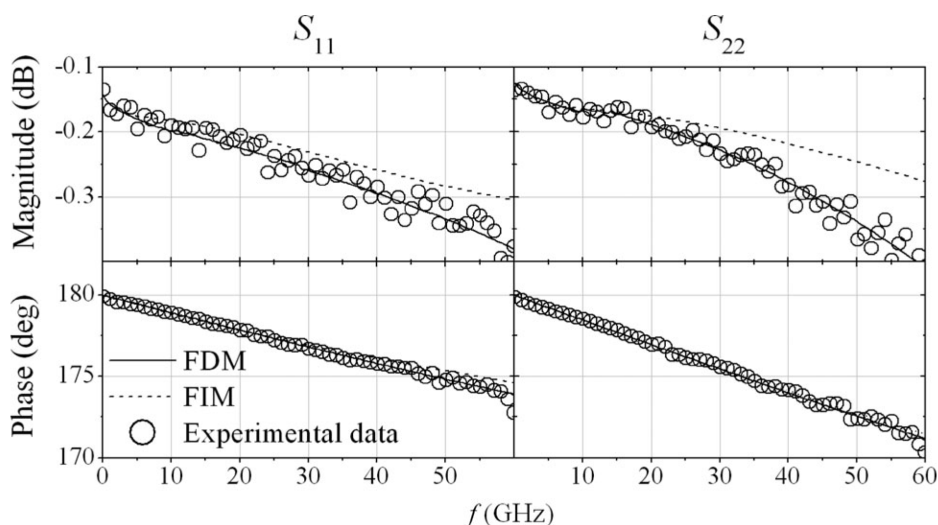

Figure 10 Comparison between simulated and experimental data corresponding to the short structure when using the models that consider *f*-independent (FIM) and *f*-dependent (FDM) series elements.

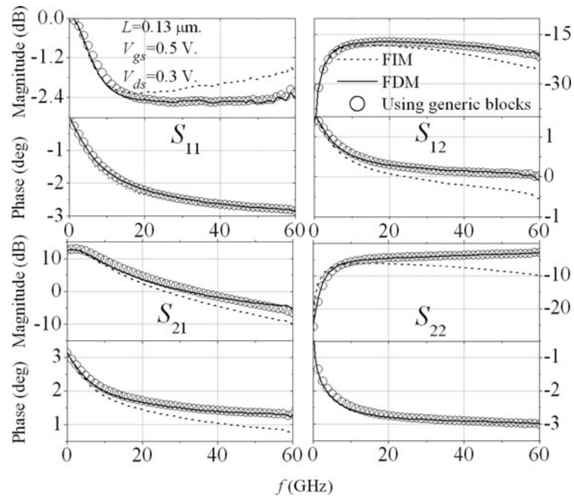

Figure 11 S-parameters for a de-embedded nMOSFET under $V_{gs} = 0.5$ V and $V_{ds} = 0.45$ V bias condition.

a total width $W_T = 192$ μm, and channel length $L = 80$ nm. The device was biased at $V_{gs} = 0.5$ V and $V_{ds} = 0.3$ V and the measurements (referred to as raw measurements) include the effect of the test fixture. Subsequently, these raw measurements (i.e., DUT including pad effects) were de-embedded to remove the effect of the test fixture using generic Z and Y blocks. This is a common way to de-embed measurements [1–3], and the corresponding results can be considered as accurate to be used as a reference for comparison. Then, the raw measurements were again de-embedded, but now representing the test fixture using the FIM and FDM; the results are compared in Figure 11. Notice the better model-experiment correlation when FDM is used, pointing out the importance of considering the f-dependence of the series elements of the test fixture.

VII. CONCLUSIONS

A simple, accurate, and physically based methodology to obtain the model parameters for a ground-shielded test fixture was proposed. The validity of this proposal was validated by correlating experimental and simulated data obtained from test fixtures with and without a DUT up to 60 GHz. In fact, the proposed methodology represents a good alternative for modeling these structures at microwave frequencies while simultaneously maintaining accuracy, simplicity, and physical significance of the obtained parameters, which allows for appropriately analyzing the effect of the pads and other interconnects when either designing a prototype for probing or selecting the most appropriate de-embedding technique for a particular application.

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BIOGRAPHIES

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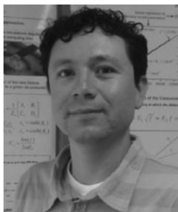

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