Multiphase Clock Generation System in CMOS Technology

By

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"The optimist thinks this is the best of all possible worlds.
The pessimist fears it is true. "

J. Robert Oppenheimer.

Agradecimientos

A la incondicionalidad de mi familia, a esa alegría que me da volver a mi casa y encontrar que aun me tienen un lugar y aun me esperan. Porque mi motivación para estudiar y progresar no es solo por satisfacción personal sino por satisfacción de ellos, porque quiero ayudar a que vivan mejor.

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Muchas Gracias a todos!

Jhoan Alberto Salinas

RESUMEN

TÍTULO:

SISTEMA DE GENERACION DE RELOJ DE MULTIPLES FASES EN TECNOLOGÍA CMOS

AUTOR:[1] JHOAN ALBERTO SALINAS DELGADO

PALABRAS CLAVE: Oscilador de anillo, Delay Locked Loops, Detector de retardo, jitter, mismatch en fase, tecnología *CMOS*.

DESCRIPCIÓN:

El presente trabajo propone el diseño de un sistema de reloj de multiples fases basado en un oscilador de anillo y un control individual para el retardo de cada fase. Este control individual permite una correción de los errores de tipo estático causados por mismatch o desbalance en las capacitancias de carga producto del layout y fabricación.

En este documento se realiza el proceso de selección de los diferente bloques necesarios para el sistema. En el caso del oscilador de anillo, se utliza una celda de retardo de doble entonado, uno para fijar la frecuencia y otro para el ajuste individual de cada celda. Además, con el fin de detectar pequeños retardos entre dos señales, se utiliza un detector basado en la descarga de un capacitor controlado por un pulso cuyo ancho es dependiente del retardo a medir.

El detector de retardo diseñado puede sensar retardos del orden de 40 ps, y posee una ganancia de $-1/20$ V/p. Por su parte, el oscilador tiene una frecuencia que varía entre 1.7 y 2.25 Ghz, un ruido de fase de -101.13 dBC/Hz a un offset de frecuencia de 1 MHz, y un consumo de potencia de 80 mW. Para el sistema completo diseñado en la tecnología de fabricación *CMOS UMC* 0.18 μm, el sistema presenta un rango de frecuencias entre 1.7 y 2.25 GHz, además de una precisión en los retardos de 1.86 ps y una compensación de errores de capacitancia de hasta 15 fF. El consumo de potencia

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del sistema es de 150 mW.

SUMMARY

TITLE:

MULTIPHASE CLOCK GENERATION SYSTEM IN CMOS TECHNOLOGY

AUTHOR:[2] JHOAN ALBERTO SALINAS DELGADO

KEY WORDS: Ring oscillator, Delay Locked Loops, Delay detector, jitter, phase mismatch, CMOS technology.

DESCRIPTION:

This work proposes a multiphase clock generator based on a ring oscillator and a delay control of every individual phase. With this individual control, correction of static errors caused by mismatch and capacitive unbalance is possible.

In this document, the selection of the architecture and the different functional blocks is reported. In the case of the oscillator, a delay cell with dual tuning method is used; coarse tuning is used for frequency variation and fine tuning is used for the control of each phase. Moreover, in order to detect small delays between two signals, a delay detector based on the discharge of a capacitor, controlled by a pulse whose width is dependent on the delay to be sensed.

The designed delay detector can sense delays in the order of 40 ps, with a gain of $-1/20$ V/ps. In the case of the oscillator, a frequency range that spans from 1.7 up to 2.25 GHz, a phase noise of -101.13 dBc/Hz measured at an offset frequency of 1 MHz, and a power consumption of 80 mW is achieved. For the whole system, designed with the UMC 0.18 μm Mixed Mode and RF CMOS technology, the clock generator achieves a frequency range from 1.7 to 2.25 GHz, with a delay accuracy of 1.86 ps and a capacitive unbalanced compensation for errors up to 15 fF. The power consumption of the clock generator is 150 mW.

[2]INAOE. Electronic department. Integrated circuit design.

List of Abbreviations

CML Current Mode Logic

CP Charge Pump

DCO Digital Controlled Oscillator

DCVSL Differential Cascode Voltage Switch Logic

DDLL Distributed Delay Locked Loop

DLL Delay Locked Loop

DU Delay Unit or Delay Cell

LF Loop Filter

MPCG Multiphase Clock Generator

PD Phase Detector

PFD Phase Frequency Detector

PLL Phase Locked Loop

PVT Process Voltage and Temperature

RVCO Ring Voltage Controlled Oscillator

SR Shift Register

VCO Voltage Controlled Oscillator

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Chapter 1

Introduction

Transistors are inherently nonlinear devices, and such characteristic brings to distortion in every circuit implemented with them. Nowadays, a wide variety of applications, such as high fidelity audio and telecommunications systems, require the suppression of that non-linear behavior. This has motivated some research in order to achieve high linearity on circuits such as exigent like power amplifiers and DAC's. Moreover, if the application requires high-speed operation, the nonlinearity problem becomes more complex because several methods and insights commonly used for design low distortion systems (as the use of filters, predistortion and feedback), increment the latency of the system.

In recent years, polyphase systems have been reported as an alternative to accomplish high linearity in RF circuits. This type of systems uses a phase difference between signal paths to cancel unwanted harmonic components and intermodulation products, allowing a performance increase without a system latency rise. An example of the use of that technique is the work reported by [3–5], which presents the design of a power upconverter by combining a power amplifier and an upconversion mixer [6].

A problem associated with the use of polyphasic systems is the dependence of harmonic suppression on the angle separation between adjacent phases. In the implementation of [3–5], a clock that generates n equal-spaced phases is needed. Despite the use of systems based in shift registers to lower jitter have been reported [7], the problem of non homogeneous spacing remains. That problem is hard to solve because, beside

dynamic phase errors such as jitter, there is static phase error, that depends on factors such as layout and mismatch, which affects the system performance. This scenario motivates to address the present work on the design of a multiphase clock generator (MPCG), with low phase error and low jitter characteristics. **The approach chosen to overcome the previously described problem is the use of a ring oscillator, which will use a detection-correction scheme between the different phases**.

With the purpose of giving the reader a theoretical framework to formalize the context in which this project is developed, this chapter describes the importance of an efficient multi-phase clock generation system for multiple paths harmonic cancellation systems. In addition, the main specifications for a MPCG, the main implementations found in literature and the proposed approach are discussed.

1.1 Cancelling Nonlinearity with Multiple Paths

Multipath technique is based on processing a signal by using multiple signal paths, in order to obtain a set of outputs with their fundamental forming a balanced system, whose sum cancels the undesired components. Figure 1.1 shows the block diagram of an n-phase harmonic cancellation system. The mathematical background of this technique, covered in detail by [3–5], is summarized as follows.

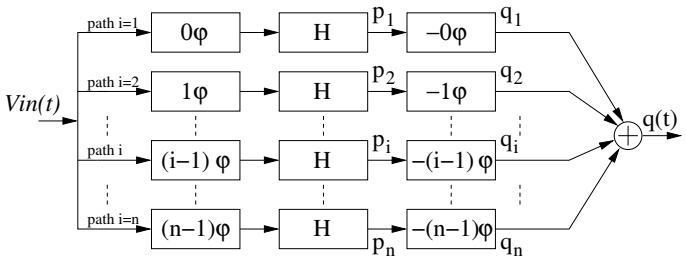
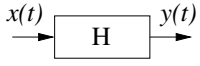


Figure 1.1: Harmonics cancellation in a n-paths n-phases system.

Let H be a memoryless weakly non-linear circuit with input-output transfer characteristic determined by:



$$y(t) = a_0 + a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) + \dots$$

To implement the method, H is divided in n smaller circuits, each circuit goes in one of the n paths. Before and after each circuit, equal but opposed phase shifts are applied. For an input signal $V_{in}(t) = A\,Cos(\omega t)$, the output of the nonlinear circuit of the i-th path (signal $p_i(t)$) is described by:

$$p_i(t) = C_0 + C_1\,A\,Cos[\omega t + (i-1)\phi] + C_2\,A^2\,Cos[2\omega t + 2(i-1)\phi] + \\ + C_3\,A^3\,Cos[3\omega t + 3(i-1)\phi] + \ldots \tag{1.1}$$

where $C_0, C_1, C_3, \ldots$ are constants. In order to align the fundamental components there are required the phase shifters $-(i-1)\phi$ after the nonlinear blocks H [6]. The output signal of these phase shifters can be written as:

$$q_i(t) = C_0 + C_1\,A\,Cos[\omega t] + C_2\,A^2\,Cos[2\omega t + (i-1)\phi] + \\ + C_3\,A^3\,Cos[3\omega t + 2(i-1)\phi] + \ldots \tag{1.2}$$

When the phase shifts are multiples of $\phi = \frac{2\pi}{n}$ in the expression of $q_i(t)$, the fundamental components add up in phase. However, all the harmonic components from the second up to the n-th form a balanced phasorial structure that cancels their contributions. The first non-cancelled harmonic is the n+1 and, in general, the non-cancelled k-th harmonics satisfy the condition:

$$k = jn + 1 \qquad j = 0, 1, 2, \ldots \tag{1.3}$$

A similar analysis about intermodulation products (IM products) can be done. When the input is $V_{in}(t) = A_1 cos(\omega_1 t) + A_2 cos(\omega_2 t)$, the Multiple-path technique cancels all IM products, except the ones at frequencies $\omega = p\omega_1 + q\omega_2$ that satisfy:

$$p + q = jn + 1 \qquad j = 0, 1, 2, \ldots \tag{1.4}$$

Implementation

With the need of a phase shifter that allows the cancellation process, in [3–5] a mixer is used as an alternative for analog domain wideband phase shifting. This also allows an

upconversion functionality that combined with the power amplification function gives rise to a power upconverter. In Figure 1.2 [3], the first set of phase shifters can be implemented in the digital domain or by means of polyphase filters, which exhibit an acceptable accuracy at low frequencies.

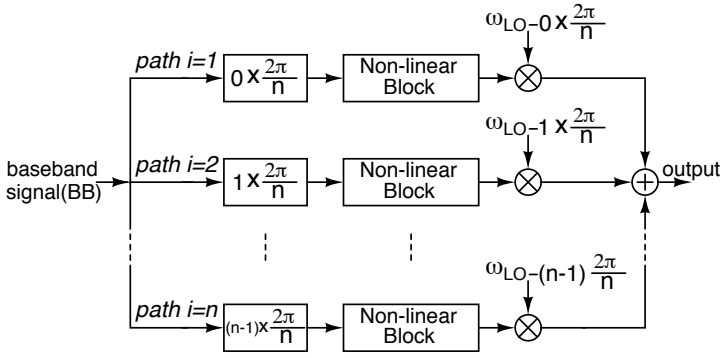


Figure 1.2: The multipath-polyphase approach with a mixer as phase shifter.

Influence of Mismatch in the Technique

Mismatch plays a significant role in the effectivity of the multipath polyphase technique to linearize circuits. In the presence of not identical blocks and paths, the distortion is not completely cancelled. Equation (1.5), taken from [3–5], quantifies the expectation $E(sup)$ of the suppression of the $k_{LO}\omega_{lo} \pm m\omega_{lo}$ harmonic in the presence of mismatch. θ corresponds to the mismatch in the first group of phase shifters, δ is the mismatch in the second group of phase shifters, ϵ is the mismatch in the coefficient of the power series from the non-linear blocks, k_{LO} and m are integers, and $E(.)$ is the expectation operator.

$$E(sup) = \frac{n^2}{(n-1)\left(\frac{E(\epsilon^2)}{a_n^2} + k_{LO}^2 E(\theta^2) + m^2 E(\delta^2)\right)} \tag{1.5}$$

From equation (1.5), [3] exposes how in general terms, the phase deviation affects more the overall system than the non-linear blocks mismatch. Behavioral simulations show how a variation of 2% angle error affects the cancellation process, limiting harmonic component suppression to 40dBc, which is pernicious for the effectivity of the

technique in applications such as IP communications, e.g. WiMAX. **This angle accuracy depends on the multiphase clock that drives the mixers, because the phases must be equidistant within a tolerance which fits to 2%**. It should be taken into account that the larger the number of paths and phases, the more effective the harmonics suppression is accomplished, but a major system complexity is required.

1.2 Multiphase Clock Generation: Definition

A polyphase system of order n is defined as an array of n clock signals with the same waveform, but with a constant delay between them. Each signal is called a **phase**, and between adjacent **phases** there is a constant delay denoted by T_d. The time delay T_d defines the clock frequency , as shown in the expression (1.6). For instance, Figure 1.3 shows the clock signals for a 4 stage system, where equation (1.6) states a period of $8\,T_d$, and a clock frequency given by $\frac{1}{8\,T_d}$.

$$freq = \frac{1}{2\,n\,T_d} \tag{1.6}$$

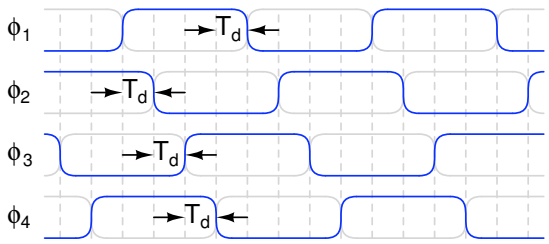


Figure 1.3: Delays in a 4-phase clock system.

1.3 MPCG Specifications

There are some specifications that need to be to fulfilled in the design of a MPCG system. Key aspects are frequency, amplitude, maximum phase error and power consumption of the system. These specifications will be detailed explained, along with a summary of the requirements that will be used for this work.

Maximum phase error

Ideally, the MPCG phases should be evenly spaced and delays T_d should be equal in every phase. However, there are two types of errors that together limit the accuracy of these delays and determine the maximum phase error. These errors are classified in static and dynamic errors. The maximum phase error is defined as the maximum deviation that a delay can have from the average of all delays between phases of the MPCG. It can be specified in time (seconds) or as an angle (degrees)[1].

Static error: In schemes that uses identical blocks, mismatch and unbalance capacitive loads, frequently caused by layout and fabrication, brings to a non uniform spacing between clock phases. This kind of error is static and can be seen as a delay offset. Most of the techniques used to reduce static error are based on well matched layouts, and the use of dummies structures that equalize the load capacitance of the different stages. Additionally, it has to be considered the effect of skew[2] and the importance of both clock generation and routing.

Dynamic error (Jitter): Jitter is defined as the uncertainty in time events, generally in the signal transition. Jitter can be caused by several factors, like noise in devices, power supply variations, jitter in the time reference, loading condition and, among many others, interference coupled from nearby circuitry. In order to reduce jitter effects, the use of system architectures that keep away jitter accumulation, and a reduced number of blocks (more circuit blocks represents more noise), is recommended. A more detailed explanation of jitter theory and the methods for simulation is addressed in Appendix A.

[1] In spite of not being a pure sinusoidal signal, The static phase error of clock signals is specified in degrees. A period T corresponds to 360^{o} and a delay T_d corresponds to $\frac{360^{o}\,T_d}{T}$ degrees [8].

[2] **Skew** is referred to the finite transit time of the signals over the wires.

Frequency

As applications requires faster clocking circuitry, the accuracy for very small delays increases circuitry requirements, and leads to many problems caused by the delay sensibility to mismatch, capacitance variations and jitter. In this scenario, the maximum phase error must be taken into account because it gives a serious constrain in the maximum allowable operation frequency.

Amplitude

Amplitude of clock signals is chosen based on the requirements of the subsequent stages. In the cases where the clock signal drives some logic circuits or switches, noise margins determines the voltage values for the low and high logic levels. It is necessary to consider that capacitance unbalance and mismatch among stages cause amplitude errors that degrades the waveforms and the delays between stages.

Power consumption

As a demand of battery based devices, low power consumption is a requisite in clock generation and distribution systems in modern electronics. However, The large amount of power associated to large signal swings at high frequency makes the design process of low power systems a tough challenge. For example, in a system with 6 delay cells, which drives an output capacitance of $C_L = 40\ f\mathrm{F}$ at 1 GHz, the necessary current for charge and discharge the output node 1.8 V in $\Delta t = 30ps$ can be approximated to:

$$I = C_L \frac{\Delta V}{\Delta t} = (40\, fF)\frac{(1.8\, V)}{(30\, ps)} = 2.4\,\mathrm{mA} \quad \text{per stage.}$$

1.4 MPCG Implementations

In order to implement a MPCG with equal spacing, a possible solution may be increase transistor size to reduce mismatch. However, parasitic capacitance will increase and the speed is degraded, making evident a trade-off between frequency and matching

between stages [8]. Sometimes, an extra calibration or compensation scheme is required to guarantee equidistant clock signals, several approaches can be found in the literature. In this section the most representative alternatives are explained in detail, highlighting their advantages and drawbacks.

DLL Based MPCG

One of the basic approaches is the use of a Delay Locked Loop (Figure 1.4). A voltage (or current) controlled delay line[3] is sensed in the reference signal P_{ref} and in the last output P_n with a phase detector. The negative feedback loop, implemented by the block PD/CP/LF, allows the synchronization in time of P_{ref} and P_n. If delay cells are identical in the delay line, all the clock phases must have the same waveform separated by homogeneous delays as it is required by a polyphase clock, as defined in section 1.2.

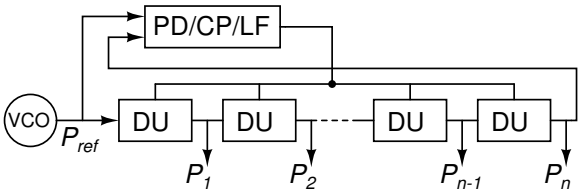


Figure 1.4: DLL based MPCG.

This approach has advantages in terms of implementation, since the use of simple layout techniques reduces the problem of static phase error. However, there are several drawbacks concerned with the lack of control in every phase. This tends to increment jitter and arising **dithering** problems in the DLL. Dithering refers to the oscillation of the control signal of the delay line that produces uncertainty in the output signals of the DLL and increments the output jitter.

The problem of Dithering is addressed by [9], who implements a system which uses a loop control unit that disables the control circuits when the DLL is locked.

[3] A **Delay cell** or Delay unit (DU) is defined as a circuit that creates a time difference between its input and its output signals. A **Delay line** is a network composed by some delay cells connected in cascade.

For that purpose, the control signal of the delay line is stored in a register while the control loop is disabled. Additionally, a system that compensates phase errors caused by environmental variations is implemented.

Shift Averaging and Interpolation

The main drawback of the above alternative is the digital calibration schemes, which requires of large extra area and power consumption. In order to address this problem, works like the reported by [10] use a resistive network to compute a phase average which reduces phase error. In addition, the resistive network can also be used to implement phase interpolation [1]. Figure 1.5 shows an example of a 1 to 5 phases interpolation scheme. The main drawbacks are the low mismatch quality of integrated resistors and their intrinsic large time constant ($\tau = RC$) that degrades speed.

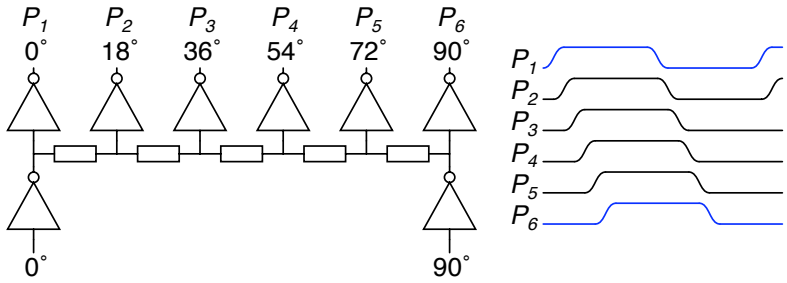


Figure 1.5: 1 to 5 phase interpolation circuit. Taken from [1].

Shift Registers Based MPCG

The work reported by [7] argues how SR based MPCG (SR-MPCG) have less problems of jitter with respect to DLLs, for a given power budget. An example of a n phases SR-MPCG is shown in Figure 1.6.

The polyphase signal is generated by a frequency division over a reference clock signal CLK_{ref}. The main advantage of this approach is that SR-MPCG have no jitter accumulation as in DDLs, additionally SR-MPCG are flexible to modify the output frequency and the duty cycle. The drawbacks are related to the frequency of the

reference signal. In order to generate a clock signal with frequency f it is required a reference signal with frequency nf, this gives a serious restriction in the number of phases implemented, because the generation of a high speed signals requires not only more power but a more carefully implementation.

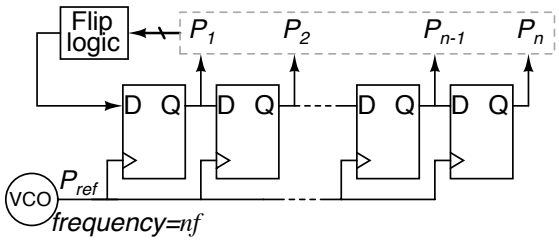


Figure 1.6: Shift Registers Based MPCG.

Distributed DLL

For DLLs and PLLs with multiphase outputs, the timing accuracies of the multiphase outputs depend on the matching among delay stages. Conventional DLLs do not address the problem of mismatch between delay stages caused by process, voltage and temperature (PVT) variations. To overcome this problem, [11] proposes an approach that tunes each delay cell individually in order to reach low jitter and high phase accuracy. The concept extends the idea of DLL to a distributed DLL (DDLL) in every phase. Nevertheless, in this implementation there are problems associated with the necessity of an external clock reference that introduces additional jitter and consumes more power.

Ring Oscillators

Although LC oscillators are well known as a good option for low jitter signal generation because of their large quality factor Q achievable with resonant networks, some problems respect to the implementation of integrated inductors, as passive or active blocks must be considered. Here, ring oscillators presents several advantages because they can be

implemented in a standard CMOS process, and require less die area than LCs. In addition, ring oscillators can provide wide tunning ranges and have the intrinsic feature to generate multiphase clock signals without the use of any external clock reference [12].

Comparison

Table 1.1 shows the reported results of some recent MPCG systems implemented in CMOS technology.

Ref.	Year	Technology *CMOS*	Freq. [GHz]	jitter rms [ps]	jitter p-p [ps]	Phase Error [ps]	Area [mm^2]	Power [mW]
[8]	2006	180 nm	0.7-2	2.45@2GHz	18.9@2GHz	3.5	1.03	81
[9]	2009	90 nm	2	1.6@2GHz	9.5@2GHz	-	0.037	7
[11]	2009	90 nm	8-10	0.293@10GHz	2.04@10GHz	1.4	0.03	15

Table 1.1: Some MPCG systems implemented in CMOS technology.

1.5 Conclusions

Most of the approaches previously presented require a clock reference signal. In the case of ring oscillators, they have the intrinsic feature of polyphase signal generation. Since the ring oscillator is an structure suitable for the use of a delay control in every phase, in this work a ring oscillator based clock generator combined with a phase correction system in every phase is selected. The independent control of each phase is beneficial in several aspects: first, it helps to minimize jitter accumulation and the static phase error; also, there is no necessary any external signal, so power consumption is saved and jitter effects are reduced. In addition, The use of a distributed control relax the requirements for layout. In the next chapter, the proposed system is explained in detail together with the analysis for the selection of the functional blocks that compose it.

Chapter 2

Ring Oscillator Based MPCG

In the previous chapter, ring oscillators are shown as a suitable option for polyphase clock generation. However, dynamic and static phase errors degrade the spacing between adjacent phases. This work addresses this problem, and proposes a delay correction system for each phase, in order to reach low jitter and high phase accuracy.

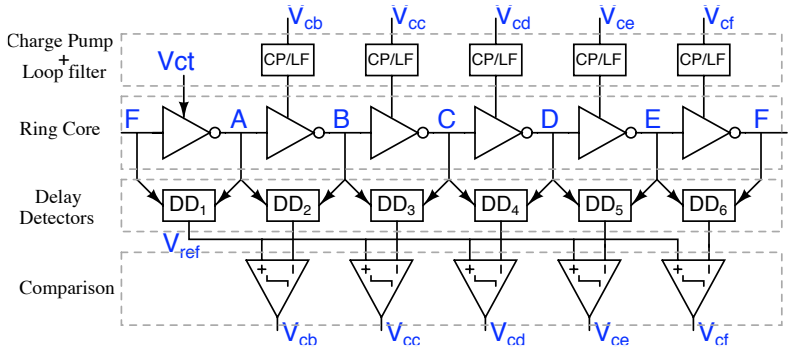
In this chapter, the system-level description of the proposed delay control system is shown; first, with a general description of the complete system and subsequently with a detailed description (i.e. topology selection, specifications and design) of the functional blocks used in this work: delay cell of the ring oscillator, phase detector, charge pump and loop filter.

2.1 System level description

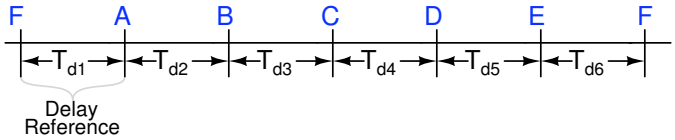
Figure 2.1(a) shows a six phases ring oscillator with delay control in all the phases. It is necessary to define two different tuning methods, one for delay accuracy and the other for frequency control.

For delay accuracy control, voltage signal Vct defines the delay T_{d1} of the first voltage controlled delay cell and defines the oscillation frequency of the ring according to the expression $freq = \frac{1}{12\,T_d}$. Delay detector (DD_1) senses T_{d1} and establishes a delay reference for the other stages by means of the voltage signal V_{ref}. After that, V_{ref} is

compared with output voltages of the other delay detectors $(DD_2, DD_3, \ldots, DD_6)$ in order to define if the charge pump increments or reduces the delay of the corresponding stage. The control loop is composed by a comparator, charge pump and a passive loop filter.



(a) Block Diagram.



(b) Delay Definition.

Figure 2.1: Proposed system.

As an example of the operation, let a capacitance unbalance at node C. This will cause an increment in delay, T_{d3}, from the phase-B to phase-C, and delay detectors DD_1 and DD_3 will give different signals. Thus, the output of the third comparator/charge pump/loop filter gives a control voltage V_{cc} that makes faster the third delay cell until the point where there is balance in the delays.

In order to stabilizing the frequency, the proposed ring oscillator can be used in a PLL based frequency synthesizer, as shown in Figure 2.2. The phase locked loop sets the control voltage Vc that fixes the frequency, and determines the frequency stability of the output signal.

In the selection of the blocks used in the system, there are several considerations that need to be taken in account, these considerations are listed below:

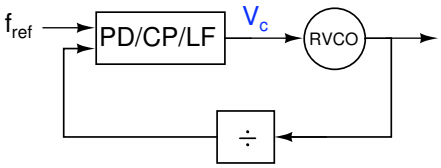


Figure 2.2: PLL based frequency synthesizer.

- Delay cells need two delay variation mechanism and rail to rail outputs.
- Delay detector must have the enough sensibility to detect small changes.
- Layout is an aspect of consideration for topology selection in high speed blocks. Topologies that delay the signal routing need to be reconsidered, and replaced by simpler solutions for its implementation.

2.2 Ring Oscillator

A ring oscillator consists of a number of inverter stages connected in a closed configuration. Depending on the oscillation amplitude and delay cell operation, two kind of oscillation regimes can be distinguished: linear and non linear. In the linear case, the oscillation frequency can be found by means of the Barkhausen criterion for linear circuits. A model of the linear case is shown in Figure 2.3 [13].

$$freq_{ring} = \frac{\tan(\pi/n)}{2\pi RC} \tag{2.1}$$

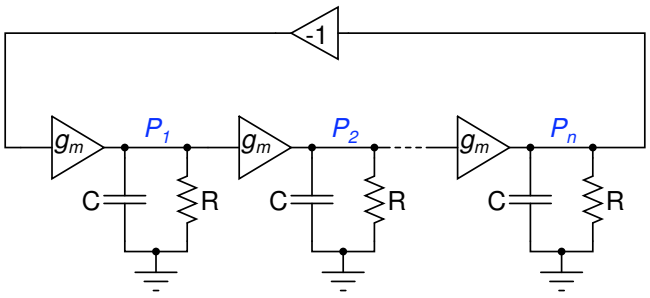


Figure 2.3: Linear model of a n-stage ring oscillator.

For the non-linear case, the oscillation frequency is found in terms of the propagation delay of each delay cell [14]. In Figure 2.4, signals for a three stage ring oscillator are shown.

$$freq_{ring} = \frac{1}{2n\,T_d} \tag{2.2}$$

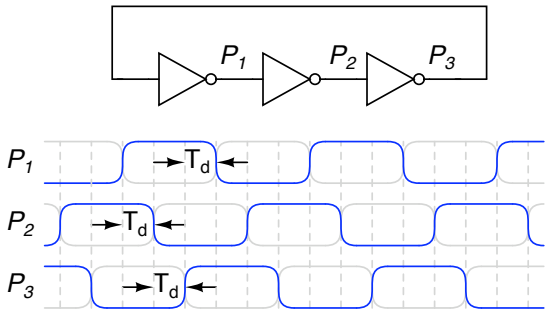


Figure 2.4: Delays in a 3-phase ring oscillator.

By using identical cells, it is possible to generate signals that satisfies the criterion for a MPCG; however, any unbalance in the load of any stage can be unfavorable for the equal spacing performance. To minimize the mismatch, dummy circuits can be used to provide symmetric loading for the VCO. Nevertheless, these circuits will not only generate additional parasitics at the RF nodes, but also in certain conditions they will not completely remove mismatch.

Tuning method

From equations (2.1) and (2.2), some possible ways to modify the frequency of the oscillator. For a fixed number of stages, the tuning method is reduced to variations in the load capacitance C, the output resistance R or the current that is applied to the capacitive load. Despite the tuning method, the control signal can be of analog or digital nature.

- **Output Capacitance**, as shown in Figure 2.5. The operation frequency can be modified with the use of varactors or capacitor banks controlled by switches. Typically switching schemes are used in the design of digital controlled oscillators (DCO).

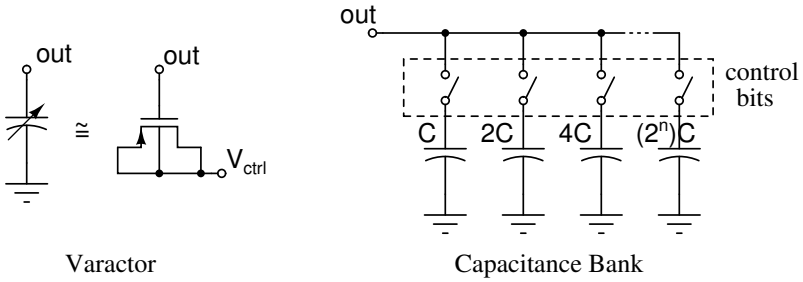


Figure 2.5: Output Capacitance Variation.

- **Output Resistance**, as shown in Figure 2.6, can be modified by using controlled resistors, for example transistors operating in triode region, symmetric loads (e.g. Maneatis cells [15]) or negative resistance networks [16].

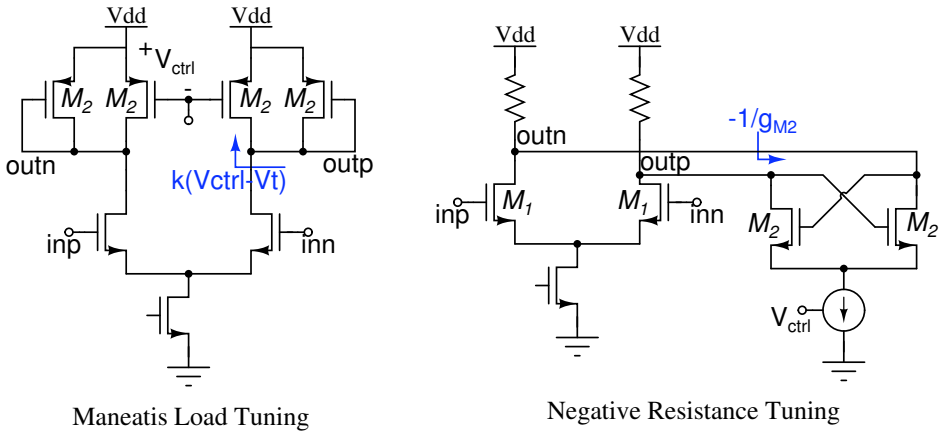


Figure 2.6: Output Resistance Variation.

- **The Current Applied to the Capacitive Load** can be modified with current starved schemes. In Figure 2.7, transistors M_p and M_n limit the current, injected or sunk to the load capacitance C_L.

2.3 Delay cell

Ring oscillator performance is defined by the characteristics of delay cells. Table 2.1, extracted from [14], summarizes the most important types of delay cells which have been used for oscillator design, describing their advantages and disadvantages. The

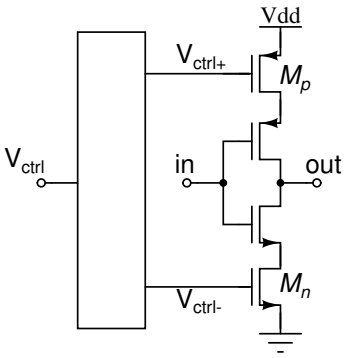


Figure 2.7: Current Starved Inverter.

selection of the basic cell must consider the frequency, the drive capacity of subsequent stages, the tuning characteristic, the signal swing and performance with regard to jitter. A classification, according to the type of signal, considers the cell as single ended, fully differential or pseudo differential:

- **Single ended** delay cells (Figure 2.8(a)) use signals referred to *gnd*. Several problems such as noise coupling from substrate and the supply rail can derive from its use; however, the use of large signal swings is favorable in terms of jitter.

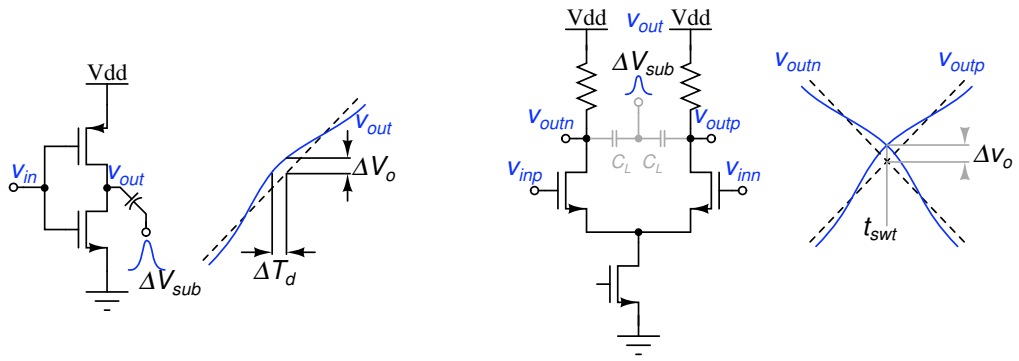
- **Fully differential** (Figure 2.8(b)) delay cells do not restrict the number of stages to be odd. By the using of a wire inversion in the output of one of the stages, an even number of phases can be implemented. A key feature of these cells is the common mode rejection, which is beneficial for noise coupling. However, low signal amplitude is associated with a higher sensitivity to jitter.

- **Pseudo differential** delay cells do not have the same amount of common mode rejection of fully differential, but the use of wide output swings improve jitter performance.

Noise coupling phenomena for single ended and fully differential delay cells is illustrated in Figure 2.8. In the single ended delay cell, substrate noise ΔV_{sub} can produce a coupling into the signal path, producing a deviation ΔV_o which conduces to a deviation ΔT_d on the switching instant t_{swt}. On the other hand, in the fully

Type of signal	Advantages	Disadvantages
Single ended	- Rail to rail swing. - Low power. - Low jitter.	- Only odd number of stages. - Susceptibility to supply substrate interference.
Fully differential	- Odd and even number of stages. - Common mode rejection.	- Small signal amplitude. - Requires a constant bias current.
Pseudo differential	- Rail to rail swing.	- Partial common mode rejection.

Table 2.1: Classification of delay cells in ring oscillators.



(a) Single Ended. (b) Fully Differential.

Figure 2.8: Single ended vs differential delay cells in terms of noise coupling.

differential delay cell, the substrate noise ΔV_{sub} acts as a common mode signal that causes a deviation in t_{swt} from the V_{outp} and V_{outn} output signals. However, no deviation in the switching instant of the difference $V_{outp} - V_{outn}$ can be appreciated.

2.4 Delay Cell Selection

Due to the requirement of differential clock signals, an analysis of fully differential and pseudo differential delay cells is necessary. **Fully differential Current mode logic**

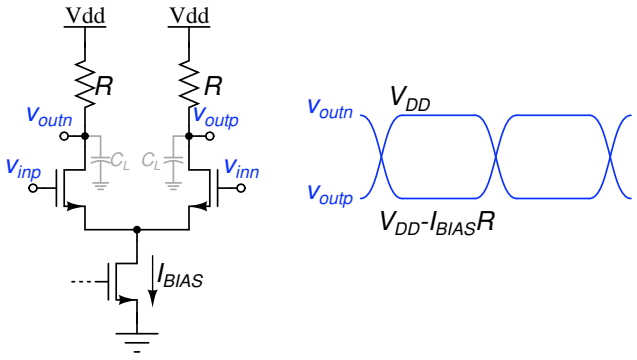


Figure 2.9: Current mode logic (CML) delay cell.

(CML), as shown in Figure 2.9, is the name of a family of circuits, whose basic block is a differential pair. The main idea is to apply a large enough input signal to the differential pair in order to make it switch and behave like a logic inverter. The main advantage of CML logic is the high-speed operation, besides its low levels of switching noise and its common mode rejection. These benefits make CML an attractive selection for many PLL and DLL applications. However, in CML logic, the output signal varies between V_{DD} and $V_{DD} - I_{bias}R$ (I_{bias} and R are defined in Figure 2.9) and the propagation delay is function of R and C_L. This causes a tradeoff between speed and signal amplitude: higher speed requires less value of resistance and lower resistance leads to lower signal amplitude. Furthermore, the implementation of low value passive resistance becomes difficult because of the low quality of integrated resistors.

As an alternative, **pseudo differential delay cells** have intrinsically almost rail to rail signals. They are based on the Differential Cascode Voltage Switch Logic (DCVSL), shown in Figure 2.10, which is composed by input transistors M_1 and M_2 and the semi-latch (M_5 and M_6) that helps to regenerate the output. Thus, high output swings, combined with high speed, motivates the use of this type of cells in the ring oscillator of the present work. However, it is necessary to face the problems of DCVSL logic concerned with the inherently larger low to high propagation delay t_{pLH} compared with the high to low propagation delay t_{pHL}. This is a problem that limits the speed and results in asymmetrical output waveforms.

For the delay cell used in this work, transistors M_7 and M_8 are added to the DCVSL

inverter in order to help the low to high transition, and improve speed and symmetry in the outputs. Additionally, with transistors M_3 and M_4, a wide range tuning method based on a negative resistance scheme is implemented. In order to make a fine control in every phase, two varactors are connected to the output of the ring. With this dual tuning method, the idea is to separate the frequency control from the precision control in the delays of the ring.

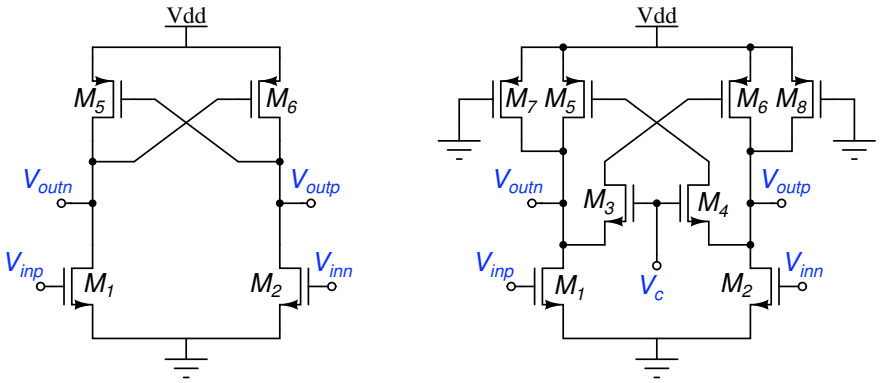


Figure 2.10: Pseudo differential delay cell.

2.5 Phase Detector

A Phase detector is a circuit that produces an output signal proportional to the phase difference of the input signals. There are several ways of implementation, ranging from multipliers to state machines. A more detailed exposition of the alternatives can be found in [1, 17, 18].

For this work, a phase detector that can detect very small delay variations, in the order $30 \pm 2\ ps$, is needed. Most of the alternatives found in literature are suitable for PLL systems where a frequency divider brings a low frequency signal that the phase detector can handle. Actually, it is difficult to get a signal of significant amplitude for a small delay variation.

The approach adopted in this work is taken from [9], and corresponds to the use

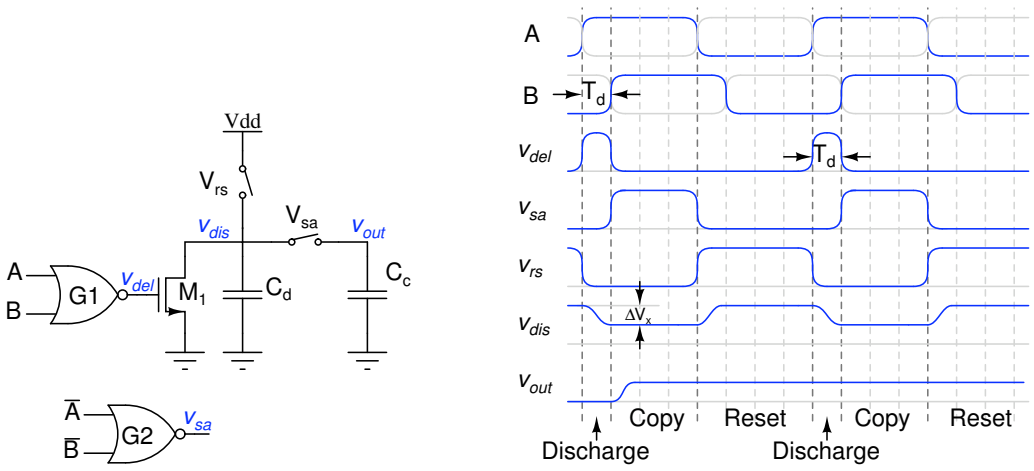
of the discharge of a capacitance with a pulse dependent on the delay T_d between two signals A and B. Figure 2.11(a) shows the used phase detector and the waveforms that help to explain the operation, which is divided in three phases: **discharge**, **copy** and **reset**.

In the **discharge** phase the NOR gate G1 generates a pulse v_{del} with duration equal to T_d, this signal turns on the transistor M_1 that discharge the node v_{dis} from V_{dd} an amount of voltage ΔV_x that depends on T_d (the bigger T_d, bigger is ΔV_x) . After that, in the **copy** phase, the signal V_{sa} generated by the NOR gate G2 closes the switch and the voltage in V_{dis} is copied to V_{out}. Finally, in the **reset** phase, the node V_{dis} is pulled to V_{dd} with the switch controlled by V_{rs}.

Additional issues about this implementation are:

- Some layout considerations need to be taken into account. Any capacitance unbalance may cause phase offset. In order to give symmetrical load to the RVCO, a differential logic must be used.

- Logic Gate must react with delays in the order few tens of picoseconds.



(a) Circuit. (b) Waveforms.

Figure 2.11: Delay Detector.

2.6 Charge Pump and Loop Filter

Every output signal of the delay detectors has to be compared with the reference delay signal V_{ref}, as seen in section 2.1 (Figure 2.1(a)). This comparison allows to decide whether to charge or discharge the control voltage of the delay cells to make them faster or slower. The circuit used for this function is the charge pump illustrated in Figure 2.12. This circuit compares V_{ref} with $V_{\Delta i}$ and by means of the output current I_{CP} indicates if the loop filter is charged or discharged. When the voltage V_{ref} is larger than $V_{\Delta i}$, $I_3 - I_2 > 0$ and the loop filter is charged. When $V_{\Delta i}$ is larger, $I_3 - I_2 < 0$ and the loop filter is discharged.

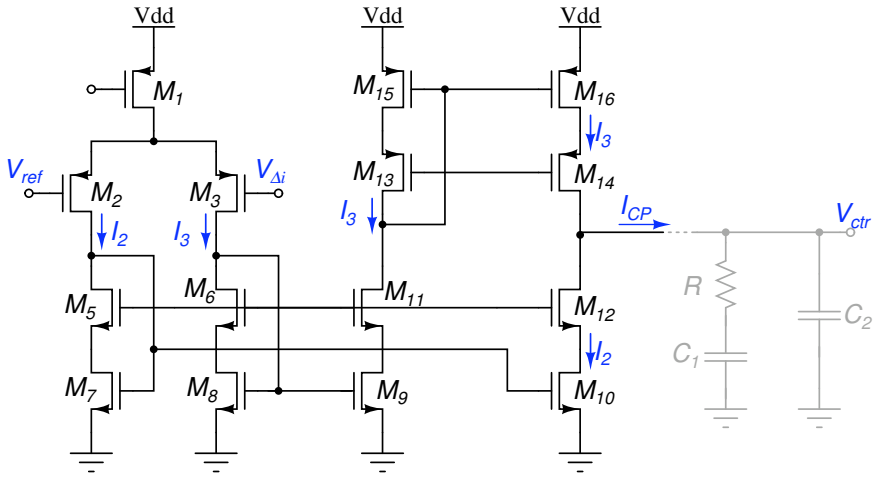


Figure 2.12: Charge Pump.

After the charge pump, a loop filter that converts the current signal I_{CP} into the voltage signal V_{ctr} that controls the oscillator is required. The used loop filter (Figure 2.13) corresponds to a second order passive low pass filter with transimpedance transfer function defined by equation (2.3). The position of the poles and zeros of the loop filter should be selected considering the dynamics and stability of the loop.

$$F(s) = \frac{V_{ctr}}{I_{CP}} = \frac{1 + s\,C_1\,R}{s\,(C_1 + C_2)(1 + s\,C_s\,R)} \tag{2.3}$$

$$\text{where} \qquad C_s = \frac{C_1\,C_2}{C_1 + C_2}$$

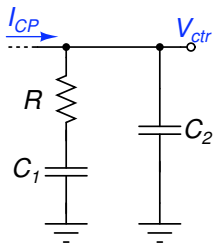


Figure 2.13: Loop filter.

2.7 Conclusions

In this chapter, the building blocks of the delay control system for the different phases of the ring oscillator are selected. Regarding the type of ring oscillator it is chosen a pseudo differential architecture with a negative resistance based tuning method. The selected delay detector is based on the discharging of a capacitor through a pulse-width dependent on the delay between adjacent phases. For the charge pump a comparator whose output current is proportional to the delay between adjacent phases is selected, and for the loop filter a passive second order low pass filter is chosen. With this set of functional blocks, in the next chapter more details and results of the implementation of the whole system are presented.

Chapter 3

Design and Simulation Results

In this chapter, some implementation details, along with the simulation results of the functional blocks presented in chapter 2, are presented. The verification and characterization of the basic blocks and the designed system is effectuated in *Spectre* using the UMC 0.18 μm Mixed Mode and RF CMOS technology.

The goal of the presented simulations is to verify the utility and limitations of the proposed system and determine the maximum phase error of the ring oscillator without the correction system, and its comparison with a similar oscillator including the correction mechanism.

3.1 Ring Oscillator

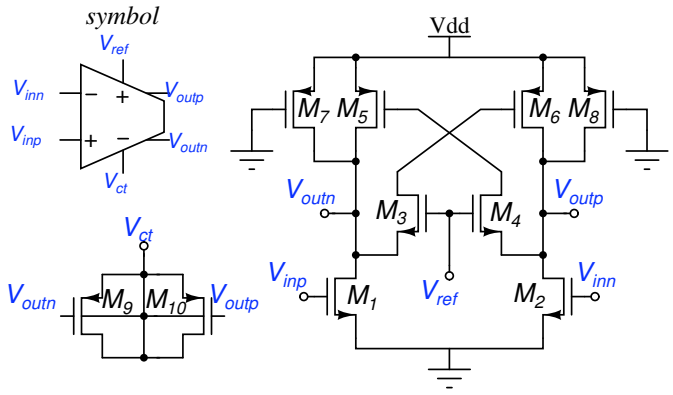
In the previous chapter, a delay cell with dual tuning method is selected. The used coarse tuning is based on a negative resistance scheme controlled by the voltage reference V_{ref}. On the other hand, the fine tuning is based on the capacitance control of a PMOS varactor, by means of the control voltage V_{ct}.

In order to consider the load of subsequent stages, the delay cell is designed for a typical load capacitance of 150 fF[1]. Transistors dimensions used for the delay cell are

[1]For each delay cell the load capacitance comes from the output buffers and the following delay cell.

summarized in Figure 3.1. It is important to emphasize that transistors M_1 and M_2 determine the high to low propagation delay t_{pHL}, while M_{5-8} determines the low to high propagation delay t_{pLH}. Transistors M_3 and M_4 act as pass transistors, which depending on the value of the voltage V_{ref}, set the maximum gate voltage and the maximum current capacity of transistors M_5 and M_6. This tuning method is used to modify the delay between input and output of the cell.

As an example, a reference voltage $V_{ref} > V_{tnM_{3,4}} + V_{dsM_{1,2}}$, produces an increment in the gate source voltage $V_{gsM_{3,4}}$, this brings to an increment in the maximum gate voltage and a reduction in the overdrive and current capacity of transistors M_5 and M_6. As a consequence the speed of the cell is reduced due to the smaller charging current of the output node.

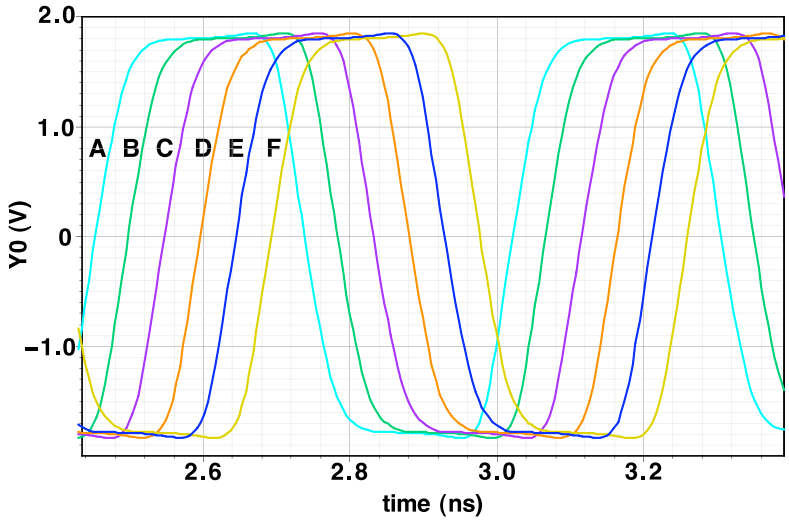


Variable	Value [μm]
W_{M1-M2}	25
W_{M3-M4}	3
W_{M5-M6}	17
W_{M7-M8}	30
W_{M9-M10}	30
L	0.18

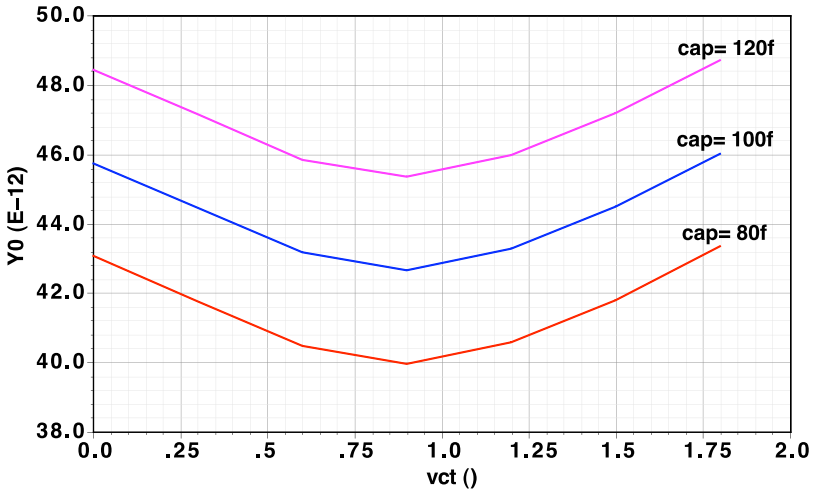
Figure 3.1: Dimensions of the delay cell.

Simulation Results of the Ring Oscillator

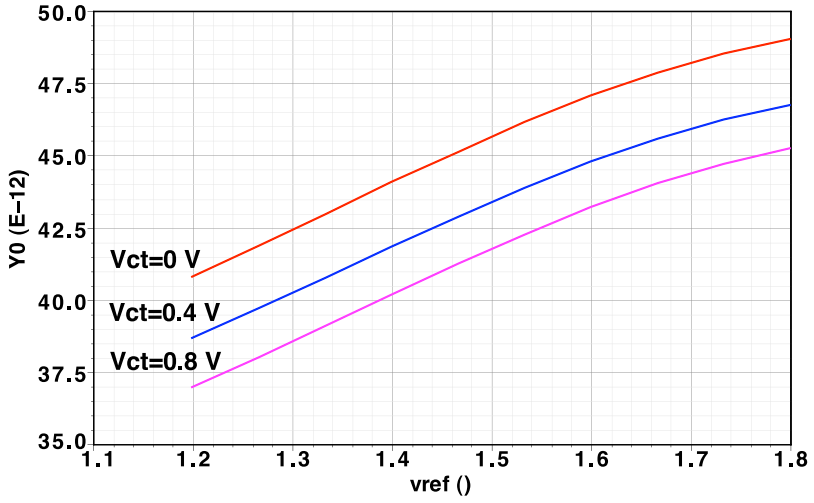
Some transient simulations help to validate the operation of the oscillator. Figure 3.2(a) shows the transient response of the ring VCO running at 1.8 GHz, where multiphase outputs with a signal swing of 1.8 V can be appreciated. From this typical transient response, several measurements can be done for the delay between adjacent phases. In the case of the balanced ring oscillator, the delay is calculated based on the frequency of oscillation by means of equation (2.2). In the case of the unbalanced ring, the delay is measured, independently in every phase, as the minimum difference of time between



(a) RVCO transient response.



(b) T_d vs C_L



(c) T_d vs V_{ref}

Figure 3.2: Transient response and delay measurements in the RVCO.

the zero crossing instants of two adjacent phases.

In order to verify the tuning range and the effect of load unbalance in the oscillator, simulations with variation of V_{ref}, V_{ct} and C_L were done. Figure 3.2(b) shows the delay tuning characteristic versus V_{ct} for some values of load capacitance with a fixed $V_{ref} = 1.3$ V. In the family of plots presented in Figure 3.2(b), **an increment of almost 2.3 ps in the delay for a load increment of 20 fF in C_L is observed**. Further simulations, effectuated with other values of V_{ref} shows that this behaviour is independent of the value of V_{ref}.

From the above consideration, it is clear that layout routing is critical for the spacing between adjacent phases, because unbalance in the loads of the order of 10 fF can produce an error of 1 ps.

Figure 3.2(c) shows the delay dependence with respect to V_{ref}. Frequency tuning range presented in Figure 3.3 is related with the delay of Figure 3.2(c) by the equation (2.2). For the designed ring oscillator, the frequency tuning range runs spans from 1.7 to 2.25 GHz. This frequency range is basically determined from the coarse control signal V_{ref}.

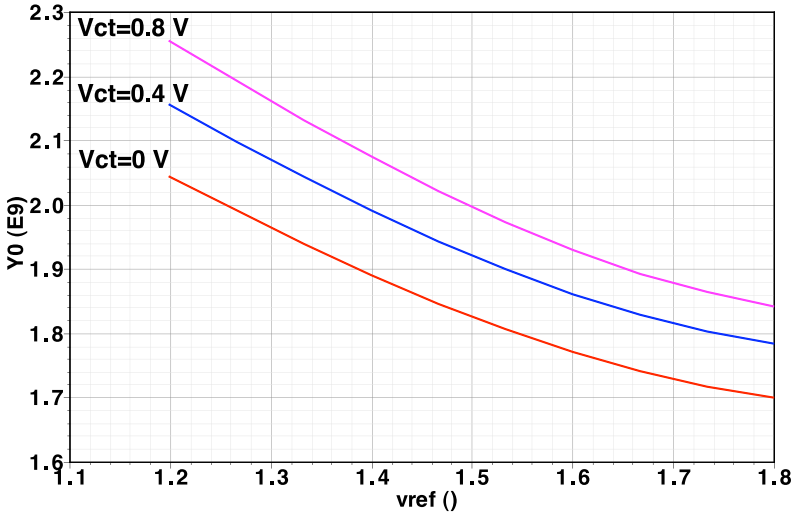


Figure 3.3: Frequency tuning curve vs V_{ref}.

It is worth to mention about the non monotonic dependence with respect to V_{ct}. This kind of dependence is due to the capacitance behavior of varactors. The main

consequence of this phenomenon is the possibility of locking in any of the pair of voltages that meets the same delay. In the design and synthesis of the full system, the definition of a range in which the delay behaviour is monotonic is necessary.

Spectral purity and delay mismatch

In order to characterize the accuracy between adjacent delays taking into account noise and mismatch, phase noise, jitter and Montecarlo simulations were effectuated respectively. The results of phase noise analysis are presented in Figure 3.4, where a value of 101.13 dBc/Hz at 1MHz offset from the fundamental oscillation frequency of 1.93 GHz is obtained. Moreover, a noise transient analysis[2] shows a peak to peak jitter of 700.29 fs. Finally, a Montecarlo analysis of 100 runs, setting $V_{ref} = 1.7$ V and $V_{ct} = 500$ mV, is done. The results are presented in Figure 3.5(b) and summarized in Table 3.1, where an average value of 44.62 ps and a standard deviation of 1.73 ps for the different delays of interest can be noticed.

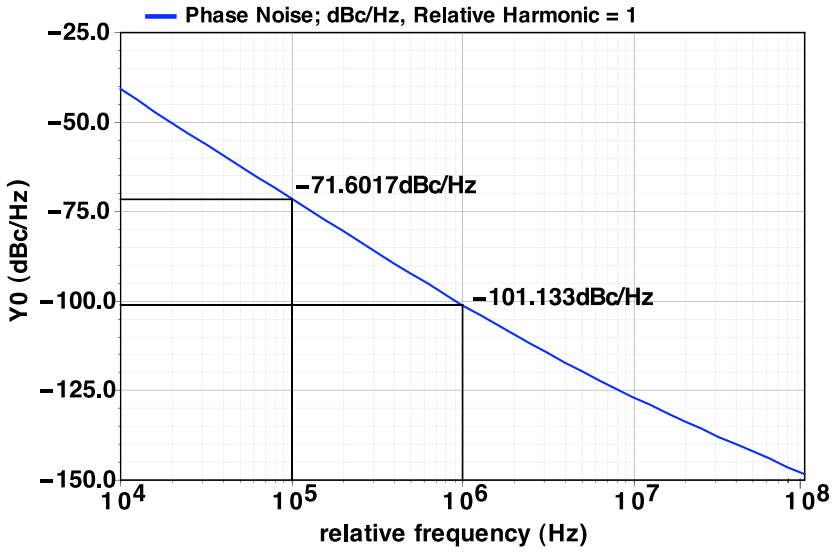
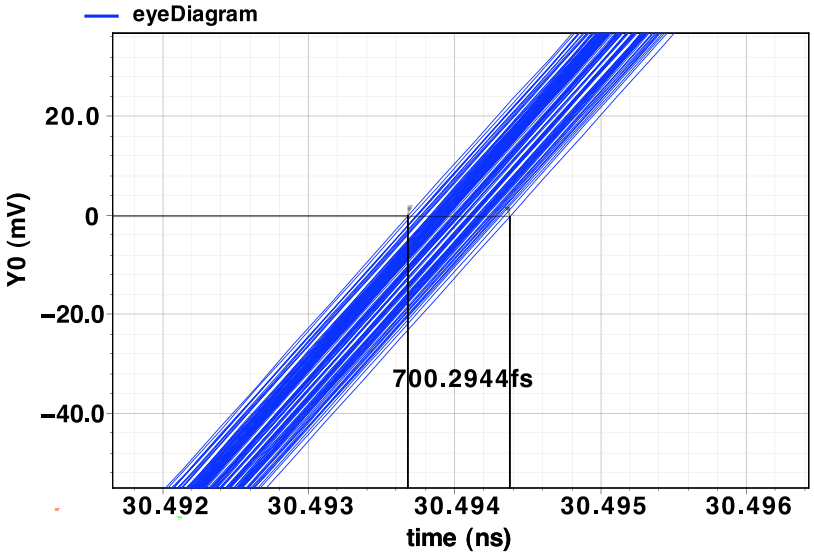
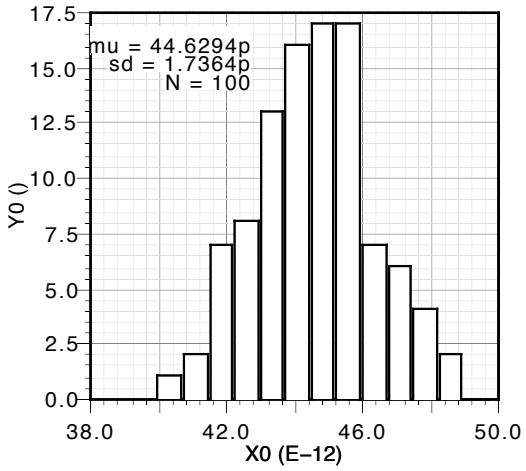


Figure 3.4: Phase Noise.

[2]See Appendix A for a description of this kind of analysis



(a) Eye Diagram.



(b) Montecarlo run for T_d.

Figure 3.5: Jitter and delay mismatch.

	AB	BC	CD	DE	EF	FA
Average [ps]	44.59	44.65	44.61	44.63	44.62	44.63
Std Deviation [ps]	1.799	1.736	1.782	1.732	1.736	1.756

Table 3.1: Montecarlo run for T_d

3.2 Delay Detector

As it was mentioned in the previous chapter, a delay detector based on the discharge of a capacitor is used in order to give a DC voltage in function of very small delays. This kind of delay detector can be modeled with a simple model based on the relation between current and voltage variation in a capacitor $\left(I \approx C\frac{\Delta V}{\Delta t}\right)$. It is necessary to consider that when a capacitor C is discharged with a current I, the amount of voltage drop in a time interval Δt can be approximated to:

$$\Delta V \approx \frac{I}{C}\Delta t \tag{3.1}$$

This relation helps to define the value of the current I and the capacitance C in order to reach the desired sensibility in the delay detector.

The implemented delay detector is shown in Figure 3.6. To generate the signals showed in Figure 2.11(b), it is necessary to take into account the inherent delay in every used cell. The implemented delay detector is composed by a NOR logic cell G_1, a pair of inverter chains B_1, a transmission gate X_1, a reset transistor M_2, a discharging transistor M_1, a storage capacitor C_d and an output capacitor C_c. The value of C_d and C_c are chosen to be 70 fF and 60 fF respectively. However, this values may need to be redefined after layout and parasitic extraction.

An example of the transient response of the delay detector for a delta difference of $\Delta T_d = 40ps$ in two signals running at 2 GHz is shown in Figure 3.7. The high and width of the pulse ***vdel*** is dependent on the difference in time between ***ap*** and ***bp***, this pulse ***vdel*** drives the amount of discharge of node ***vdis***. After the discharge, the voltage stored in node ***vdis*** is copied to ***vout***.

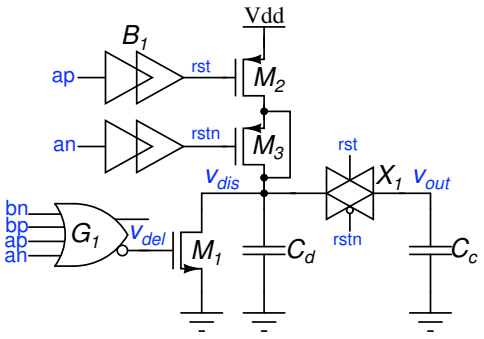


Figure 3.6: Implemented delay detector.

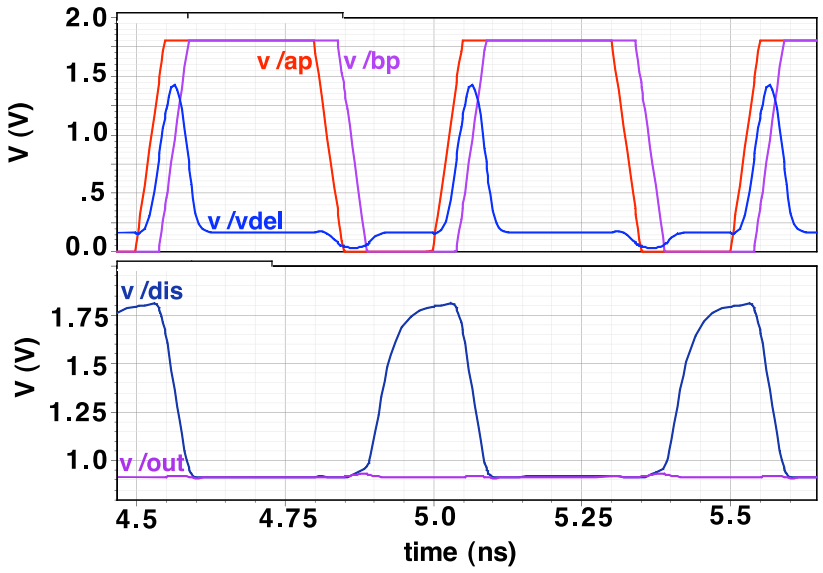


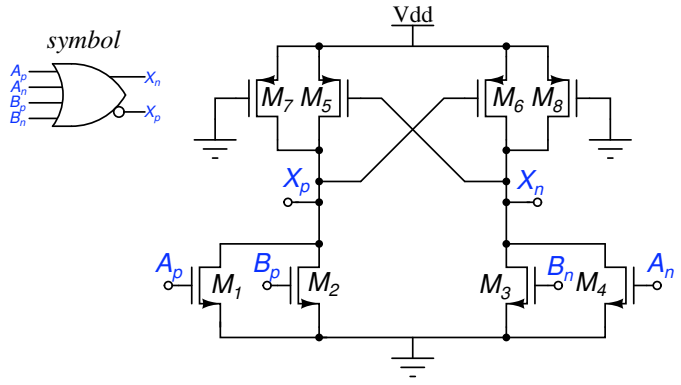
Figure 3.7: Delay detector transient response.

Basic Blocks of Delay Detector

The first block used to implement the delay detector is the **NOR logic gate**. This circuit must generate a significant pulse from a small delay. In order to give the oscillator a constant load capacitance in every phase, a differential DCVSL logic is used. The used dimensions for every transistor are summarized in table 3.8(a). Transistors $M_{7,8}$ are added to give faster low to high transitions and lower t_{pLH}; in this way, equal t_{pLH} and t_{pHL} can be equalized.

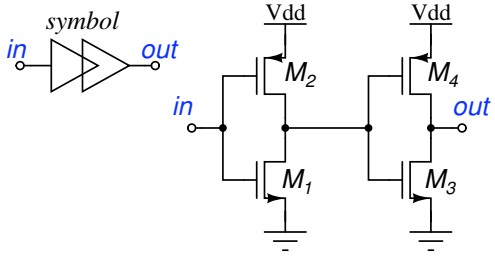
The **inverter chain** will provide the ***rst*** signal for the reset transistor (M_2 in Figure 3.6). Figure 3.8(b) shows the used dimensions. Two inverter chains are used in order

give equal capacitive load to the ring core. In the **transmission gate** and the reset transistor M_3, dummy switches are used to reduce the effect of charge injection. By rule of thumb, the size of the dummy transistor is half the size of the switch transistor [16].



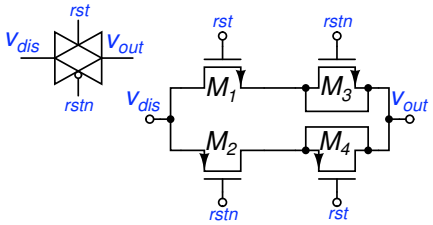
Variable	Value [μm]
W_{M1-M2}	30
W_{M3-M4}	30
W_{M5-M6}	20
W_{M7-M8}	13
L	0.18

(a) NOR gate.



Variable	Value [μm]
W_{M1}	8.2
W_{M2}	16.4
W_{M3}	15
W_{M4}	30
L	0.18

(b) Inverter chain.



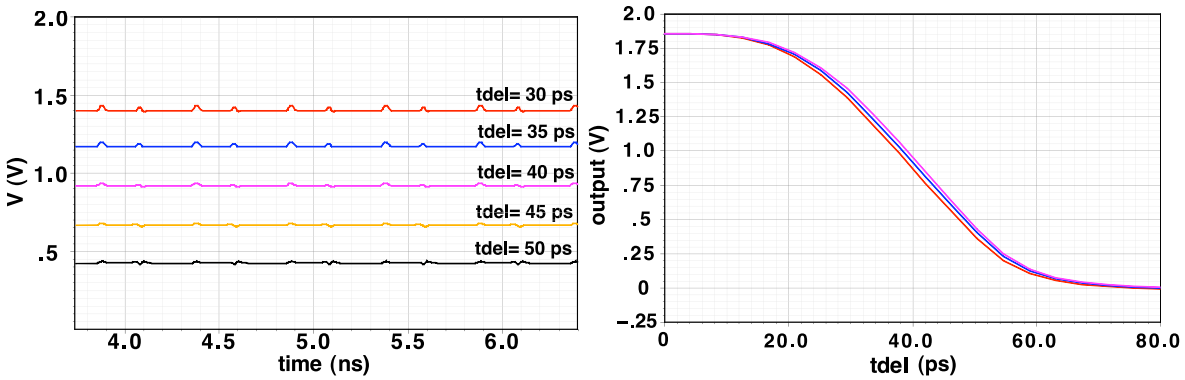
Variable	Value [μm]
W_{M1}	3
W_{M2}	3
W_{M3}	1.5
W_{M4}	1.5
L	0.18

(c) Transmission gate.

Figure 3.8: Dimensions of the delay detector.

Simulation Results of Delay Detector

A transient simulation for several values of delay in the input signals allow to determine the detection range and the linearity of the delay detector. Figure 3.9(a) shows the transient response of the output signal in function of the input delay. A voltage range from 0.4 to 1.4 V for input delays from 30 *p*s to 50 *p*s can be observed. The ripple in the output signals is due to the reset and copying switching. In order to attenuate this ripple, an increment in the output capacitor is required. By using the average value of the obtained output signals, a delay to voltage transfer characteristic can be estimated (Figure 3.9(b)).



(a) Transient response

(b) Average vs delay

Figure 3.9: Output variation vs delay.

3.3 System Characterization

The full implementation of the whole system is shown in Figure 3.10. It is important to mention the use of additional buffers to regenerate the output of the RVCO and keep symmetrical the capacitive load. Additionally, a careful connection of all the differential phases with the correct polarity is necessary in order to prevent error in delay detection an correction.

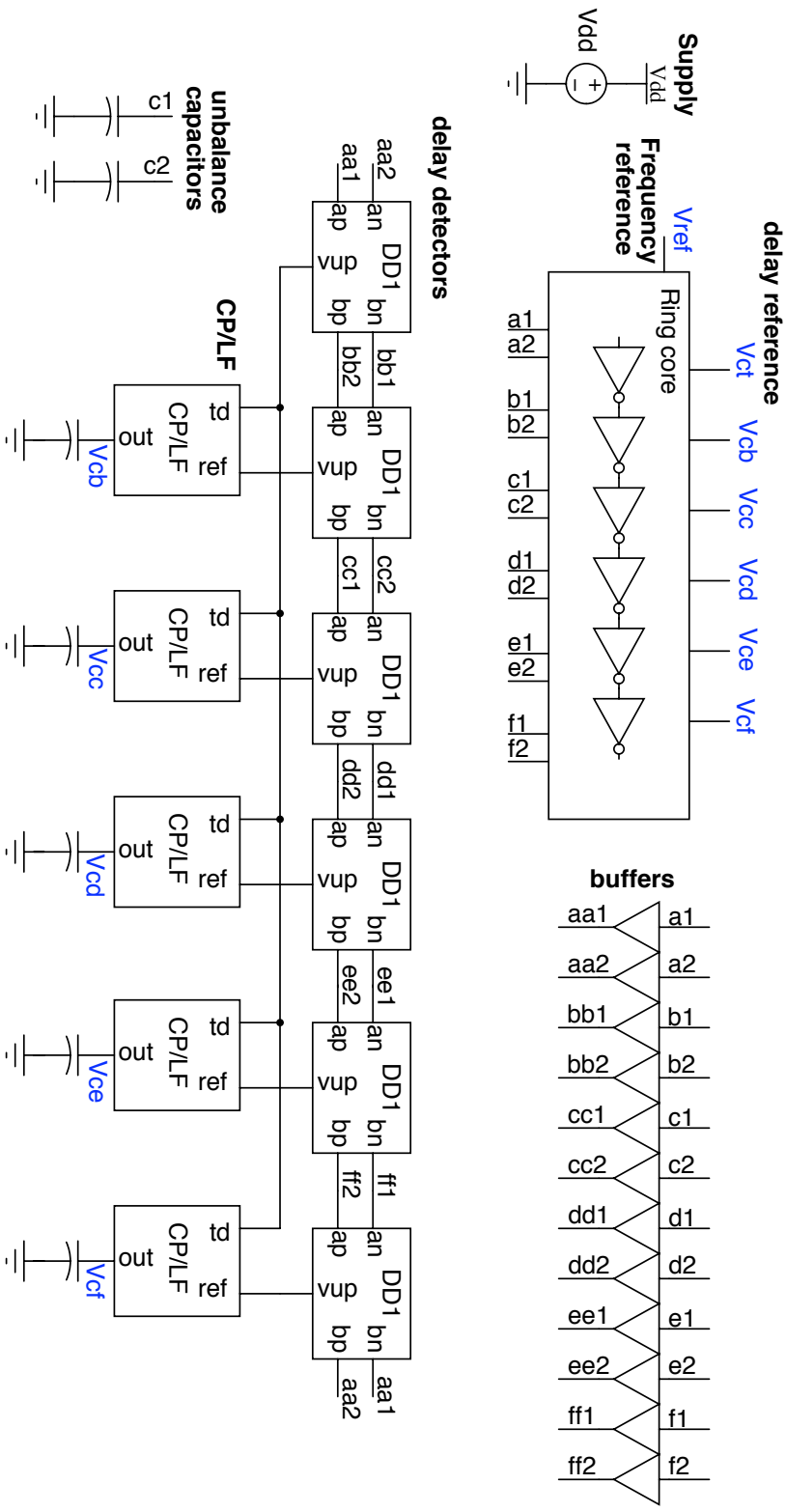


Figure 3.10: Implemented multiphase clock generation system.

To verify the operation of the system, a transient simulation of the delay detectors response is done. This response is presented in the Figure 3.11, which shows how the system can correct and equalize the delay between the different phases of the ring. The time required for this correction corresponds to 25 ns.

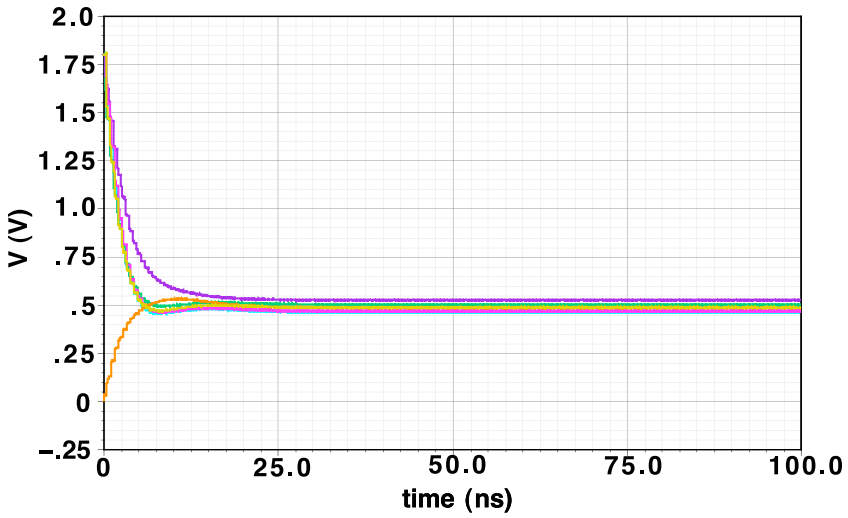


Figure 3.11: Delay detectors transient response.

With the purpose of characterize the accuracy between adjacent delays taking into account capacitive unbalance and mismatch, three main tests were applied in simulation. These test are explained below:

- **Capacitive unbalance** the first is a transient analysis with some capacitive unbalance on the loads of the ring oscillator. In this test, capacitors of 5 fF, 10 fF, 15 fF, and 20 fF were added to the C phase of the ring. These values corresponds to typical values of capacitance unbalance after layout routing. The corresponding delay in the different phases is summarized in Table 3.2. It is important to notice that the system can correct static phase errors caused by capacitive non-symmetry in the loads, this correction can be accomplished for capacitive unbalances up to 15 fF.

- **Noise transient analysis** A transient noise analysis is done in order to verify the effect of noise on the transition instant of the multiphase outputs. Figure 3.12

	T_{AB} [ps]	T_{BC} [ps]	T_{CD} [ps]	T_{DE} [ps]	T_{EF} [ps]	T_{FA} [ps]
$C_L = 0\,fF$	44.91	44.83	44.84	44.84	44.83	44.87
$C_L = 5\,fF$	44.75	44.98	44.75	44.83	44.83	44.85
$C_L = 10\,fF$	44.74	45.13	44.72	44.80	44.81	44.91
$C_L = 15\,fF$	44.85	45.24	44.75	44.78	44.81	44.90
$C_L = 20\,fF$	44.71	45.80	44.81	44.74	44.81	44.94

Table 3.2: Delays for capacitance unbalance for the whole system.

shows the eye diagram for the system, where a peak to peak jitter of 1.399 *p*s is achieved.

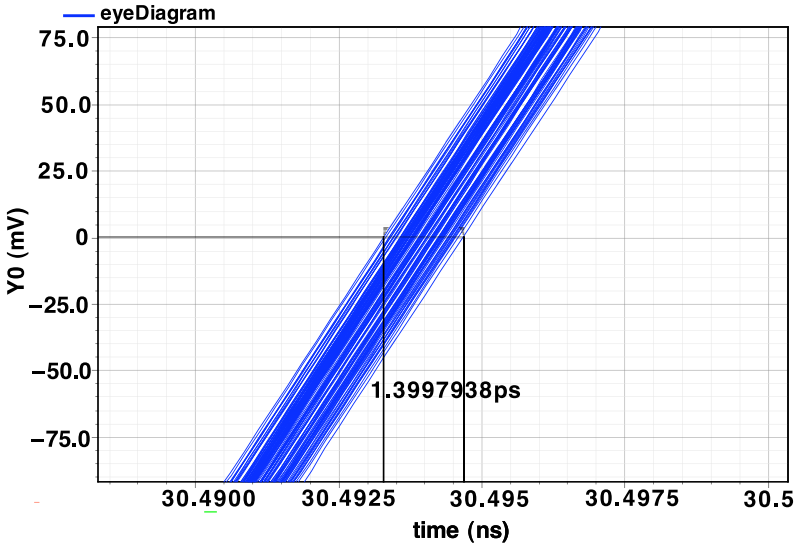


Figure 3.12: Eye diagram for the close loop system.

- **Montecarlo analysis** Finally, a Montecarlo analysis is used in order to verify the variation of the different delays of the ring. In this test, 100 simulations with 3σ process and mismatch variations were effectuated, keeping $V_{ref} = 1.7$ V and $V_{ct} = 500$ mV. The results are presented in Figure 3.5(b) and summarized in Table 3.3, which shows an average value of 44.62 *p*s and a standard deviation of 1.73 *p*s for the different delays of interest. This result is similar to that of the isolated RVCO because of the effect of mismatch in the loop components, i.e.

delay detector, charge pump and loop filter.

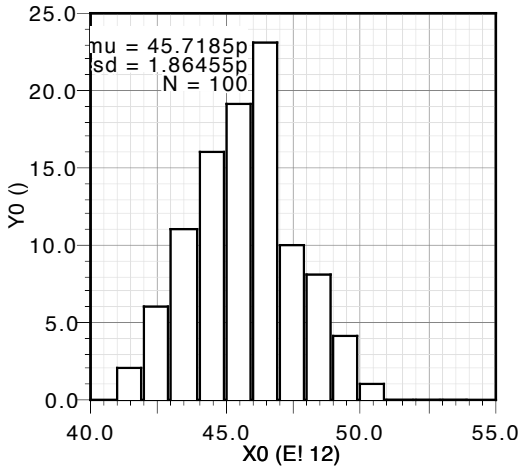


Figure 3.13: Montecarlo run for T_d for the whole system.

	AB	BC	CD	DE	EF	FA
Average [ps]	44.69	45.95	45.78	45.96	45.71	45.95
Std Deviation [ps]	1.755	1.924	1.854	1.910	1.864	1.902

Table 3.3: Montecarlo run for T_d for the closed loop system.

3.4 Summary of results

The designed six-phase clock generation system, can operate in a frequency ranges that spans from 1.7 to 2.25 GHz with an delay accuracy of 1.86 ps against mismatch, peak to peak jitter of 1.4 ps and a compensation of capacitive unbalances up to 15 fF. The systems consumes 150 mW.

Chapter 4

Conclusions and Future Work

4.1 Conclusions

From the process carried out in this research project, several conclusions can be drawn.

- Ring oscillators are suitable for multiphase clock signal generation; however, their structure is based on identical inverter stages. Some careful design is required in the critical aspect of uniform load capacitance for the different phases. The selection and connection of the subsequent stages must guarantee the same load for all the phases to prevent error in subsequent delay detection an correction.

- The simulation results of the whole system shows that DDLL is a good alternative in terms of reduction of load capacitance unbalance. However for mismatch in the different inverter stages the technique is limited, basically for the mismatch sensibility of the different blocks of the control loop.

- Obtain accuracy in the use of very small delays is a complicated task, mainly limited by the mismatch in the building blocks of the loop and the jitter originated by the different noise sources of the system.

- Very low delay detection is restricted by the speed of the functional blocks, layout symmetry, mismatch and jitter. The delay detector proposed in this work can be

exploited at higher speed; however, some problems concerned with the generation of the clock signals for the switches, and the uncertainty in the capacitor values of the storage and output capacitor are aspects that need to be taken in account.

- For high speed operation in logic blocks, an excessive increase in the size of the transistors, looking for an increment in the speed, causes the predominance of parasitic capacitances that degrade the speed. Typically there is a maximum size for the transistors to which a further increase reduces the operation speed.

4.2 Future Work

As part of future activity and research in the topic of Multiphase clock generation systems, it is suggested:

- Fabrication and experimental test of the proposed system.
- Research and work in the implementation of MPCG based on DCOs. It is expected that the use of digital control techniques gives more robustness to process, voltage and temperature variations. However, this kind of implementation generally requires of more area and power.
- Evaluation and use of time to digital converters in order to implement the delay correction system. For example, in the literature, the implementation of a family of circuits called delay amplifiers can be found. This kind of circuits have the potential to relax the specifications of some blocks in the control loop of a DLL and improve the temporary resolution [19].
- An interesting subject for future very high speed applications is the use of distributed techniques to design mm-wave circuits. It is recommended the design for solutions for multiphase clock in the range of mm-wave.

Appendix A

Jitter: "The Effects of Noise Visible in Time Domain"

In chapter 1, it is stated that the main causes of delay error in a MPCG are static and dynamic phase errors. **Static phase errors** are caused by mismatch between stages and load unbalance. On the other hand, **dynamic phase errors** are related to jitter, which is defined as the uncertainty in the time events, generally the transition of a signal. Jitter originates big problems in high speed circuits, and imposes a performance limit in electrical systems that everyday use higher and higher signal rates.

Jitter can be specified in several ways, and the classification can be done based on different points of view. For example, in the literature it is distinguished between edge to edge, cycle to cycle and long term jitter. Also, depending on the nature of the circuit block or system there are defined synchronous and accumulating Jitter [2].

Given the importance of jitter in high speed MPCG systems, in this appendix, a review of basic theory and simulation methods for jitter is done. This review gives a theoretical framework for the analysis and simulations made in chapter 3.

A.1 Definition and Specification

A signal with jitter $v_n(t)$ can be modeled as a noiseless periodic signal $v(t)$ with a variable time delay $j(t)$, where j corresponds to a zero-mean stochastic process characterized by an standard deviation σ_j, which can be expressed in terms of peak to peak or rms jitter. As a form of noise, jitter must be treated as a random process and characterized in terms of statistical quantities, such as variance and standard deviation.

$$v_n(t) = v(t + j(t)) \tag{A.1}$$

A.2 Jitter Classification

Based on the measurement method, jitter can be classified in:

- **Edge-to-edge jitter:** As seen in Figure A.1, edge to edge jitter J_{ee} is the variation in the delay between a triggering event and a response event. It is only valid for input driven circuits, not for autonomous systems like oscillators.

Figure A.1: Edge to edge jitter. [2]

- **Long-term or k-cycle jitter:** is a measure of the uncertainty in the length of k cycles. The standard deviation of the length of a single period, is often referred to as the period jitter.

- **Cycle-to-cycle jitter:** Let $T_i = t_{i+1} - t_i$ to be the period the i-th cycle. Then the cycle-to-cycle jitter J_{cc} is the uncertainty in the length T_i.

Based on the nature of the block, the jitter produced in PLLs can be classified in two forms:

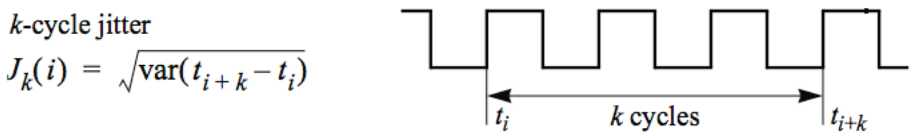


Figure A.2: Long-term or k-cycle jitter. [2]

Figure A.3: Cycle-to-cycle jitter. [2]

- **Synchronous jitter** is present in circuits where a transition in the output is a consequence of a transition in the input, for example phase-frequency detectors PFD, Charge pumps CP and frequency detectors FD. In this case jitter corresponds to the variation in the propagation delay between the input and the output of the circuit.

- **Accumulating jitter** is the jitter present in autonomous circuits such as oscillators. In autonomous circuits output transitions are not result of transitions at their inputs, but rather are result of the previous transition in the output. In this case, jitter is a variation in the delay between an output transition and the subsequent output transition.

A.3 Sources of jitter

In general, several factors can give rise to jitter. [20] identifies and quantifies the effect of broadband noise, phase noise, spurs, slew rate and bandwidth over jitter performance. A complete jitter analysis taking into account these sources predict that the total jitter corresponds to the sum of all the components, as described in equation (A.2).

$$Jitter^2_{\text{Total}} = Jitter^2_{\text{Noise floor}} + Jitter^2_{\text{Phase noise}} + Jitter^2_{\text{Spur}} \tag{A.2}$$

A.3.1 Broadband noise

Broadband noise or noise floor corresponds to the intrinsic noise in every circuit component. It is due to discrete or random movement of charge in the devices. In semiconductor devices, it is common to find noise modelled as thermal noise, shot noise, flicker noise, etc. The effect of a voltage variation Δv in the crossing instant is approximated to [2, 20]:

$$Jitter^2_{\text{Noise floor}} = \frac{v_{n\text{RMS}}}{S} \tag{A.3}$$

A.3.2 Phase noise

Due to the limitations of most jitter-measuring equipment, it is often easier to characterize the purity of a low-noise signal by measuring its phase noise in the frequency domain, rather than measuring jitter in the time domain. It is important to find a link between jitter and phase noise specification, [20] proposes equation (A.4) to quantify periodic jitter in terms of the Lorentzian $L(f)$ integrated in the range of $-f_{offset}$ to f_{offset}.

$$Jitter^2_{RMS}(\tau) = 8\frac{T_o^2}{4\pi^2}\int_0^{f_{\text{offset}}} L(f)\sin^2(\pi f\tau)df \tag{A.4}$$

A.3.3 Spurs

The effect of crosstalk from nearby circuits, supply coupling and defects in the reference can be seen in the frequency domain with the rise of spurs at determined frequencies. An expression for the relation between frequency domain spurs and jitter can be deduced with a similar analysis to that performed with phase noise [20].

$$Jitter^2_{RMS}(\tau) = 4\frac{T_o^2}{4\pi^2}\sum_n L(f_n)\sin^2(\pi f_n\tau)df \tag{A.5}$$

A.4 Jitter Estimation

Jitter estimation can be done with the analysis presented in [14]. The method consists of the following steps:

- Calculate an expression for the noise-free output $v(t)$.
- Calculate the slope $S(t) = \frac{dv(t)}{dt}$.
- For the noisy output, calculate the rms voltage noise σ_v at the threshold crossing time.
- Using the slope $S(t)$ and the rms voltage noise σ_v, determine the rms jitter σ_t with the expression $S(t) = \frac{\sigma_v}{\sigma_t}$.

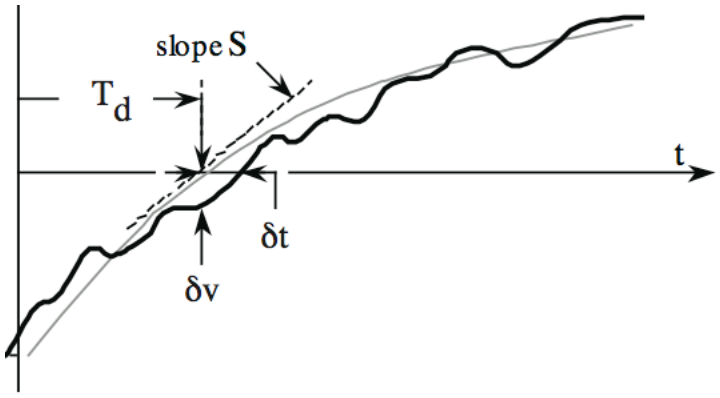


Figure A.4: Relation between jitter and noise voltage.

A.5 Jitter Simulation

Jitter simulation can be done with a transient noise analysis, a circuit analysis that tries to estimate the solution of the stochastic differential equation that models the circuit operation. The approach commonly used for this kind of analysis is to set a regular transient analysis, and then evaluate the noise models and inject the random device

signals at each time step [21]. In these days, noise transient analysis is incorporated by several simulators like HSpice or Spectre.

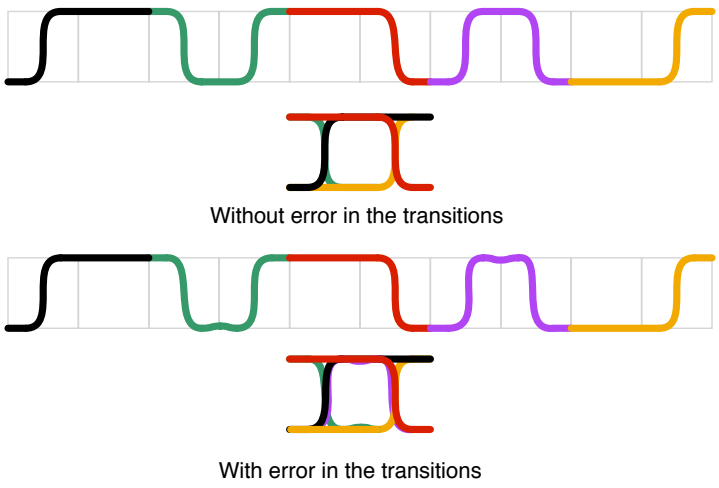
In Chapter 3, transient noise simulations were effectuated in order to estimate the jitter in the ring oscillator and the whole system. For a proper simulation, a frequency range of interest for the noise models is required. This frequency range is set with two parameters called `noisefmax` and `noisefmin`. The value of `noisefmax` is recommended to be fixed in a value higher that the circuit bandwidth and the stop time of the transient analysis in a sufficiently large value in order to sample low frequency noise correctly [21].

After the transient noise analysis, jitter can be evaluated in several forms, Cadence calculator can estimate the period in function of each cycle of oscillation or give an Eye Diagram, a useful tools for the analysis of jitter explained below.

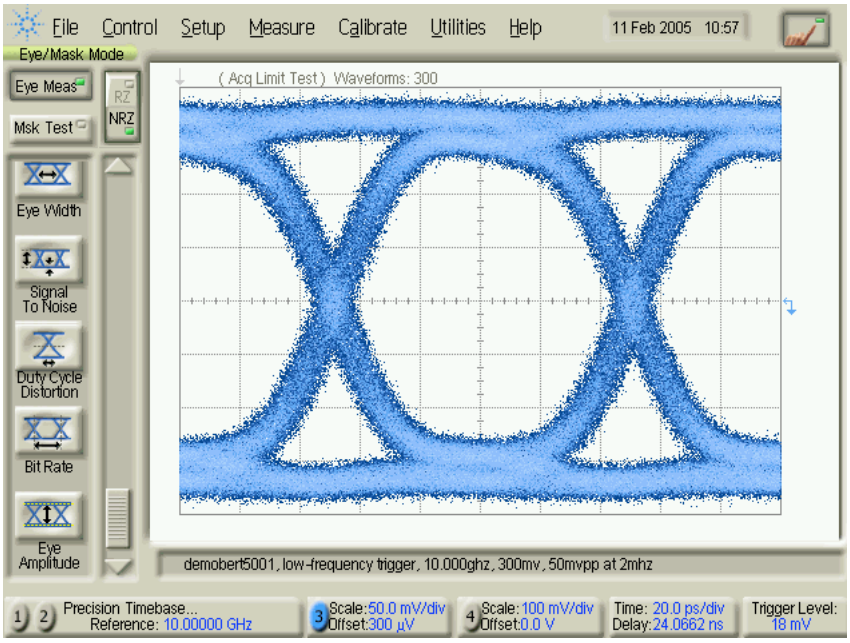
A.5.1 Eye Diagram

The eye diagram is a useful tool for the qualitative analysis of signal used in digital transmission. It provides a quick evaluation of system performance and can offer information about the nature of channel imperfections and a first-order approximation of signal-to-noise, clock timing jitter and skew. An eye diagram is created when many short segments of a waveform are superimposed such that the nominal edge locations and voltage levels are aligned. Figure A.5(a) shows an example of eye diagram for a signal without error and with error in the transitions. In the former, the transitions are aligned in the eye diagram, in the case of any error in the transitions, the transitions in the eye diagram are not aligned.

In chapter 3, eye diagrams are used in order to estimate the tolerances of the delays between all the different phases. It is worth to notice that the transient noise analysis only takes into account the noise that comes from the devices (broadband noise), nor the noise from other sources depicted in section A.3.



(a) Generation.



(b) Example of lab measurement.

Figure A.5: Eye Diagram.

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