Synthesis of Piece-Wise Linear Functions and its Application to Chaotic Oscillators

by

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In partial fulfillment of the requirements for the degree of

MASTER IN SCIENCES WITH SPECIALLITY IN ELECTRONICS

in the

National Institute of Astrophysics, Optics and Electronics
July 2008
Tonantzintla, Puebla

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Abstract

Although chaotic systems were first introduced to describe dynamical behaviors by modeling natural complex phenomena, they have been an important subject of research during the last two decades mainly because of the growing of the computing available resources. Nowadays, chaos research is present in very different fields to model complex behaviors such as: behavior of the human being, the market prices until physical relations between celestial corps, the modeling of fluids dynamics and information encrypting.

As many phenomena in nature, most of the chaotic systems can be described and modeled by electrical circuits, which are then denoted as chaotic oscillators. There are several known forms to implement them, the majority of the electronic realizations are based on the use of operational amplifiers (Opamps) and in some cases, on more complex blocks like those which realize mathematical operations just as multiplication and division, with electrical signals mainly voltages.

Among all the kinds of chaotic oscillators, there is a set which only requires differential operators and the use of destabilizing functions known as "piece wise linear functions" or PWL functions. Such kinds of systems are among the simplest to be implemented by using electronic circuits; however, they are capable of achieving very complex dynamics. On the other hand, the implementation of PWL-based chaotic oscillators at the integrated circuit level, is becoming an important field of research. In this manner, this Thesis is devoted to implement such PWL-based chaotic systems using VLSI design techniques.

The main contribution of this work is related to the use of unity-gain cells to build

behavioral models and later to realize simulations using HSPICE and standard CMOS technology of $0.35\mu m$. This implies for an analog circuit designer to take into account practical considerations with respect to the limited dynamical ranges, the system bandwidth and other characteristics analyzed in the singular blocks which conform the chaotic oscillator.

Resumen

Si bien los sistemas caóticos fueron primero introducidos para describir comportamientos dinámicos por medio del modelado de fenómenos naturales complejos, han sido materia importante de investigación principalmente los últimos veinte años debido a la facilidad del procesamiento de datos que se ha desarrollado en materia de cómputo. Actualmente se desarrolla investigación en muy diversos campos para modelar comportamientos complejos como: las conductas y patrones del ser humano, la fluctuación de la economía hasta las relaciones físicas entre cuerpos celestes, el modelado de las dinámicas de fluidos y el encriptamiento de información.

Al igual que muchos otros fenómenos en la naturaleza, la mayoría de los sistemas caóticos se pueden describir y modelar por medio de circuitos, los cuales se denominan osciladores caóticos. Existen varias formas de implementarlos, la mayoría de las realizaciones electrónicas se basan en el uso de Amplificadores Operacionales (Opamps por sus siglas en inglés) y en algunos casos, bloques más complejos para realizar operaciones matemáticas tales como el producto o la división de señales eléctricas generalmente de voltaje.

Entre todos los tipos de osciladores caóticos hay un conjunto que puede ser realizado simplemente con las relaciones diferenciales entre sus variables y el uso de funciones desestabilizantes conocidas como "funciones lineales a tramos" o funciones PWL. Dichos tipos de sistemas están entre los más sencillos para realizar por medio de circuitos electrónicos; sin embargo, son capaces de producir dinámicas muy complejas. Por otro lado, la implementación de sistemas caóticos basados en técnicas PWL a nivel de circuito integrado se esta volviendo un importante campo de investigación. De esta forma, esta

tesis esta dedicada a implementar dichos sistemas caóticos PWL utilizando técnicas de diseño VLSI.

La principal contribución de este trabajo está relacionada con el uso de celdas de ganancia unitaria para construir modelos comportamentales y posteriormente realizar simulaciones usando HSPICE y una tecnología CMOS estandard de 0.35μm. Esto implica para el diseñador de circuitos analógicos el tomar consideraciones prácticas respecto de los rangos dinámicos limitados, el ancho de banda, y otras características analizadas en los bloques que conforman el oscilador caótico.

Acknowledgements

This work is dedicated especially to my wife Judith Onchi V. and my mother Ada Adela Guerra A.†, to all my family and close friends.

My most sincere gratitude for the guidance and encourage of my advisors, Dr. E. Tlelo Cuautle in INAOE and Dr. Carlos Sánchez L. in UAT, thanks for all their support.

I also want to thank Dr. Cesar Cruz, who welcomed me in CICESE, to Dr. Georges Gielen in KUL for his willing and to all my teachers as well as Dr. Murphy Arteaga, Martha Olmos, Cornelio Posadas and Ricardo Núñez and also to all the INAOE staff.

Thanks to all my partners and friends, specially to Francisco Sánchez, Ismael Cosme, Ivick Guerra, Heraldo Saez, Oriana de las Nieves and Manuel Pacheco.

And to the CONACyT (Consejo Nacional de Ciencia y Tecnología) for its essential support through the scholarship.

Contents

Chapter 1

INTRODUCTION

Chaotic systems have been extensively examined and studied by many people during the last two decades [1]. Some of the first dynamical systems were proposed in order to model observed natural phenomena; for example, the Lorentz system was modeling the convection heat in the atmosphere [2]. Using these equations, chaotic behavior has been probed according to mathematical criteria (Lyapunov [3, 4]) and computer simulations. Newer systems have started as differential equation sets disturbed by a specific signal to achieve chaos in different dynamics as shows Suykens [5], Yalçin [6]; or by a nonlinear relation generally polinomial, for instance Chen [7] and Rössler [8].

The physical realization of chaotic systems on laboratory conditions has been a subject of investigation in the field of electronics [9, 10, 11, 12, 13]. In electronics, differential equations have first been implemented in straight form using passive components and relating the currents or voltages observed, to the system variables. But the designed topology can change according to the used technique. This Thesis provides some descriptions using basic modular techniques in voltage and current mode.

Most of the chaotic circuits are characterized for having a nonlinear active component which enhances chaotic oscillations within some specific conditions, subject of previous mathematical research. There are many ways to achieve nonlinearity in circuit implementation. The most basic and straightforward are stair, hysteretic or saturated functions [1, 14]. This means that besides the need for differential relations, chaotic

systems require complex mathematical operations in time delaying or operations based in nonlinear relations.

The main concern of this Thesis is to provide chaotic oscillators with nonlinear functions in piecewise form to generate chaotic behavior as recently reported in mathematical research in the references of authors like Chua[15], Lü [14], Suykens [5] and Yalçin [6], to mention a few. In the following, chaotic systems will be described at the behavioral level down to the transistor level using a 0.35μm CMOS standard technology.

1.1 Chaotic Systems

A periodic oscillator is characterized for having a well defined waveform which is constantly repeated according to a period and does never establish in a single value. A chaotic oscillator is produced by a chaotic system and has no period. Chaotic systems are deterministic and dynamical [16, 17].

A deterministic system always reaches the same points starting from a specific condition (initial condition); this means that such system dynamics are reproducible. In contrast, a nondeterministic (stochastic) system can present different behavior each time that it is run-in.

A dynamical system is a system which evolves in time or in its own states. An n-order dynamical system is defined by the state equation $\dot{x} = f(x)$, $x(t_0) = x_0$, for autonomous or $\dot{x} = f(x,t)$, $x(t_0) = x_0$ for non-autonomous systems. Where $\dot{x}$ is the state at time t and f is the vector field which is time independent in the former case. The system can be linear or nonlinear according to f [16]. A classic chaotic system is a nonlinear deterministic autonomous dynamical system which shows apparently random behavior defined into some boundaries of its space of states. It is extremely sensitive to initial conditions; in practice, two equal systems will never have the same trajectories in a real circuit. Here, the main characteristics of chaotic systems are recalled, although there is not a formal definition for chaotic systems.

The word "trajectory" is used to denote the evolution of the different states of a dynamical system. These states are generally plotted one against another in the called

"phase plot", which gives more insight about the attraction points and boundaries. For chaotic behavior, attractors are called "strange attractors" or "scrolls" [18].

The Lyapunov exponent's spectrum gives a quantitative description of the divergence or convergence of system trajectories [3, 4]. A positive Lyapunov exponent is an indicator of the exponential divergence of the trajectories, and then a good indicator of the chaotic regimen of an arbitrary system. In practice, exponents are calculated numerically and plotted to show such zones in which the system manifest chaotic behavior. Wolf et al. [3] describe a well-known algorithm for doing so.

Chaotic systems and their classification are still in subject of research [19]. For the scope of this work, autonomous chaotic systems are classified from the point of view of the implementation circuit as:

- Those which are implemented using products between variables, quadratic or cubic terms or some polynomial destabilizing function of degree bigger than one. (Lorentz [2], Rössler [8], Chen [7]).
- Those which have no variable products in its terms and a piece wise linear function as destabilizing function. (Generalized Chua [5], Saturated multiscroll [14]).

This Thesis is focused in the second group. The main examples of such systems are cited below in order of scroll generation potential exhibition within the chaotic attractor.

- Chua's circuit
- Hyperchaotic coupled Chua's circuits
- Generalized Chua's circuit
- Saturated Multiscroll

1.2 Problem Description

In the field of generating strange attractors, the first physical limitation of electronic systems is the supply voltage used. This is easily overcome by scaling the equation

system. However, any circuit non-ideality will make the system to perform different from the expected chaotic dynamics, eventually loosing attractors for this limited range of work of practical circuits.

In order to achieve complexity, Chua's circuit has been expanded by modifying its nonlinear characteristic element, the Chua's diode [20, 21]. This element is an active component which enhances destabilization by showing two different negative conductance slopes. In a more recent application [10], Suykens has shown that Chua's diode can be modeled by a voltage controlled current source VCCS in parallel with an equivalent impedance (resistor) and adding segments to the nonlinear function of the diode (the VCCS) to obtain the generalized Chua's circuit, which exhibits progressively more attractors.

The Chua's system has been standardized to be destabilized by a 1x1 positive saturated function (a unity slope function limited by ± 1, [22]) thus making possible the use of active integrators (Opamps in voltage-mode for example) instead of the passive components. The nonlinearity can also be made by different approaches. The most popular is the Opamp-based [9], others are based in different elements such as CFOAs [23, 24], current conveyors [25], current operators [26, 27, 28, 29], operational transconductance amplifiers [30] or even digital complex systems [31].

The first hyperchaotic system was proposed by Rössler in 1979 [33]. However, simple oscillators like Chua's circuit can be coupled to obtain hyperchaotic oscillators, as showed Kapitaniak [32] in his work, weakly coupling two Chua's oscillators to produce a double-double-scroll attractor in the phase plane between states of both systems taken as one single system.

Another important finding has been made in applying piece wise linear (PWL) destabilizing functions to the systems reported by Yalçin et al. in [6] and later by Lü in [14]. The structure of the equations is such that scrolls are created as the PWL function increases in stair (or saturated) segments. It is also important to note that these scrolls can grow in different planes according to the variable which carries the PWL function, making possible to achieve more complexity by linking a function in more than one

variable. Thus, scrolls will appear in two different directions (two dimensions) or in a three dimensional phase diagram. Such technique is known as multiscroll in 1D, 2D and 3D [6, 14]. The circuits used to implement the PWL behavior are based on the saturation concept of amplifiers [14, 34].

Ideally, an amplifier will have no saturation points, but as it is being supplied by a voltage rail, the transfer function reaches its saturation points near the supply voltage level, changing its linear shape for constant saturated values. This kind of PWL responses can be obtained by any amplifier.

Actually as electronics become more compact and power supply reduces its limits, the scheme of the circuits to implement these systems must be adapted to continue working. As a result, new technologies and techniques must be adopted. In this manner, this Thesis proposal is based on the 0.35μm AMS CMOS technology and the concept of unity gain cells as the simplest processing transistor-based cell which allows to work with more compact circuits and lower voltage levels than by applying the opamp-based techniques.

The design of a System on Integrated Chip (SoIC) also enhances the noise immunity and integration levels; thus making the circuit portable [35]. In addition, several approaches are described to achieve multiscroll behavior, making the generation of multiscroll systems systematic for integrated monolithic chip.

There are still many other chaotic oscillators which describe famous systems like Rössler family [8], the Lorentz system [2] and the Chen system [7], but these ones are based on signal products as their active destabilizing sources. Possible assemblies of such oscillators may use commercial multipliers AD633 or AD743, as described in [36], [37] respectively. Since this work is focused on the design of PWL-based chaotic oscillators, these systems are not in the scope of this Thesis.

1.3 Objectives and Contributions

In order to achieve better circuit performance and therefore practical utility, this work is based on elemental transistor modules called unity gain cells (UGCs), such as: voltage

follower (VF), current follower (CF), and current mirror (CM) [38]. Furthermore, it is shown that the performance of these cells is much better than a common Opamp with higher bandwidth capability and portability. On the other hand, current conveyors (CCs) can also be synthesized from UGCs according to [39]. In this manner, another objective is to show that the use of current conveyors gives an important advantage in modeling equation systems in mixed mode design and allows more versatile circuit implementation for chaotic oscillators [40].

For the Chua's and Saturated multiscroll circuits, a nonlinear destabilizing function will be generated by using unity gain cells and current conveyors. Therefore, voltage and current-mode arrangements will be explored with this technique showing the diversity in using these mixed mode cells.

1.4 Thesis Organization

This Thesis is organized as follows: Chapter 2 introduces basic research in chaos, as well as the characteristic behavior of the chaotic systems of interest.

Chapter 3 describes the use of UGCs and current conveyors to desing integrated chaotic circuits from a point of view of behavioral modeling. General performance of the system is obtained by adding some parasitic effects in the modeling process.

Chapter 4 proposes three different techniques to produce piece wise linear destabilizing functions to enhance chaotic oscillations. Basically, that techniques are based on the use of current mirrors, voltage and current followers, and current conveyors. The proposed transistor based topology to implement the mentioned circuits is described and simulation is provided using the 0.35μm AMS CMOS technology parameters.

Finally, Chapter 5 draws some conclusions about the work and refers to some applications of chaotic oscillators for future research as well as for this particular work.

Chapter 2

CHAOTIC SYSTEMS

2.1 Research in Chaos

Chaotic systems are hidden in nature, economy, physics, astronomy, etc. Newton himself discovered accidentally these dynamics when trying to calculate the trajectory of a planet orbiting a star. Following the laws of gravitational attraction, a single body like a planet will surround a fixed attractive point, the star, describing an elliptic path. If one assumes that there are two stars, the problem has no analytical solution. The trajectory can be calculated numerically starting from an arbitrary point showing strong dependence on initial conditions and divergence from similar others. The problem is known as the three body gravitational problem; both stars represent attraction points or attractors [41].

The Lorenz system is another relevant example that was developed as a set of equations that might describe turbulence in the upper atmosphere [2]. Researches took a long time in attending what Edward Lorenz proposed in the 60's, the Lorenz attractor.

Later, Leon O. Chua proposed the Chua's chaotic oscillator; one of the most popular chaotic systems due to its simple construction and rich dynamics [42]. The system dynamics are described completely by a circuit which exhibits two different attractors when ploting one variable against the other, which is called phase diagram. The capability to model such systems resides in the use of passive components like capacitors and

inductors, which allow a dynamical system to be described by the relations of currents and voltages. Thus, system trajectories are obtained when its states are equated to currents and voltages into the circuit. Opamp-based schemes are very popular in implementing mathematical functions and impedance couplings for this and many other systems [9].

Intensive research has been done since Chua's circuit was created. Still nowadays, new chaotic systems are proposed [43, 44, 45] and new ways to implement them are also developed [1]. Chaotic systems are studied theoretically because of its capability to model problems like the atmosphere behavior, liquid mixing, decision models, cell growing, synchronization, finances and market behavior. In the other side, in applied engineer field, chaotic systems are implemented by circuits, lasers or impellers to generate random values, robust control systems, synchronization systems, secure communications, homogeny mixings, etc.

2.2 Systems Review

Chaotic systems based on a PWL destabilizing function are reviewed in this section.

2.2.1 Chua's Circuit

Leon O. Chua introduced one of the first electronic chaotic oscillators [15, 42]. The circuit is described by the third order system of differential equations given by (2.1), where the destabilizing function is described by (2.2). This circuit in Figure 2.1 is made by passive components, a resistor, two capacitors, one inductor and a nonlinear element called Chua's diode, which is described by (2.2). The chaotic system is powered only by a negative conductance component which is called the Chua's Diode, therefore this device works as a negative resistor showing two different conditioned values according to $F(v_R)$ in (2.2).

$$C_1 \frac{dv_{C1}}{dt} = G(v_{C2} - v_{C1}) - F(v_{C1}),$$

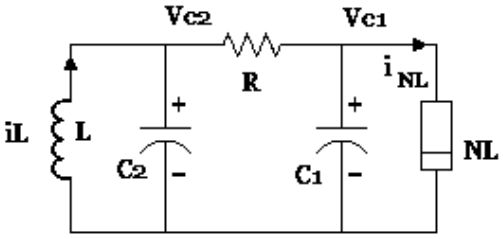


Figure 2.1: The Chua's circuit

$$\begin{aligned} C_2\frac{dv_{C2}}{dt} &= G(v_{C1}-v_{C2})+i_L, \\ L\frac{di_L}{dt} &= -v_{C2}. \end{aligned} \tag{2.1}$$

$$F(v_R) = G_b V_R + \frac{1}{2}(G_a - G_b)(|v_R + B_p| - |v_R - B_p|). \tag{2.2}$$

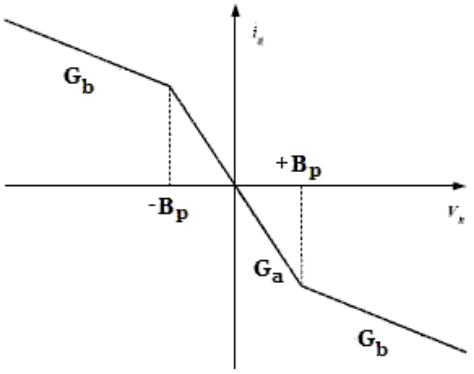


Figure 2.2: The Chua's Diode PWL behavior described by $F(v_R)$

To normalize the system of equations in an adimensional representation, a time constant $\tau = \frac{G}{C_2}t$ is assigned to the system letting $\dot{x_i} = \frac{dx_i}{d\tau}$. In addition, the following equivalences are made:

$$x_1 = \tfrac{v_{C1}}{B_p}, \qquad x_2 = \tfrac{v_{C2}}{B_p}, \qquad x_3 = \tfrac{i_L}{B_p G},$$
$$\alpha = \tfrac{C_2}{C_1}, \qquad \beta = \tfrac{R^2 C_2}{L}, \qquad a = RG_a, \qquad b = RG_b.$$

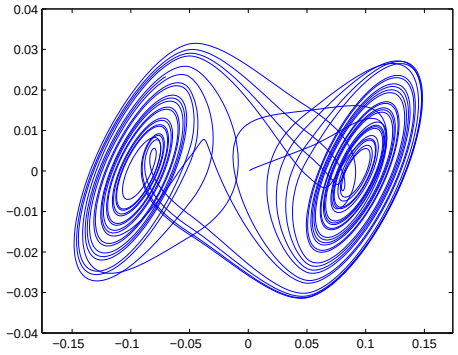


Figure 2.3: The Chua's Double-scroll between variables x_2 and x_1.

Figure 2.3 shows the characteristic phase plot between circuit states. The trajectories oscillation grows in one of the attracting points and then reaches a limit which makes it change to the other attractor and start again. The final equations of the system are described by (2.3) and (2.4). Practical values for the constants are $\alpha = 9$, $\beta = 100/7$, $a = -8/7$ and $b = -5/7$. As an initial condition a voltage of 1mV is assumed in node v_{C1}.

$$\begin{aligned} \dot{x_1} &= \alpha(x_2 - x_1 - f(x_1)), \\ \dot{x_2} &= x_1 - x_2 + x_3, \\ \dot{x_3} &= -\beta x_2. \end{aligned} \tag{2.3}$$

$$f(x_1) = bx_1 + \frac{1}{2}(a-b)(|x_1+1| - |x_1-1|). \tag{2.4}$$

2.2.2 Hyperchaotic Chua's System

Kapitaniak showed in [32] that by arranging two independent Chua's circuits and by coupling them in a form previous to synchronization, a hyperchaotic circuit is obtained from the simple Chua's one as shown in Figure 2.4. The system has now six states, and two positive Lyapunov exponents (see appendices A and B). Equation set (2.5) describes Figure 2.5, while the PWL function (2.6) remains the same.

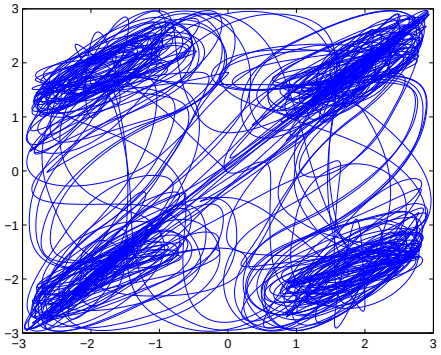


Figure 2.4: Phase plot x1, x4 of the hyperchaotic Chua's system.

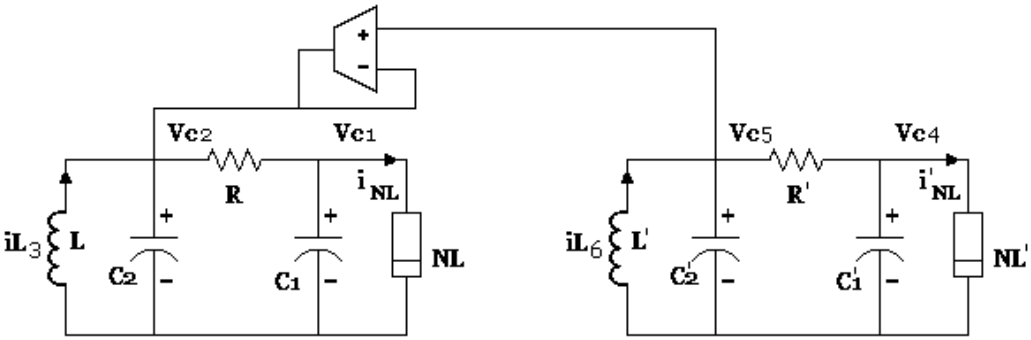


Figure 2.5: Hyperchaotic Chua's circuit.

$$
\begin{aligned}
\dot{x_1} &= \alpha(x_2 - x_1 - f(x_1)), \\
\dot{x_2} &= x_1 - x_2 + x_3 + k(x_5 - x_2), \\
\dot{x_3} &= -\beta x_2. \\
\dot{x_4} &= \alpha(x_5 - x_4 - f(x_4)), \\
\dot{x_5} &= x_4 - x_5 + x_6, \\
\dot{x_6} &= -\beta x_5.
\end{aligned}
\tag{2.5}
$$

$$f(x) = bx + \frac{1}{2}(a-b)(|x+1| - |x-1|). \tag{2.6}$$

2.2.3 Multiple Scroll Circuits

Generalized Chua's Circuit

A generalization was made to the Chua's circuit by Suykens and Vandewalle [5]; although, it is not the only one, it can exhibit multiple-scroll behavior. It was initially developed in [20, 21], and it is described by the system (2.7), and the destabilizing function (2.8). The nonlinear I-V function $h(x_1)$ shows more segmentations allowing more scrolls to arise.

$$\begin{aligned} \dot{x_1} &= \alpha(x_2 - h(x_1)), \\ \dot{x_2} &= x_1 - x_2 + x_3, \\ \dot{x_3} &= -\beta x_2. \end{aligned} \tag{2.7}$$

$$h(x) = m_{2q-1}x + \frac{1}{2}\sum_{i=1}^{2q-1}(m_{i-1} - m_i)(|x + c_i| - |x - c_i|). \tag{2.8}$$

Where, as given in [5], the parameter $q = n$ corresponds to n number of double scrolls presented taking the following vectors for m and c:

- 2-scroll, $q = 1$

$$\begin{aligned} m &= [-1/7; 2/7], \\ c &= 1 \end{aligned} \tag{2.9}$$

- 4-scroll, $q = 2$

$$\begin{aligned} m &= [-1/7; 2/7; -4/7; 2/7], \\ c &= [1; 2.15; 3.6] \end{aligned} \tag{2.10}$$

- 6-scroll, $q = 3$

$$\begin{aligned} m &= [-1/7; 2/7; -4/7; 2/7; -4/7; 2/7], \\ c &= [1; 2.15; 3.6; 8.2; 13] \end{aligned} \tag{2.11}$$

And also by changing the sign of m one can obtain $n = 2q - 1$ scrolls with the following values:

- 1-scroll, $q = 1$

$$\begin{aligned} m &= [1/7; -2/7], \\ c &= 1 \end{aligned} \tag{2.12}$$

- 3-scroll, $q = 2$

$$\begin{aligned} m &= [0.9/7; -3/7; 3.5/7; -2.4/7], \\ c &= [1; 2.15; 4] \end{aligned} \tag{2.13}$$

- 5-scroll, $q = 3$

$$\begin{aligned} m &= [0.9/7; -3/7; 3.5/7; -2.7/7; 4/7; -2.4/7], \\ c &= [1; 2.15; 3.6; 6.2; 9] \end{aligned} \tag{2.14}$$

Saturated Multiscroll System

A very structured approach for multiple-scroll systems were first presented by Yalçin in [6] using a stair case nonlinear PWL function. The system can be expanded in two or three directions by adding more nonlinearities to each term of the equation set. This is the so called 2- and 3-dimentional *scroll grid attractors*, which will not be developed in this work.

In order to achieve multiscroll behavior in a more practical way. Lü [14] developed a similar set of equations described on (2.15) which is controlled by saturated functions, avoiding the sharpness of the staircase functions and making it more suitable for physical implementations. The equation set described is known as the 1-D n-Scroll.

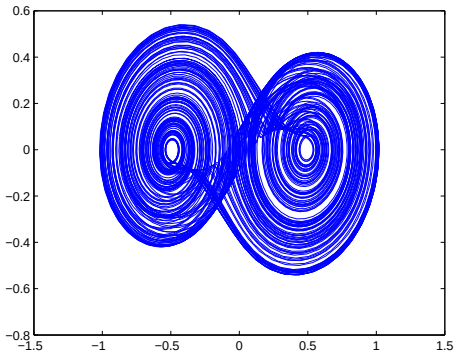


Figure 2.6: A simple 1D Two-scroll saturated system.

$$\begin{aligned} \dot{x_1} &= x_2, \\ \dot{x_2} &= x_3, \\ \dot{x_3} &= -ax_1 - bx_2 - cx_3 + d_1 f(x_1, k_1, h_1, p_1, q_1). \end{aligned} \tag{2.15}$$

$$f(x;k,h,p,q) = \begin{cases} (2q+1)k, & \text{if } x > qh+1 \\ k(x-ih)+2ik, & \text{if } |x-ih| \leq 1,\ -p \leq i \leq q \\ (2i+1)k, & \text{if } ih+1 < x < (i+1)h-1,\ -p \leq i \leq q-1 \\ -(2p+1)k, & \text{if } x < -ph-1. \end{cases}$$

Basically, the nonlinear function is a set of saturated functions, each one composed by two *saturated plateaus* in the output limits and a *saturated slope* in between them. In general the slope is related to the gain of certain amplifier, for high gains, the PWL function approaches a staircase. Parameters a, b, c, d_1 are usually equal to 0.7, parameter h determines the spacing between saturated functions, k determines the saturation point and the i places between $-p$ and q determine the number of these functions.

Chapter 3

SIMULATING PWL-BASED CHAOTIC OSCILLATORS

As described in [47], the systematic analog circuit design is a multilevel approach. Each stage has a different level of abstraction. At the top level, any analog system can be first described as an equation set [48, 49]. Then it is modeled in a behavioral level. Later, the model is described as a set of functional blocks; as more non-idealities are added to the model, its behavior is checked to keep it between certain boundaries. Transistor level is then used to describe the full system and later, layout can be done to prepare the circuit to be manufactured.

3.1 Unity Gain Cells

This Thesis is based on the use of unity gain cells UGCs and second generation current conveyors (CCIIs) because of their good characteristics in wider bandwidth and lower power consumption [50], as well as the circuit simplicity compared with traditional Opamps. For details about the selected topologies one can see [39].

Each of the four main UGCs are non-inverting or inverting followers in voltage or current mode and their representation is shown in Figure 3.1. They are ideally characterized by the following relations:

- Voltage Follower (VF) has $Vout = Vin$, $Iin = 0$ with no relevance in the output current.
- Voltage Mirror (VM) has $Vout = -Vin$, $Iin = 0$ with no relevance in the output current.
- Current Follower (CF) has $Iout = Iin$, $Vin = 0$ with no relevance in the output voltage.
- Current Mirror (CM) has $Iout = -Iin$, $Vin = 0$ with no relevance in the output voltage.

Figure 3.1: Symbolic notation of the UGCs.

3.2 The Second Generation Current Conveyor

The CCII is a mixed mode processing cell, terminal Y is a voltage input and terminal X is a current input. They show high and low input impedance respectively (Figure 3.2) [51]. All generations of current conveyors have the characteristic of copying the voltage between terminals X and Y. Originally, the first generation current conveyor (CCI) was a block in which the current trough Y terminal was equal to the current in X and the current in Z was also conveyed to be equal than in X. The third and last generation of current conveyors (CCIII) and is very similar to the first, it only changes the direction of the current in the Y terminal. The most used of them is the CCII; equation (3.1) gives the ideal behavior of the CCII circuit.

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{3.1}$$

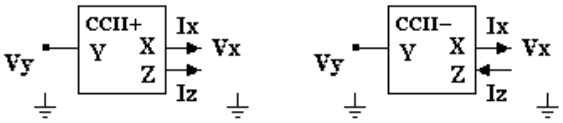
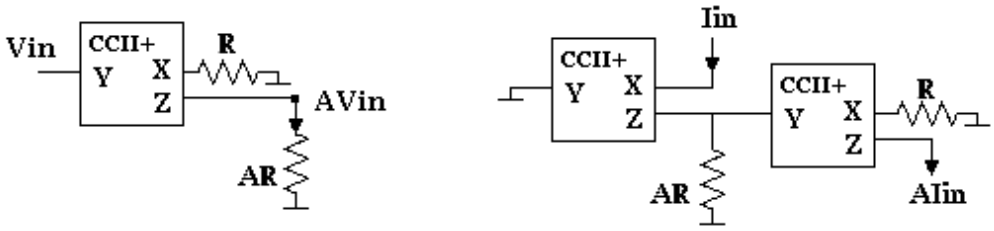


Figure 3.2: The CCII positive and negative representations.

The use of the CCII has proved to be very versatile in a wide range of applications, and recently, in the implementation of chaotic oscillators [24, 25, 40]. Next, some basic arrangements will show the different usage of this cell within chaotic oscillators.

In voltage or current-mode, amplification will be performed based on the Ohm's law. Figure 3.3 shows simple approaches for doing so based in the value of the resistance multiplier A.



(a) (b)

Figure 3.3: The CCIIs as voltage or current amplifiers.

As all dynamical systems, chaotic systems require signal integrators. These can also be done by arranging CCIIs for the two signal natures, voltage and current [51, 52]. Figure 3.4 and equation (3.2) show this technique. This operation will define the main nature of a system. For all voltage mode circuits, a voltage mode integrator will be selected too and for current-mode will be done in the same way. It is important to notice that the topologies of the chaotic oscillators proposed in this work will not be strictly in voltage nor current mode but mixed mode.

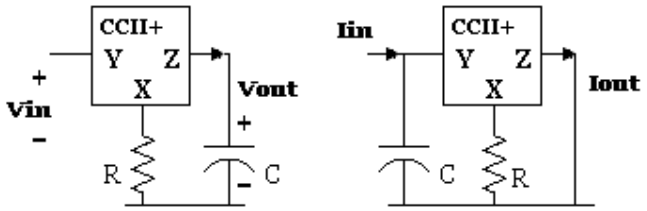


Figure 3.4: The CCII connected as a voltage and current integrator, respectively.

$$V_o = \frac{1}{RC}\int V_{in}dt, \qquad I_o = \frac{1}{RC}\int I_s dt \tag{3.2}$$

3.3 Simulation of Chaotic Oscillators

In order to prove the chaotic behavior of the circuits proposed in this Thesis, macromodels of the main non-idealities of the CCIIs are built and the entire behavior of the system is observed. Later, transistor cells will replace all the macromodels. Such models are relatively simple, one of their main characteristics are the impedances on all the terminals of the CCII [51]. Limitations in the excursion level and bandwidth are taken into account when the operation is expected to exceed these parameters. The general macromodel for a voltage amplifier proposed in [40] is shown in Figure 3.5, it can be divided in three main blocks:

- The input block describes the input impedance of the circuit. The obtained poles of non-intermediate blocks are far away from the circuit BW.

- The intermediate block models the dynamic range of the device (this depends on the power supply and saturation voltages) as well as the output offset and also the dominant pole, fixing BW. The slew rate corresponds to the current through the resistor in between the capacitance.

- The output block couples the output impedance of the circuit to the transferred signal.

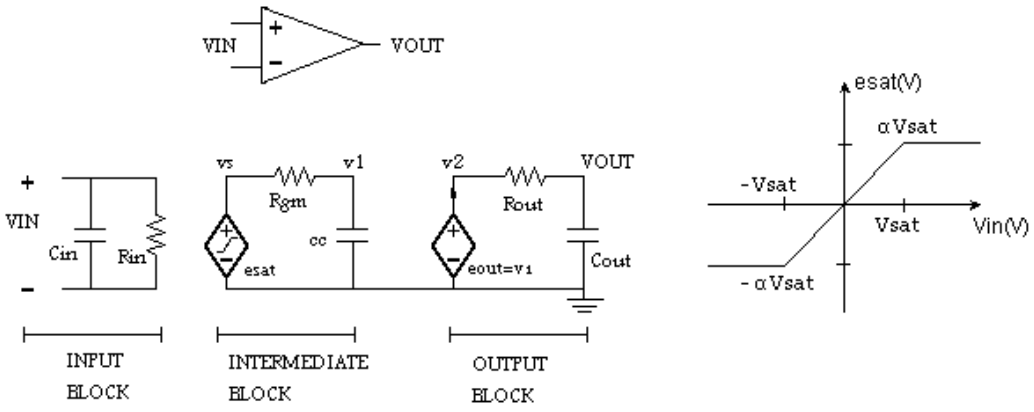


Figure 3.5: Voltage-amplifier macromodel proposed in [40] including input and output impedances and limitations in gain, bandwidth, slew rate and saturation.

In similar way, any of the previous described UGCs are modeled and also a general macromodel for the CCII can be shown in Figure 3.6.

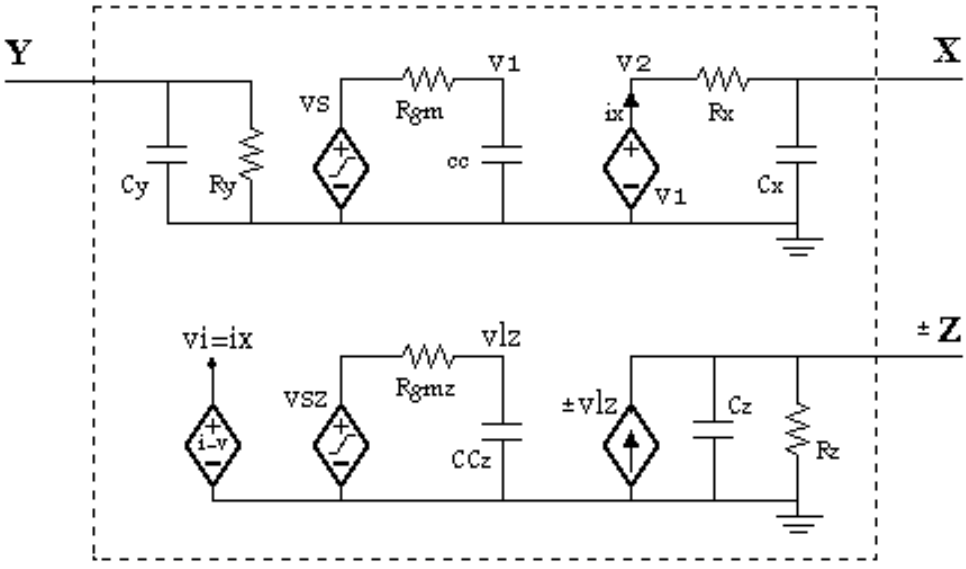


Figure 3.6: CCII macromodel including impedances on its terminals and limitations in gain, bandwidth, slew rate and saturation.

In the following, the parasitic effect R_X in terminal X of the CCII is considered for all the designs because of its remarkable influence of the cell gain. The value of this parameter is examined in the next Chapter.

Next, the different circuits are presented to simulate chaotic oscillators using some of the CCII parameters that will be investigated in the following Chapter. Here, these circuits are macromodeled to prove that the system is efficient given a current controlled current source as the piece wise linear (PWL) function, which is characterized by low saturation slopes in many cases to allow an easier implementation later at a transistor level.

3.3.1 Simple Chua's Circuit

As described in Chapter 2 and deeply analyzed in [15], Chua's circuit can be driven to chaos by selecting an appropriate set of parameters as shown in (3.3). These values will produce the known double attractor characteristic of the circuit as shown in Figure 3.7. Note that in this case, PWL non-idealities are not taking part of this system, while they will be considered in the following Chapter. A fully behavioral model is found in [53] as well as a description for scaling the system dynamics, which is based in changing only parameter τ and achieved after scaling C_1, C_2 and L.

In addition, the Chua's system (2.3) can be represented in (3.4) in order to implement the PWL function as a simple saturated nonlinearity with slope equal to one, this is also, an *equivalent Chua's circuit* [22], Figure 3.8 shows its block diagram.

$$\begin{aligned} \alpha &= 9, \\ \beta &= 100/7, \\ a &= -8/7, \\ b &= -5/7. \end{aligned} \tag{3.3}$$

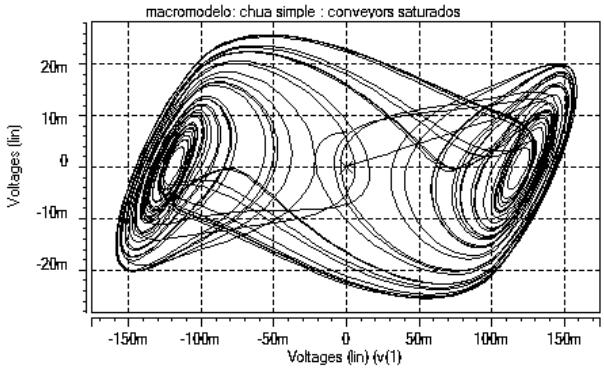


Figure 3.7: Phase plot of the Chua's strange attractors.

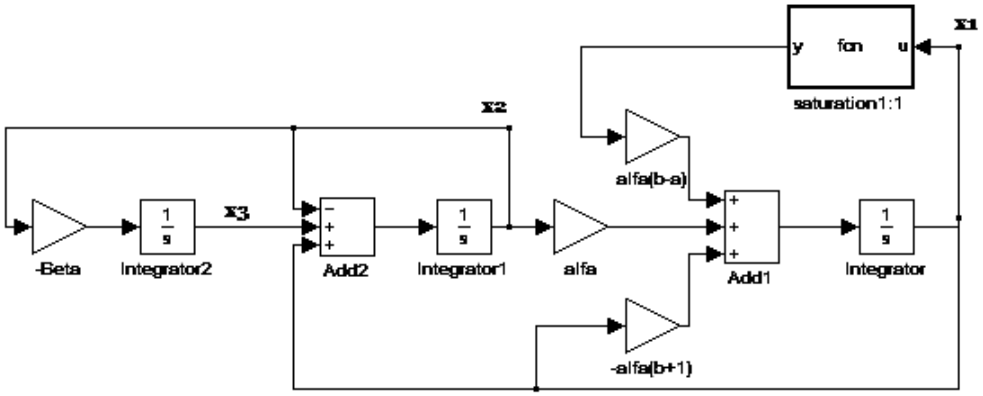


Figure 3.8: Chua's equivalent circuit block diagram.

$$\begin{aligned} \dot{x_1} &= \alpha(b+1)x_1 + \alpha x_2 + \alpha(b-a)h(x_1), \\ \dot{x_2} &= x_1 - x_2 + x_3, \\ \dot{x_3} &= -\beta x_2, \\ h(x_1) &= \frac{1}{2}(|x_1+1| - |x_1-1|). \end{aligned} \tag{3.4}$$

Using this perspective, the voltage and current-mode circuits are built. The integrators and gain blocks are realized with the afore-mentioned technique. Figure 3.9 shows the system phase plot both in voltage and current-mode for the behavioral CCII-based

Chua's circuit.

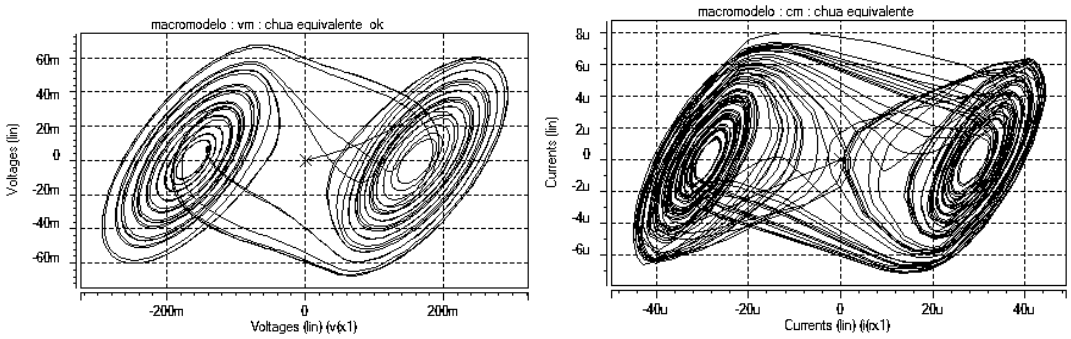


Figure 3.9: Phase plot of the voltage and current-mode Chua's attractors.

3.3.2 Hyperchaotic Chua's Circuit

The hyperchaotic Chua's system is generated directly by coupling two simple Chua's circuits as shown in Figures 3.10 and 3.11. The circuit could be realized entirely by the voltage or current-mode approach described earlier. The PWL function of the straight forward manner presented will be detailed in Chapter 4.

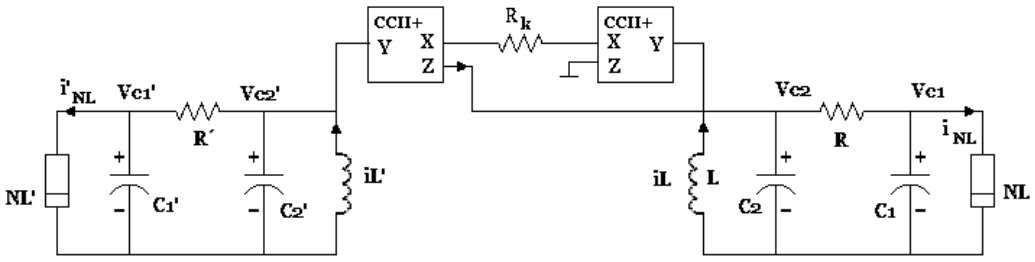


Figure 3.10: Hyperchaotic Chua's circuit using CCIIs as for coupling.

Having this circuit directly assembled from the original Chua's circuit, one can observe that two of the six states of the new circuit are described by currents. Therefore, the difference between states x_2 and x_2' is projected as the potential difference between both X terminals of the CCIIs, transformed to current by the total resistance of this branch and finally copied to be part of the state x_3; thus, parameter $K = 1/(2R_x +$

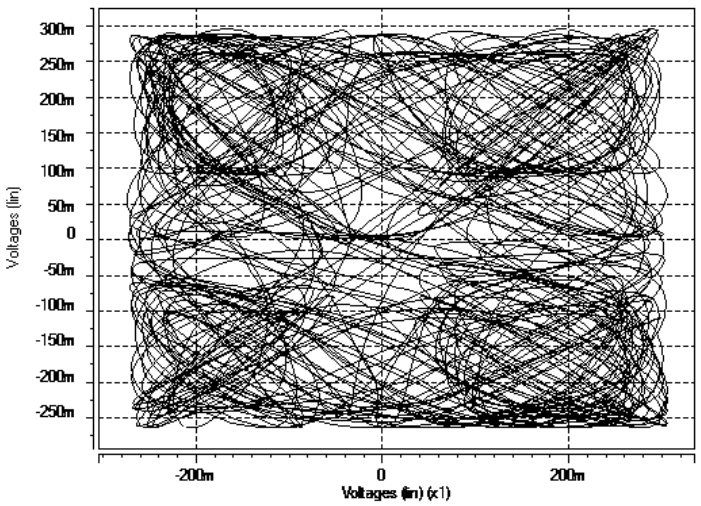


Figure 3.11: Phase plot of the hyperchaotic Chua's circuit x1 - x1' plane projection.

$R_K) = 66.7\mu A/V$.

By keeping reduced values for K, the right side original circuit is neither independent from the left side circuit nor has it the chance to synchronize. Therefore, trajectory x_1 from the first part of the system generates an extra double scroll attractor with respect to trajectory x_1' from the second part as shown in the double-double-scroll attractor of Figure 3.11.

3.3.3 Generalized Chua's Circuit

As explained before, the generalized Chua's circuit comes from the same diagram of Figure 2.1, but just changing the PWL function $f(x)$ to $h(x)$ as reports [5] and describes (3.5) in simplified mode from (2.8), enabling multiple scroll generation. Details of these functions are shown in Figure 3.12. Note that the plotted PWL functions are equal to $h(x) - x_1$, to allow detailed observance.

$$h_{2scroll} = \left(\frac{2}{7} - 1\right) x - \frac{3}{7} SAT(-1, 1), \tag{3.5}$$

$$h_{3scroll} = \left(\frac{2}{7} - 1\right) x - \frac{3.9}{7} SAT(-1, 1) + \frac{6.5}{7} SAT(-2.15, 2 - 15) - \frac{5.9}{7} SAT(-4, 4),$$

$$h_{4scroll} = \left(\frac{2}{7} - 1\right) x - \frac{3}{7} SAT(-1, 1) + \frac{6}{7} SAT(-2.15, 2 - 15) - \frac{6}{7} SAT(-3.6, 3.6).$$

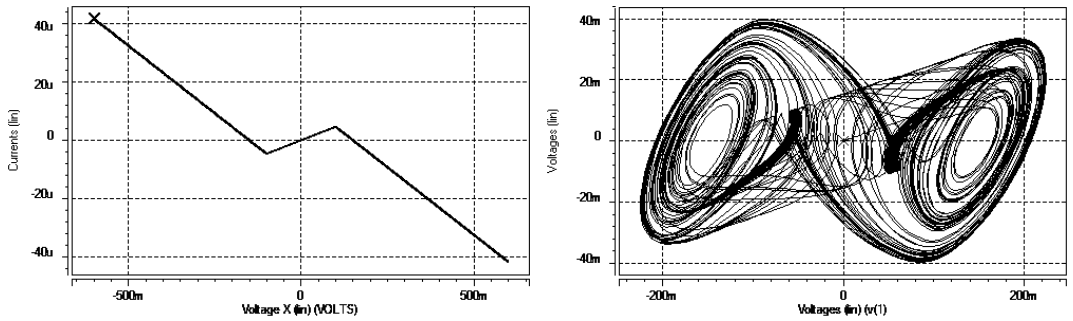
For simplicity, expression $SAT(-Bp, Bp)$ indicates a saturated function of unitary slope limited between points $\pm Bp$.

3.3.4 Saturated Multiscroll Circuit

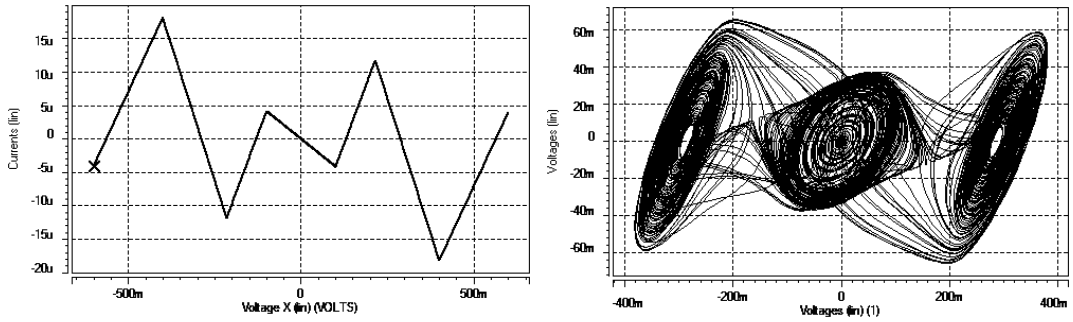
As already seen in the generalized Chua's circuit figures, it creates several scrolls each time the PWL function grows in terms, but these attractors lose dimensions as they grow in number. This is more remarkably noted in circuit implementations due to the more non-ideal effects that play in. A more robust multiscroll approach is the saturated multiscroll system due to the simplest PWL function requirements as will be shown here.

Note that multiscroll systems are also limited by the bounding parameters of their components such as supply voltages and current handling capabilities. But by modeling, the system limits and potentialities become patent for the designer and can be rescaled.

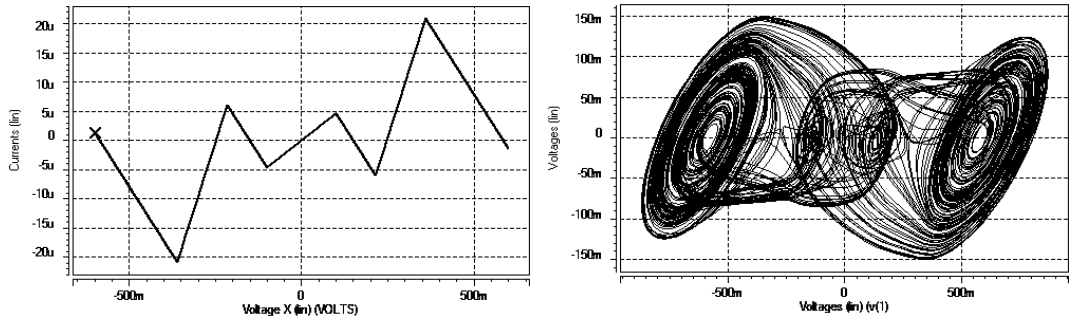
Diagrams for the voltage and current-mode systems are shown in Figures 3.13 and 3.15, as well as strange attractors in dependence of the saturated function previously described by (2.2.3). The control parameter $a = b = c = d_1 = R_{sum}/R_x$ is just controlled by this resistance R_{sum}.



(a) 2-Scroll



(b) 3-Scroll



(c) 4-Scroll

Figure 3.12: Generalized Chua's PWL functions and phase plots for (a) two, (b) three and (c) four strange attractors.

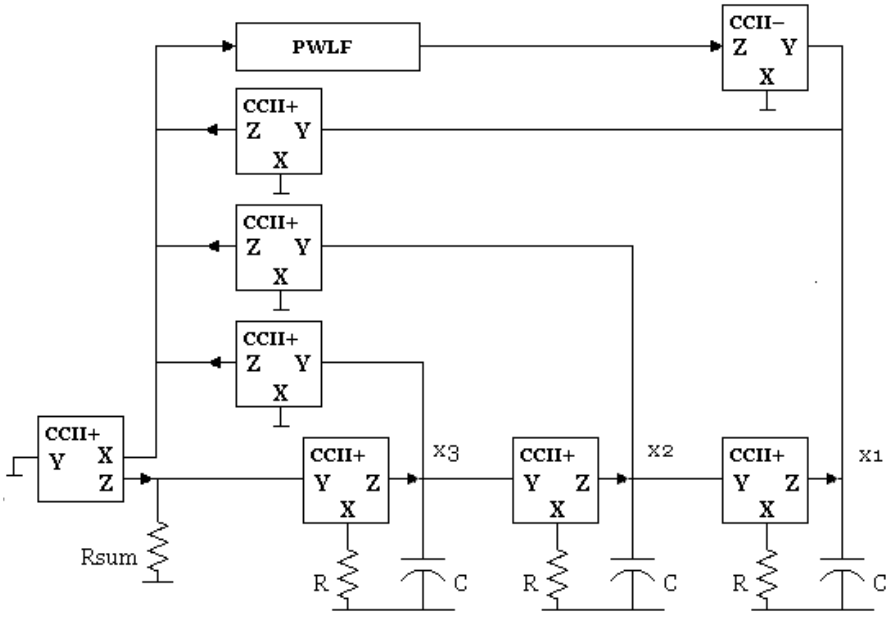
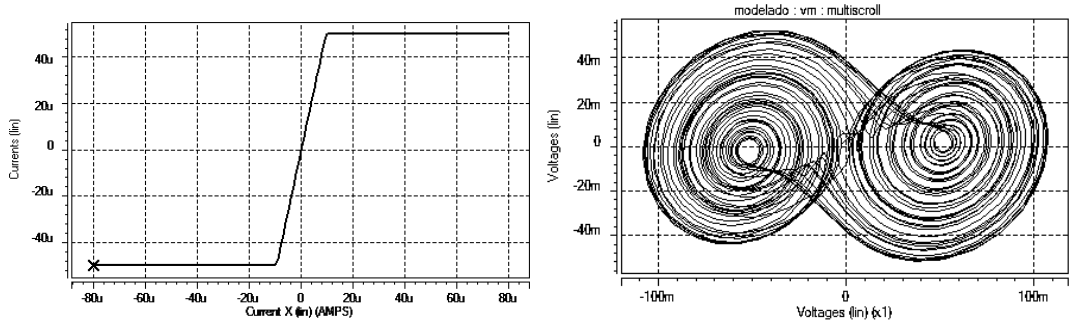
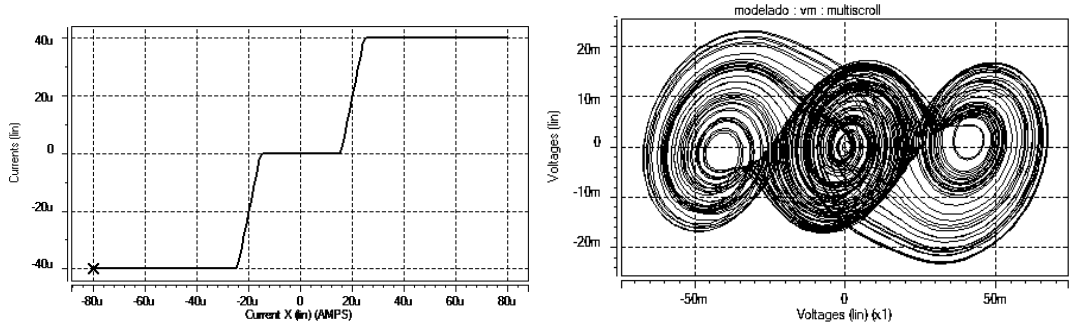


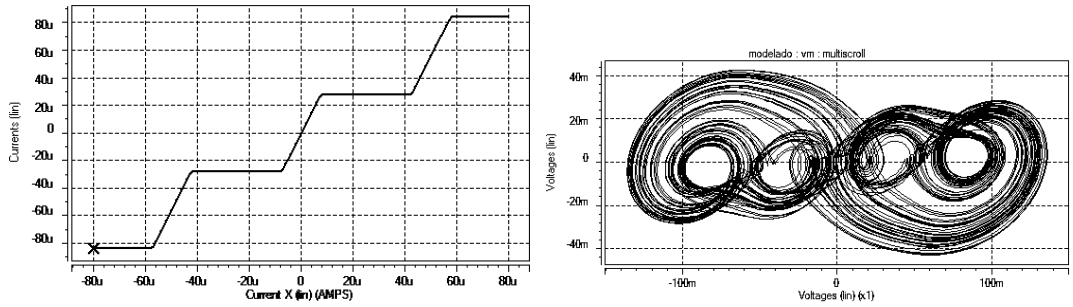
Figure 3.13: CCII-based multiscroll circuit in voltage-mode.



(a) 2-Scroll



(b) 3-Scroll



(c) 4-Scroll

Figure 3.14: Multiscroll voltage-mode circuit PWL functions and phase plots for (a) two, (b) three and (c) four strange attractors.

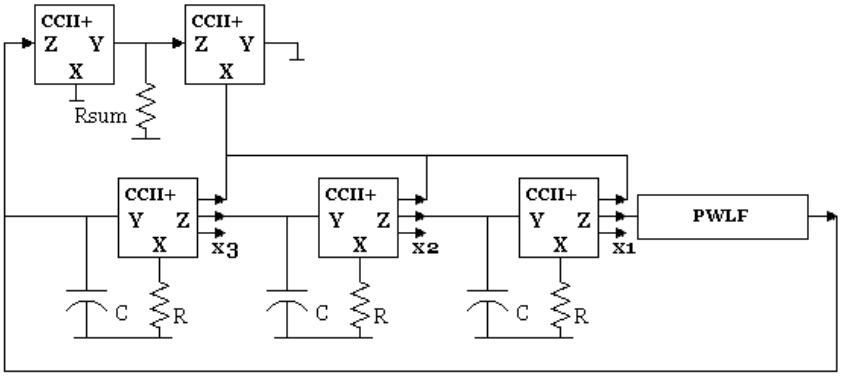
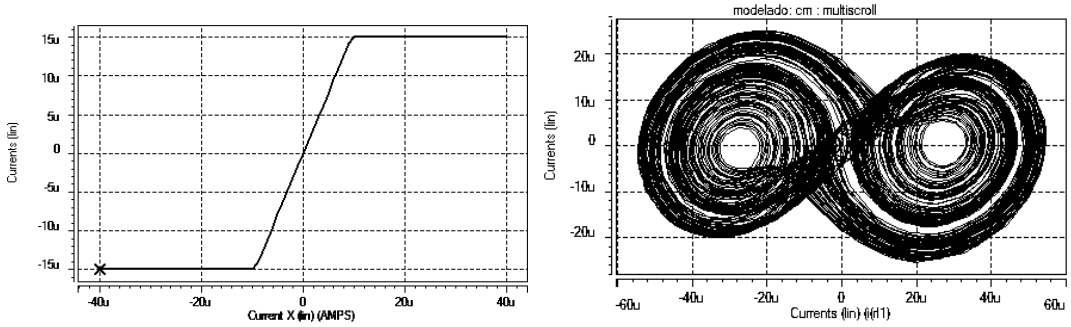
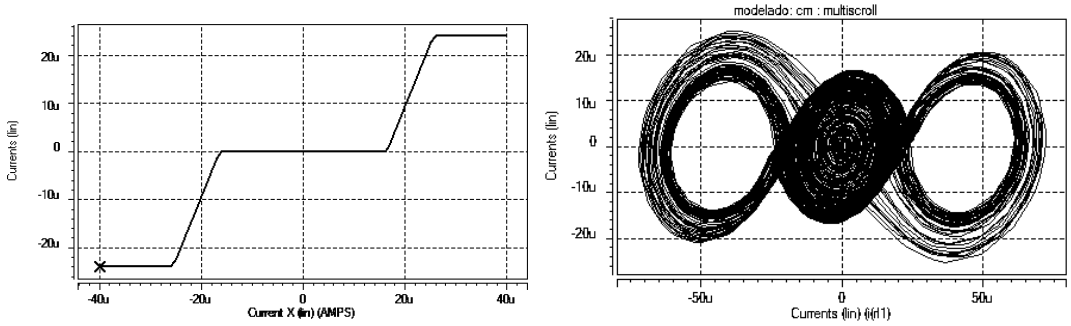


Figure 3.15: CCII-based multiscroll circuit in current-mode.



(a) 2-Scroll



(b) 3-Scroll

Figure 3.16: Multiscroll current-mode circuit PWL functions and phase plots for (a) two and (b) three strange attractors.

Chapter 4

SYNTHESIZING PWL FUNCTIONS

In order to synthesize PWL functions using UGCs and/or current conveyors for the already described chaotic systems, several approaches are described next. HSPICE simulations will be also presented showing the performance of such transistor level systems in 0.35μm AMS technology. Such systems are mainly based on the CCII. A more detailed description of this cell will be first given. For simplicity, all the CMOS schematics in this Thesis use three terminals assuming the bulk terminal always in the positive supply V_{DD} for PMOS or the negative supply V_{SS} for NMOS transistors.

4.1 The CCII Building Block

A simple cell is the CCII based in the push-pull amplifier of Figure 4.1. This connection provides symmetry to the circuit, which makes it more lineal [51]. In addition, high current handling between terminals X and Z, as well as low impedance in terminal X is observed:

$$Z_X = \frac{1}{\sqrt{2I_b}(\sqrt{\beta_N} + \sqrt{\beta_P})}, \qquad \beta_{N/P} = \mu_{N/P} C_{ox} \frac{W_{N/P}}{L}. \tag{4.1}$$

Where subindex N or P implies NMOS or PMOS transistors.

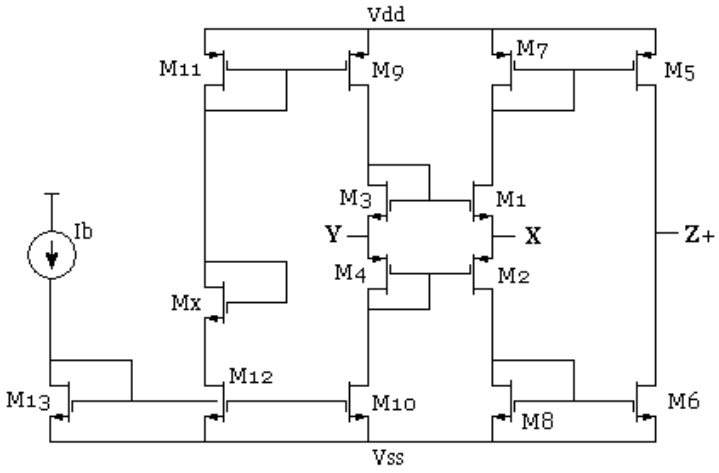


Figure 4.1: Push-Pull CCII.

Multiple scroll circuits are very sensible to the signal offsets which lead their dynamics far from the attraction basin thus losing attractors. For this reason, some systems use coupling stages. To take advantage of the typical characteristics of the CCII terminals, transistors are dimensioned keeping good matching between internal mirrors and therefore reducing offset currents in all terminals. Transistor Mx is introduced for this purposes. Once introduced, reduces the V_{ds} difference between bias transistors restricting the offset currents in terminal Y.

Some of the main characteristics of push-pull CCII are mentioned in the first column of Table 4.1 and Table 4.2. Macromodels of the earlier chapter have been constructed from this data.

As comented before, it is possible to synthesize a CCII starting from the combination of a VF and a CF [39]. One attractive topology for the VF is developed in [54] and shown in Figure 4.2.

Therefore, a CCII can be generated from this cell by using transistors M9 and M10 as current references for the Z branch. These will copy the current trough X in the following form: The extra current flowing trough M3 and M4 will cease to flow trough M1 and M2 and consequently trough M10 and M9, thus transmitting this behavior to

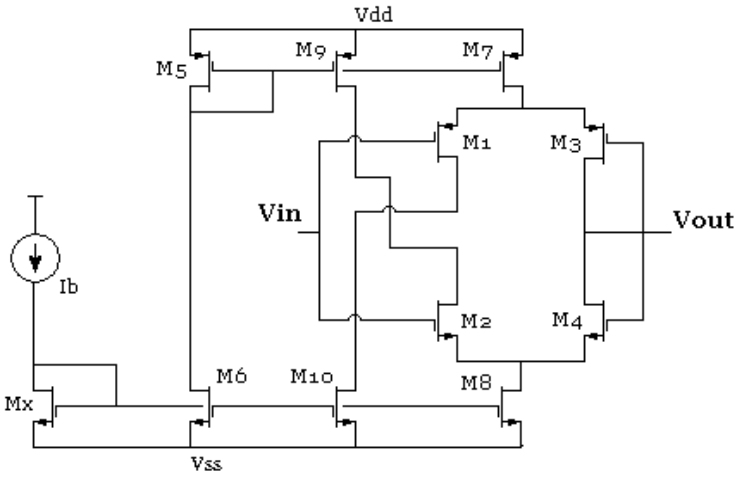


Figure 4.2: Sinthesized VF from [54].

the Z new branch. This current will be limited by the total current in M7 and M8 because of the differential-pair arrangement. This maximum current will be governed by the bias current. Some characteristics of this CCII are described in Tables 4.1 and 4.2 (second column), as well as Figure 4.3. Figure 4.4 describes the parasitic resistance behavior for this CMOS implementation and also an exponential tendency function has been fitted on it (4.2).

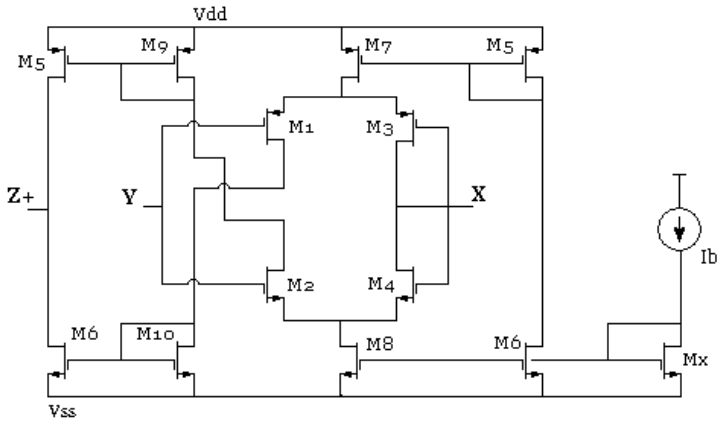


Figure 4.3: Differential-pair CCII.

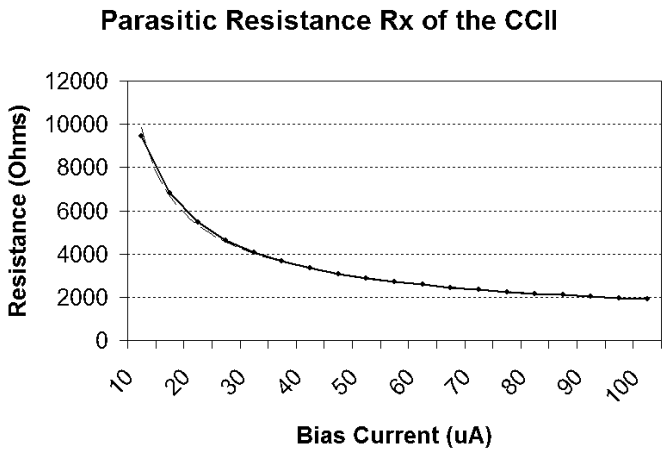


Figure 4.4: Parasitic resistance of the differential CCII R_X showing exponential tendency line.

$$R_X = 9844(2 \cdot 10^5 \cdot I_b - 1)^{-0.557} \tag{4.2}$$

4.2 Generation of PWL Functions

PWL approximations in voltage mode are common fact of many experimental works in chaos [9, 10, 13, 11, 12]. However, it is clear that while basing these realizations on Opamps, such circuits require lot of space and power consumption is high. The following configurations are based in mixed-mode cells but mainly in current techniques that work in integrated circuit level using low supply levels and power requirements.

4.2.1 PWL functions synthesized by UGCs

An ingenious way to generate symmetric PWL functions is based on the use of UGCs as described in [55]. The use of these cells is more attractive than other topologies in which frequency ranges are related to the product gain-bandwidth [50]. In this case, a negative slopes resistor is shown in Figure 4.5(a). In general, the obtained function can be negative or positive depending on the sign of the used current follower.

Table 4.1: Principal characteristics of the CCIIs.

	Push-Pull	Differential-Pair	Units
Voltage gain	0.983	0.963	-
BW (RL=100KΩ, 1pF)	101	47	MHz
Current gain	1.01	0.999	-
BW (RL=500Ω, 1pF)	97	141	MHz
Input impedance	250	inf	KΩ
R_X	1012	2884	Ω
R_Z	630	696	KΩ
Input offset (Y)	1.6	0	nA
Output offset (X)	43	110	μV
Output offset (Z+)	38	100	nA
Output offset (Z-)	-26	-	nA
Bias current	25	50	μA
Power	372	604	μW

Table 4.2: Transistor dimensions of the CCIIs.

W/L ($L = 1\mu$)	Push-Pull	Differential-Pair
M1, M3	55	50
M2, M4	120	30
M5, M7	11	60
M6, M8	10	6.3
M9, M11	21	7
M10, M12, M13	10	1.4
Mx	12	6.3

In this case, a negative current follower (CF-) generates a negative slope function by having $R_1 < R_2$. The current injection to node Vx is higher than the current coming from input port (Iin). The diagram also shows the main parasitic effect, the output resistance of CF-, which eventually allows all the current to flow trough it when Vin overcomes Vx. This is only possible due to the CF saturation. When increasing the current trough R_1, the CF- will reach its saturation point I_{satCF} producing the break point $Vin = Bp$. From this point, the current will not grow more with the increasing of Vin, this corresponds to the positive slope m_{0D} of Figure 4.5(b). Later, the circuit input current will be null in the point $Vin = Vx = E$.

To simplify calculations of the negative slope and the breakpoint one assume $r_0 \gg R_1, R_2$; nevertheless, this value plays an important role in determining the positive slope and the point E because this resistance is the main current leaving path. Its absence would suppose a saturated output level $m_{1D}Bp$ thus avoiding the point E.

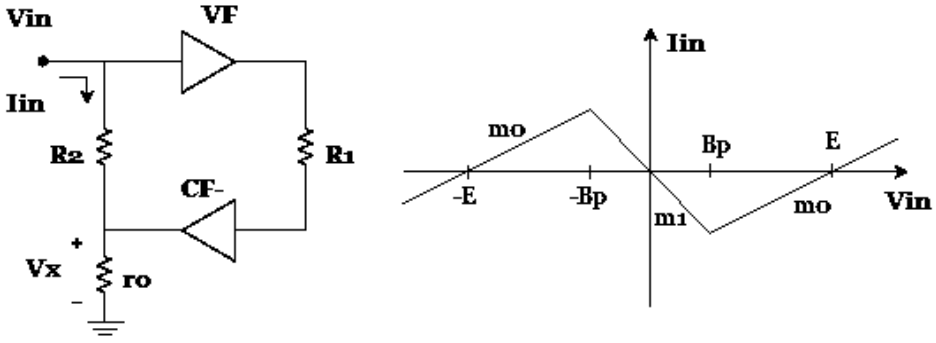


Figure 4.5: Negative resistor (a) schematic, (b) performance.

$$\begin{aligned} m_{1D} &\approx \lim_{r_0 \to \infty} \left(\frac{R_1 - r_0}{R_1(R_2 + r_0)} \right) = \frac{-1}{R_1}, \\ Bp &= R_1 I_{satCF}, \\ E &= I_{satCF} r_0, \\ m_{0D} &= \frac{1}{R_2 + r_0} \end{aligned} \tag{4.3}$$

Chua's simple circuit is ideal for the PWL descriptions given by the UGCs approach.

According to this, the system is calculated for an output resistance $r_0 = 700k$ and a $50\mu A$ saturation current. In Figure 4.6(a) the dashed lines results from each of the two circuits containing a VF and a saturated CF. The solid line is the summation of this current functions; slopes $m_0 = m_{0Da} + m_{1Db}$ and $m_1 = m_{1Da} + m_{1Db}$ are pointed in the graph as approximated to $250\mu A/V$ and $400\mu A/V$ respectively.

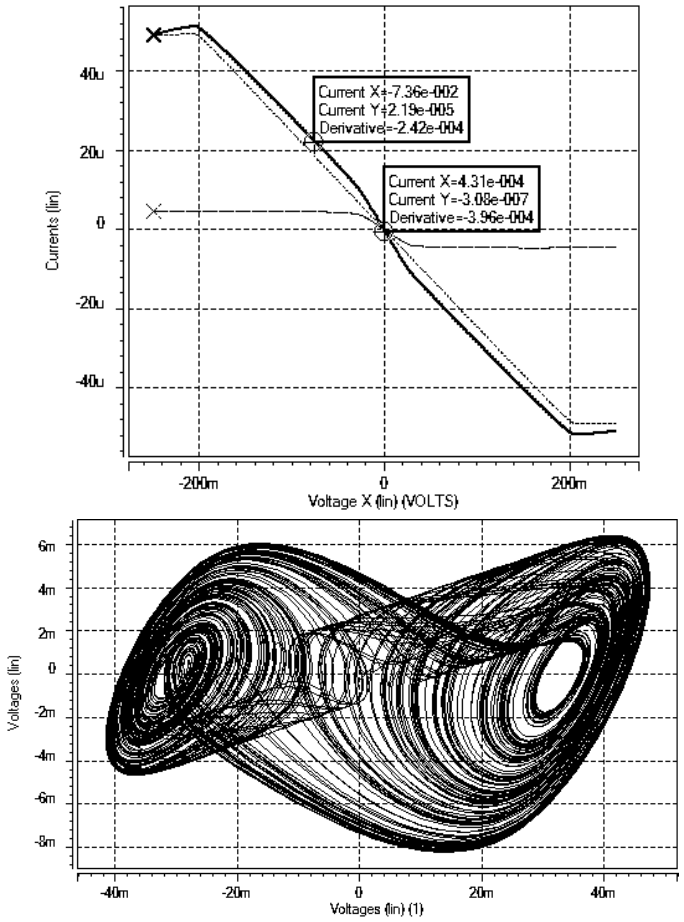


Figure 4.6: UGCs realization of Chua's circuit, (a) the PWL functions, (b) the double scroll attractors.

The circuit characteristic attractors are shown in Figure 4.6(b). The values have been calculated starting from the resistance $R = 2856\Omega$, and adjusted to perform proper operation. The circuit parameters are $R = 2756\Omega$, $C_1 = 195pF$, $C_2 = 1.75nF$ and $L = 1.1mH$.

4.2.2 PWL functions synthesized by current mirrors and rectifiers

The generation of PWL functions in current-mode has been the subject of several authors [56, 28, 26] and its simplicity is based in the fact that breakpoints can be realized as a sum of currents processed by several cells. In fact these cells require low transistor amount. On the other hand, when arranging several functions in current-mode in parallel form, the obtained function loses precision not just for the matching required between current mirrors but the lack of coupling in the node of sum, which in general means different drain-source voltages and then inaccurate current copies.

A frequently referred strategy [26, 56] is the use of saturated current functions as shows Figure 4.7. According to this, the input transistors are first copying a current greater than I_2 forcing the output transistors to cutoff and then the output current is limited to I_3. As less current is subtracted at the input, the current I_2 activates the second stage then raising the output current. When applying a current over the value of I_1, the first stage goes to cutoff and the second mirror copies I_2 completely to be presented at the output (less I_3).

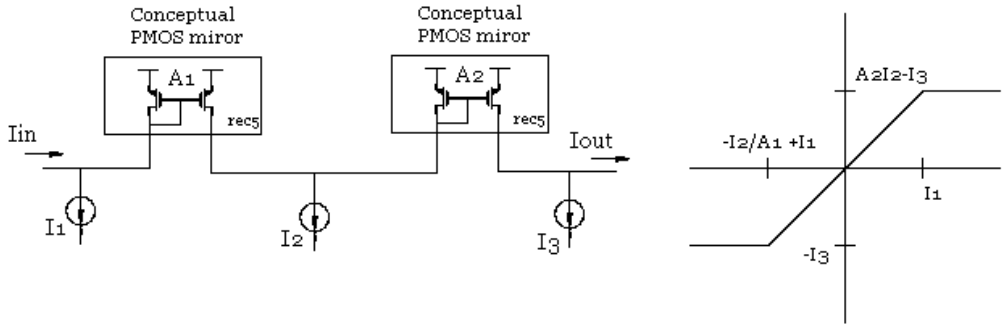


Figure 4.7: Saturated current functions (a) scheme, (b) performance.

Assuming symmetry, the saturated-like function can be described as a slope m and the breakpoint Bp wich are related by (4.4). If the first stage gain is $A_1 = 1$, the rest of the parameters are given by (4.5).

$$Bp_i = I_1 = -\Big(- \frac{I_2}{A_1} + I_1 \Big),$$
$$mBp_i = A_2(I_2) - I_3 = -(-I_3). \tag{4.4}$$

$$\begin{aligned} I_1 &= Bp_i, \\ I_2 &= 2Bp_i, \\ I_3 &= mBp_i, \\ A_2 &= m. \end{aligned} \tag{4.5}$$

A circuit is developed to work in the appropriate limits realizing the copy of the current in one half of the plane. This cell is based on the full wave rectifier reported in [57] and shown in Figure 4.8.

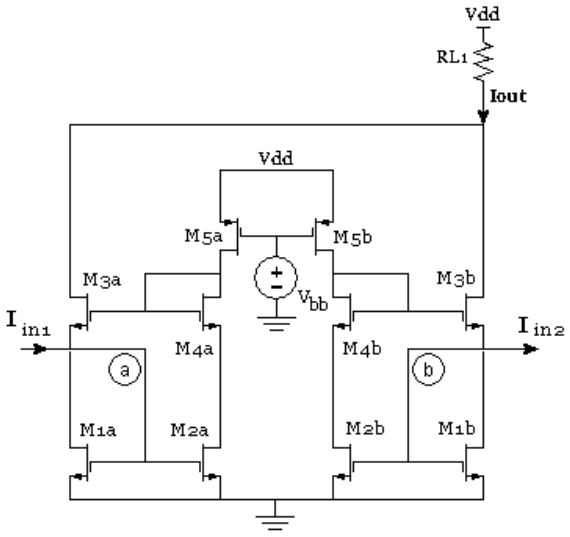


Figure 4.8: Full wave current rectifier of [57].

As described in [57], transistors M5a and M5b biases their corresponding branches. Transistors M3a and M3b alternates between saturation and cut off mode depending on the voltages a and b which strongly depends on the current direction. In this way the left and right circuit parts alternate operation over the resistance R_L.

In order to rectify one half of the signal and maintain low input impedances, one of the two components of the rectifier is taken and a dual circuit is added to make it work on the other polarity thus allowing an extra path for the input opposite direction current. The circuit is shown in Figure 4.9. Figure 4.10 describes the current behavior for both different charges R_{L1} and R_{L2}. The slope in the input voltage points for the input resistance of the circuit and is shown to be low in a reasonable range.

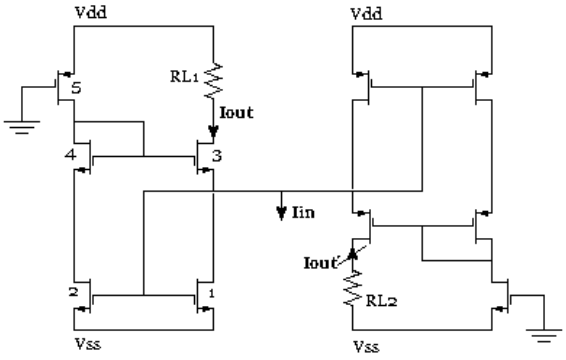


Figure 4.9: Circuit for separated half-wave rectification.

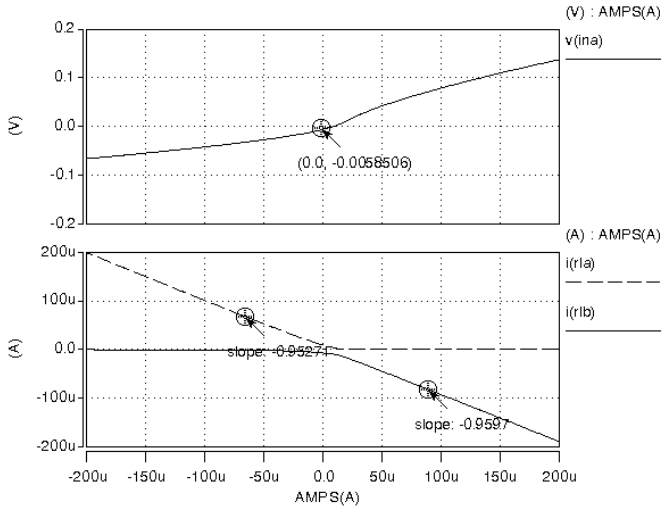


Figure 4.10: Performance of the half-wave rectifier.

The concerning current flows trough R_{L1}, to avoid a charge connected to the supply

level, this current is mirrored as shown Figure 4.11. Transistor M8 stands for biasing purposes, but it will generate a current offset. This is corrected by adding an extra mirror as shown in Figure 4.12, where resistor R_{L2} has been replaced by transistor M55 in triode.

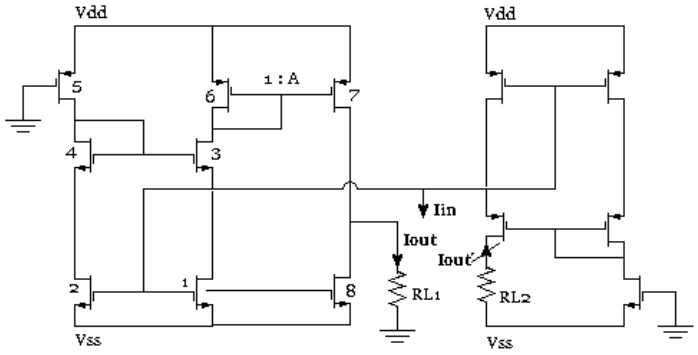


Figure 4.11: The rectification cell showing standard output.

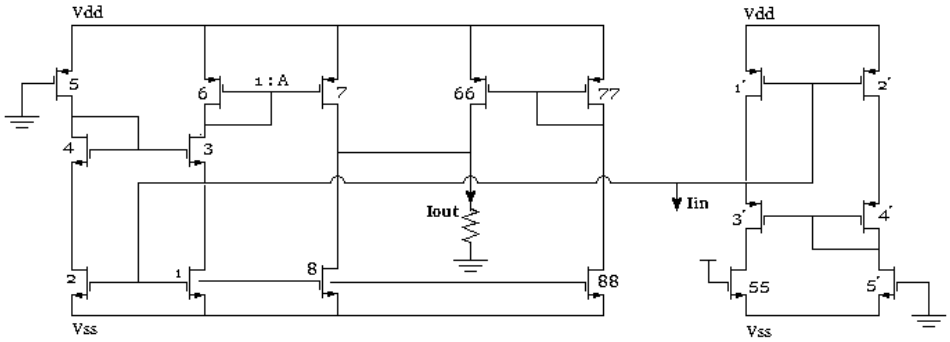


Figure 4.12: The proposed rectification cell.

Finally the performance of the cell is shown in Figure 4.13. Table 4.3 lists some important characteristics of the circuit. One of the main non-idealities of the circuit is the mismatch between drain-source voltages of transistors M1, M8 and M88 which reduces the gain of the circuit. Another effect is a sensible offset presented at the input port which depends on the dimensions of the input transistors. In order to maintain low impedance, this effect is allowed and incorporated to the saturated function model

as part of the currents I_1 and I_2.

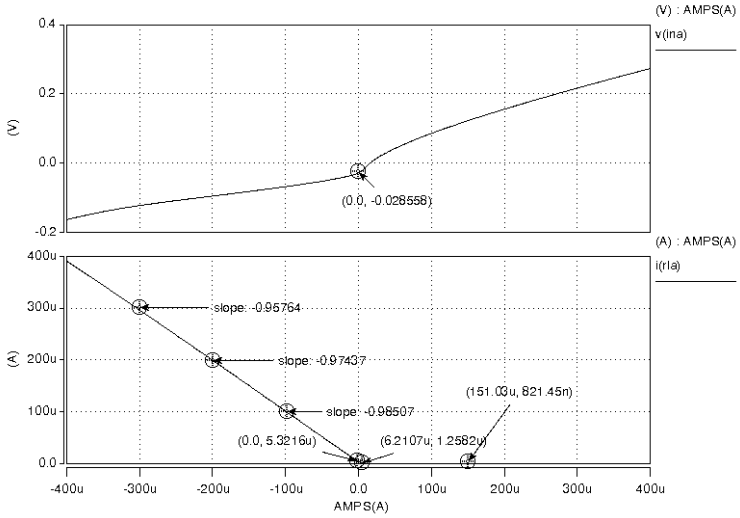


Figure 4.13: General performance of the proposed cell.

Table 4.3: Principal characteristics of the cell.

Active BW (500Ω, 1pF)	120MHz
Current gain	0.974
Input impedance	$< 850\Omega$
Output offset	$< 0.5\mu A$
Input offset	$7\mu A$
Excursion level	$> \pm 300\mu A$

If the new model of Figure 4.14 is considered and taking $A_1 = 1$, equations (4.4) and (4.5) will change to (4.6) and (4.7)

$$Bp_i = I_1 + i_{off} = -\Big(- \frac{I_2 + i_{off}}{A_1} + I_1 + i_{off} \Big),$$
$$mBp_i = A_2(I_2 + i_{off}) - I_3 = -(-I_3). \tag{4.6}$$

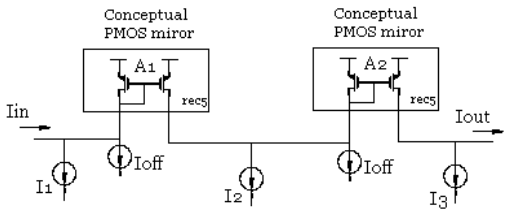


Figure 4.14: Saturated model including offset current of the cells.

$$\begin{aligned} I_1 &= Bp_i - i_{off}, \\ I_2 &= 2Bp_i - i_{off}, \\ I_3 &= mBp_i, \\ A_2 &= m. \end{aligned} \tag{4.7}$$

The obtained saturated function is tested in the voltage and current-mode Chua's circuits approach shown in Figures 4.15 and 4.16, the generated double scrolls are shown in Figure 4.17 for each one.

Additionally, the stair-case function modeled in Chapter 3 is developed by this technique and applied to the multiscroll voltage-mode circuit described in Figure 3.13 to

Table 4.4: Transistor dimensions of the cell.

W/L $(L = 1\mu)$	
M1, M2, M8, M88,	0.35
M3, M4	38.4
M5	1.5
M6, M7, M66, M77	35
M1', M2'	1.5
M3', M4'	38.4
M55, M5'	0.35

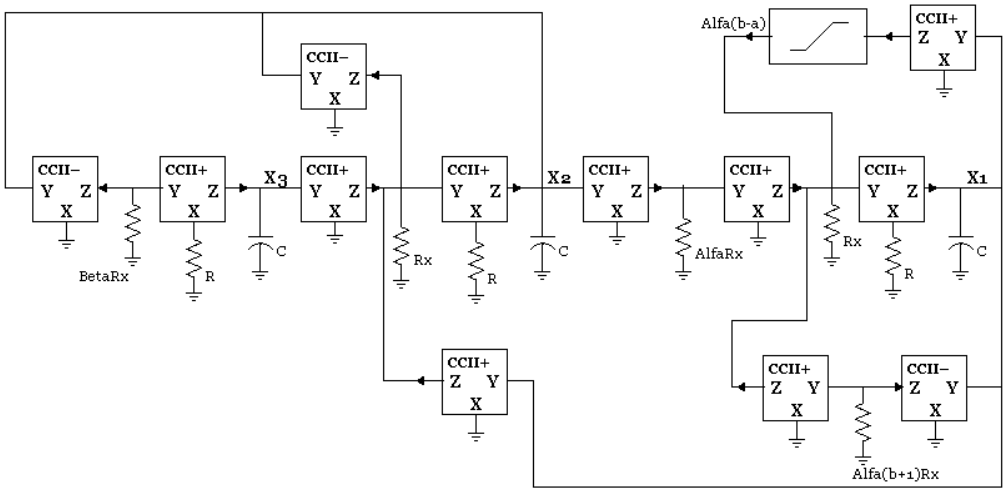


Figure 4.15: Voltage-mode realization of the Chua's oscillator.

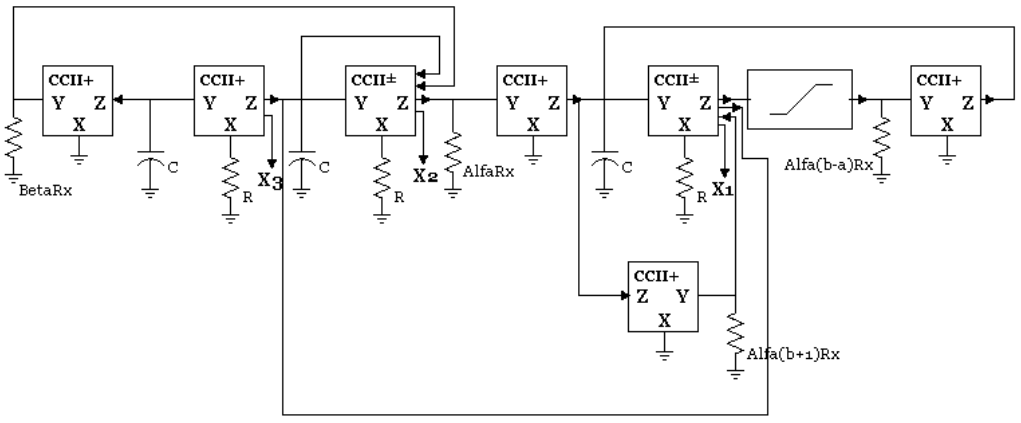


Figure 4.16: Current-mode realization of the Chua's oscillator.

generate 2, 3 and 4 scrolls as shown in Figure 4.18. Offsets are pointed as a determining factor to the appearance of multiple scrolls. The mirror construction process allows the adjusting of these offset currents because of the current source located at the end of each stage.

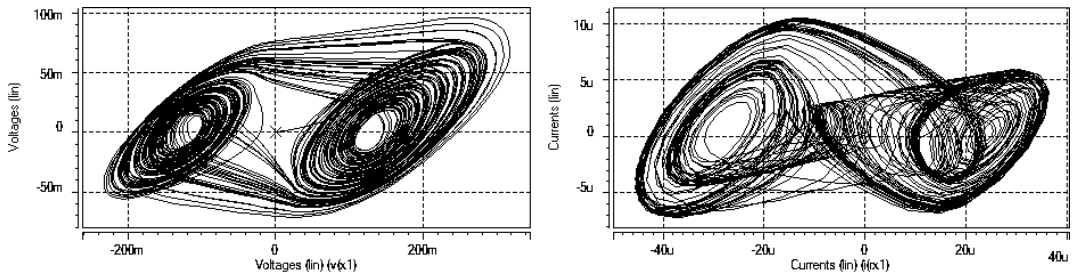


Figure 4.17: Chua's Double scroll for (a) the voltage-mode and (b) the current-mode circuit.

4.2.3 PWL functions synthesized by saturated CCIIs

The use of CCIIs allows the designer to use the mixed nature of these blocks to generate saturated functions in current-mode. Many of the existent schemes [23, 30, 34] obtain saturated forms by controlling the supply level of the used blocks: CCIIs, OTAs, Opamps, etc; by using different supply levels for each saturated form. A less expensive approximation is to produce such functions in current and only changing the bias current for each different breakpoint.

To saturate a CCII, the differential-pair is an ideal topology due to the bias limited current that can be handled by terminal X, and consequently Z. If more current is demanded, the circuit response will be constant. For practical purposes, a saturated current follower can be built by connecting two of these block in series, the first controlling the variable input impedance of the second and offering a lower input impedance due to a constant and relatively high bias current Ib_1; this block can also be based on the push-pull CCII due to its wide application range. As for the second, the bias current Ib_2 is selected equal to the desired breakpoint. The saturated CF and its response are shown in figures 4.19 and 4.20. The input voltage shown in Figure 4.20(b) describes an input resistance of $3.3k\Omega$ according to the slope and the bias curret, which is handled by the preceding CCII. The voltage excursions at the input node will be small for large input current, this improves the interstage errors in the circuit [30].

In order to generate multiple breakpoints, these blocks can be combined directly in parallel, but if shifting is expected, an arrange with intermediate current sources can

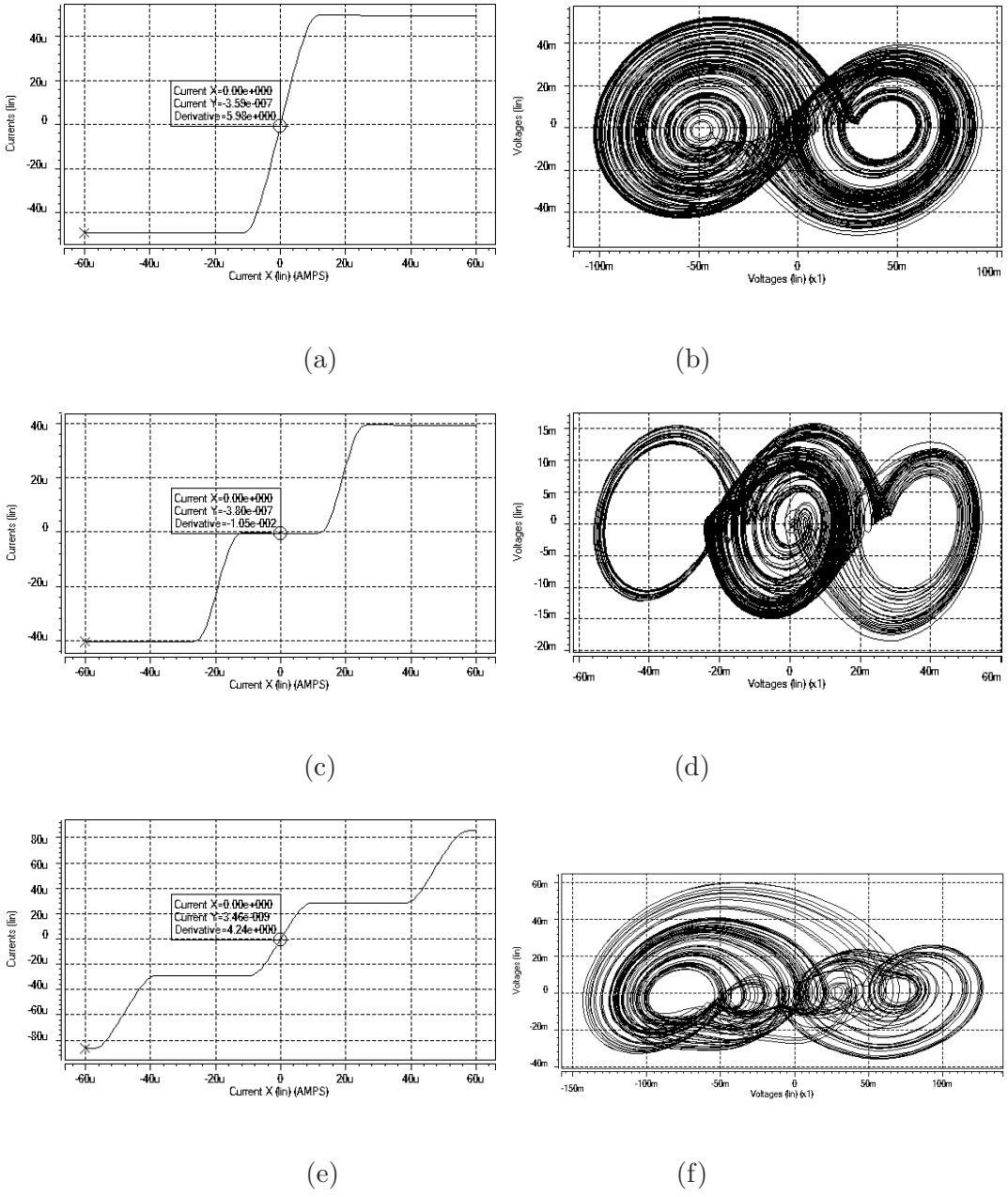


Figure 4.18: PWL functions for the voltage-mode (a) 2, (c) 3 and (e) 4 scroll circuit and the corresponding scrolls (b), (d) and (f).

be easily applied as shown in Figure 4.21.

The positive CCII with Y and Z terminals connected together is suitable for negative

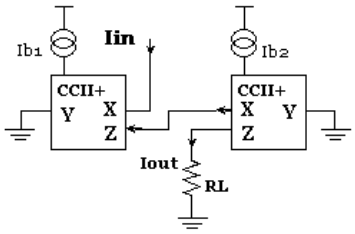


Figure 4.19: Saturated CF based on current-saturation of the CCII.

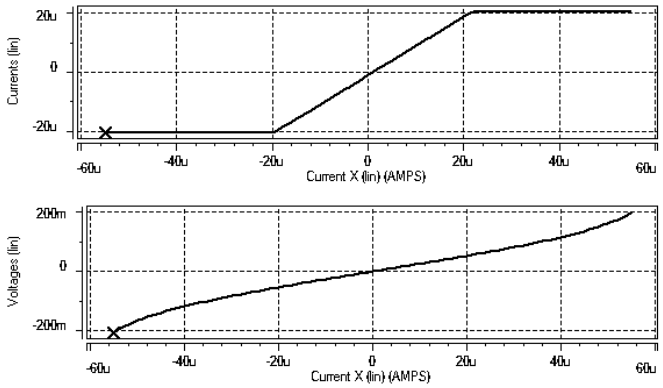


Figure 4.20: Performance of the saturated CCII, (a) output current, (b) input voltage.

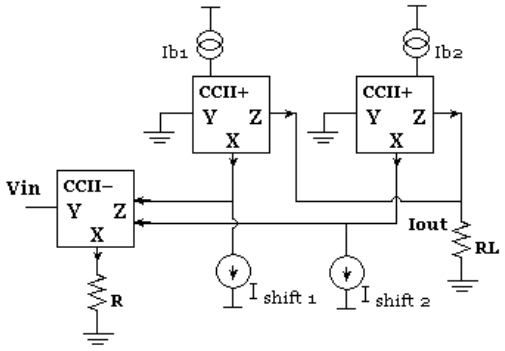


Figure 4.21: Multiple step PWL generator.

impedances simulation. Its value is directly related to the parasitic resistance seen at R_X which is also controlled by the bias current. In this manner, a simple PWL function can be directly realized by connecting two of these *saturated* CCIIs for generating the

slope and breakpoint taking as a reference the behavior of the parasitic resistance shown in Figure 4.4, in this case $Ib_1 = 35\mu A$ and $Ib_2 = 70\mu A$. The double scroll diagram and the circuit are shown in Figure 4.22.

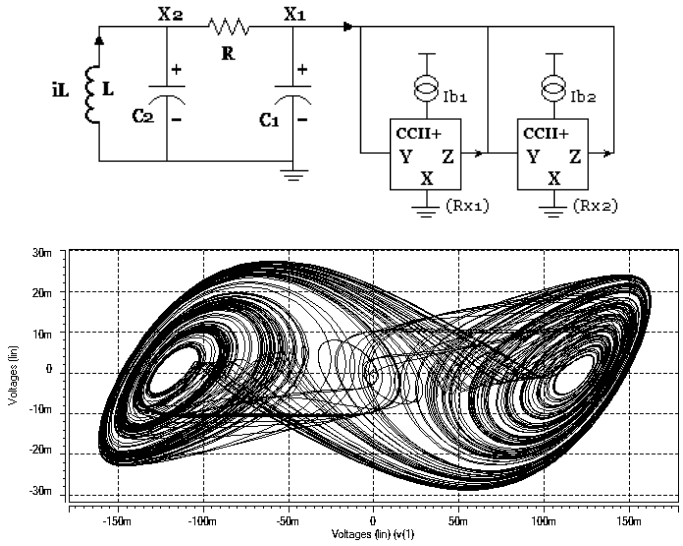


Figure 4.22: Schematic and scroll behavior of the direct Chua's circuit using saturated CCIIs.

A simple realization for Chua's hyperchaotic circuit only needs the coupling stage shown earlier in Figure 3.10. The obtained hyperchaotic attractors are shown in Figure 4.23. Compare with that of Figure 3.11.

By arranging more than one saturated CCIIs, the stair-case function can be done. In this case, the current-mode multiscroll circuit is shown in Figure 3.15 using the topology shown in Figure 4.24.

Because of the obtained performance, the saturated approach has been applied to voltage-mode multiscroll circuits to observe their performance against the rectifiers approach. The obtained results are shown in Figure 4.25. A current gain stage at terminal Z has been sometimes necessary to increase slopes in order to promote the generation of more scrolls according to theory [14].

In addition, the generalized Chua's circuit has been carefully recalculated around the resistance R in order to require appropriate bias currents for slopes and, as these

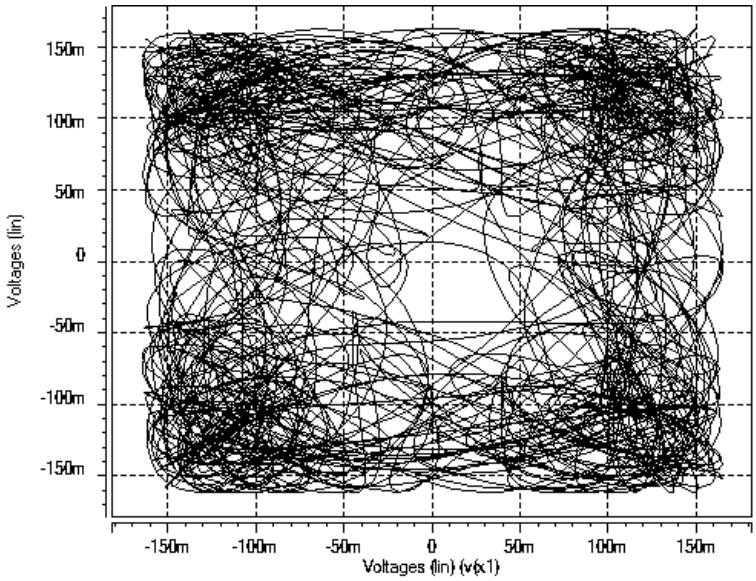
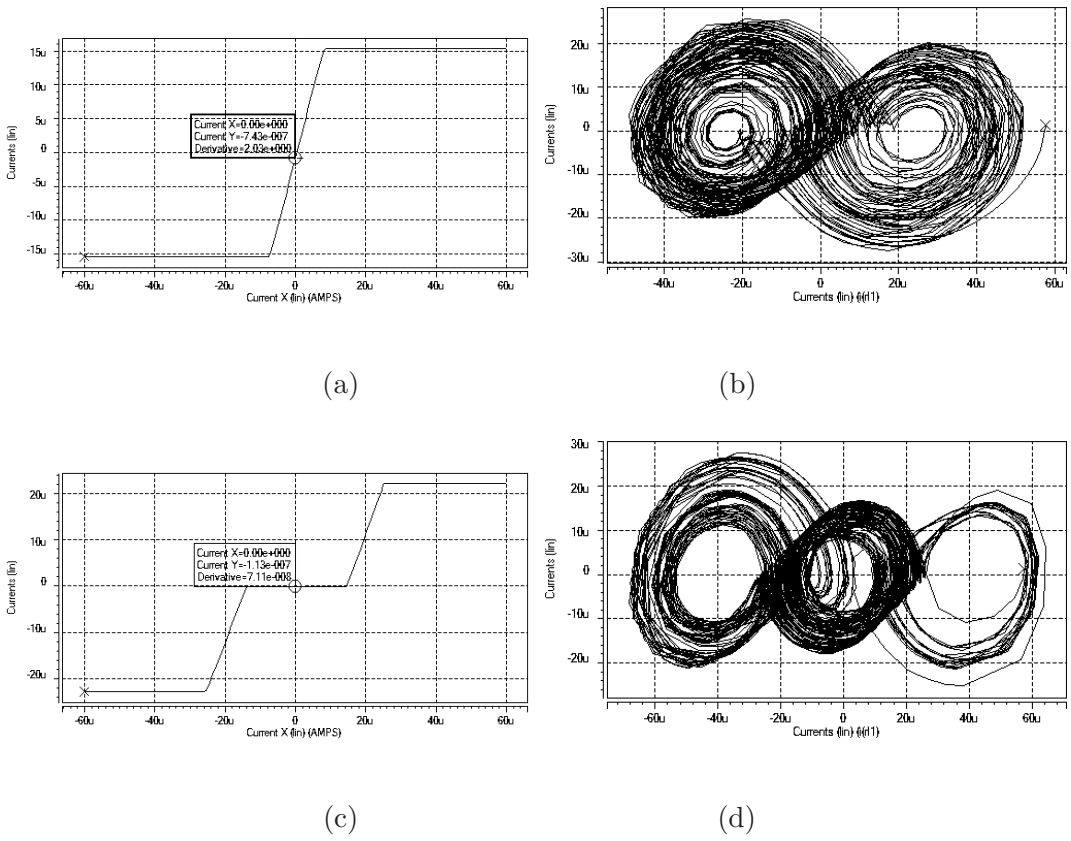


Figure 4.23: Phase projection x_4 to x_1 of CCII-based hyperchaotic Chua's circuit.

slopes are related to the conductance of the CCII by $R_X = R/coef_i$, where $coef$ is the PWL function coefficient from expression (3.5). The following relation must be valid for this implementation.

$$min((R/coef_i) > R_X(Ib_i)) \tag{4.8}$$

Where Ib_i represents the saturation current which defines the function breakpoints determined in (3.5). The circuit schematic and scroll behavior is shown in Figures 4.26, 4.27 and 4.28 for two, three and four scrolls, respectively. The scroll asymmetry is caused by the numerous contributions of currents to the PWL function which are affected by the CCII limited current gain for low resistances in R_X. The circuit parameters are listed in Table 4.5.



(a) (b)

(c) (d)

Figure 4.24: PWL functions for the current-mode (a) 2 and (c) 3 scroll circuit and the corresponding scrolls (b) and (d).

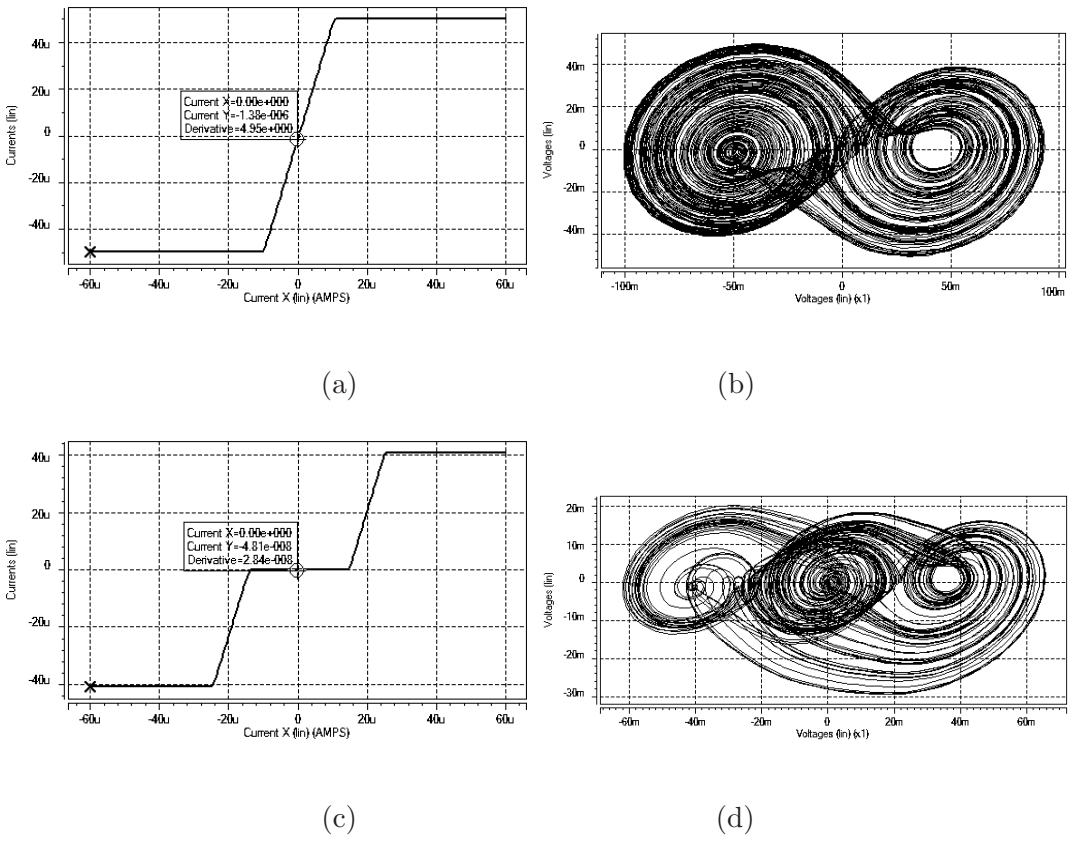


Figure 4.25: PWL functions for the voltage-mode (a) 2 and (c) 3 scroll circuit and the corresponding scrolls (b) and (d).

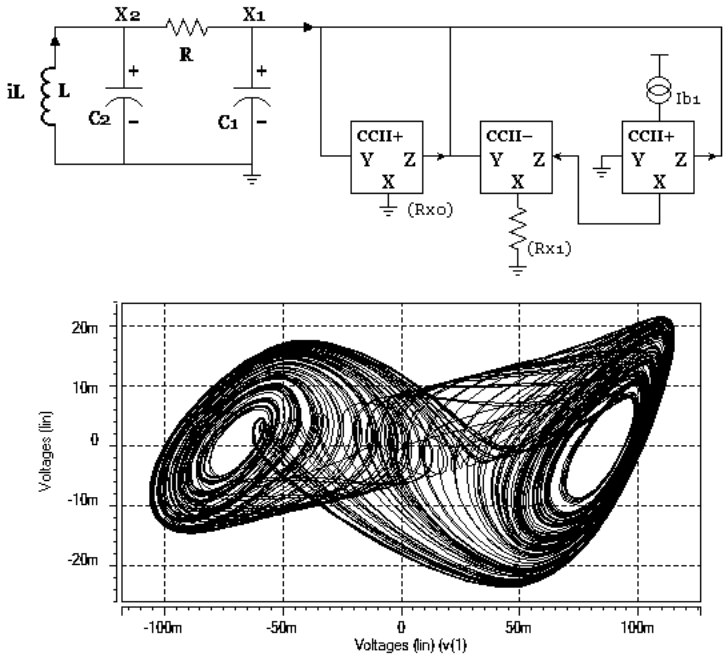


Figure 4.26: The generalized Chua's circuit for 2-scrolls, (a) schematic and (b) phase plot.

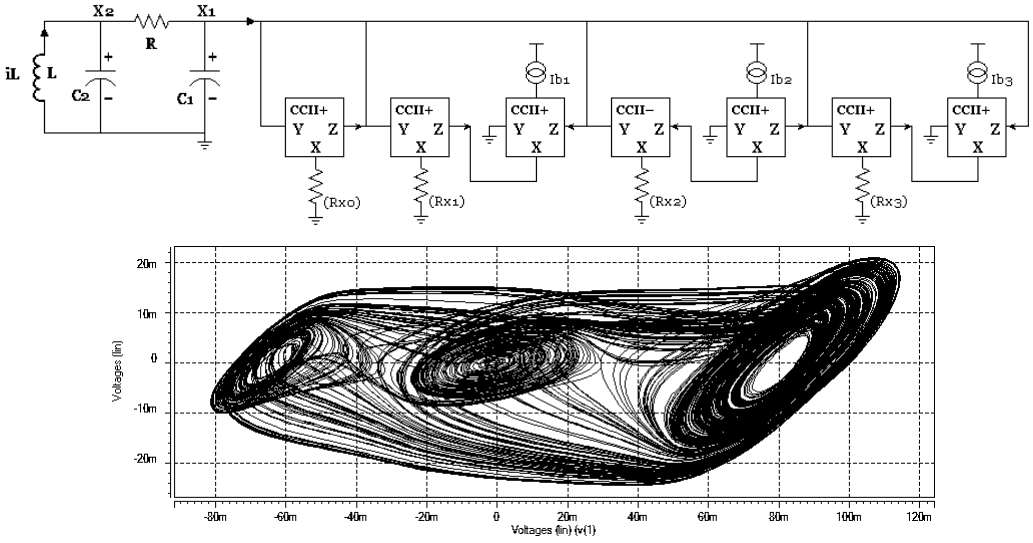


Figure 4.27: The generalized Chua's circuit for 3-scrolls, (a) schematic and (b) phase plot.

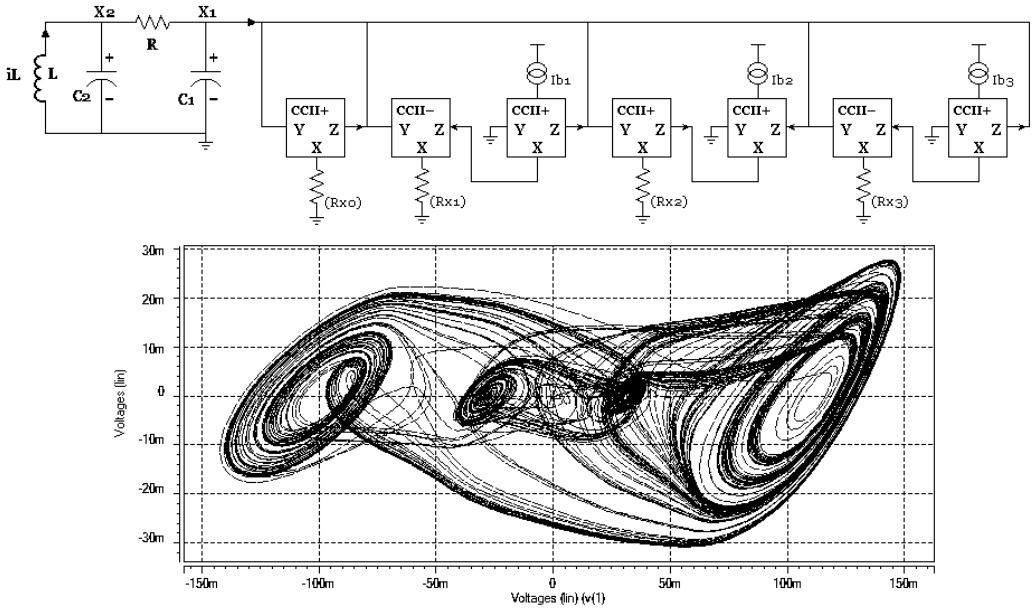


Figure 4.28: The generalized Chua's circuit for 4-scrolls, (a) schematic and (b) phase plot.

Table 4.5: Principal characteristics of the CCII-based Generalized oscillators.

Parameters	Components	2-scroll	3-scroll	4-scroll	units
Circuit	R	713	1400	955	Ω
	C_1	3	0.7	1.58	nF
	C_2	27.3	6.3	14.3	nF
	L	1	1	1	mH
PWL function	R_{X0}	1012	1117	1400	Ω
	R_{X1}	1687	2692	2333	Ω
	Ib_1	30	9.5	8.5	μA
	R_{X2}	-	1615	1166	Ω
	Ib_2	-	33.5	37	μA
	R_{X3}	-	1780	1166	Ω
	Ib_3	-	56.5	62	μA

Chapter 5

CONCLUSIONS

In the present work, a special set of chaotic systems has been reviewed, these are characterized for being based in a PWL function to produce chaos. The characteristics of the most known of them were described in order to obtain chaotic response under circuit conditions.

The second generation current conveyor has been proposed as a fundamental building block in mixed-mode processing to realize integro-differential operations and the other required by chaotic systems. In this way, it has been proposed to use the CCII as an alternative to design chaotic oscillators mainly when integrated level schemes are required; moreover, simulations are based in standard 0.35 μm CMOS technology.

Some approaches were introduced for the PWL characteristic function generation. Some of them are based on current-processing simple blocks and others are based on special blocks arrays which take advantage of particular circuit parameters such as the output resistance, the parasitic resistance R_x and the saturation bias current.

In this last case, the PWL function was synthesized by using the bias current limit as part of the design in a specific CCII topology. Descriptions of the relevant characteristics were given for the practical use in a variety of applications. However, the design of circuits based on system description is presented based on the building blocks macromodeling, thus following a systematic circuit synthesis. Chaotic systems have been tested initially under these models and lately under transistor level description.

Macromodels have been provided for the CCII an also for voltage and current followers.

5.1 Future Work

From the exposed topic, several lines of research have remarkable importance for future work:

- To optimize performances of the proposed chaotic oscillators, in order to follow with the layout generation and fabrication of the proposed circuits to prove the chaotic dynamics already obtained by simulation. Parallel to this is to adapt the designs to the characteristics of the commercial CFOA AD844 macromodel.

- Improving the frequency performance of these circuits is an important issue in communications; for this reason, an in-depth analysis of the nonlinear topologies is required in particular for the multiscroll circuit. A current-comparator scheme is desired to minimize the response time, a fact which would allow the circuit dynamics to have more equilibrium points and therefore, more amount of scrolls.

- For all the CCII-based systems, an improved CCII block in offset and output resistance is still required. A minimal parasitic resistance R_X value would allow to work on higher ranges and to have mode flexibility in design due to the fact that transconductances between ports Y and Z, would not be necessary related to the inverse of this R_X value. It is also important to point that for high frequencies, the variation of this parasitic would not be the enough to change the system parameters and lose chaotic behavior.

- Encryption and private information transmission is one of the chaotic circuit potential applications. Once selected a synchronization technique, several systems must be tested in frequency and correlation analysis to choose a good transmitter/receiver system. The signal embedding process must be studied in order to find an adequate modulation or transmission technique to guarantee information confidentiality.

- Chaotic oscillators nowadays require a more simple an portable design in order to be applied in several subjects in electronics, such as the data encryption process and the random number series generation process.

- Finally, and not less important to mention is that the PWL function synthesis techniques presented in this Thesis could be applied in decision taking fuzzy models and in signal processing methods of variable gain among others.

Appendix A

Chaos Indicators

As stated before Lyapunov exponents spectrum is generally used to show how much two trajectories can diverge from slightly different initial conditions. A brief review is given about this topic as well as Poincaré maps.

A.1 Lyapunov Exponents

Given the system constants, Lyapunov exponents generalize its eigenvalues at an equilibrium point. They can determine the stability of all kinds of steady-state behavior [16]. In fact, the spectrum of Lyapunov Exponents indicates the divergence or convergence of the trajectories of a chaotic system. A positive exponent implies exponential divergence of the trajectories and therefore sensitivity to initial conditions. A method to compute them by using time series is given by Wolf et al. [3].

For a continuous dynamical system of dimension n, the evolution from the initial conditions in an infinitesimal n-dimensional region is observed. The *i-th* one-dimensional Lyapunov exponent gives de average exponential rate of divergence of infinitesimally nearby initial conditions in each i-axis. Taking y_0 as a tangent vector which points the direction of the infinitesimal displacement from x_0 a orientation dependent definition for the Lyapunov exponents is [58]:

$$\lambda \equiv \lim_{n\to\infty} \frac{1}{n} ln \frac{|y_n|}{|y_0|} \tag{A.1}$$

In this way, zero exponents indicate that the system has no fixed point in the i-direction. While negative exponents are consequence of stable systems. Positive exponents imply exponential divergence (instability). Then, those bounded systems which also have positive exponents refer to the existence of a folding process which is changing its trajectories (chaotic systems).

Lyapunov exponents are actually the most useful test for chaotic behavior. A system is considered to be chaotic if it has one or hyperchaotic if it has several positive Lyapunov exponents [32, 59]. As more positive the exponent is, more complex the system behavior due to the higher rate of new information that the system is producing.

A.2 Poincaré Maps

A chaotic n-dimensional system can also be analyzed by using Poincaré surface of section method or "Poincaré maps", which are $(n-1)$ dimensional projections of the system trajectories (see figure A.1 as an example). For 3-dimensional systems, an arbitrary point in the 2-dimensional map uniquely determines the next point, since the previous can be the initial condition of the system. The opposite relation is also valid reversing time and taking the last point as initial condition; thus these maps are invertible [58].

Naturally, the surface must be oriented appropriately to constantly intersect the trajectories. Maps can be one-sided or two-sided if they present one or both directions of the intersection respectively [16]. Poincaré maps reduces the space dimension by one, making easier to follow the trajectory dynamics for analysis and also giving a geometric representation for each type of dynamical system. In this way, these with i-period will show i points for one-sided maps and these with no period will show a closed loop (for quasiperiodic systems and infinite time) or a fractal (for chaotic systems) [60].

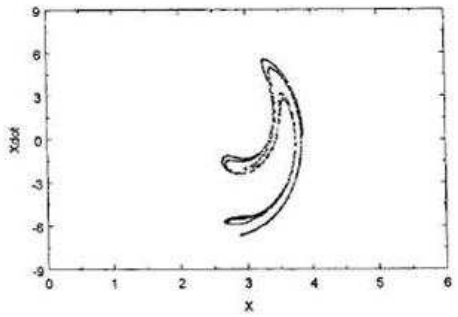


Figure A.1: The Poincaré map of the Duffing oscillator shown in [61]

Appendix B

Reported characteristics of the used systems

B.1 Chua's circuit

$\alpha = 9$

$\beta = \frac{100}{7}$

$a = \frac{8}{7}$

$b = \frac{5}{7}$ Lyapunov exponents: $\lambda_{1,2,3} = 0.3271, 0, -2.5197$

Referente [42]

B.2 Hiperchaotic Chua's circuit

Using the same parameters before and a voltage coupling $k = 1.15$

Lyapunov exponents: $\lambda_{1,2,3,4,5,6} = 0.43, 0.41, 0, 0, -3.74, -3.85$

Referente [62]

B.3 Multiscroll circuit

$a = b = c = d_1 = 0.7$

Double scroll

$K = 10, h = 20, p = 0, q = 0$

Lyapunov exponents: $\lambda_{1,2,3} = 0.1042, 0, -0.8043$

Triple scroll

$K = 10, h = 20, p = 0, q = 1$

Lyapunov exponents: $\lambda_{1,2,3} = 0.1276, 0, -0.8258$

Referente [14]

Appendix C

Published Papers

- J. M. Muñoz-Pacheco, E. Tlelo-Cuautle, R. Trejo-Guerra, C. Cruz-Hernández, *"Synchronization of n-Scrolls Chaotic Systems Synthesized from High-Level Behavioral Modeling"*, Proceedings of the 7th International Caribbean Conference on Devices, Circuits and Systems, (IEEE ICCDCS) ISBN: 978-1-4244-1957-9, Mexico, 2008.

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- R. Trejo-Guerra, E. Tlelo-Cuautle, C. Cruz-Hernández, C. Sánchez-López and M. Fakhfakh *"Current Conveyor Realization of Synchronized Chua's Circuits for Binary Communications"*, Design & Technology of Integrated Systems in Nanoscale Era (IEEE DTIS) ISBN 978-1-4244-1577-9, Tozeur, Tunisia, March 25-28, 2008.

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