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"An Accurate On-Chip Interconnect Modeling Methodology for the Design of Clock Generation and Distribution Networks"

by

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Dedicatoria

A las personas que más amo en mi vida.

Mis padres:

Eloisa Díaz González

y

Victor Rodolfo González Analco

Mis hermanos:

Rudy,

Elo,

y

Edith

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Abstract

On-chip interconnections play a key role in the design and implementation of current and future clock generation and distribution networks used for synchronization of high-performance integrated systems; therefore, an accurate modeling (i.e. electrical representation) of the interconnections used in this type of networks is essential and it represents an important research area.

In global and local clock networks, the interconnection lines in combination with a set of gain stages are used to simultaneously generate and distribute high-frequency synchronization signals throughout the integrated circuit. Therefore, in the design of this type of networks, the electrical equivalent circuit model provides important information about the characteristics of the interconnections used in the implementation; then, based on this information, an accurate design of the gain, compensation, and output stages can be carried out.

Traditionally, the interconnection lines used in the design of integrated systems have been represented by electrical equivalent circuit models obtained from basic analytical expressions and technology parameters provided by the foundry; however, the accuracy of these models is limited specially for the representation of interconnections operating within the Gigahertz (GHz) frequency range where the frequency dependence of the interconnect parameters can not be neglected. Therefore, in the design of high-speed integrated systems (e.g. clock generation and distribution networks) it is necessary to implement accurate equivalent circuit models for the representation of the interconnections; for this reason, in this thesis the establishment of a modeling methodology that allows circuit designers to perform an accurate representation of

the interconnection lines used in the design and implementation of global and local clock networks is presented.

The modeling methodology is developed directly from S-parameter measurements of fabricated test structures and includes: the interconnect parameter extraction procedure, the equivalent circuit model selection, and the determination of the minimum number of sections required in the equivalent circuit for the accurate representation of interconnects of certain lengths within specific frequency ranges, while considering the frequency-dependent nature of the associated parameters.

The interconnect modeling methodology is applied to a set of fabricated interconnection lines typically used in the design and implementation of global and local clock networks. Likewise, in order to show the accuracy and application of the proposed methodology in the design and implementation of current and future clock generation and distribution networks, the design and fabrication of several expanded three-stage ring oscillators using interconnections with lengths in the order of millimeters are carried out. In addition, the design of local clock networks implemented by interconnecting and coupling expanded ring oscillators is presented.

In the design of integrated systems, the circuit designer is responsible for defining the methodology used to obtain the equivalent circuit model which represents the interconnection lines used in the corresponding implementation. Nevertheless, in the design of high-frequency clock networks, interconnection lines play an essential role in the generation and distribution of the clock signals; therefore, an inaccurate representation of the interconnections used in the implementation of this type of networks will be reflected in an inadequate system performance. So, the proposed modeling methodology represents an appropriate alternative to solve some of the problems related with the electrical representation of the interconnections used in the design and implementation of current and future clock generation and distribution networks.

Chapter 1

Introduction

1.1 Importance of Interconnects and their Accurate Modeling

Nowadays, design of microprocessors that perform many functions at high speed and low power consumption is very important for the implementation of multimedia equipment (e.g. computers, cell phones, video games, video cameras, audio players, etc.). In a high-performance microprocessor, a large number of functions is carried out in a synchronous digital way; therefore, the incorporation of a clock network responsible for generating and distributing the synchronization signal (to all points where the signal is required in the microprocessor) is indispensable.

In current microprocessors, the clock signal is generated at a single point and distributed throughout the integrated circuit (IC) using a global clock generation and distribution network (GCGDN), usually implemented by a phase-locked loop circuit (PLL) and a clock distribution network (CDN) [1]. However, due to the continuous downscaling of the technology, increase in area of the integrated circuits, and physical limitations of the interconnection materials, the generation and the distribution of a clock signal at high operating frequencies, with low time uncertainty (i.e. low skew

and jitter), and low power consumption are increasingly difficult to achieve using the global clock networks [2] [3] [4].

In order to solve the problems related to global clock networks, currently, one of the design philosophies that are under study is the local clock generation and distribution networks (LCGDN). In this case, the clock signal is generated at different points in the IC by interconnecting and coupling of oscillators implemented by interconnection lines and gain stages. Thus, the area in which the clock signal has to be distributed (coverage area) is reduced; so that it is possible to generate and distribute clock signals at high operating frequencies and with a low time uncertainty [5], [6], [7].

As it is well known, on-chip interconnections play a key role on determining the performance of high-frequency analog, digital, and mixed signal systems, especially in current and future fabrication technologies which have pushed the operating frequency of integrated systems within the GHz frequency range. Nevertheless, in the design and implementation of global and local clock networks, the interconnection lines are essential in the generation and distribution of the clock signal; hence, an accurate modeling (electrical representation) and characterization (parameter extraction) of the interconnections commonly used in this type of systems are very important, representing an important research area.

Traditionally, the interconnections have been modeled using a single lumped capacitance C to represent the parasitic load introduced by the line. However, due to the continuous down-scaling of the technology, the finite resistance of the metal traces has also taken importance in limiting the performance of on-chip interconnections; therefore, RC models have been used to carry out the corresponding representation at relatively high frequencies [8]. Likewise, in high-speed IC technologies that exhibit sub-nanosecond switching, the inductance associated with the metal traces as well as the conductance associated with the inter-metal dielectric can not be neglected. Hence, it is necessary to consider RLC and $RLCG$ equivalent circuit models for precise representation of practical on-chip interconnects used in the design of high-frequency systems.

In previously reported research work dedicated to state-of-the-art interconnections, the corresponding representations are achieved by means of RC and RLC distributed equivalent circuit models including the total resistance, inductance, and capacitance of the interconnection line. In these models, the values of per-unit-length resistance (R_l), inductance (L_l), and capacitance (C_l) are obtained from basic analytical expressions and technology parameters provided by the foundry (i.e. a frequency invariant model) [9], [10], [11]; unfortunately, the values of R_l, L_l, and C_l, are assumed to be constant with frequency, which is fundamentally incorrect within the GHz frequency range. These models are widely used by circuit designers to quickly estimate delays of different paths within the circuits; however, in designs meant to operate at high frequencies the simulation results may substantially vary from experimental data due to an inaccurate modeling of the interconnections.

In order to take into consideration the frequency dependence of the interconnect parameters and effects that become apparent at high frequencies for proper representation of the interconnection lines, the approaches in [12], [13], [14] carry out parameter extraction directly from S-parameter measurements. Nonetheless, this procedure has been rarely used in practical integrated circuits since many designers assume that a frequency invariant model is sufficient to represent the interconnection lines. However, in the design of high-frequency circuits such as global and local clock networks, an exact representation of the interconnections is essential; so, one of the contributions of this proposal is encouraging designers to use experimentally implemented interconnect representations even though many authors still use the frequency invariant model for on-chip interconnections.

In the design of integrated systems containing a large number of interconnections, another aspect that must be taken into account by the circuit designer is the number of sections required in the equivalent circuit to represent the interconnections, which is related to the accuracy and computation time required to carry out the corresponding simulations. In several works, interconnection lines have been represented by a distributed equivalent circuit model implemented with n sections, e.g. 20 sections as

shown in [15]. Obviously, using a large value for n allows one to accurately represent an interconnection up to higher frequencies than in the case of using a small value for n; unfortunately, this also increases the simulation time that is considerably higher in the design of ICs containing thousand of interconnections. Therefore, the determination of the number of sections in which the equivalent circuit model has to be divided for properly representing a line of a given length and operating up to a given frequency is very important; nevertheless, the procedure to determine the number of sections is not clearly stated in previous approaches.

The main contribution of this proposal is the establishment of a methodology that allows circuit designers to perform an accurate representation of the interconnection lines used in the design and implementation of global and local clock generation and distribution networks. This methodology (developed from S-parameter measurements) includes the parameter extraction procedure, the equivalent circuit model selection, and the determination of the minimum number of sections required in the equivalent circuit for accurate representation of interconnects of certain lengths within specific frequency ranges while considering the frequency-dependent nature of the associated parameters.

1.2 Document Organization

This thesis is organized as follows:

- Chapter 2 shows a qualitative analysis of global and local clock generation and distribution networks recently under study. In this analysis the key role of the interconnections in the design and implementation of current and future global and local clock networks is highlighted.

- Chapter 3 shows the parameter extraction associated with typical on-chip interconnections used in the design and implementation of global and local clock generation and distribution networks. In the first part of this chapter, a description of on-chip interconnections is presented; then, the interconnect parameter

extraction developed from S-parameter measurements of fabricated test structures is carried out.

- Chapter 4 presents the interconnect modeling methodology. In this chapter, the equivalent circuit model selection and determination of the minimum number of sections required in an equivalent circuit model for the proper representation of interconnections used in the design of integrated systems is carried out. In addition, a summary of the main steps required to develop the interconnect modeling methodology is presented.

- Chapter 5 shows the design application of the proposed interconnect modeling methodology. In order to show the accuracy and application of the interconnect modeling methodology in the design and implementation of clock generation and distribution networks, the design and fabrication of several expanded three-stage ring oscillators is carried out. In addition, the design of local clock networks implemented by interconnecting and coupling three-stage ring oscillators is included.

- Chapter 6 presents the conclusions and suggested future work.

- Appendix A shows the fabricated silicon prototype and test setups used to perform the measurements. Firstly, a description of the fabricated interconnection line test structures and expanded three-stage ring oscillators is presented. Also, a description of the test setups used to perform the measurements of the fabricated interconnection lines and ring oscillators is shown in the second part of this appendix.

- Appendix B shows the application of the modeling methodology to a set of fabricated structures. Firstly, the values of Z_C, γ, R_l, L_l, and C_l of the fabricated structures are obtained; then, the determination of the minimum number of sections required in the equivalent circuit for accurate representation of interconnects of certain lengths within specific frequency ranges is carried out.

- Appendix C presents a summary of the features and performance of the fabricated ring oscillators. In this appendix, simulated and experimental results of the implemented oscillators are presented; in addition, the schematic, layout, and photograph of each one of the fabricated oscillators are included.

- Appendix D shows a list of the publications derived from this work.

Chapter 2

Clock Generation and Distribution Networks

In this chapter, a qualitative analysis of global and local clock generation and distribution networks recently under study is presented. The analysis shows the basic concepts and the key role of interconnections in the design and implementation of current and future clock networks.

2.1 Global Clock Generation and Distribution Networks

In current high-performance microprocessors, the global clock generation and distribution network (GCGDN) is responsible for generating and distributing the clock signal (i.e. the most widely distributed signal on the chip) to all points where the signal is required (e.g. latches, flip-flops, and other synchronous blocks). In a GCGDN, the clock signal is generated and multiplied by the phase locked loop (PLL) circuit; then, the signal is distributed throughout the IC using a clock distribution network (CDN) as shown in Fig. 2.1 (a). There are several network topologies used for clock distribution [1]; nevertheless, H-trees and Grid distribution networks implemented by

buffers and interconnection lines are most commonly used in the design and implementation of global clock networks.

In a GCGDN, the clock signal generated by the PLL is distributed over a certain area by the distribution network. However, due to the continuous scaling of the technology, increase in area of integrated circuits, and physical limitations of the interconnection materials; there is a maximum distance in which the clock signal can be distributed. This region is known as isochronous, and the corresponding distance is inversely proportional to the operating frequency; the associated coverage area can be seen in Fig. 2.1 (b).

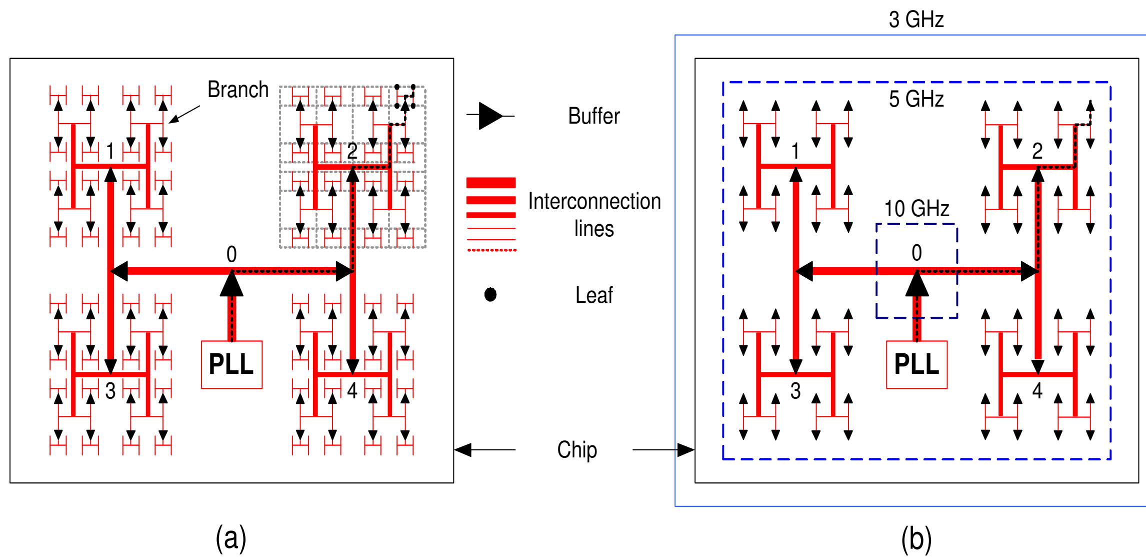


Figure 2.1: (a) Global clock generation and distribution network. (b) Isochronous regions.

Another important problem related to global networks is the design and implementation of a perfectly balanced distribution network. In an ideal case, the clock signal generated by the PLL circuit is simultaneously distributed to all final points (i.e. leaf). Nevertheless, due to the mismatches associated with the length of the interconnections, process variations, electromagnetic coupling, load restrictions, and block distribution in complex integrated systems, the design and implementation of perfectly balanced networks is increasingly difficult. Thus, if the clock distribution

network presents unbalanced branches, the time uncertainty is considerably increased.

The GCGDNs are well understood and widely used in the implementation of integrated systems; nonetheless, the requirements of high operating frequency, low time uncertainty, and low power consumption for current and future integrated systems are increasingly difficult to satisfy using global networks.

In order to generate and distribute a clock signal at high operating frequency and low time uncertainty using global clock networks, several improvements and compensation techniques have been proposed [2], [3], [4]. Nevertheless, the main disadvantages of these proposed techniques are: a) higher power consumption, b) high complexity, and c) area.

2.2 Local Clock Generation and Distribution Networks

One of the design philosophies recently under study is the local clock generation and distribution networks (LCGDN), implemented by interconnecting and coupling oscillators. In a LCGDN, the clock signal is generated at different points in the IC, as shown in Fig. 2.2; in this way, the coverage area and length of the interconnections are reduced. Thus, the generation and distribution of high-frequency signals with low time uncertainty are achieved.

In a local clock network, the operating frequency, amplitude, and phase of the generated signals strongly depend on the characteristics of the oscillator used in the implementation. Also, another important feature of this type of networks is the phase averaging process. In a clock network implemented by interconnecting and coupling oscillators, the phase of the generated signals is averaged at each coupling point; therefore, the phase differences among the signals generated by each oscillator are reduced by this averaging process [6].

In general, there are three types of local clock networks which are classified according to the type of oscillator used for the implementation: a) LCGDN using ring

oscillators, b) LCGDN using traveling wave oscillators, and c) LCGDN using standing wave oscillators.

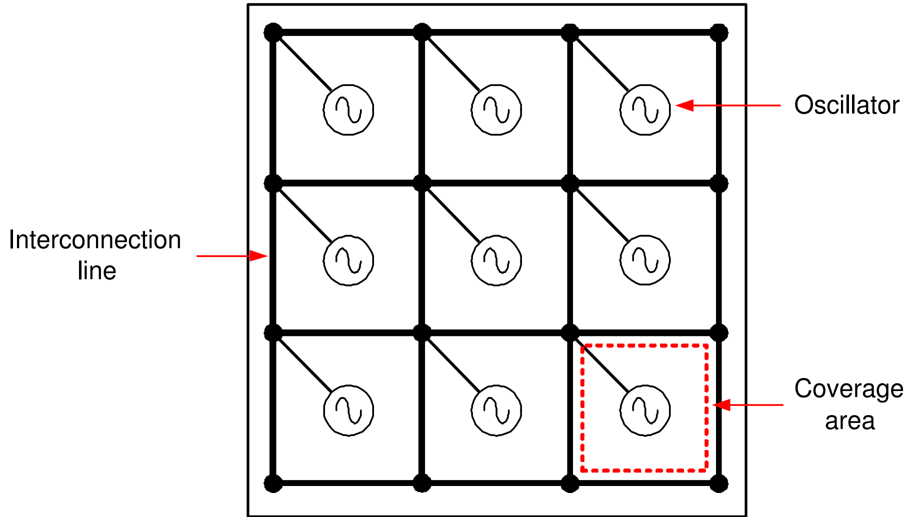


Figure 2.2: Local clock generation and distribution network.

2.2.1 LCGDN using Ring Oscillators

A ring oscillator is a feedback circuit implemented by N gain stages in a close loop that generates by itself (i.e. without excitation) a periodic signal at frequency f if and only if the oscillation Barkhausen criteria are satisfied [16]:

$$|H(j\omega)| \geq 1 \tag{2.1}$$

$$\angle H(j\omega) \geq 180^\circ \tag{2.2}$$

where $\omega = 2\pi f$.

Figure 2.3 shows a LCGDN implemented by interconnecting ring oscillators [17]. In this network, the clock signal is generated at different points of the integrated circuit by a set ring of oscillators which are implemented by three gain stages in a closed loop (Fig. 2.3(a)); then, the generated signal is distributed to all points where it is required using a grid distribution network.

The local clock network shown in Fig. 2.3 generates and distributes clock signals with high-swing output voltage and operating frequency given by:

$$f = \frac{1}{2Nt_d} \tag{2.3}$$

where N and t_d are the number of gain stages and the corresponding delay, respectively. As can be observed in Fig. 2.3, the outputs of the ring oscillators are interconnected by the grid network, which produces a phase locked of the generated signals.

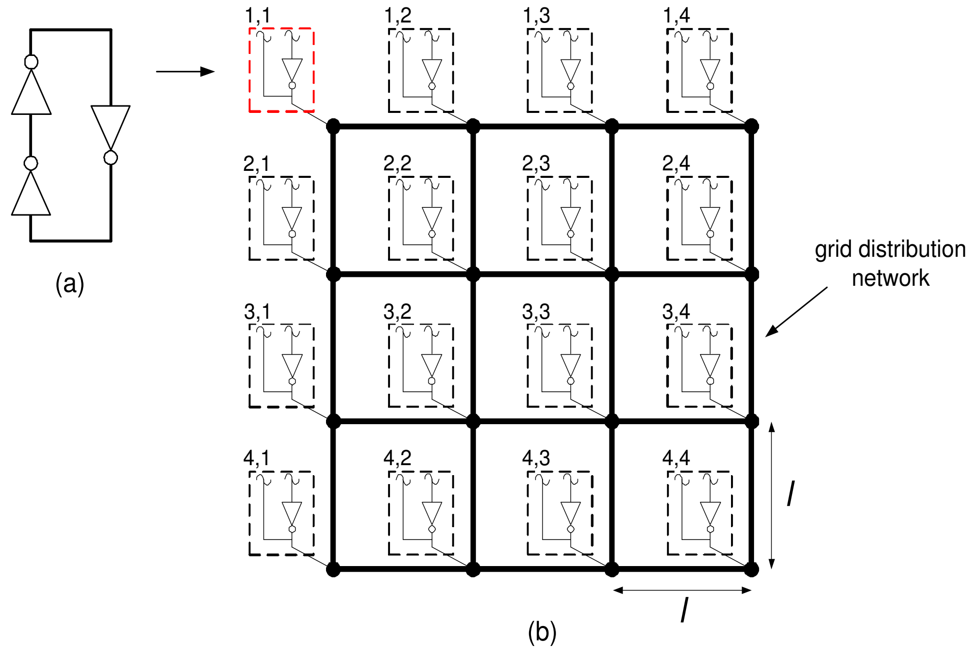


Figure 2.3: (a) Three-stage ring oscillator. (b) Local clock generation and distribution network implemented by interconnecting ring oscillators [17].

A LCGDN can be implemented by interconnecting and coupling ring oscillators as shown in Fig. 2.4 [18]. The local network simultaneously generates and distributes clock signals at different places of the integrated system by repeating the basic generation and distribution block which is an expanded ring oscillator implemented by three gain stages interconnected using interconnections with lengths in the order of millimeters (Fig. 2.4(a)). Notice that in this network the coupling among oscillators

is carried out through the gain stages and interconnection lines; due to this type of coupling, the effect of the phase averaging process is higher at each coupling point.

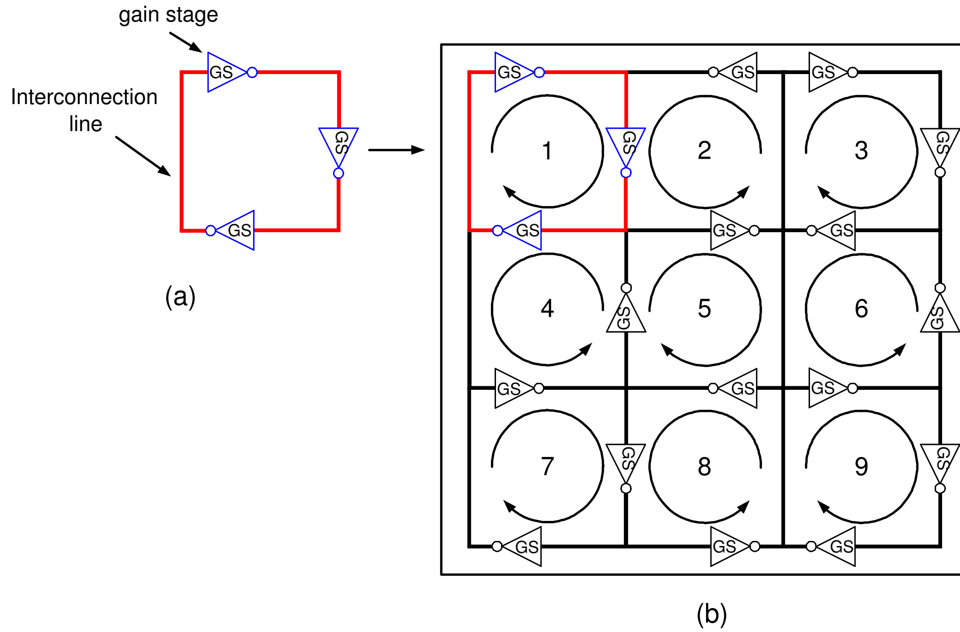


Figure 2.4: (a) Expanded three-stage ring oscillator. (b) Local clock generation and distribution network implemented by interconnecting and coupling ring oscillators [18].

The LCGDN implemented by interconnecting and coupling expanded ring oscillators simultaneously generates and distributes clock signals with high-swing output voltage and operating frequency given by:

$$f = \frac{1}{2Nt_d + 2Nt_l} \tag{2.4}$$

where t_l represents the delay associated with the interconnection lines.

2.2.2 LCGDN using Traveling Wave Oscillators

Traveling wave oscillator theory states that a voltage wave can indefinitely travel through a closed loop interconnection providing a full cycle signal around the ring, as can be seen in Fig. 2.5(a).

Figure 2.5(b) shows a LCGDN implemented by interconnecting and coupling rotary traveling wave oscillators (RTWO) [5]. The RTWO is a ring implemented by an interconnection line (exhibiting LC characteristics) with a cross connection of the inner and outer ports to cause a signal inversion. Thus, in the ideal case (i.e. if there were no losses in the interconnection), a voltage wave travels on the ring providing a full clock cycle every rotation of the signal through the ring. However, in actual implementations, it is necessary to connect a set of antiparallel gain stages around the ring to overcome the losses associated with the interconnections (Fig. 2.5(b)).

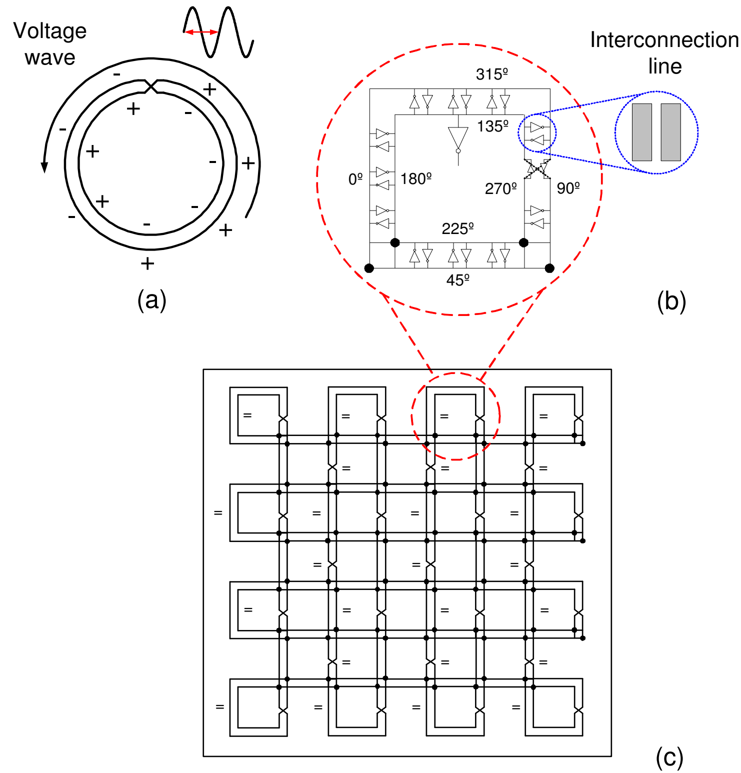


Figure 2.5: (a) Traveling wave concept. (b) RTWO. (c) Local clock generation and distribution network implemented by interconnecting and coupling RTWOs [5].

In [19], the authors propose a local clock network implemented by interconnecting and coupling reflection and regeneration traveling wave oscillators (R^2TWOs) as shown in Fig. 2.6. The R^2TWO is a ring implemented by an interconnection line and a gain stage with matched impedance (Fig. 2.6(a)). In this type of oscillators, a

voltage wave is reflected and regenerated at the input and output of the gain stage producing a full clock cycle.

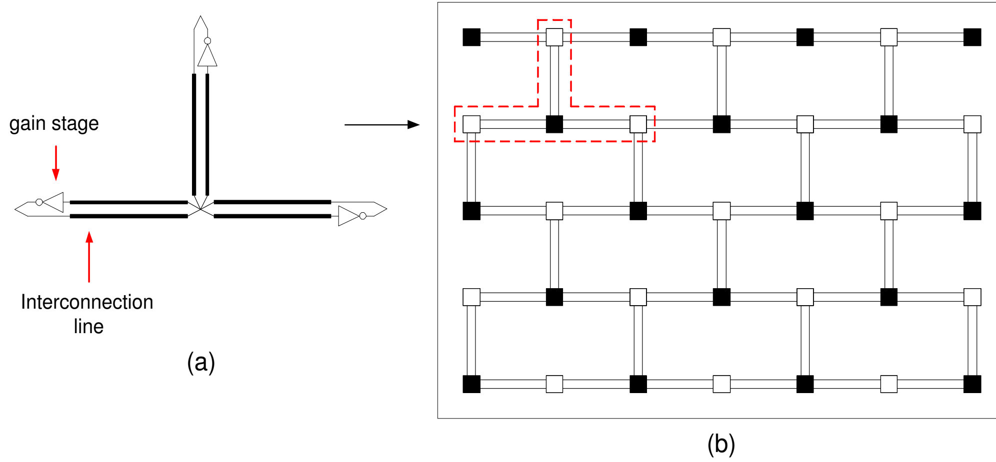


Figure 2.6: (a) R^2TWOs. (b) Local clock generation and distribution network implemented by interconnecting and coupling R^2TWOs [19].

A local clock network implemented by interconnecting and coupling traveling wave oscillators, simultaneously generates and distributes clock signals with high-swing output voltage and operating frequency, given by [5], [19]:

$$f = \frac{1}{2l\sqrt{LC}} \tag{2.5}$$

where l and L are the length and inductance of the interconnection line, respectively; and C represents the capacitance associated with the interconnection and gain stages.

In a LCGDN using traveling wave oscillators, the coupling among oscillators is carried out through interconnections that force phase lock of the generated signals. Also, due to the structure of the traveling wave oscillators, the phase of the clock signal depends on the position where the signal is obtained in the ring.

2.2.3 LCGDN using Standing Wave Oscillators

Standing wave theory states that when two identical waves which are propagating in opposite directions interact, a standing wave is generated. The simple way to generate a voltage standing wave is to send an incident wave through an interconnection and reflect it using a short circuit termination (Fig. 2.7(a)). In the ideal case, and upon any noise event, a voltage standing wave is generated; nonetheless, the losses associated with practical on-chip interconnects cause amplitude mismatch between the incident and reflected waves resulting in a residual traveling wave. Therefore, in order to overcome the interconnect losses a set of compensation stages is needed. The main characteristic of a standing wave is that the phase of the generated signal is independent of the position where the signal is obtained [6].

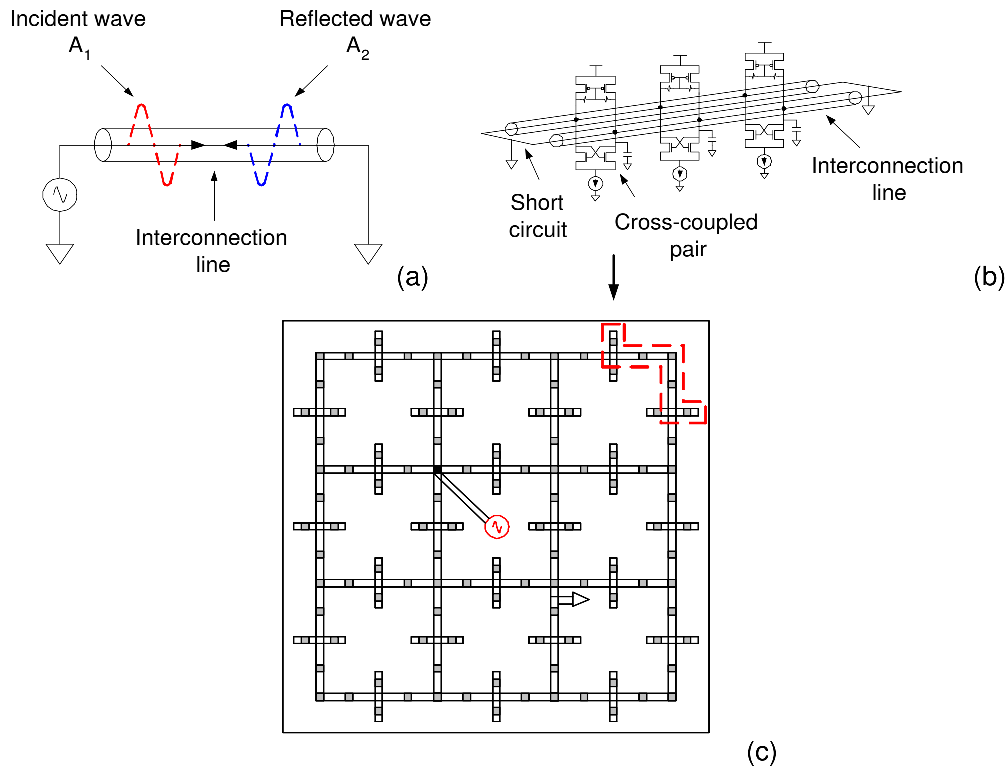


Figure 2.7: (a) Standing wave concept. (b) SWO. (c) Local clock generation and distribution network implemented by interconnecting and coupling SWOs [6].

Figure 2.7 shows a LCGDN implemented by interconnecting and coupling standing wave oscillators (SWOs) [6]. The SWO is implemented by two interconnections short-circuited at both ends, and a set of compensation stages are used to reduce the interconnect losses (Fig. 2.7(b)). The local clock network shown in Fig. 2.7 simultaneously generates and distributes clock signals with low-swing output voltage and operating frequency given by equation (2.5).

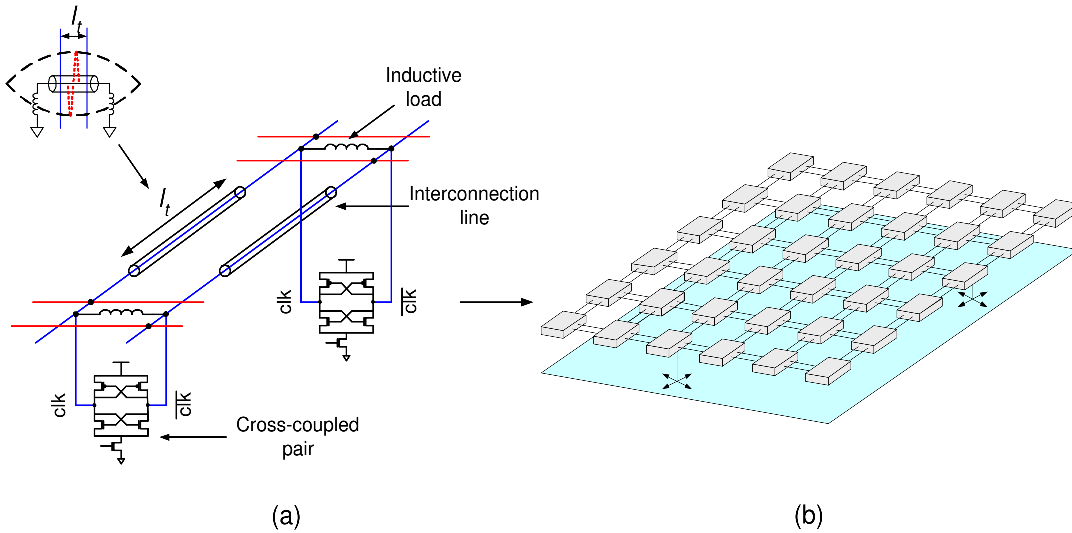


Figure 2.8: (a) ILSWO. (b) Local clock generation and distribution network implemented by interconnecting and coupling ILSWOs [20].

In order to generate and distribute clock signals with high-swing output voltage, a modified standing wave oscillator is proposed in [20]. Figure 2.8 shows a LCGDN implemented by interconnecting and coupling inductive load standing wave oscillators (ILSWOs). The ILSWO is implemented by two interconnections with two inductive loads at both ends that are included to eliminate low-amplitude from a conventional standing wave oscillator; notice that two compensation stages are used to reduce the impact of the interconnection losses (Fig. 2.8(a)). The LCGDN simultaneously generates and distributes clock signals with high-swing output voltage and operating frequency given by [20]:

$$f = \frac{Z_C}{2\pi L_{ind}} tan \frac{\pi - l\sqrt{LC}}{2} \quad (2.6)$$

where Z_C and L_{ind} are the characteristic impedance of the interconnect and the value of the inductive load, respectively.

In a LCGDN using standing wave oscillators, the coupling among oscillators is carried out through interconnections that reduce the phase difference among the generated signals.

In the design of local clock networks it is important to note the following:

- The interconnection lines play an essential role in the design of oscillators used in the implementation of LCGDNs.
- The operating frequency of local clock networks is determined by the operating frequency of the oscillator used in its implementation.
- The total power consumption and coverage area of local networks are proportional to the number of oscillators used in the implementation.
- The type and number of gain stages required by an oscillator is determined by the losses associated with the interconnection lines.
- The interconnection and coupling of oscillators reduce the phase difference among the generated signals.

2.3 The Key Role of the Interconnections in the CGDNs

As previously shown, in the design of global and local clock networks, the interconnection lines in combination with the gain stages are used to simultaneously generate and distribute high frequency clock signals throughout the integrated circuit. Therefore, in the design of this type of networks, the electrical equivalent circuit

model provides important information about the characteristics of the interconnections used in the implementation; then, based on this information, an accurate design of the gain, compensation, and output stages can be carried out.

For the case of the local clock networks, it was shown that the performance of this type of networks strongly depends on the characteristics of the oscillator used in the implementation; thus, in the design of this type of networks, the main performance metrics (e.g. operating frequency, output voltage, power consumption, coverage area, etc.) are determined by the basic oscillator. Also, it was shown that once that the basic oscillator has been designed, the implementation of simple and complex local clock networks can be carried out in a practical and relatively simple way. Therefore, the establishment of a methodology that allows circuit designers to perform an accurate representation of the interconnection lines used in the design and implementation of global and local clock generation and distribution networks is very important.

2.4 Summary

- In a high-performance microprocessor, a large number of functions is carried out in a synchronous digital way; therefore, the incorporation of a clock network responsible for generating and distributing the synchronization signal is essential.

- In actual microprocessors, the clock signal is generated at a single point and distributed through the integrated circuit using a global clock generation and distribution network.

- The global clock networks are well understood and widely used to generate and distribute the synchronization signals in actual high-performance microprocessors. However, due to the continuous down scaling of the technology, increase of operating frequency and area of the integrated circuits, the use of these clock networks is reaching its limit.

- The local clock networks implemented by interconnecting and coupling oscillators represent one of the main alternatives to resolve the problems related with global clock networks.

- Performance metrics of global and local clock networks (e.g. operating frequency, power, output voltage, time uncertainty, etc.) strongly depend on the characteristics of the interconnections used in their implementation.

- In the design and implementation of global and local clock generation and distribution networks, the interconnection lines play an essential role in the generation and distribution of the clock signal; therefore, an accurate modeling of the interconnections used in this type of networks is very important.

- Due to the importance of the interconnections in the implementation of the clock networks, the design flow of this type of integrated systems must start with an accurate modeling of the interconnects. Then, an accurate design of the gain, compensation, and output stages can be carried out.

Chapter 3

Interconnect Parameter Extraction Procedure

In this chapter, the parameter extraction associated with typical on-chip interconnections used in the design and implementation of global and local clock networks is presented. Firstly, a description of on-chip interconnections is presented; then, the interconnect parameter extraction developed from S-parameter measurements of fabricated test structures is carried out.

3.1 On-Chip Interconnect Structure

In today's IC design, one of the most used structures is the microstrip line. In general, there are two ways to implement a microstrip line on a silicon IC substrate [21]. In the first one, a microstrip line lies on top of a SiO_2 layer that in turn lies on a silicon substrate, and backside metallization acts as the ground plane. In the second case, the microstrip line lies on top of one of the inter-metal dielectric SiO_2, and a metal grid underneath works as the ground or return path plane. This work is focused in the latter case, and the lines used for the corresponding analysis are fabricated in Austriamicrosystems 0.35 μm process.

Figure 3.1 shows a simplified microstrip line implemented in the Metal 4 level that lies on top of the inter-metal dielectric level-3 (IMD3), where w, t, and l are the width, thickness, and length of the interconnection, respectively; h and gnd are the thicknesses of the inter-metal dielectric and ground plane, respectively. The nomenclature "Metal $[x]$ over Metal $[y]$, $w = [z]$ μm" will refer to a microstrip line implemented in the Metal x level, using the Metal y level as a ground plane, and a conductor width of z micrometers, respectively. Table 3.1 shows the thickness for different metal and inter-metal dielectric levels available in Austriamicrosystems 0.35 μm process technology.

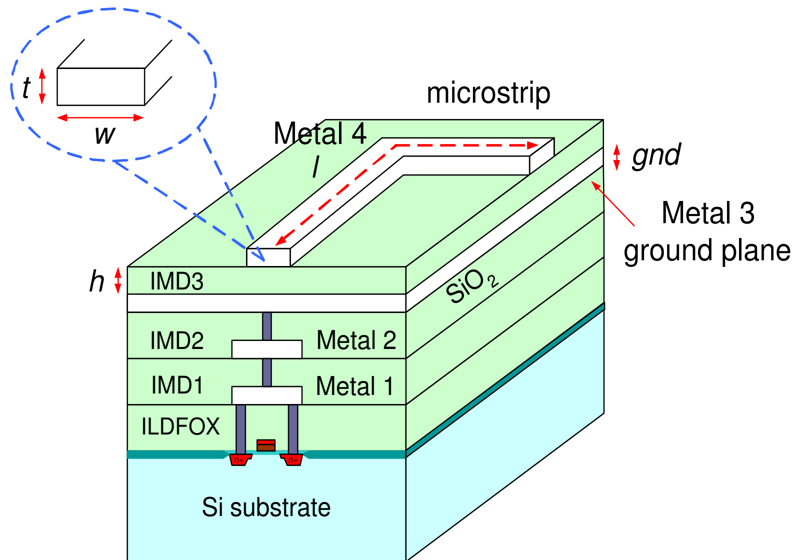


Figure 3.1: Simplified structure of a typical on-chip microstrip interconnection implemented in Austriamicrosystems 0.35 μm process.

In order to carry out an accurate modeling of the interconnects (i.e. analytical, electrical representation) typically used in the design and implementation of system on chip applications, a precise parameter extraction procedure is essential. In general, the parameter extraction of an interconnection line can be performed from: a) basic mathematical expressions and technology parameters, and b) S-parameter data.

Table 3.1: Austriamicrosystems 0.35 μm process parameters.

Parameter	Thickness (nm)	Parameter	Oxide Thickness (nm)
Metal 4	925	IMD4	1030
Metal 3	640	IMD3	1000
Metal 2	640	IMD2	1000
Metal 1	665	IMD1	1000

3.2 Parameter Extraction from Technology Parameters

Traditionally, the parameter extraction associated with the interconnection lines has been carried out from basic analytical expressions based on interconnect structure and process parameters provided by the foundry. In this parameter extraction, the values of R_l, L_l, and C_l of an interconnection line are obtained from [22], [23], [24]:

$$R_l = \frac{R_{sh}}{w} \tag{3.1}$$

$$L_l = \mu\frac{h}{w} \tag{3.2}$$

$$C_l = \epsilon\frac{w}{h} \tag{3.3}$$

where R_{sh} is the sheet resistance of the metal traces; while, μ and ϵ are the magnetic permeability and dielectric permittivity of the inter-metal dielectric, respectively. Table 3.2 shows the values of R_l, L_l, and C_l for a Metal 4 over Metal 3, w=2 μm interconnection line obtained from equations (3.1)-(3.3) and using Austriamicrosystems 0.35 μm process parameters. Notice the frequency independence of the interconnect parameters when they are obtained using this extraction procedure.

The parameter extraction procedure from technology parameters has been widely used by circuit designers; however, the precision of this parameter extraction procedure is limited, specially for interconnection lines operating within the GHz frequency range where the frequency dependence of the interconnect parameters and high-frequency effects can not be neglected. Therefore, it is clear that in the design of current and future high-speed integrated circuits, a precise parameter extraction procedure is necessary.

Table 3.2: Resistance, inductance, and capacitance per-unit-length for the microstrip line Metal 4 over Metal 3, w=2 μm obtained from technology parameters.

w (μm)	R_l (kΩ/m)	L_l (nH/m)	C_l (pF/m)
2	20	226	201

3.3 Parameter Extraction from S-Parameter Data

As it is well known, multi-port networks can be characterized by different equivalent circuit parameters such as impedance *(Z)*, admittance *(Y)*, transfer *(ABCD)*, scattering *(S)* parameters, among others. Figure 3.2 shows a typical two-port network.

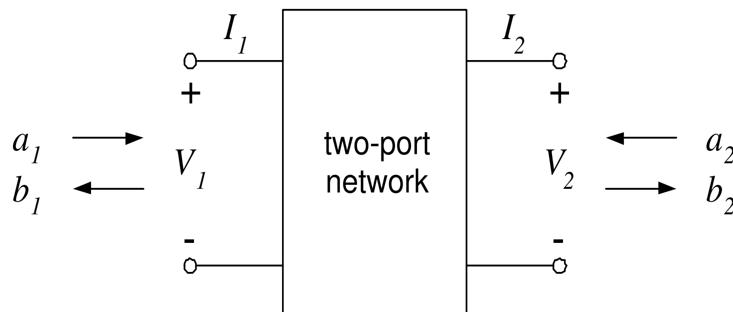


Figure 3.2: Typical two-port network.

The impedance matrix relates voltages V_1, V_2 to currents I_1, I_2:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} V_2 \\ V_1 \end{bmatrix} \tag{3.4}$$

where Z_{11}, Z_{12}, Z_{21}, and Z_{22} are obtained from:

$$\begin{aligned} Z_{11} &= \frac{V_1}{I_1}\Big|_{I_2=0} \quad Z_{12} = \frac{V_1}{I_2}\Big|_{I_1=0} \\ Z_{21} &= \frac{V_2}{I_1}\Big|_{I_2=0} \quad Z_{22} = \frac{V_2}{I_2}\Big|_{I_1=0} \end{aligned} \tag{3.5}$$

The admittance matrix is the inverse of the impedance matrix, $Y = Z^{-1}$.

The $ABCD$-matrix relates the voltage and current V_1, I_1 at port 1 to those at port 2, V_2, I_2:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \tag{3.6}$$

where A, B, C, and D are obtained from:

$$\begin{aligned} A &= \frac{V_1}{V_2}\Big|_{I_2=0} \quad B = \frac{V_1}{I_2}\Big|_{V_2=0} \\ C &= \frac{I_1}{V_2}\Big|_{I_2=0} \quad D = \frac{I_1}{I_2}\Big|_{V_2=0} \end{aligned} \tag{3.7}$$

Conventional small signal parameters Z, Y, and $ABCD$ parameters have been widely used in the characterization of multi-port networks. However, these parameters are not suitable for high-frequency network characterization because the “open” and “short” circuit terminations required to measure these data can not be achieved at high frequencies; short circuit terminations have magnetically induced inductance while open circuit terminations have capacitance due to electric field fringing at high frequencies. On the other hand, S-parameters do not use open and short terminations

to characterize the network; instead, these parameters are defined in terms of incident (a_1, a_2) and reflected (b_1, b_2) waves:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{3.8}$$

where S_{11}, S_{12}, S_{21}, and S_{22} are obtained from:

$$\begin{aligned} S_{11} &= \tfrac{b_1}{a_1}\Big|_{a_2=0} \quad S_{12} = \tfrac{b_1}{a_2}\Big|_{a_1=0} \\ S_{21} &= \tfrac{b_2}{a_1}\Big|_{a_2=0} \quad S_{22} = \tfrac{b_2}{a_2}\Big|_{a_1=0} \end{aligned} \tag{3.9}$$

where Z_0 is the reference impedance typically set to 50 Ω.

Thus, due to the properties and the way in which the S-parameters are defined, these parameters are the most commonly used in the correct characterization of multi-port networks at high frequencies. Therefore, in this thesis, a parameter extraction procedure developed directly from S-parameter measurements is used to carry out an exact determination of the interconnect parameters considering their frequency dependence and effects that become apparent at high frequencies.

3.3.1 De-Embedding Procedure

Figure 3.3 shows a test structure typically used to perform the S-parameter measurements of an interconnection line. As can be seen, ground-signal-ground pads are indispensable to access the device under test (DUT). Hence, a de-embedding procedure is required to eliminate the parasitic contribution introduced by the pad-to-line discontinuities. Fortunately, for practical purposes the values of the characteristic impedance Z_C and propagation constant γ (per-unit-length) do not vary from line to line as long as materials and cross section of the lines are the same, which allows to remove the parasitic contribution of the pad-to-line discontinuities from the measurement of two interconnection lines.

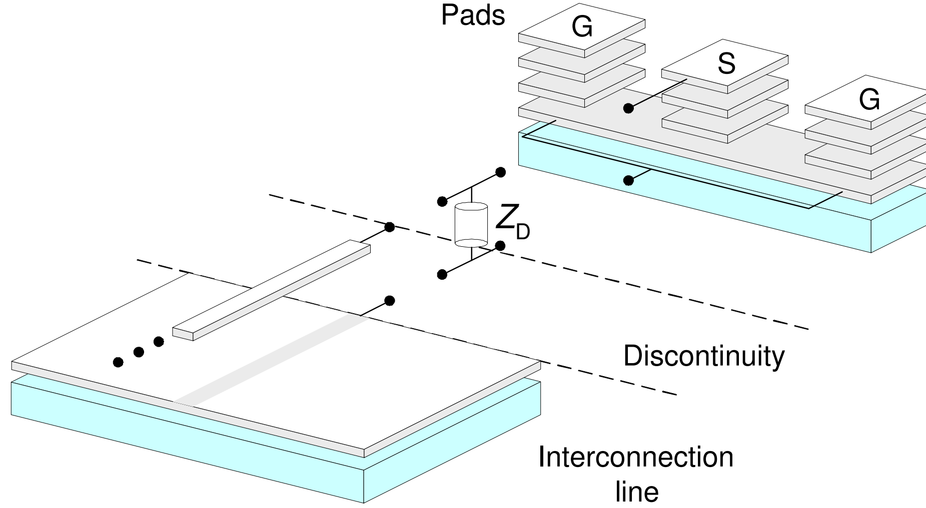


Figure 3.3: Interconnection line test structure [25].

First, consider two interconnection line test structures of length l_1 and l_2 ($l_1 < l_2$) as shown in Fig. 3.4. If the test structures are properly designed; then these structures are perfectly symmetric about the y axis, therefore:

$$S = Swap(S), \qquad Z = Swap(Z), \qquad Y = Swap(Y) \tag{3.10}$$

where $Swap(\ )$ swaps ports 1 and 2 of an S, Z, or Y matrices, this is:

$$Swap\left(\begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix}\right) \equiv \left(\begin{bmatrix} a_{22} & a_{21} \\ a_{12} & a_{11} \end{bmatrix}\right) \tag{3.11}$$

As can be observed in Fig. 3.3 an interconnection line test structure can be decomposed into a cascade of 3 two port networks consisting of the pads, interconnection line, and pad-to-line discontinuities (Z_D). Thus, the transmission matrix (i.e. $ABCD$-matrix) of the interconnection line test structure $M^t_{l_i}$, can be represented by [25]:

$$M^t_{l_i} \equiv M_{P1} M_{l_i} M_{P2} \tag{3.12}$$

where M_{l_i}, M_{P1}, and M_{P2} are the $ABCD$-matrices of the interconnection line, left pad, and right pad, respectively.

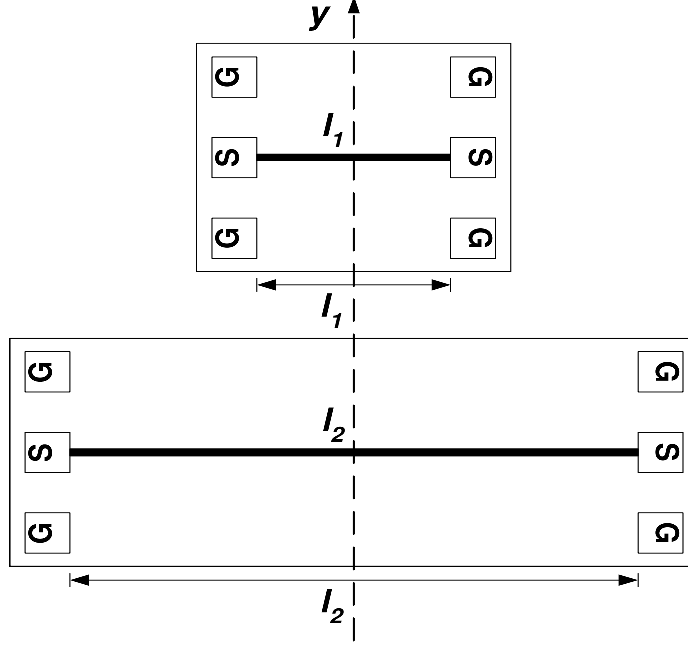


Figure 3.4: Two interconnection line test structures [25].

Now, to only determine the parameters of the interconnection line; first, the transmission matrix of an hybrid structure $M^h_{l_2-l_1}$ is determined from [25]:

$$M^h_{l_2-l_1} \equiv M^t_{l_2} \times [M^t_{l_1}]^{-1} \tag{3.13}$$

where $M^t_{l_2}$ is the transmission matrix of the interconnection line test structure of length l_2 and $[M^t_{l_1}]^{-1}$ is the inverse transmission matrix of the interconnection line test structure of length l_1.

Once that $M^h_{l_2-l_1}$ is determined, the Y-matrix of the interconnection line is obtained using [25]:

$$Y_{l_2-l_1} \equiv \frac{Y^h_{l_2-l_1} + Swap(Y^h_{l_2-l_1})}{2} \tag{3.14}$$

where $Y_{l_2-l_1}$ and $Y^h_{l_2-l_1}$ are the Y parameter representations of $M_{l_2-l_1}$ and $M^h_{l_2-l_1}$, respectively.

Assuming that a lossy transmission line of length $l_2 - l_1$ can be represented by [25]:

$$M_{l_2-l_1} \equiv \begin{bmatrix} A & B \\ C & D \end{bmatrix} \equiv \begin{bmatrix} cosh\ \gamma(l_2-l_1) & Z_C sinh\ \gamma(l_2-l_1) \\ \frac{1}{Z_C} sinh\ \gamma(l_2-l_1) & cosh\ \gamma(l_2-l_1) \end{bmatrix} \tag{3.15}$$

The characteristic impedance Z_C and propagation constant γ can be directly obtained from:

$$Z_C = \sqrt{\frac{B}{C}} \tag{3.16}$$

$$\gamma = \frac{cosh^{-1} A}{l_2 - l_1} \tag{3.17}$$

In the previously described de-embedding procedure, the corresponding Y and $ABCD$ matrices are directly obtained using a two-port network parameter conversion [23].

3.3.2 Interconnect Test Structures

Figure 3.5 shows the layout of the test structures used to perform the interconnect parameter extraction. As previously mentioned, the de-embedding procedure used in this thesis requires two test structures with the same characteristics but different lengths (short and long test structures); however, in the implementation of these structures it is important to take into account the following aspects: 1) The implementation of very short test structures (e.g. l_1=10 μm) is not suitable for a proper de-embedding procedure; the main problem related with short structures is the inadequate establishment of the wave propagation modes during the measurement process, which is reflected in an inaccurate obtention of the corresponding S-parameters. 2). If the length of the long structure is very similar to the length of the short structure (e.g. l_1=400 μm and l_2=410 μm), the resulting hybrid structure $M^h_{l_2-l_1}$ can provide inaccurate information of the characteristics of the studied interconnection line; therefore, as a design rule, the length of the long structure must be at least twice the length of the short structure. 3) In order to meet the metal density

rules in current and future technologies, the metal ground planes must be slotted; nevertheless, if these slots are much shorter than the wavelength, they will not affect the line characteristics significantly [25].

The test structures shown in Fig. 3.5 consist of a microstrip interconnection line implemented as described in Fig. 3.1 with a width w=2 μm, and lengths l_1=400 μm and l_2=1000 μm. The ground plane is constructed with horizontal and vertical crossed lines forming small slots (6 x 12 μm) in the Metal y level. Notice that these slots are smaller than the wavelength λ within the analyzed frequency range (0.01 to 35 GHz); thus, this grid is sufficiently small to be considered as a solid metal plane for the studied wavelength (λ=8.5 mm) [25]. Access to the microstrip lines is provided by 95 x 95 μm^2 signal pads constructed in the Metal 4 level. Additionally, 95 x 95 μm^2 grounded pads are used to contact the ground plane by using ground-signal-ground (GSG) device probes of 150 μm pitch. Table 3.3 and Figure 3.6 show the characteristics and a photograph of some of the fabricated interconnection line test structures.

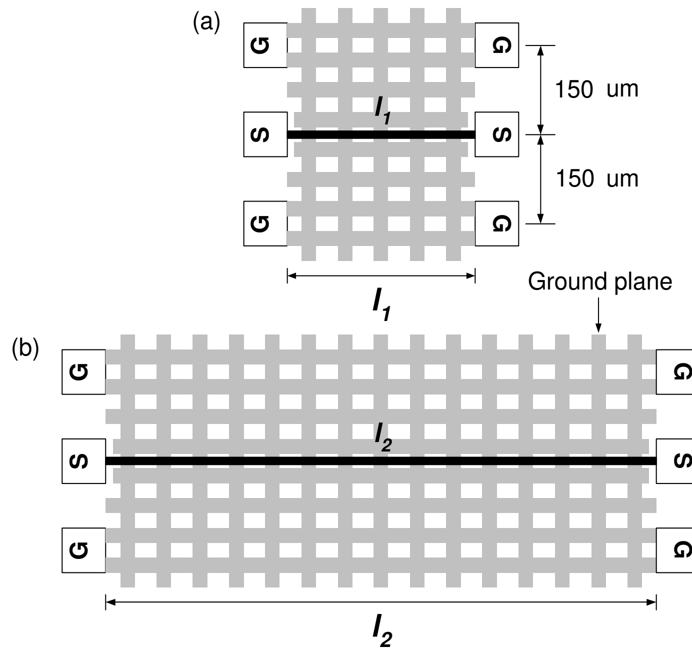


Figure 3.5: Microstrip interconnection line structures: (a) Short line l=400 μm. (b) Long line l=1000 μm.

Table 3.3: Characteristics of fabricated interconnection line test structures.

Item	Test structure
(a)	Metal 4 over Metal 1, w=2 μm, l=400 μm
(b)	Metal 4 over Metal 1, w=4 μm, l=400 μm
(c)	Metal 4 over Metal 3, w=2 μm, l=400 μm
(d)	Metal 4 over Metal 3, w=4 μm, l=400 μm
(e)	Metal 4 over Metal 1, w=2 μm, l=1000 μm
(f)	Metal 4 over Metal 1, w=4 μm, l=1000 μm
(g)	Metal 4 over Metal 3, w=2 μm, l=1000 μm
(h)	Metal 4 over Metal 3, w=4 μm, l=1000 μm
(x)	Other test structures

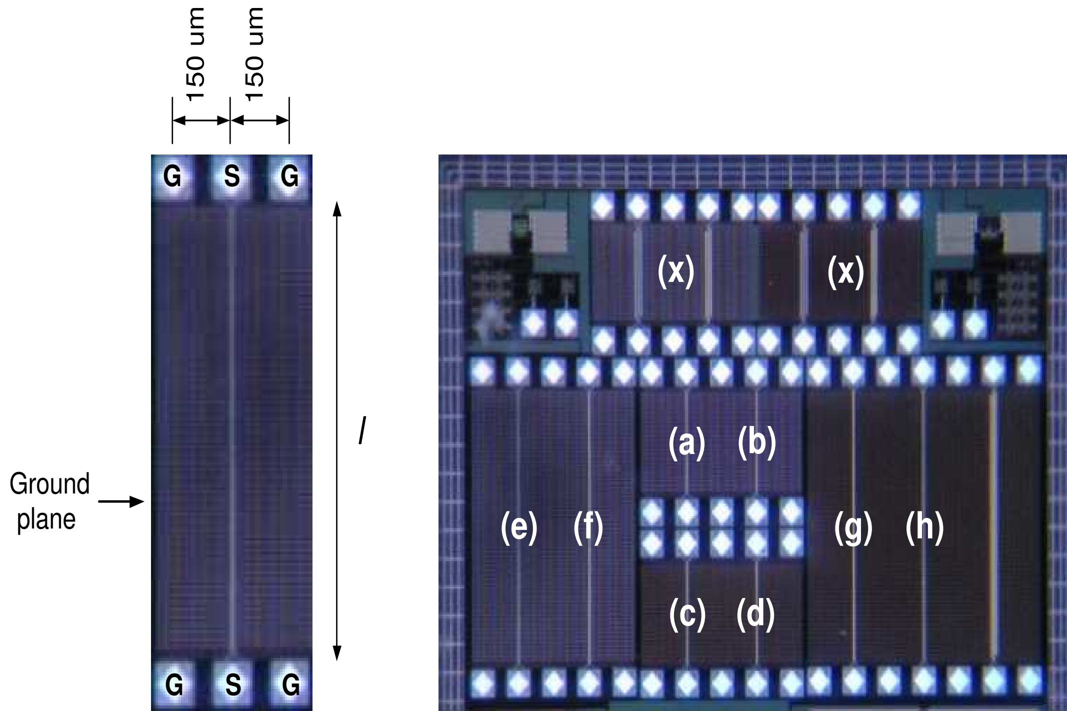


Figure 3.6: Photograph of fabricated interconnection line test structures.

As it is well known, the values of the characteristic impedance and propagation constant associated with an interconnection line implemented in a given fabrication technology strongly depend on the width and thickness of the metal, inter-metal dielectric, and ground plane levels. Likewise, as previously shown, the de-embedding procedure for obtaining Z_C and γ from the S-parameters requires measurements of two identical lines varying only the length. Then, the geometry and materials have to be the same for the method to work. So, in case that either the width and thickness of the metal, inter-metal dielectric, or ground plane levels change, Z_C and γ also change and different set of test structures and measurements have to be performed to carry out the corresponding parameter extraction.

3.3.3 Measurements and Parameter Extraction

In order to perform the extraction of R_l, L_l, and C_l parameters of the interconnection lines described in the previous section, the corresponding S-parameters were measured from 0.01 to 35 GHz using an HP8510C vector network analyzer (VNA) with semi-rigid cables and corresponding GSG coplanar probes described above (device probes). The VNA system was previously calibrated up to the probe tips by using an impedance-standard-substrate (ISS) provided by the probe manufacturer and the line-reflect-match (LRM) procedure. A more complete description of the test setup used to perform the S-parameter measurements is presented in the Appendix A of this thesis.

Once that the S-parameters have been obtained, the values of Z_C and γ of the fabricated lines are determined applying the de-embedding procedure described in Section 3.3.1 to two lines with the same characteristics but different lengths (e.g. 400 and 1000 μm). Figures 3.7 and 3.8 show the extracted Z_C and γ for the fabricated interconnection lines (Metal 4 over Metal 3, w=2 μm), respectively; notice the smooth and physically expected resulting curves when plotting the obtained data versus frequency which is indicative of an adequate de-embedding procedure.

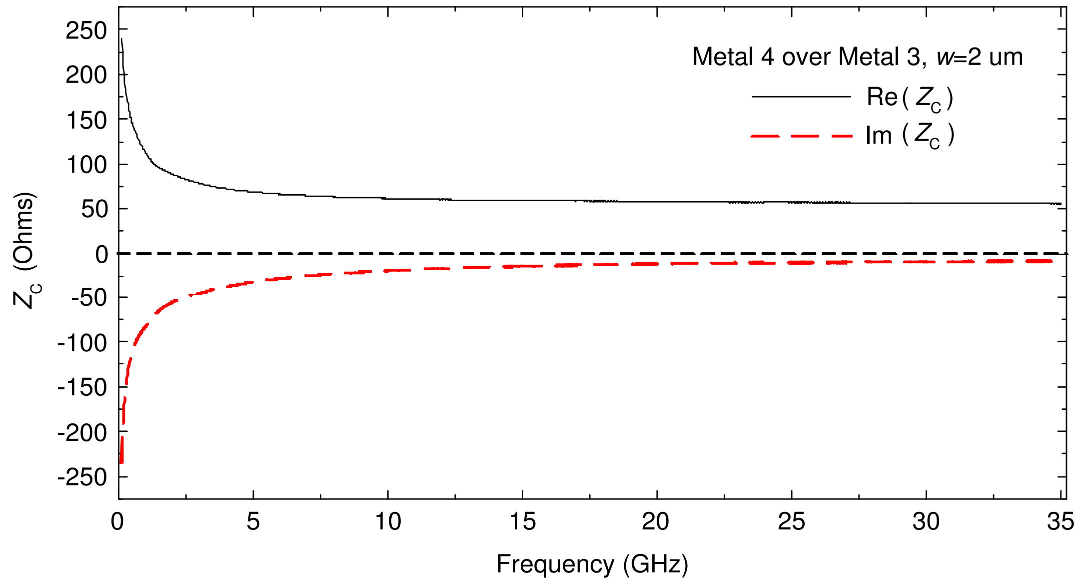


Figure 3.7: Experimental characteristic impedance for the fabricated microstrip line Metal 4 over Metal 3, w=2 μm.

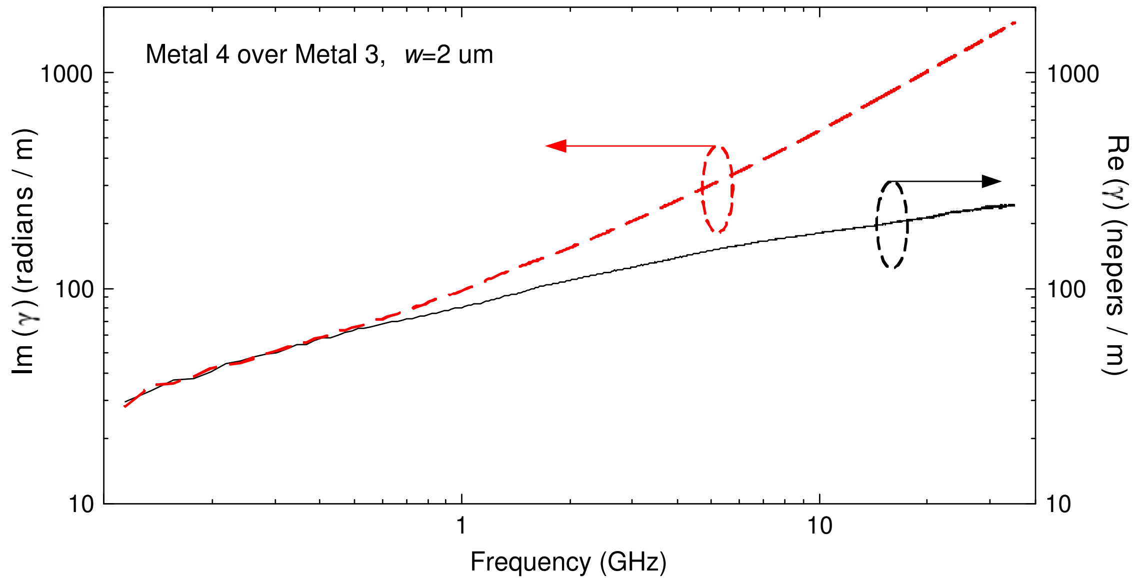


Figure 3.8: Experimental propagation constant for the fabricated microstrip line Metal 4 over Metal 3, w=2 μm.

After determining Z_C and γ, the values for R_l, L_l, C_l parameters associated with the interconnection line can be directly obtained from [12], [13]:

$$R_l = Re(\gamma Z_C) \tag{3.18}$$

$$L_l = \frac{Im(\gamma Z_C)}{2\pi f} \tag{3.19}$$

$$C_l = \frac{Im(\gamma / Z_C)}{2\pi f} \tag{3.20}$$

where:

$$\gamma Z_C = R_l + j2\pi f L_l \tag{3.21}$$

$$\frac{\gamma}{Z_C} = G_l + j2\pi f C_l \tag{3.22}$$

Figure 3.9 shows the obtained values for R_l, L_l, and C_l for the fabricated interconnection line (Metal 4 over Metal 3, w=2 μm) up to 35 GHz, whereas the impact of the G_l was neglected due to the very low value of this parameter within the analyzed frequency range. From this figure it is possible to observe the frequency dependence of the R_l, L_l, and C_l parameters obtained from S-parameter measurements. Since resistance is mainly related to metal losses, this parameter exhibits an increase with frequency owing to the skin effect [12], [26]. The inductance parameter is also related with the metal line and ground plane structure; and the corresponding curve drops with frequency to preserve causality (i.e. the energy stored by the equivalent inductance of the structure decreases when the energy associated with the resistive effect increases). For the case of the capacitance, the corresponding curve is approximately constant since the permittivity of the dielectric only suffers a relatively small change within the analyzed frequency range. As a comparison, in this figure the values for R_l, L_l, and C_l of the studied interconnection obtained from technology parameters are included. Notice the frequency independence of the interconnect parameters obtained

from technology parameters as well as the large discrepancy when they are compared to the interconnect parameters obtained from experimental data.

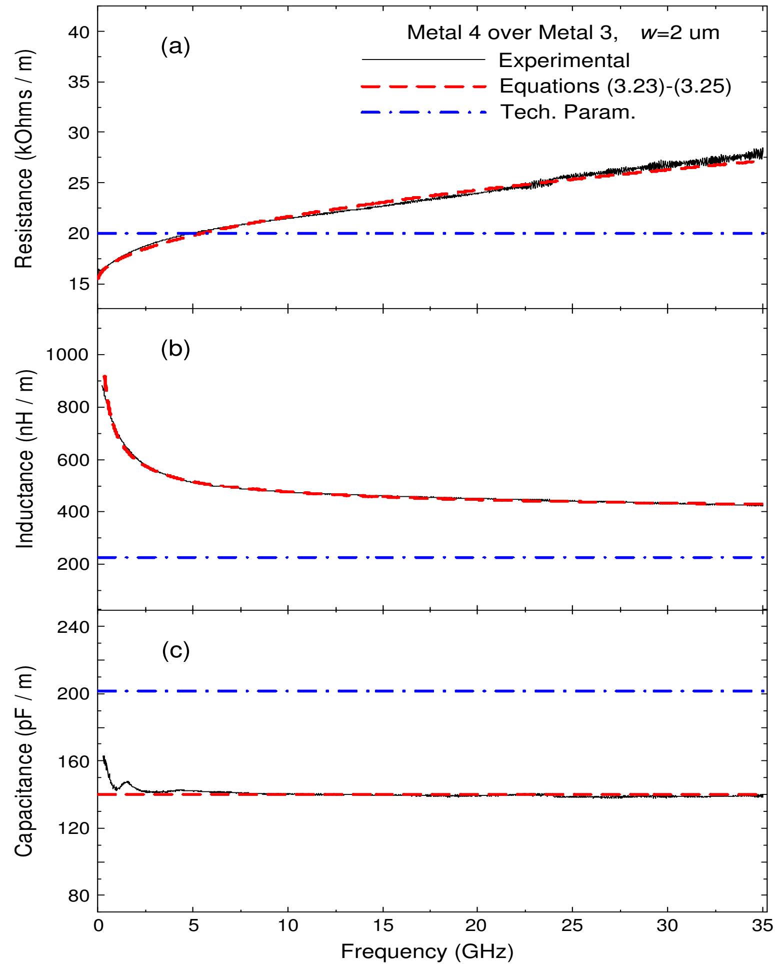


Figure 3.9: (a) Resistance, (b) Inductance, and (c) Capacitance per-unit-length for the fabricated microstrip line Metal 4 over Metal 3, w=2 μm.

As it is well known, the values of R_l, L_l, and C_l strongly depend on the geometric structure of the interconnection, properties of the conductor and dielectric materials, and process variation; however, it is important to mention that all these variables are taken into account when the interconnect parameter extraction is carried out directly from S-parameter measurements.

Now, in order to incorporate the values of the interconnect parameters into simulation environments (e.g. eldo, hspice, spectre, etc.) commonly used in the design of integrated systems, the values for R_l, L_l, and C_l are calculated using:

$$R_l = R_0 + \sqrt{f} R_{sk} \tag{3.23}$$

$$L_l = L_\infty + \frac{R_{sk}}{2\pi\sqrt{f}} \tag{3.24}$$

$$C_l \approx C_0 \tag{3.25}$$

where R_0 and R_{sk} are the per-unit-length dc resistance and skin effect resistance, respectively; while, L_∞ is the per-unit-length inductance at high frequencies [27]. For the case of C_l, the dependence of this parameter with frequency and conductivity is typically quite weak; therefore, the values for C_l can be approximated by the per-unit-length dc capacitance C_0 assuming perfect conductors [28].

Finally, once the values of R_l, L_l, and C_l have been determined, the values of total resistance (R_T), total inductance (L_T), and total capacitance (C_T) for an interconnection line of a certain length l_i are determined from:

$$R_T = R_l l \tag{3.26}$$

$$L_T = L_l l \tag{3.27}$$

$$C_T = C_l l \tag{3.28}$$

The previously described parameter extraction procedure is applied to a set of fabricated interconnection lines and the corresponding curves are presented in Appendix B.

3.4 Summary

- An accurate parameter extraction procedure is essential to carry out a precise modeling of interconnections used in the design and implementation of integrated systems (e.g. design of high-performance clock generation and distribution networks).
- The parameter extraction procedure developed directly from S-parameter measurements allows to perform accurate determination of the interconnect parameters (R_l, L_l, G_l, and C_l) considering their frequency dependence and effects that become apparent at high frequencies.
- In order to carry out the interconnect parameter extraction procedure, the design and fabrication of two interconnection lines with the same characteristics but different lengths is required.
- A de-embedding procedure is necessary to eliminate the parasitic contribution introduced by the pad-to-line discontinuities in the measurement process.
- The values of R_l, L_l, and C_l of an interconnection line are determined from Z_C and γ which are directly related to the width and thickness of the metal, inter-metal dielectric, and ground plane layers; therefore, the parameter extraction procedure must be repeated for lines with different Z_C and γ.

Chapter 4

Interconnect Modeling

In this chapter, a procedure for the equivalent circuit model selection and the determination of the minimum number of sections required in the electrical equivalent circuit for accurate representation of on-chip interconnections used in the design and implementation of integrated systems is presented.

4.1 Development of the Methodology

Once that the electrical parameters of the interconnection lines have been obtained, the problem consists in determining the equivalent circuit model for a proper representation. In general, on-chip interconnections can be represented by means of:

- *RC lumped or distributed equivalent circuit* (Fig. 4.1(a)), which is applicable when the operating frequency is so low that the delay and losses of the interconnection line mainly depend on the resistance and capacitance of the line; however, the use of this equivalent circuit model is limited for correct representation of typical on-chip interconnects working at frequencies of GHz.

- *LC lumped or distributed equivalent circuit* (Fig. 4.1(b)), which is valid when the interconnection is considered as lossless (i.e. Re(γ)$\approx$0); nevertheless, this model

is very inaccurate to represent actual on-chip interconnects where the resistance associated with the metal lines has taken importance in their performance.

- *RLC lumped or distributed equivalent circuit* (Fig. 4.1(c)), which includes the resistive, inductive, and capacitive effects, is widely used to represent on-chip interconnects (assuming that dielectric conductivity is negligible) working at frequencies of GHz.

- *RLCG lumped or distributed equivalent circuit* (Fig. 4.1(d)), this is the most complete model used to represent on-chip interconnects working at very high frequencies where conductance can not be neglected.

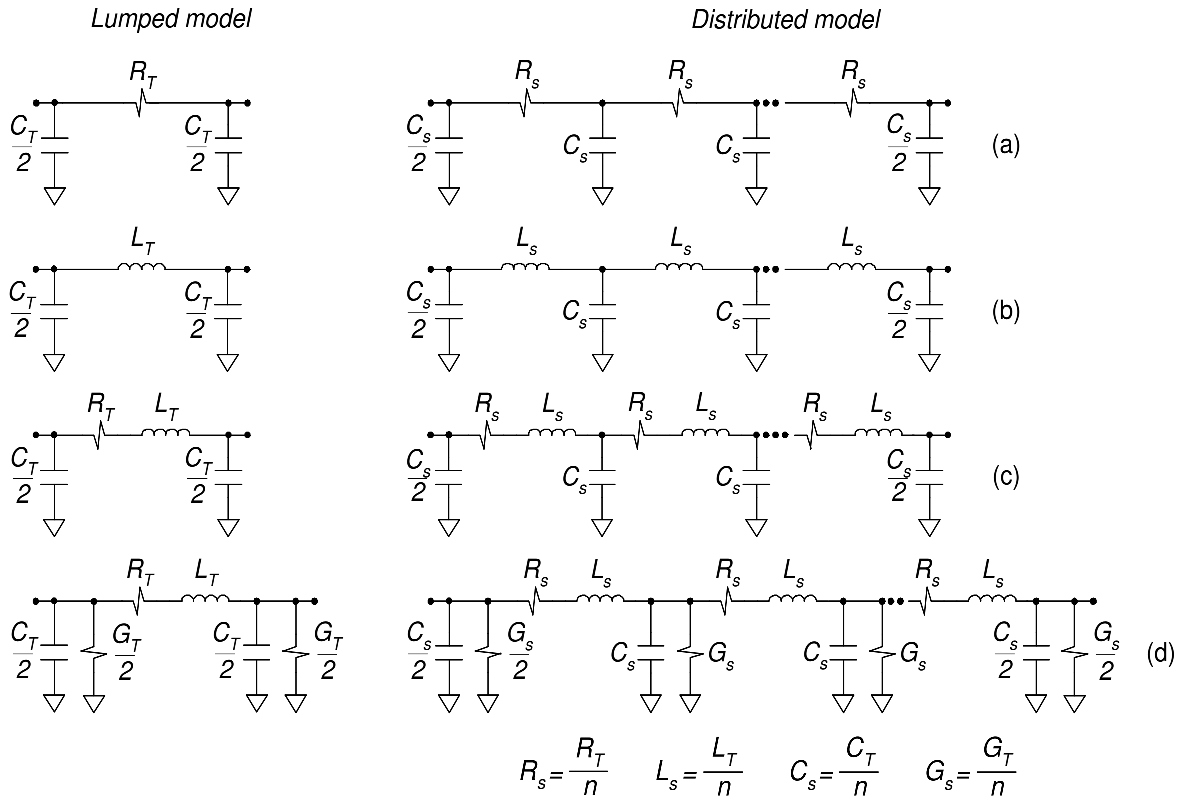


Figure 4.1: *Lumped* and *distributed* electrical equivalent circuit models: (a) *RC*. (b) *LC*. (c) *RLC*. (d) *RLCG*.

As explained later (Section 4.1.2), the selection between a *lumped* and a *distributed* model strongly depends on the line length and the operating frequency. For the case of the distributed model, the corresponding implementation is carried out by assuming that the interconnection line can be represented by means of an RC, LC, or RLC equivalent circuit model implemented with n stages connected in a cascade configuration, as can be observed in Fig. 4.1. Obviously, using a large value for n will allow to represent the interconnect up to higher frequencies than in the case of using a small value for n. Unfortunately, this also increases the computation time, which may be considerable, especially in the design of systems with a large number of interconnections with lengths in the order of millimeters. Therefore, the determination of the optimal model as well as the minimum value for n for precise representation of interconnection lines of certain lengths within specific frequency range is desirable. This determination is carried out by correlating experimentally determined data with equivalent circuit simulations corresponding to lines of different lengths.

In order to perform the simulation-experiment correlations, the S-parameter data associated with interconnections of certain lengths are obtained by applying Transmission Line Theory [23].

The $ABCD$-matrix corresponding to an uniform transmission line is given by:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} cosh(\gamma l_i) & Z_C sinh(\gamma l_i) \\ \frac{1}{Z_C} sinh(\gamma l_i) & cosh(\gamma l_i) \end{bmatrix} \tag{4.1}$$

where the subscript i is used to distinguish between the parameters of lines with different lengths. Thus, once that the experimental Z_C and γ have been determined, the $ABCD$-parameters of a line with arbitrary length l_i can be obtained by using (4.1) and the corresponding S-parameters are directly obtained using a two-port network parameter conversion [23]. In this work, these S-parameters are assumed to be the experimental data associated with an homogeneous section of line with a given length. Thus, the obtained equivalent circuit models are compared with these data to verify the corresponding accuracy.

To take into account the frequency dependence of the interconnect parameters in the equivalent circuit model simulations, the determination of the *ABCD*-matrix associated with the studied models is mandatory. For instance, consider the *RLC lumped* equivalent circuit model shown in Fig. 4.2 which has the structure of a typical two-port π-model (Fig. 4.2(b)).

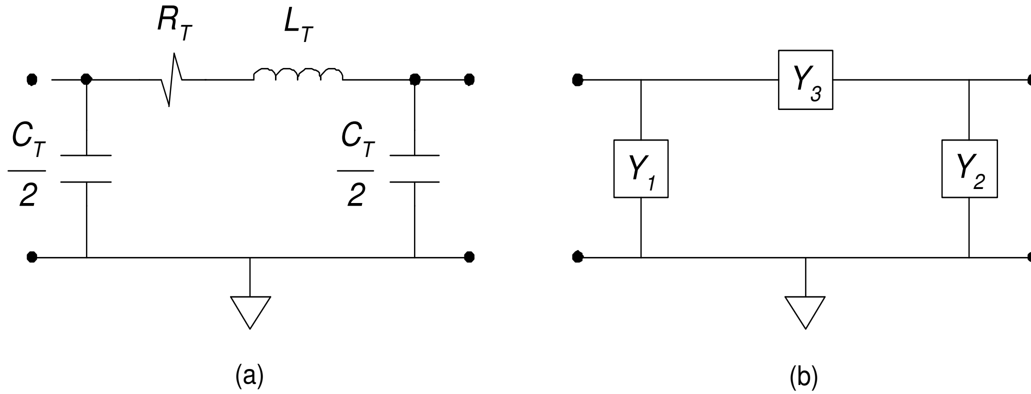


Figure 4.2: (a) *RLC lumped* equivalent circuit model. (b) Typical two-port π-model [23].

The *ABCD*-matrix associated with the *RLC lumped* equivalent circuit model is given by [23]:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1+\frac{Y_2}{Y_3} & \frac{1}{Y_3} \\ Y_1+Y_2+\frac{Y_1Y_2}{Y_3} & 1+\frac{Y1}{Y3} \end{bmatrix} \tag{4.2}$$

where Y_1, Y_2, and Y_3 are obtained from:

$$Y_1 = Y_2 = j\omega\frac{C_T}{2} \tag{4.3}$$

$$Y_2 = \frac{1}{R_T + j\omega L_T} \tag{4.4}$$

Once that the *ABCD*-parameters of the equivalent circuit model are determined; once again, the corresponding *S*-parameters are directly obtained using a two-port network parameter conversion. Now, these *S*-parameters are used to carry out the simulations of the studied equivalent circuit models. It is important to mention

that the $ABCD$-parameters for any type of equivalent circuit model can be obtained directly from the Y and Z parameters of the analyzed network.

4.1.1 Equivalent Circuit Model Selection

As previously stated, on-chip interconnects can be represented by means of RC, LC, RLC *lumped* or *distributed* equivalent circuits. Therefore, with the purpose of verifying the accuracy of the previously mentioned model approaches, several simulation-experiment comparisons are carried out. For the time being, it will be assumed that n=6 sections are sufficient to represent the *distributed* nature of an interconnection line with l=1000 μm within the measured frequency range. Thus, using this value, the validity of the RC and LC equivalent circuit models is verified.

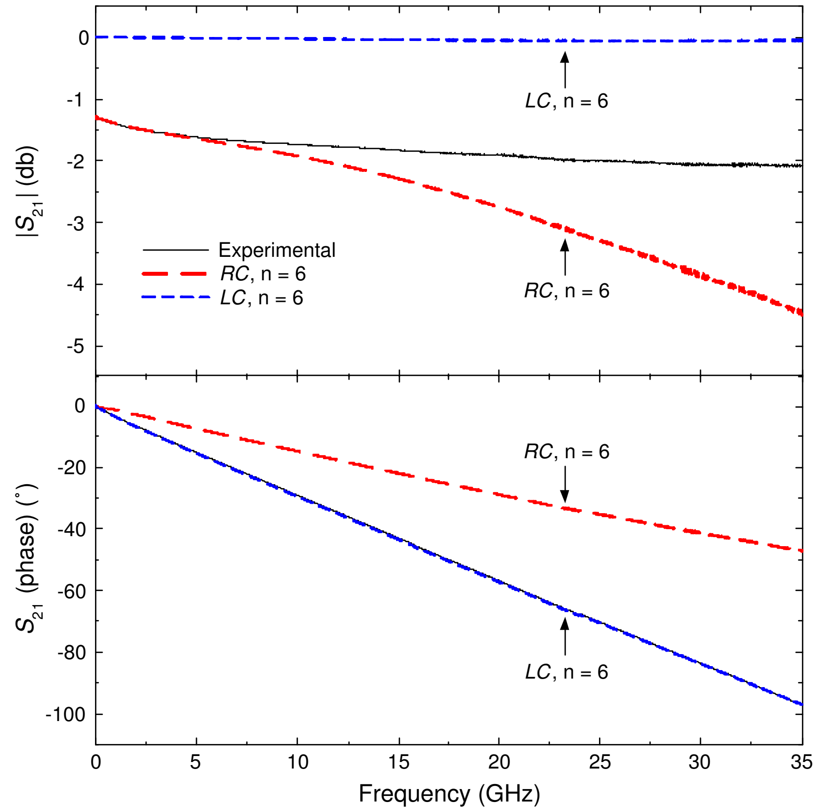


Figure 4.3: Experimental insertion losses compared with simulated data using RC and LC distributed equivalent circuit models for the line with l=1000 μm.

Figure 4.3 shows the experimental and simulated insertion losses (i.e. magnitude $|S_{21}|$ and phase $\angle S_{21}$, respectively) for a Metal 4 over Metal 3, w=2 μm interconnection with l=1000 μm up to 35 GHz. As can be seen, an *RC distributed* equivalent circuit model can be used to accurately represent the $|S_{21}|$ parameter of the interconnection only up to around 5 GHz; also, notice that an inaccurate representation of the $\angle S_{21}$ parameter is obtained using this equivalent circuit model. Now, for the case of the *LC distributed* equivalent circuit model, a considerable deviation of the $|S_{21}|$ parameter corresponding to the *LC* model from the experimentally determined data can be observed; nevertheless, observe that this model is adequate to properly represent the $\angle S_{21}$ parameter. Hence, based on these results it is evident that a combination of the *RC* and *LC* models (i.e. an *RLC* equivalent circuit model) is indispensable to accurately represent the on-chip interconnection lines under study.

4.1.2 Lumped and Distributed Equivalent Circuit Model Regions

Once it has been demonstrated that the *RC* and *LC* models are insufficient to adequately represent the delay and losses associated with the interconnection lines used in this work, the frequency ranges of validity for the *RLC lumped* and *RLC distributed* equivalent circuit models, as well as the criteria for the determination of the minimum number of sections (required in a *distributed* model), are presented.

Figure 4.4 shows the experimental and simulated insertion losses for a Metal 4 over Metal 3, w=2 μm interconnection line with length l=1000 μm. In this figure the corresponding simulated data are obtained using an *RLC lumped* and *RLC distributed* equivalent circuit model implemented with 2, 4, and 6 sections. Firstly, notice the large discrepancy between the experimental and simulated data obtained using an *RLC lumped* equivalent circuit; more precisely, when the interconnection is modeled by an *RLC lumped* equivalent circuit, the corresponding insertion losses are properly represented up to about 4 GHz. This frequency limit is determined when the difference between the experimental and simulated $|S_{21}|$ is ≥ 1 %, as shown in the

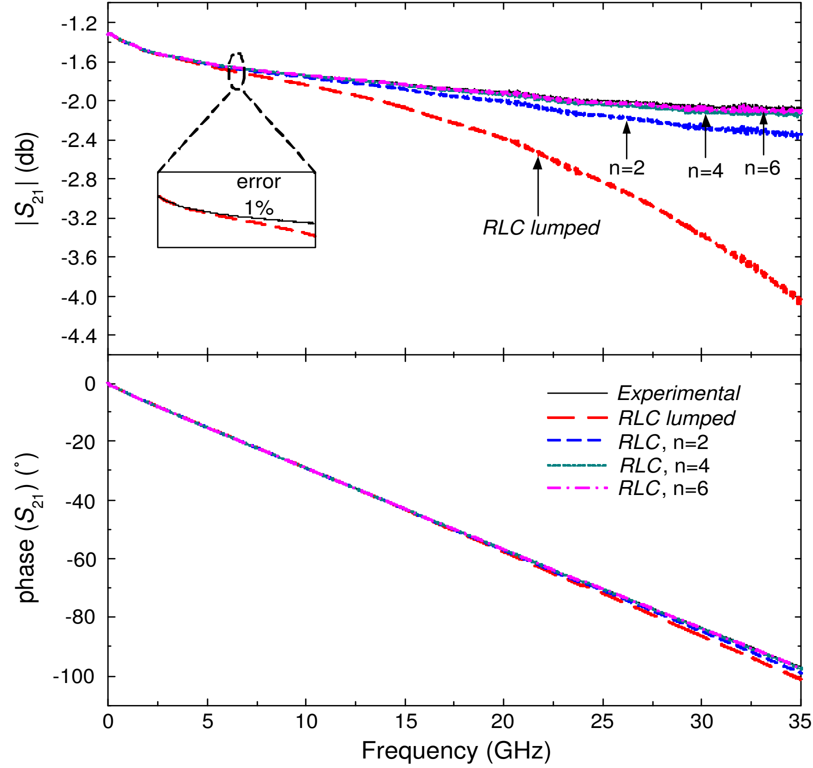


Figure 4.4: Experimental insertion loss compared with simulated data using *RLC lumped* and *RLC distributed* (2, 4, and 6 sections) equivalent circuit models for the line with l=1000 μm.

inset of Fig. 4.4. Now, when the interconnection is modeled by an *RLC distributed* equivalent circuit implemented with 2, 4, and 6 sections, the corresponding $|S_{21}|$ and $\angle S_{21}$ parameters are correctly represented up to 8, 17, and 30 GHz, respectively by using the previously mentioned criteria. Then, as previously shown, the $|S_{21}|$ and $\angle S_{21}$ parameters associated with an interconnection line of a certain length can be accurately represented at higher frequencies using an *RLC distributed* equivalent circuit model implemented with a greater number of sections.

Now, in order to establish the boundary between the *RLC lumped* and *RLC distributed* model regions, and to verify the accuracy of the *distributed* models using different number of sections, the previously described procedure is applied to a set of interconnections with l=100, 200, 400, 1500, 2000, 2500, and 3000 μm.

As expected, the corresponding $|S_{21}|$ and $\angle S_{21}$ parameters associated with long interconnections are larger than short and moderately long lines. Hence, in this case the circuit designer must decide if it is feasible to use a long interconnection line, or it is necessary to segment the line and use buffers [8]. In an homogeneous interconnection, the length (l) for which the line can be considered as short enough to be represented by means of a simple *lumped* equivalent circuit model is inversely proportional to the phase constant β. To write this relation as an equation, a proportionality constant (Δ) has to be included, which yields: $l = \Delta/\beta$. To express this equation in a more intuitive way, β is written in terms of the L_lC_l elements and frequency ($\beta = 2\pi f\sqrt{L_lC_l}$), which yields [29]:

$$l = \frac{\Delta}{2\pi f\sqrt{L_lC_l}} \tag{4.5}$$

where Δ is an arbitrary constant (dependent on the acceptable error for the S-parameters) typically set to 0.25.

Indeed, based on the results obtained by applying the simulation-experiment procedure described in this section to a set of interconnection lines with different lengths, it has been shown that the boundaries of the *RLC distributed* equivalent circuit model regions are proportional to the number of sections n and the value of Δ. This is logical since the larger n is, the longer the line that can be represented by an n-stage model at a given frequency; mathematically this is expressed as:

$$l = \frac{n\Delta}{2\pi f\sqrt{L_lC_l}} \tag{4.6}$$

Figure 4.5 shows the combination of l and f for which the Metal 4 over Metal 3, w=2 μm interconnections can be represented by an *RLC lumped* model and when it can be represented by an *RLC distributed* equivalent circuit model implemented with n=2, 4, 6, 8, 10, and 12 sections. In this figure, the experimental data are obtained using the simulation procedure and error criterion previously established, whereas the theoretical curves are obtained using equation (4.6). Notice that this equation allows predicting the maximum length of a line that can be accurately represented by an

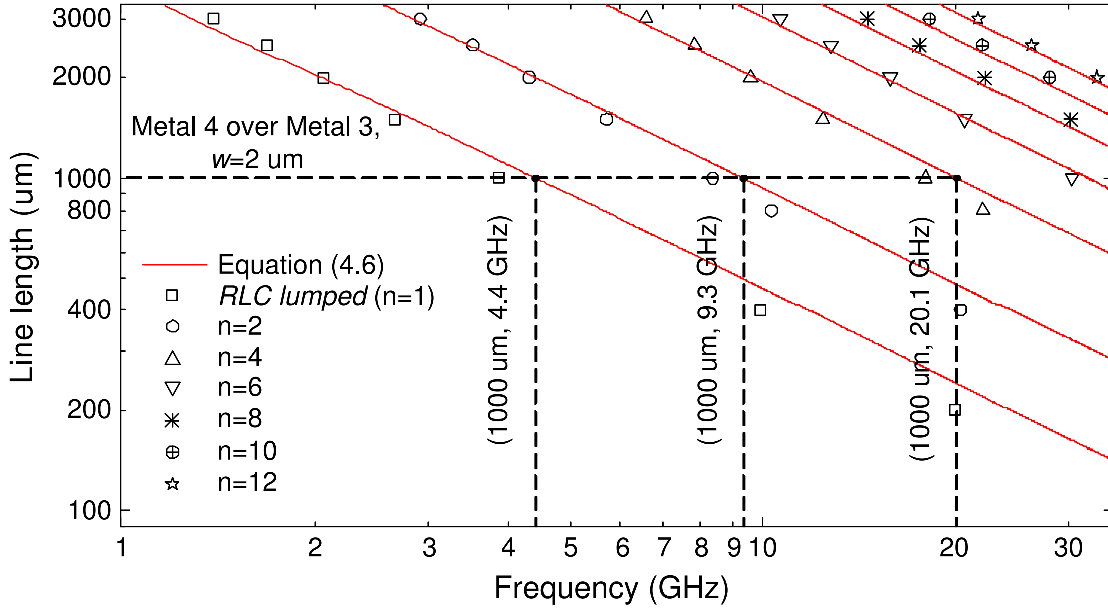


Figure 4.5: *RLC lumped* and *RLC distributed* equivalent circuit model regions using 2, 4, 6, 8, 10 and 12 sections for interconnection lines Metal 4 over Metal 3, w=2 μm.

RLC lumped equivalent circuit model (i.e. n=1) at a given frequency. Nonetheless, when n increases by sectionalizing the *RLC* model, this length also increases as it has been previously discussed. This fact is reflected in equation (4.6), predicting that by sectionalizing the model in n stages the length of the line that can be properly represented increases by a factor of n with respect to the corresponding *lumped* model at a given frequency.

As can be observed in Fig. 4.5, an *RLC lumped* equivalent circuit is sufficient to accurately represent the delay and losses of short interconnection lines (e.g. 100 and 200 μm) within the analyzed frequency range. Now, consider an interconnection line with l=1000 μm; this line can be correctly represented by an *RLC lumped* equivalent circuit only up to about 4.4 GHz, as can be seen in Fig. 4.5. If the same interconnection is modeled by an *RLC distributed* equivalent circuit implemented with 2 sections, the delay and losses of the line can be properly represented up to 9.3 GHz. When the same *RLC distributed* equivalent circuit is implemented with 4 sections, the interconnection line under study can be adequately represented up to 20.1 GHz. For the

case of an interconnection line with l=3000 μm; this line can be modeled by an RLC *lumped* equivalent up to about 1.4 GHz. Now, if the same interconnection is modeled by an RLC *distributed* equivalent circuit implemented with 2, 4, and 6 sections, the line can be correctly represented up to 2.8, 6.3, and 10.1 GHz, respectively; obviously, increasing the number of sections in the equivalent circuit model allow to represent this interconnection up to higher frequencies, as can be observed in Fig. 4.5.

In the design of integrated circuits, power and ground lines located in the lowest metal levels provide a virtual reference plane for the interconnection lines [25]. Therefore, to carry out the determination of the minimum number of sections required in the equivalent circuit model for precise representation of interconnection lines typically used in the design of integrated systems, the simulation-experiment procedure (previously described) is applied to an interconnection line implemented in the Metal 4 level using the Metal 1 as a ground plane (Metal 4 over Metal 1, w=2 μm) and the corresponding results are presented in Fig. 4.6.

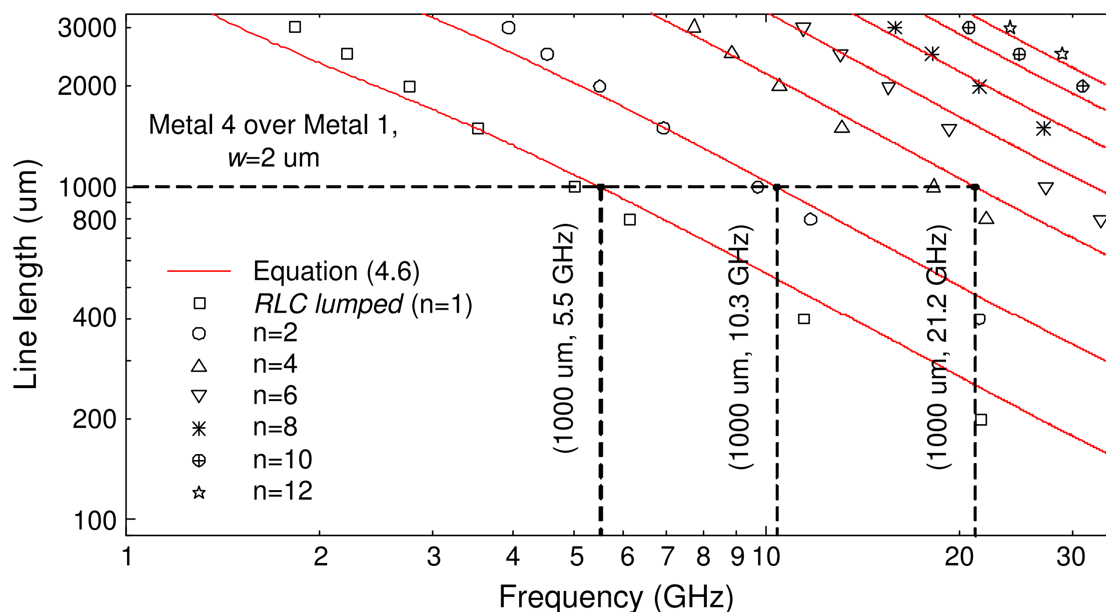


Figure 4.6: *RLC lumped* and *RLC distributed* equivalent circuit model regions using 2, 4, 6, 8, 10 and 12 sections for interconnection lines Metal 4 over Metal 1, w=2 μm.

As an example, consider an interconnection line with l=1000 μm; this line can be modeled by an *RLC lumped* equivalent circuit only up to about 5.5 GHz. Now, when the interconnection line under study is modeled by an *RLC distributed* equivalent circuit implemented with 2 sections, the line can be adequately represented up to 10.3 GHz. If the same *RLC distributed* equivalent circuit is implemented with 4 sections, the delay and losses associated with the interconnection line can be accurately represented up to 21.2 GHz.

Notice the good correlation between the experimental data and theoretical curves obtained using the proposed equation; hence, a plot of this type provides important information to analytically determine the minimum number of sections required in an equivalent circuit model for proper representation of interconnections given the maximum operating frequency. In consequence, the equivalent circuit model used to represent the interconnection lines in the simulations of complex systems can be simplified saving computation time.

The previously described modeling methodology is applied to a set of fabricated interconnections and the corresponding results are presented in Appendix B.

4.1.3 Technology Scaling

Now, the proposed modeling methodology is applied to an interconnection line designed using the 8 Metal TSMC (Taiwan Semiconductor Manufacturing Company) 0.13 μm process. Figure 4.7 shows the simplified structure of a microstrip line implemented in the Metal 8 level using the Metal 7 as a ground plane.

For this case of study, the S-parameters associated with the studied interconnection lines are obtained from 0.01 to 35 GHz using an electromagnetic simulator (Advanced Design System), where it is necessary to specify: a) the geometric structure of the interconnection line, inter-metal layer, and ground plane (i.e. width, thickness, length, height, etc.); and b) the properties of the materials used to fabricate the metal and inter-metal layers. Thus, once that the corresponding S-parameters have

been determined, the interconnect parameter extraction, the equivalent circuit model selection, and the determination of the minimum number of sections are carried out.

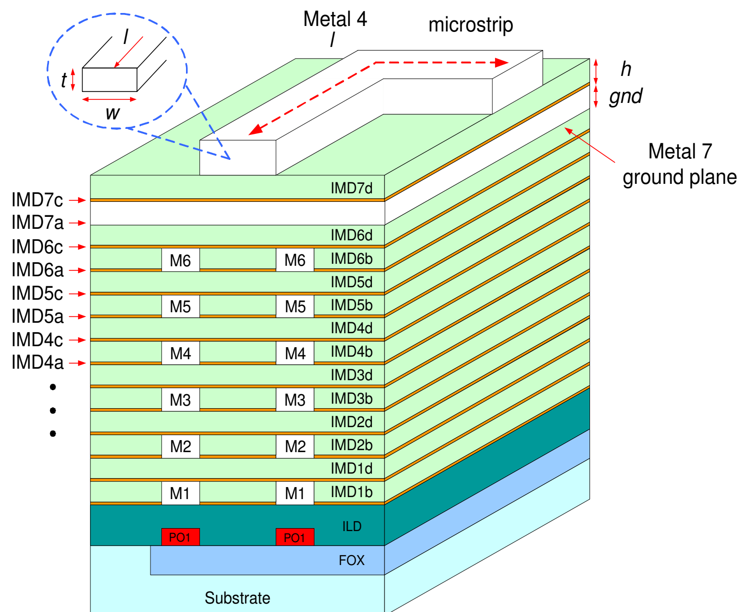


Figure 4.7: Simplified structure of a typical on-chip microstrip interconnection implemented in TSMC 0.13 μm process.

Figure 4.8 shows the combination of l and f for which the Metal 8 over Metal 7, w=4 μm interconnection can be represented by an *RLC lumped* model and when it can be represented by an *RLC distributed* equivalent circuit model implemented with n=2, 4, 6, 8, and 10 sections. As an example, consider an interconnection line with l=1000 μm; this line can be modeled by an *RLC lumped* equivalent circuit only up to about 4.8 GHz as can be seen in Fig. 4.8. Now, if the same interconnection is modeled by an *RLC distributed* equivalent circuit implemented with 2 sections, the delay and losses associated with the line can be properly represented up to 9.8 GHz. Finally, when the same *RLC distributed* equivalent circuit is implemented with 4 sections, the interconnection line under study can be adequately represented up to 20.1 GHz.

More details related to the modeling of the Metal 8 over Metal 7, w=4 μm interconnection line implemented using the TSMC 0.13 μm process are presented in Appendix B.

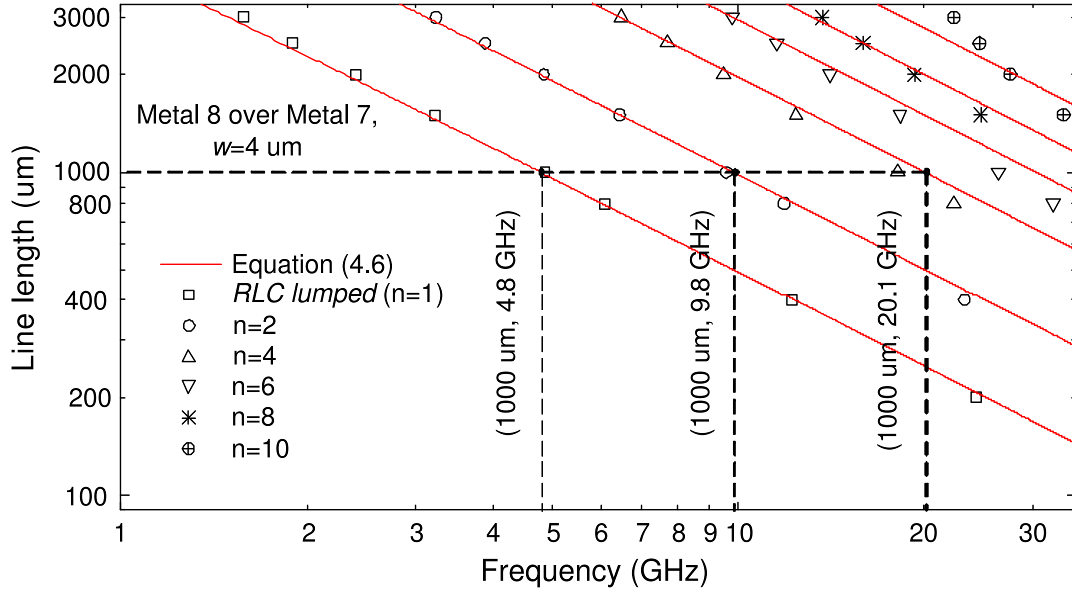


Figure 4.8: *RLC lumped* and *RLC distributed* equivalent circuit model regions using 2, 4, 6, 8, and 10 sections for interconnection lines Metal 8 over Metal 7, w=4 μm.

4.2 Establishment of the Modeling Methodology

The proposed modeling methodology can be used by circuit designers to perform accurate representation of any type of interconnection by applying the following main steps:

1. Perform the design and fabrication of at least two interconnection lines with the same characteristics but different lengths.
2. Measure the S-parameters associated with the lines within the desired frequency range using a Vector Network Analyzer.
3. Eliminate the parasitic contribution introduced by the pad-to-line discontinuities in the measurement process by applying a line-line de-embedding procedure.
4. Determine the values of Z_C, γ, R_l, L_l, and C_l of the studied interconnection line.

5. Select an equivalent circuit model (e.g. RC, LC, and RLC) that accurately represents the analyzed interconnection line at a given frequency range.

6. Determine, using equation (4.6), the boundary between the *lumped* and *distributed* equivalent circuit regions as well as the minimum number of stages required to properly represent an interconnection line at a given frequency.

4.3 Summary

- The proposed interconnect modeling methodology allows circuit designers to carry out the equivalent circuit model selection and the determination of the number of sections required in an equivalent circuit model for precise representation of on-chip interconnections typically used in the design and implementation of integrated systems.

- The equivalent circuit model selection as well as the determination of the number of sections strongly depend on the line length and the operating frequency.

- An RLC equivalent circuit model is indispensable to accurately represent the delay and losses associated with typical on-chip interconnections operating within the GHz frequency range.

- For a given interconnection line there is a combination of length and frequency that determines when the interconnection can be represented by a *lumped* model and when can be represented by a *distributed* model implemented with n sections.

- The boundaries of the *lumped* and *distributed* equivalent circuit model regions are analytically determined using equation (4.6).

Chapter 5

Design Application

In this chapter, the application of the interconnect modeling methodology in the design of clock generation and distribution networks is presented. In order to show the accuracy and application of the proposed modeling methodology in the design and implementation of basic clock generation and distribution blocks, the design and fabrication of several expanded three-stage ring oscillators are carried out. In addition, the design of local clock networks implemented by interconnecting and coupling expanded ring oscillators is included.

5.1 Design and Fabrication of Ring Oscillators

As previously stated, the local clock generation and distribution networks implemented by interconnecting and coupling oscillators (i.e. basic clock generation and distribution block) represent an attractive alternative to solve the problems associated with global clock networks. In the design of basic blocks used in the implementation of local networks, the interconnection lines play an essential role in the generation and distribution of clock signals; hence, an accurate electrical representation of the interconnection lines used in the design and implementation of these networks is very important.

Figure 5.1 shows a LCGDN implemented by interconnecting and coupling ring oscillators. This network simultaneously generates and distributes clock signals at different points of the integrated system by repeating the basic block which is a single-ended three-stage ring oscillator.

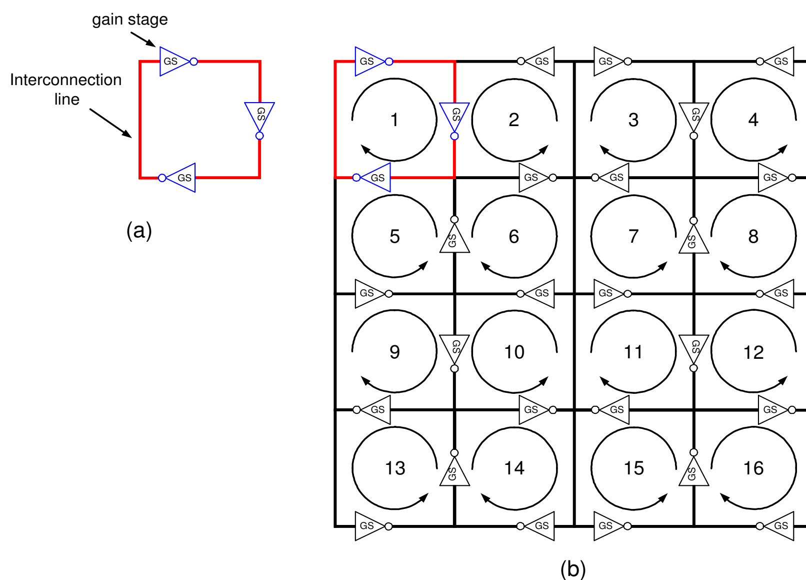


Figure 5.1: (a) Ring oscillator. (b) Local clock generation and distribution network.

Figure 5.2(a) shows a *lumped* ring oscillator implemented by N gain stages connected in a closed loop using very short interconnections; in this case, the space among the gain stages is reduced to the maximum. The *lumped* ring oscillator generates a periodic signal with operating frequency given by:

$$f = \frac{1}{2Nt_d} \tag{5.1}$$

where N and t_d are the number of gain stages and the corresponding delay, respectively.

Figure 5.2(b) shows an *expanded* ring oscillator implemented by N gain stages connected in a closed loop using interconnections with lengths in the order of millimeters. The expanded ring oscillator simultaneously generates and distributes a periodic signal with operating frequency given by:

$$f = \frac{1}{2Nt_d + 2Nt_l} \tag{5.2}$$

where t_l is the delay associated with the interconnection lines. Notice that the operating frequency of the *expanded* ring oscillator is directly related to the delay of the gain stages and the interconnections. This feature of ring oscillators will allow to verify the accuracy of the electrical equivalent circuit models obtained using the proposed interconnection line modeling methodology.

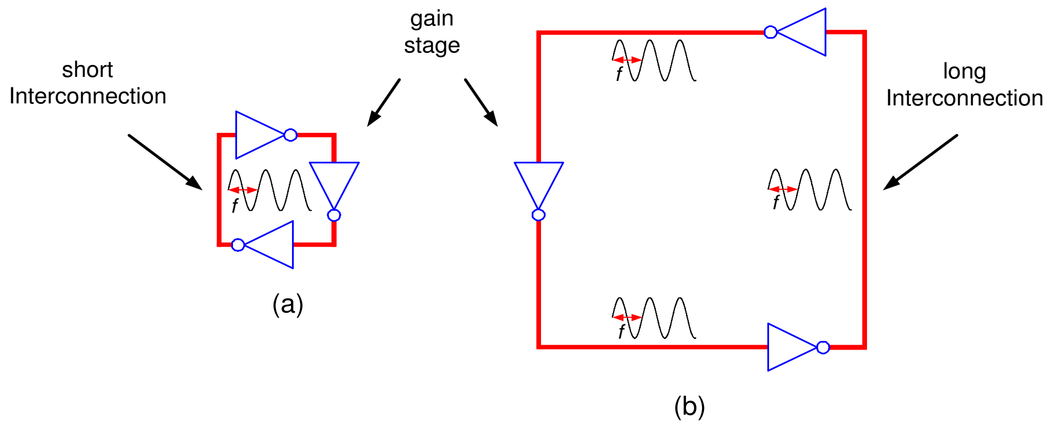


Figure 5.2: (a) Lumped ring oscillator. (b) Expanded ring oscillator.

In order to show the applicability and accuracy of the proposed interconnection line modeling methodology in the design of clock generation and distribution blocks used in the implementation of local clock networks, the design and fabrication of several ring oscillators using interconnection lines with w=2 μm and $l_1 = l_2 = l_3$=0, 1000, 1500, 2000, and 3000 μm (lengths typically used in these systems) are carried out. The oscillators are designed and fabricated using the Austriamicrosystems 0.35 μm process, a power supply of 3.3 V, and the Metal 4 level for the interconnection lines. Figures 5.3 and 5.4 show the schematic, layout, and a photograph of a three-stage ring oscillator.

As can be observed in Fig. 5.3, meandering interconnection lines are used in the implementation of the ring oscillators. In [30], an analysis of the impact of the bends in the interconnections is presented.

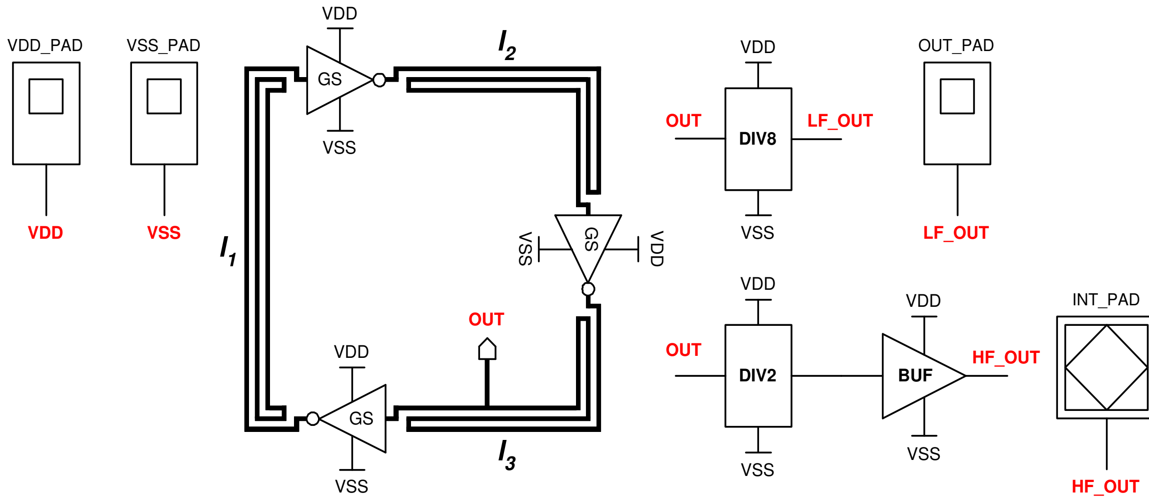
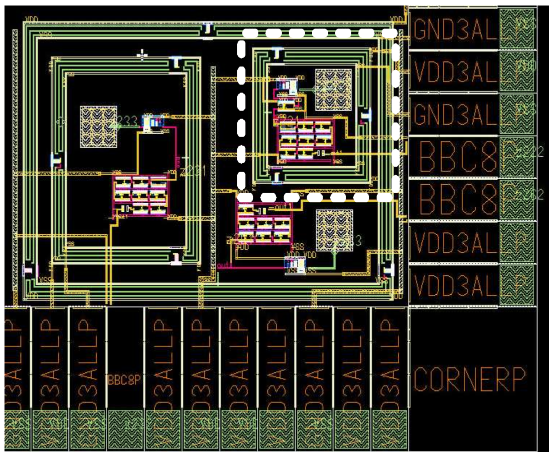
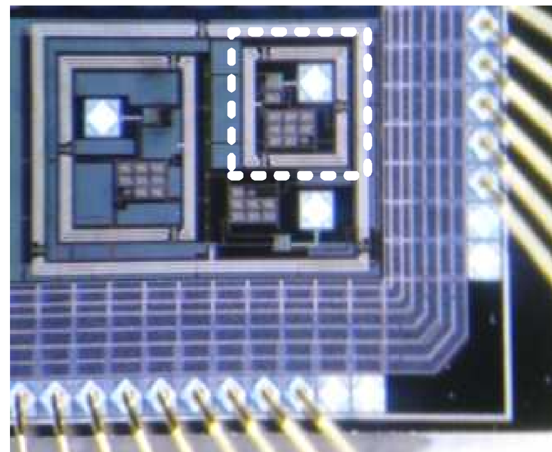


Figure 5.3: Schematic of an expanded three-stage ring oscillator.



(a)



(b)

Figure 5.4: Expanded three-stage ring oscillator: (a) Layout. (b) Photograph.

The experimental results obtained in [30] show a variation of 0.03 db between the S-parameters associated with interconnection lines (l=300 μm) with 45° and 90° bends at 20 GHz. Based on these results, it is evident that there is an impact of the bends in the S-parameters for very short lines. However, it is important to mention that the magnitude of the S_{11} and S_{12} parameters associated to interconnection lines with lengths in the order of millimeters, is considerably much larger than the magnitude of the variation generated by the bends. For this reason, the impact of the bends is not significant in the performance of the meandering interconnection lines used in the design and implementation of the expanded ring oscillators. Furthermore, with the purpose to reduce electromagnetic coupling in the meandering interconnection lines, the maximum separation allowed among interconnections is performed.

Now, in order to verify the accuracy of the equivalent circuit models obtained by applying the interconnect modeling methodology, the experimental and simulated operating frequencies of the implemented three-stage ring oscillators are compared.

For the case of the simulated operating frequency, the interconnections used in the implementation of the ring oscillator are replaced by the electrical equivalent circuit model; then, the corresponding simulations are performed in Eldo from Mentor Graphics software. Figure 5.5 shows a simulated transient response of an expanded three-stage ring oscillator.

For the case of the experimental frequency, *Off-chip* and *On-chip* measurements are performed. For *Off-chip* measurements, the high-frequency signal (OUT) generated by the oscillator is divided by a factor of 2^N; where N is the number of high-frequency dividers used in the implementation (e.g. if 8 dividers are used, the division factor is 2^8=256). Then, the divided signal (LF_OUT in the range of MHz) is fed to the output pad (OUT_PAD) that is responsible to drive the external load (e.g. bonding wires, pin package, device probes, etc.). The *Off-chip* measurements are performed using an Infiniium 54833A Oscilloscope with flexible cables and the corresponding oscilloscope probes. Figure 5.6 shows the measured *Off-chip* transient response of an expanded three-stage ring oscillator.

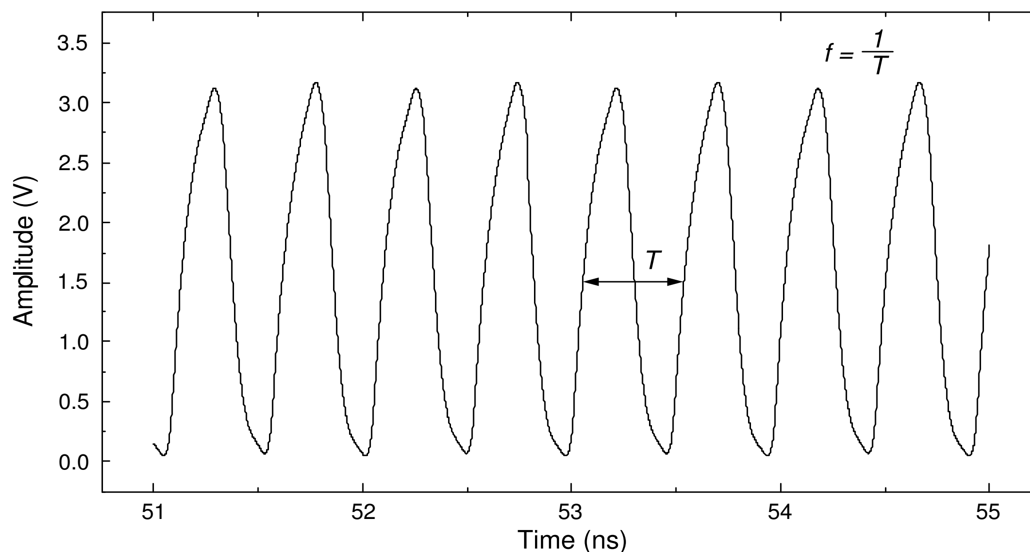


Figure 5.5: Simulated transient response of an expanded three-stage ring oscillator.

For *On-chip* measurements, the high-frequency signal (OUT) generated by the oscillator is divided by a factor of 2 (e.g. 2^1=2); then, the divided signal (HF_OUT) is fed to the high-frequency buffer (BUF) which is responsible to drive the load associated with the internal pad (INT_PAD) and the device probe. The *On-chip* measurements are performed using an Advantest R3265A series spectrum analyzer (SA) with a semi-rigid cable and the corresponding on-chip one point probes. Figure 5.6 shows the measured output spectrum of an expanded three-stage ring oscillator. A more complete description of the test setups used to perform the *Off-chip* and *On-chip* measurements is presented in the Appendix A of this thesis.

Table 5.1 shows a performance summary of the implemented three-stage ring oscillators. In this table, the *Operating frequency* represents the average experimental frequency which is obtained by measuring six oscillators fabricated in six different chips. The *Output voltage* and *Power consumption* denotes the amplitude of the generated signal and power consumption (this value does not include the power of the dividers, buffers, pads, etc.) of the ring oscillator, respectively; these values are obtained through simulations. Finally, the *Coverage area* represents the area in which the generated signal can be distributed trough the integrated circuit.

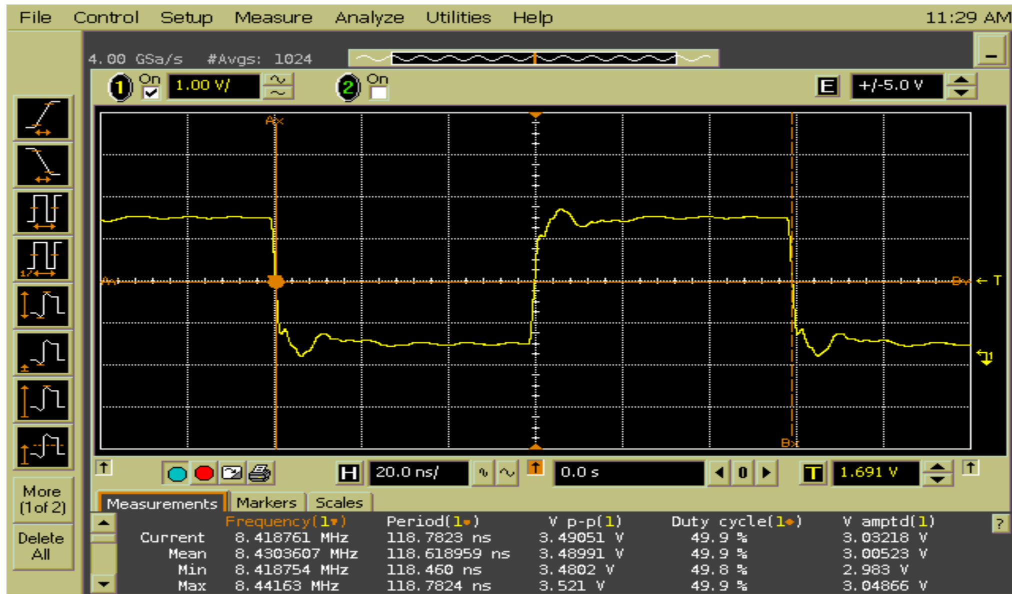


Figure 5.6: Measured *Off-chip* transient response of an expanded three-stage ring oscillator.

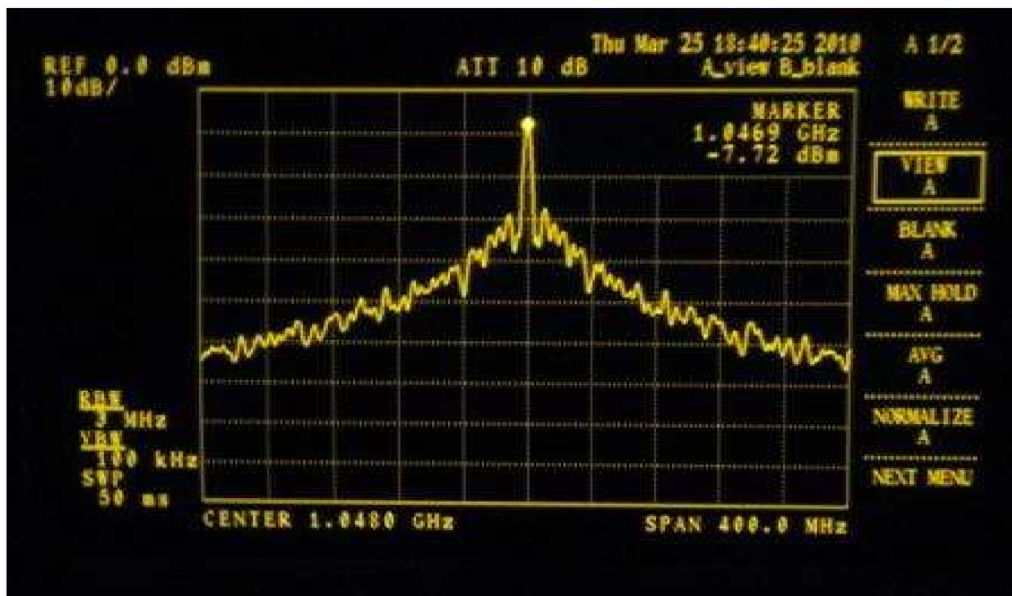


Figure 5.7: Measured *On-chip* output spectrum of an expanded three-stage ring oscillator.

Table 5.1: Performance summary of fabricated three-stage ring oscillators.

Process Technology	Austriamicrosystems 0.35 μm				
Oscillator Type	Single-ended				
Power supply voltage (V)	3.3				
Interconnection width (μm)	2				
Interconnection length (μm) l_1=l_2=l_3	70	1000	1500	2000	3000
Operating frequency OUT (GHz)	2.58	2.14	2.00	1.84	1.53
Output voltage OUT (V)	3.06	3.12	3.16	3.18	3.19
Power consumption (mW)	33.25	31.34	30.42	29.61	28.04
Coverage area (mm x mm)	0.07 x 0.07	0.75 x 0.75	1.125 x 1.125	1.5 x 1.5	2.25 x 2.25

Figure 5.8 shows the experimental and simulated operating frequency for the implemented three-stage ring oscillators varying the length of the interconnection lines. In this figure, the *RLC* (*lumped*, n=6, and n=12) simulated data are obtained considering the parasitic effects of the gain stages while the interconnection lines are represented by an *RLC lumped* and *RLC distributed* equivalent circuit models implemented with n=6 and 12 sections obtained by applying the proposed methodology. The Post Layout (*P. Layout*) simulations also consider the parasitic effects of the gain stages; nevertheless, the interconnections are represented by the equivalent circuit model provided by the parameter extraction tool from Calibre on Mentor Graphics software. *Experimental* data denotes the measurement results which are used as a reference to carry out the corresponding comparison with the simulated data. The deviations of simulated from experimental data allow to determine which one of the models is the most precise and appropriate to represent an interconnection line. Thus, the error parameter is defined as:

$$Error = \frac{(Experimental - Simulation) * 100}{Experimental} \tag{5.3}$$

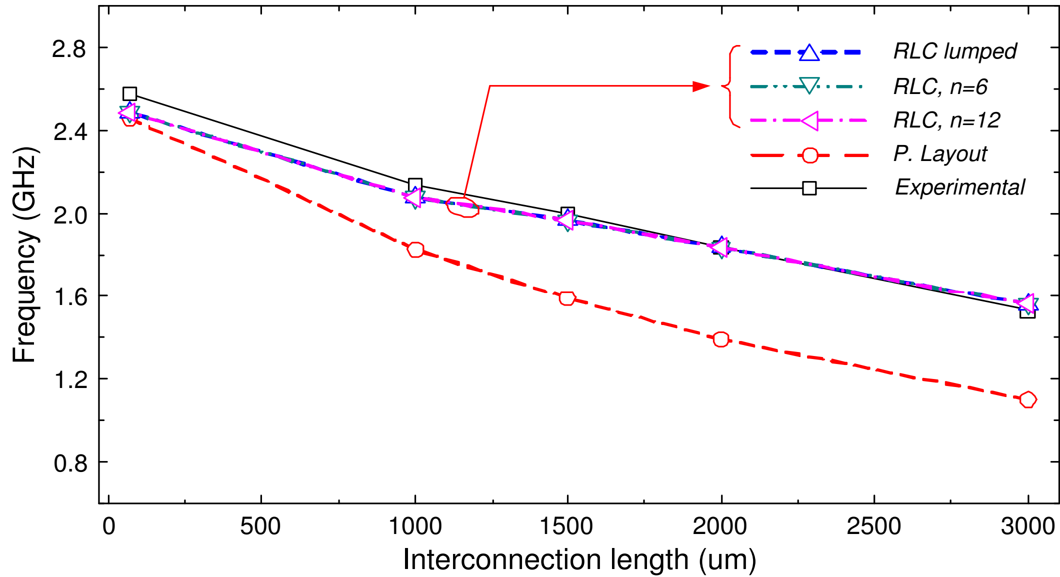


Figure 5.8: Experimental operating frequency of three-stage ring oscillators compared with simulated data using *RLC lumped* and *RLC distributed* (n=6 and 12 sections) equivalent circuit models.

From Fig. 5.8, notice the large discrepancy between the *Experimental* and *P. Layout* simulation data; more precisely, when the interconnection lines are represented by the equivalent circuit model provided by the parameter extraction software, the average error is 18 %. It is important to note that the accuracy between the *Experimental* and *P. Layout* simulation data only depends on the equivalent circuit model generated by the extraction tool; this tool automatically generates a distributed equivalent circuit which only takes into account the resistance of the metal lines and capacitance associated with the inter-metal dielectric. In fact, this parameter extraction tool uses data provided by the chip manufacturer, which commonly provides nominal values for material properties obtained at fixed frequencies (in some cases even at dc). As can be observed in Fig. 5.8, the *P. Layout* simulated operating frequency of the ring oscillators is lower than the *Experimental* data; this is mainly because the equivalent circuit model provided by the extraction tool used in the post layout simulations overestimates the delay associated with the interconnection lines used in the implementation. Now, observe the good correlation between the experimental

and simulated data obtained using the *RLC lumped* and *RLC distributed* equivalent circuits implemented with 6 and 12 sections; thus, when the interconnection lines are represented by these equivalent circuits, the average error is 2 %. It is important to mention that in these simulations the information corresponding to an interconnection line fabricated in the Metal 4 level using the Metal 1 as a ground plane is used; this is because in the design of integrated circuits, the power and ground lines located in the lowest metal levels provide a virtual reference plane for the interconnection lines [25].

Notice that the simulated data obtained using the *RLC lumped* and *RLC distributed* equivalent circuits implemented with 6 and 12 sections show the same average error. In order to explain these results, consider the experimental operating frequency for the implemented three-stage ring oscillator using interconnection lines with l=1000 μm which is f=2.14 GHz. According to the results obtained in Chapter 4 (specifically the information shown in Fig. 4.6), at this operating frequency, an interconnection line with l=1000 μm can be accurately represented by an *RLC lumped* equivalent circuit; for this reason, when the interconnection line is represented by an *RLC distributed* equivalent circuit implemented with a greater number of sections, the error percentage remains constant. Obviously, the use of an equivalent circuit implemented with a minimum number of sections reduces the computation time required to perform the corresponding simulations that is considerable high, especially in the design of systems with a large number of interconnects.

5.2 Design of Local Clock Generation and Distribution Network

Once that the applicability and accuracy of the interconnect modeling methodology in the design of basic clock generation and distribution blocks has been shown; the design of a LCGDN is presented. The local clock network is designed using the

Austriamicrosystems 0.35 μm process, power supply of 3.3 V, and parameters associated with an interconnection line implemented in the Metal 4 level using the Metal 1 level as a ground plane.

5.2.1 2 x 2 Oscillators Array

Figure 5.9 shows a local clock network implemented by interconnecting and coupling the basic clock block, which in this case is an expanded three-stage ring oscillator, using interconnection lines with w=2 μm and l=1000 μm. Notice that in this network, the coupling among oscillators is carried out through the interconnections and gain stages A3, A4, A5, and A6. In the implementation of this local network, the interconnection and coupling of four expanded three-stage ring oscillators allow to generate and distribute clock signals with the same operating frequency, phase, and output voltage at four different points in the integrated circuit.

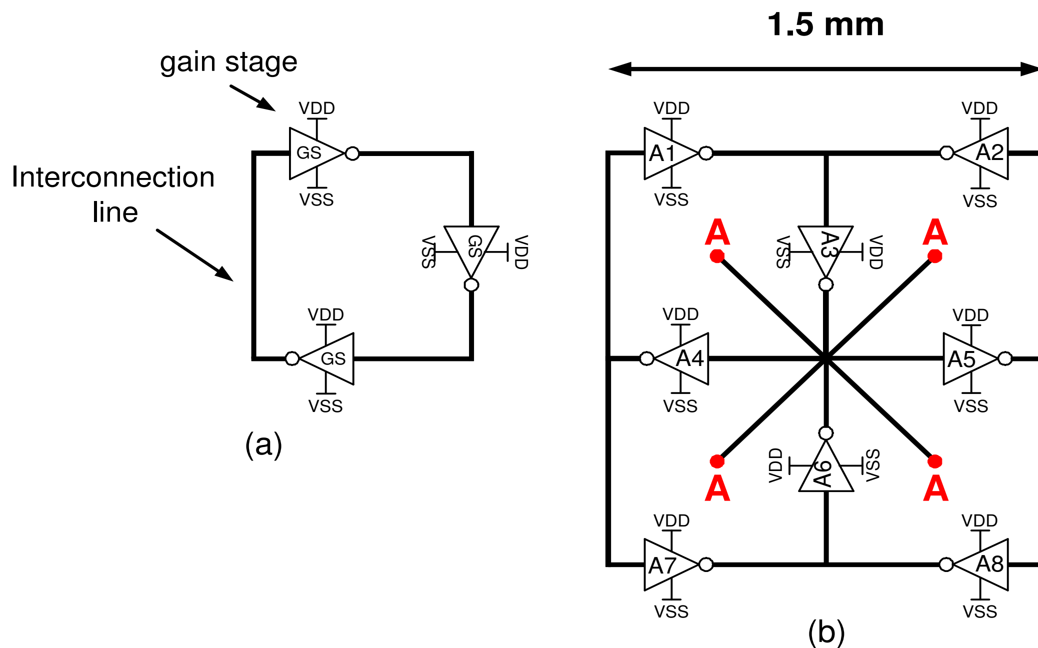


Figure 5.9: (a) Basic block: expanded three-stage ring oscillator. (b) Local clock network implemented by interconnecting and coupling expanded ring oscillators.

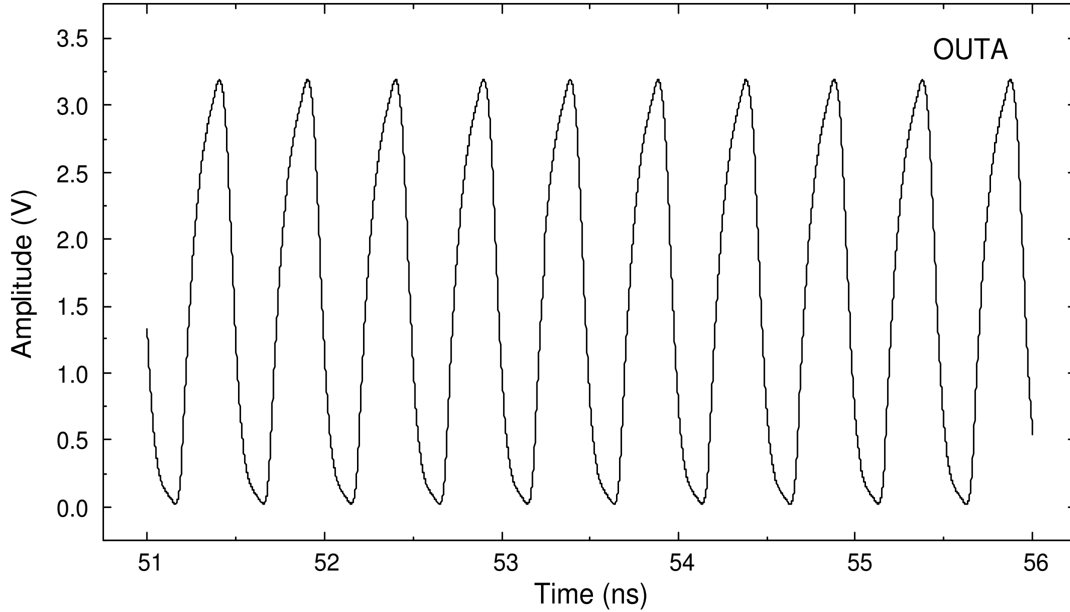


Figure 5.10: Simulated transient response of local clock network implemented by interconnecting and coupling expanded ring oscillators.

Table 5.2: Performance summary of local clock network implemented by interconnecting and coupling expanded ring oscillators.

Process Technology	AMS 0.35 μm
Basic block	Three-stage ring oscillator
Power supply voltage (V)	3.3
Interconnection width (μm)	2
Interconnection length (μm)	1000
Interconnection model	*RLC lumped* model
Operating frequency (GHz)	2.02
Output voltage (V)	3.16
Power consumption (mW)	71.50
Coverage area (mm x mm)	1.5 x 1.5

Figure 5.10 and Table 5.2 show the simulated transient response and performance summary of the clock network shown in Fig. 5.9. This network simultaneously generates and distributes signals with operating frequency of 2.02 GHz and output voltage of 3.16 V at 4 different points of the integrated system which produces a coverage area of 1.5 mm x 1.5 mm and a total power consumption of 71.5 mW.

5.2.2 4 x 4 Oscillators Array

Now, in order to implement a clock network which generates and distributes clock signals in a higher area, the interconnection and coupling of a larger number of ring oscillators is required. Figure 5.11 shows a local clock network implemented by interconnecting and coupling the basic clock block which in this case is an array of four expanded three-stage ring oscillators.

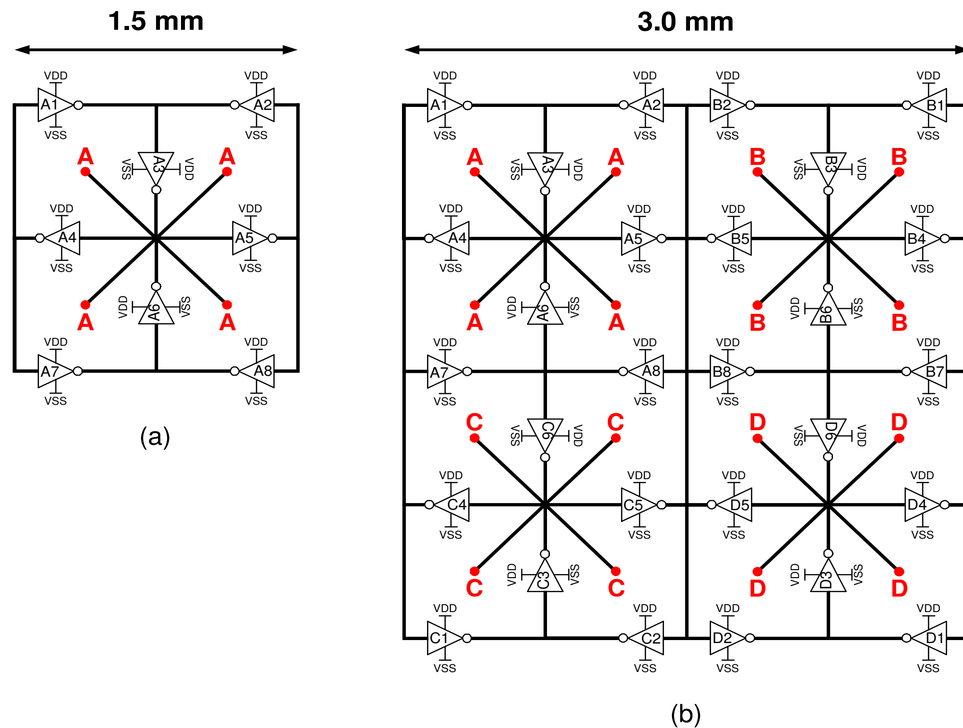


Figure 5.11: (a) Basic block: array of expanded ring oscillators. (b) Local clock network implemented by interconnecting and coupling arrays of expanded ring oscillators.

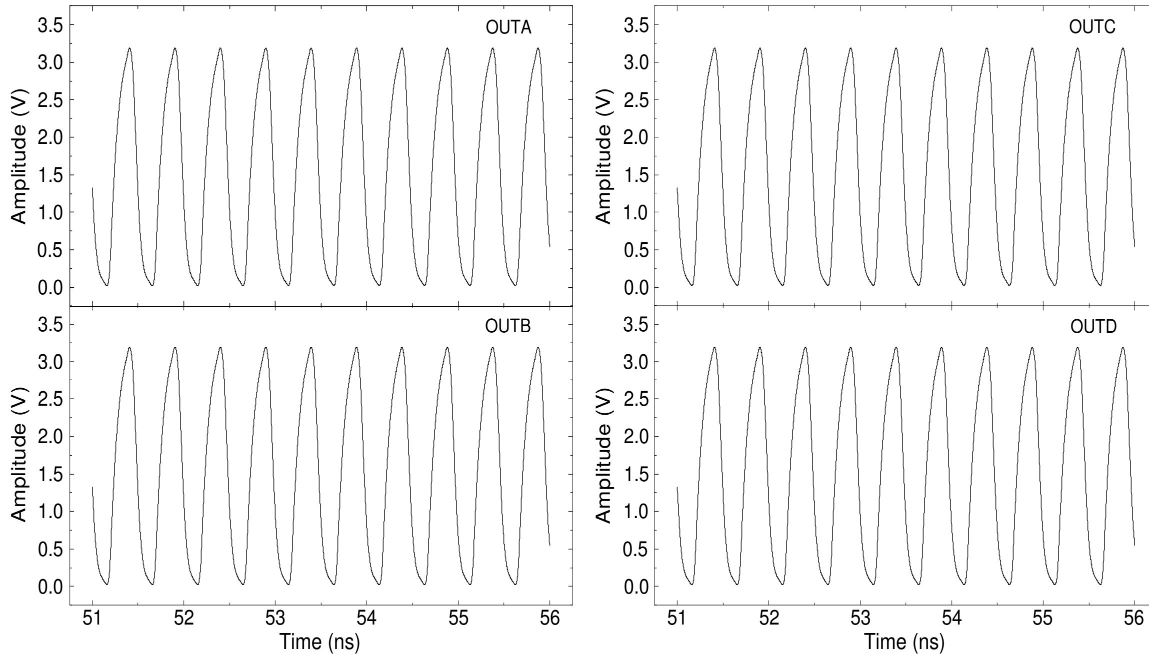


Figure 5.12: Simulated transient response of local clock network implemented by interconnecting and coupling arrays of expanded ring oscillators.

Table 5.3: Performance summary of local clock network implemented by interconnecting and coupling arrays of expanded ring oscillators.

Process Technology	Austriamicrosystems 0.35 μm			
Basic block	array of three-stage ring oscillators			
Power supply voltage (V)	3.3			
Interconnection width (μm)	2			
Interconnection length (μm)	1000			
Interconnection model	*RLC lumped* model			
Block	A	B	C	D
Operating frequency (GHz)	2.02	2.02	2.02	2.02
Output voltage (V)	3.16	3.16	3.16	3.16
Power consumption (mW)	71.50	71.50	71.50	71.50
Coverage area (mm x mm)	1.5 x 1.5	1.5 x 1.5	1.5 x 1.5	1.5 x 1.5
Total power consumption (mW)	286			
Total coverage area (mm x mm)	3.0 x 3.0			

Notice that in this network the coupling among arrays of oscillators is carried out through the interconnections and gain stages A7, A8, B7, and B8. In the implementation of this local network, the interconnection and coupling of four basic clock blocks allow to generate and distribute clock signals with the same operating frequency, phase, and output voltage at sixteen different points in the integrated circuit. Figure 5.12 and Table 5.3 show the simulated transient response and performance summary of the clock network shown in Fig. 5.11. Now, this network simultaneously generates and distributes signals with operating frequency of 2.02 GHz and output voltage of 3.16 V at 16 different points of the integrated system which results in a coverage area of 3.0 mm x 3.0 mm and a total power consumption of 286 mW.

As can be seen in the results shown in Table 5.3, each one of the blocks in the local clock network generates and distributes clock signals with operating frequency of 2.02 GHz and output voltage of 3.16 V at 4 different points of the integrated system which produces a coverage area of 1.5 mm x 1.5 mm and a total power consumption of 71.5 mW. This is mainly because the clock network is implemented by interconnecting and coupling the same clock generation and distribution block. In addition, it is important to mention that each one of these basic blocks is operating under the same voltage, coverage area, and load conditions; therefore, it is logical that the performance metrics of the A, B, C, and D blocks are equal. Notice that the operating frequency of the LCGDN networks is determined by the operating frequency of the basic clock block; while the total power consumption and coverage area are directly proportional to the number of basic blocks used in the implementation.

In the design of the local clock networks previously described, the interconnection lines have been represented by an *RLC lumped* equivalent circuit model, which according to the results obtained in Chapter 4, is sufficient to properly represent interconnections with w=2 μm and l=1000 μm up to 5.5 GHz.

As shown in the previously described design application, the interconnection lines play an essential role in the design and implementation of local clock networks; therefore, the proposed modeling methodology allows circuit designers to perform

the determination of the electrical equivalent circuit for accurate representation of on-chip interconnections typically used in the design of this type of networks. Thus, once that the electrical equivalent circuit model has been obtained, the design of complex systems (e.g. local clock network implemented by interconnecting and coupling 32 ring oscillators) can be carried out in a practical and relatively simple way.

5.3 Summary

- The interconnection lines play an essential role in the performance of global and local clock generation and distribution networks; therefore, the determination of an equivalent circuit model for accurate representation of the interconnections used in this networks is very important.

- In the design of global and local clock networks, the electrical equivalent circuit model provides important information about the characteristics of the interconnections used in the implementation; then, based on this information, a precise design of the gain, compensation, and output stages can be carried out.

- The proposed interconnect modeling methodology allows circuit designers to carry out the determination of the electrical equivalent circuit model for precise representation of the interconnections used in the design and implementation of global and local clock networks.

- Once the equivalent circuit model used to represent the interconnection lines is obtained, the design of simple and complex systems can be carried out in a practical and relatively simple way.

- For the case of the local clock networks, it was shown that the performance of this type of networks strongly depends on the characteristics of the oscillator used in the implementation; therefore, a proper design of the basic clock

generation and distribution block (e.g. ring oscillator, traveling wave oscillator, standing wave oscillator, etc.) is indispensable.

- In the design of basic clock generation and distribution blocks, it was demonstrated that the error between the experimental and simulated operating frequency of the expanded ring oscillators is reduced up to 2 % when the interconnection lines used in the implementation are represented with the equivalent circuit models obtained by applying the proposed interconnect modeling methodology.
- It was shown that an *RLC lumped* equivalent circuit is sufficient to properly represent the interconnections used in the design application presented in this work.
- The determination of the minimum number of sections required in the equivalent circuit is important to reduce the computation time which is considerably higher in the design of complex systems containing a large number of interconnections.

Chapter 6

Conclusions

In this thesis an accurate modeling methodology for on-chip interconnections used in the design and implementation of global and local clock generation and distribution networks was presented.

Nowadays, the design of a clock network that simultaneously generates and distributes signals at high operating frequencies, with a low time uncertainty, and a low power consumption is essential for the synchronization of high-performance microprocessors used in the implementation of high-speed multimedia equipment. In actual microprocessors, the global clock networks are widely used to generate and distribute the synchronization signals. However, due to the continuous downscaling of the technology, the increase of the operating frequency and area of the integrated circuits, the mismatches associated with the length of the interconnections, the process variations, electromagnetic coupling, load restrictions, and block distribution in complex integrated systems, the use of global clock networks is reaching its limit. Hence, it is clear that a change in the generation and distribution of the clock signals is inevitable. Therefore, the local clock generation and distribution networks implemented by interconnecting and coupling oscillators represent one of the alternatives to resolve the problems related with global clock networks.

The current and future clock design trends make it necessary to implement accurate equivalent circuit models for the representation of interconnections used in the

implementation of a given application. Thus, one of the contributions of this proposal is encouraging circuit designers to use electrical equivalent circuit models directly obtained from experimental data that allow to carry out a precise representation of the interconnection lines used in the design and implementation of high-frequency clock generation and distribution networks. Therefore, in order to provide circuit designers with guidelines to perform experimental model implementations, in this thesis, the establishment of a modeling methodology developed from S-parameter measurements of fabricated interconnection line test structures is presented.

In the proposed modeling methodology, it was shown that through an appropriate exploitation of the S and $ABCD$ parameters associated with on-chip interconnections, the interconnect parameter extraction, the equivalent circuit model selection, and the determination of the minimum number of sections required in the equivalent circuit for accurate representation of interconnects of certain lengths within specific frequency ranges can be performed. It is important to mention that the equivalent circuit model selection as well as the determination of the minimum number of sections strongly depend on the line characteristics and the operating frequency. It was shown that an RLC equivalent circuit model is necessary to accurately represent the characteristics (i.e. the delay and losses) associated with on-chip interconnections operating within the GHz frequency range. Also, it was shown that for a given interconnection line there is a combination of length and frequency that determines when the interconnection can be represented by a *lumped* model and when can be represented by an *distributed* model implemented with n sections.

The presented interconnect modeling methodology developed from S-parameter measurements of fabricated test structures and application of the transmission line theory can be used by circuit designers to perform precise electrical representation of typical interconnections used in current and future integrated circuit applications fabricated in different technologies.

In the design of integrated systems, the circuit designer is responsible for defining the methodology used to obtain the equivalent circuit model which represents the

interconnection lines used in the corresponding implementation. Nevertheless, in the design of high-frequency clock networks, the interconnection lines play a key role in the generation and distribution of the clock signals; therefore, an inaccurate representation of the interconnections used in the implementation of this type of networks will be reflected in an inadequate system performance. So, the proposed modeling methodology represents an appropriate alternative to achieve an accurate design and implementation of current and future clock generation and distribution networks.

6.1 Future Work

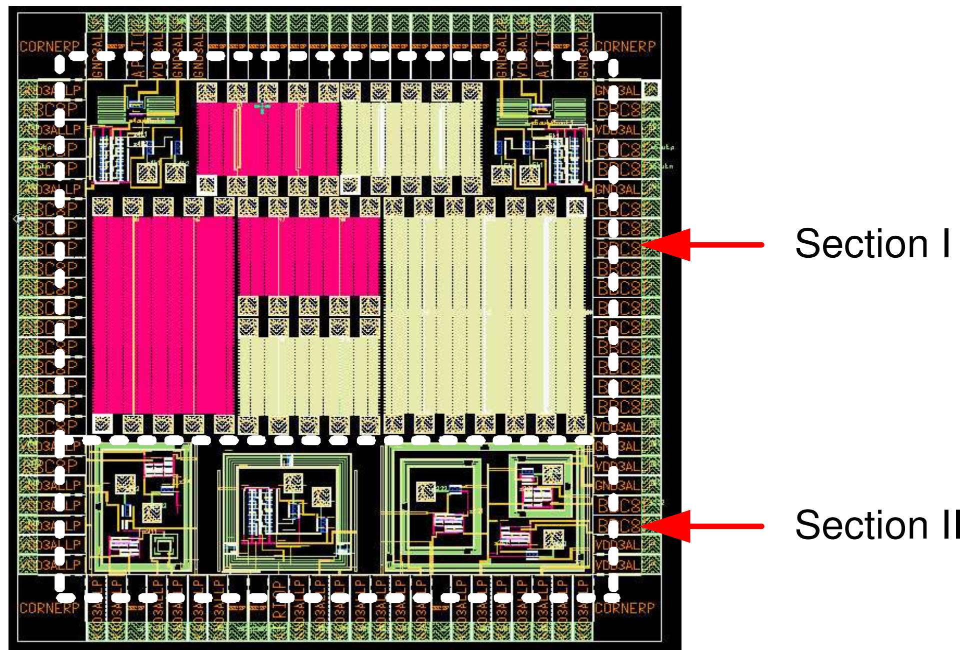
Certainly, the interconnection lines play and will continue playing a key role in the design and implementation of current and future global and local clock generation and distribution networks. As shown in this thesis, an interconnect modeling methodology developed from S-parameter measurements of fabricated interconnection line tests structures allows circuit designers to perform accurate electrical representation of on-chip interconnections operating within the GHz frequency range. Undoubtedly, this methodology developed from experimental data is the most accurate and proper alternative to carry out the modeling of on-chip interconnections; however, it is important to mention that the weak point of this methodology is related to the design and fabrication of test structures for interconnections with different values of Z_C and γ (i.e. changing the width and thickness of the metal, inter-metal dielectric, or ground plan layers). Thus, one alternative to solve this inconvenient is through the design and fabrication of test structures with representative dimensions (e.g. interconnections with different width, length, ground plane, etc.); then, by applying interpolation/extrapolation the implementation of an scalable model can be achieved. Nevertheless, although this possible solution sounds trivial there is much complexity in developing an accurate scalable model; therefore, this is a topic for future contributions.

Appendix A

Silicon Prototype

This appendix shows the fabricated silicon prototype and test setups used to perform the measurements. Firstly, a description of the fabricated interconnection line test structures and expanded three-stage ring oscillators is presented. Also, a description of the test setups used to perform the measurements of the fabricated interconnection lines and ring oscillators is shown in the second part.

Figure A.1 shows the layout and a photograph of the integrated circuit prototype which is designed and fabricated using a 4 Metal Austriamicrosystems 0.35 μm process. As can be observed in this figure, the prototype is divided in two main sections.



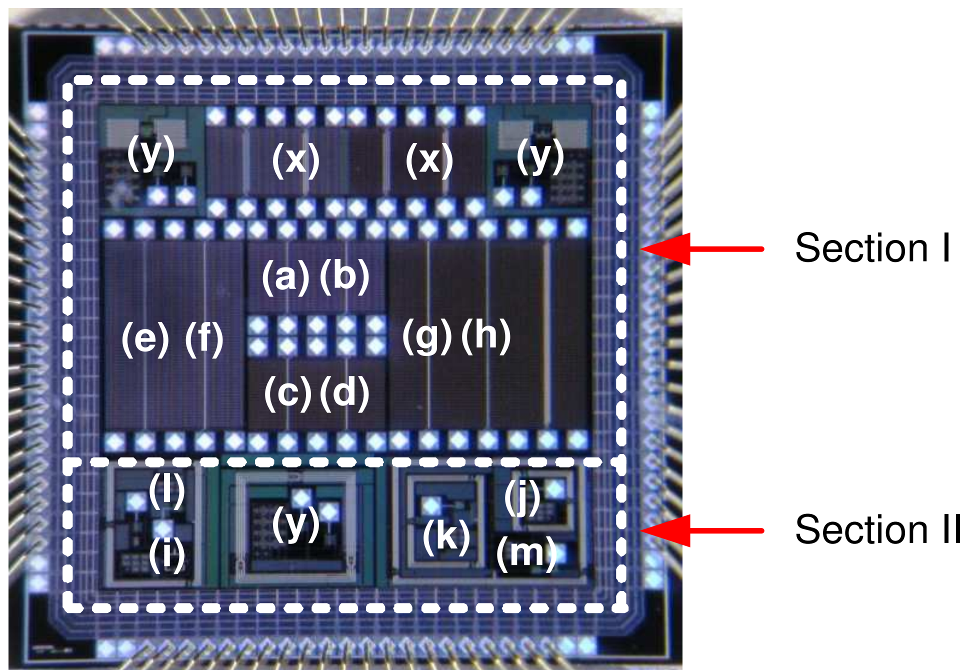


Figure A.1: Integrated circuit prototype: (a) Layout. (b) Photograph.

A.1 Section I

Section I contains a set of interconnection line test structures with different characteristics (e.g. different width, length, ground plane, etc.) which are used to carry out the parameter extraction associated with typical on-chip interconnections used in the design of integrated systems.

(a) Interconnection line with w=2 μm and l=400 μm implemented in the Metal 4 level using the Metal 1 level as a ground plane.

(b) Interconnection line with w=4 μm and l=400 μm implemented in the Metal 4 level using the Metal 1 level as a ground plane.

(c) Interconnection line with w=2 μm and l=400 μm implemented in the Metal 4 level using the Metal 3 level as a ground plane.

(d) Interconnection line with w=4 μm and l=400 μm implemented in the Metal 4 level using the Metal 3 level as a ground plane.

(e) Interconnection line with w=2 μm and l=1000 μm implemented in the Metal 4 level using the Metal 1 level as a ground plane.

(f) Interconnection line with w=4 μm and l=1000 μm implemented in the Metal 4 level using the Metal 1 level as a ground plane.

(g) Interconnection line with w=2 μm and l=1000 μm implemented in the Metal 4 level using the Metal 3 level as a ground plane.

(h) Interconnection line with w=4 μm and l=1000 μm implemented in the Metal 4 level using the Metal 3 level as a ground plane.

(x) Other test structures.

A.2 Section II

Section II contains several ring oscillators using interconnection lines with w=2 μm and l=0, 1000, 1500, 2000, and 3000 μm implemented in the Metal 4 level. More details regarding ring oscillators are presented in the Appendix C.

(i) *Lumped* three-stage ring oscillator using interconnection lines with w=2 μm and l=70 μm.

(j) *Expanded* three-stage ring oscillator using interconnection lines with w=2 μm and l=1000 μm.

(k) *Expanded* three-stage ring oscillator using interconnection lines with w=2 μm and l=1500 μm.

(l) *Expanded* three-stage ring oscillator using interconnection lines with w=2 μm and l=2000 μm.

(m) *Expanded* three-stage ring oscillator using interconnection lines with w=2 μm and l=3000 μm.

(y) Other test structures.

A.3 Test Setup for S-parameter Measurements

The S-parameter measurements of the fabricated interconnection line test structures are performed using the test setup shown in Fig. A.2 which is implemented by:

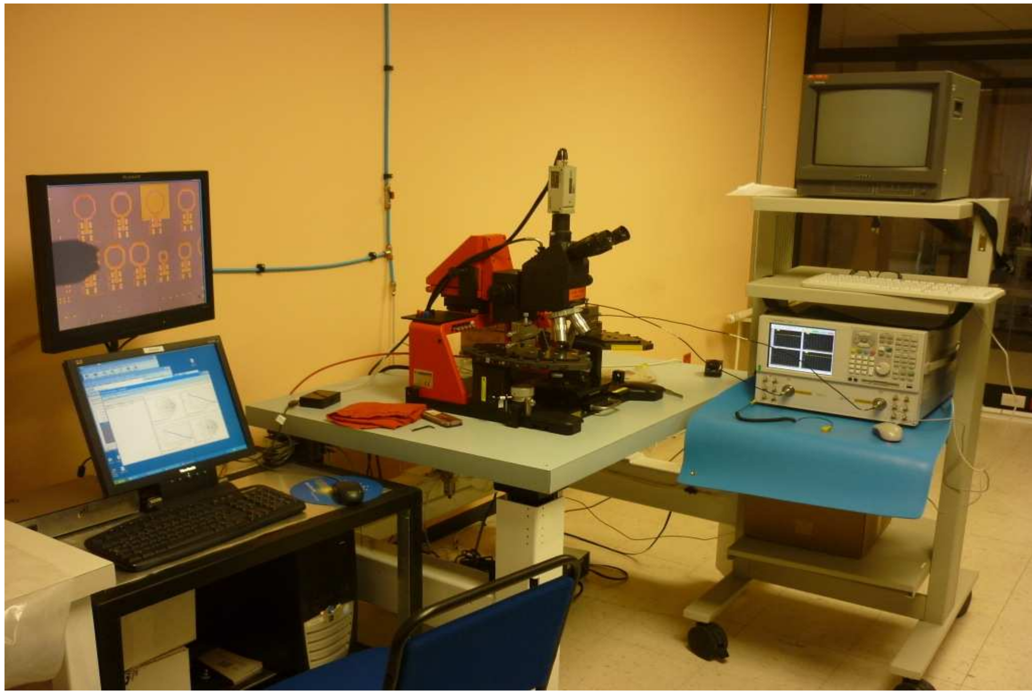


Figure A.2: Test setup for the S-parameter measurements of the fabricated interconnections.

a) 1 Vibration Isolation Table: Newport HL-3648W-OPT

b) 1 Manual Probe System: Cascade Microtech PM5

c) 2 Manual High-Frequency Probe-Head: Cascade Microtech PH110HF

d) 2 Microwave Probes: GSG Coplanar Probes

e) 2 Semi-rigid Cables

f) 1 PNA Network Analyzer: Agilent Technologies E8361A

g) 1 Impedance Standard Substrate: Cascade Microtech ISS

h) 1 Monitor and Video Camera: Sony

i) 1 Workstation Tower: Tektronix K475

Figure A.3 shows a photograph of the integrated circuit die used to perform the S-parameter measurements of the fabricated interconnection line test structures.

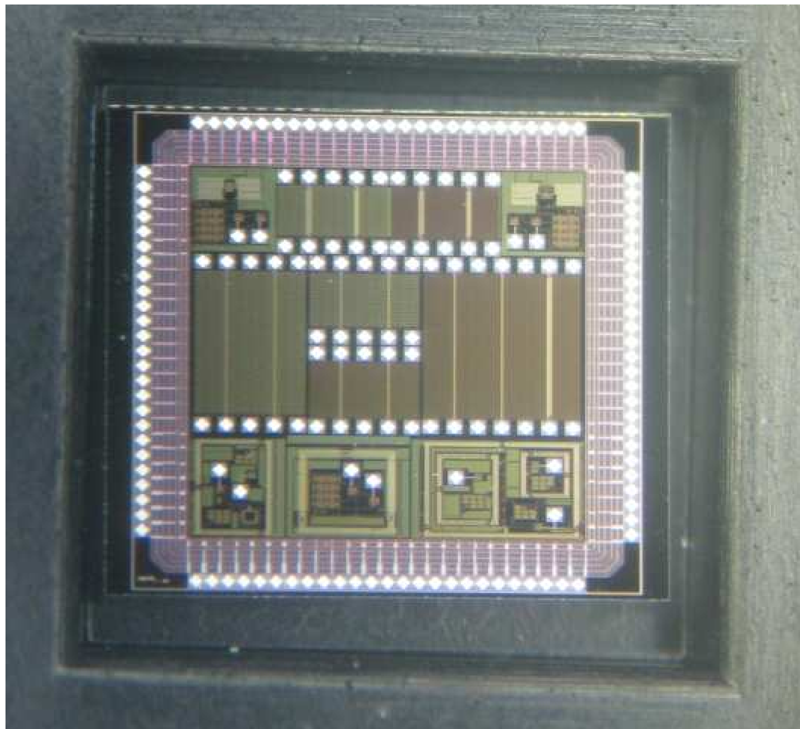


Figure A.3: Photograph of the integrated circuit die.

A.4 Test Setup for Off-Chip Measurements

The Off-chip measurements of the fabricated three-stage ring oscillators are performed using the test setup shown in Fig. A.4 which is implemented by:

Figure A.4: Test setup for the Off-Chip measurements of the fabricated three-stage ring oscillators.

a) 1 Workstation: GADU Systems

b) 1 Printed Circuit Board

c) 1 Test socket:

d) 1 DC Power Supply: Agilent E3640A

e) 1 Oscilloscope: Infiniium 54833A

f) 1 Passive probe

A.5 Test Setup for On-Chip Measurements

The On-chip measurements of the fabricated three-stage ring oscillators are performed using the test setup shown in Fig. A.5 which is implemented by:

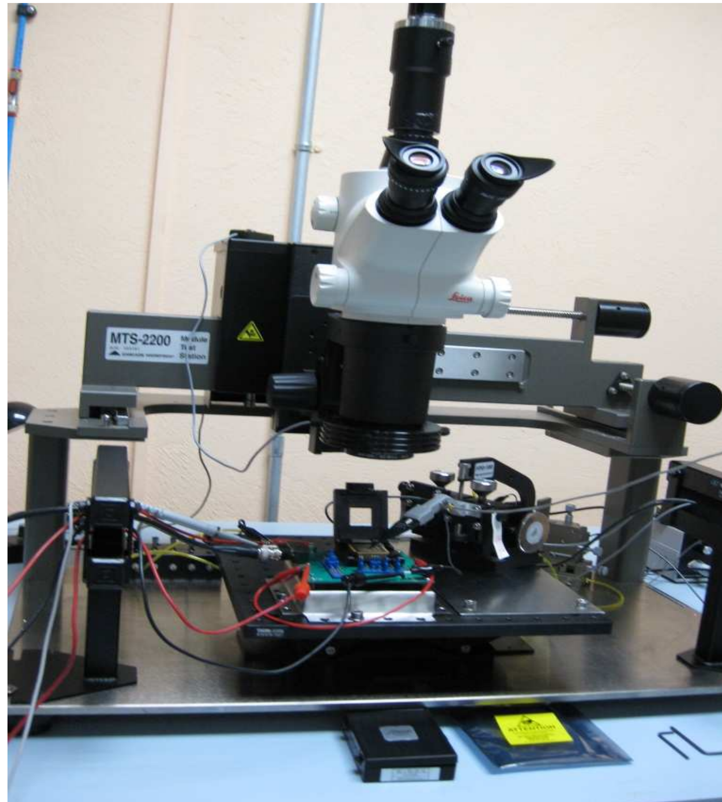


Figure A.5: Test setup for the On-Chip measurements of the fabricated three-stage ring oscillators.

a) 1 Vibration Isolation Table: Newport HL-3648W-OPT

b) 1 Manual Probe System: Cascade Microtech MTS-2000 Series

c) 1 High-Performance Probe Positioner: Cascade Microtech DCM 200 Series

d) 1 Microwave Probe: Picoprobe Model 35

e) 1 Semi-rigid Cable

f) 1 Printed Circuit Board

g) 1 Test socket:

h) 1 DC Power Supply: Agilent E3640A

i) 1 Spectrum Analyzer: Advantest R3265A

j) 1 Workstation Tower: Tektronix K475

Figure A.6 shows a photograph of the integrated circuit package used to carry out the Off-chip and On-chip measurements of the fabricated three-stage ring oscillators.

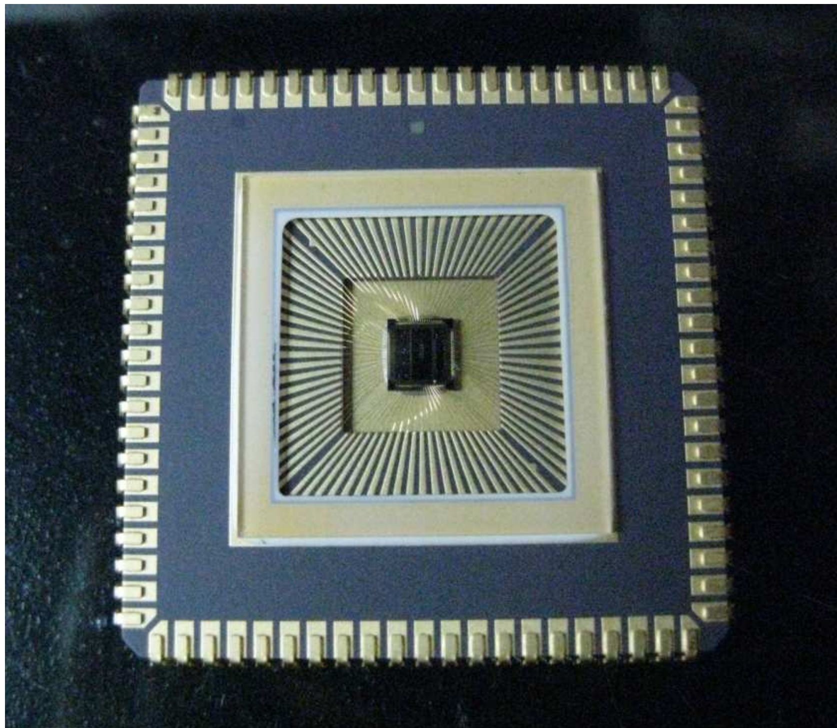


Figure A.6: Photograph of the integrated circuit package.

Appendix B

Application of the Modeling Methodology

The proposed modeling methodology is applied to the fabricated interconnection lines (previously described in Appendix A) and the corresponding results are presented in this appendix. Firstly, the values of Z_C, γ, R_l, L_l, C_l associated with the fabricated lines are obtained; then, the determination of the minimum number of sections required in the equivalent circuit for accurate representation of interconnects of certain lengths within specific frequency ranges is carried out.

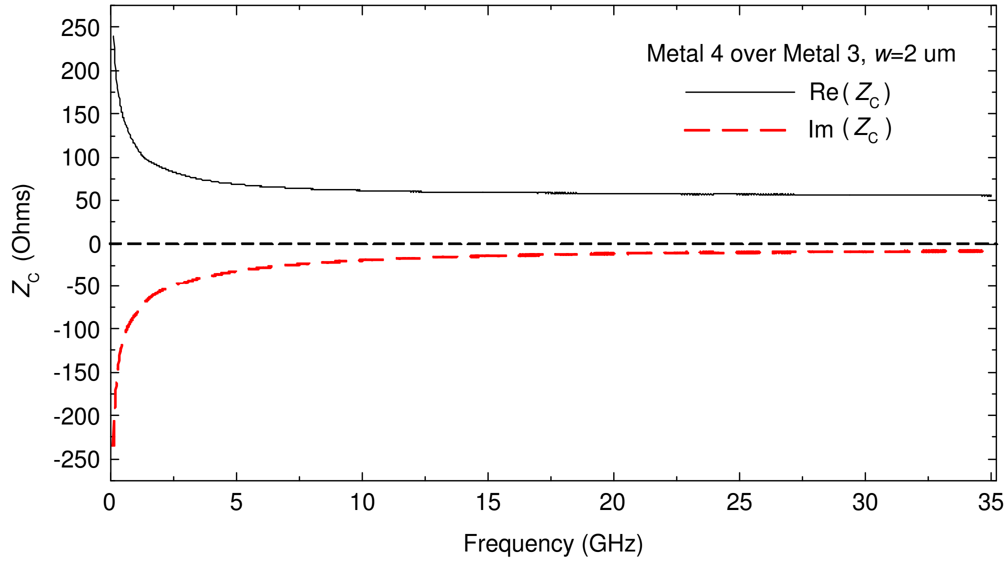


Figure B.1: Experimental characteristic impedance for the fabricated microstrip line Metal 4 over Metal 3, w=2 μm.

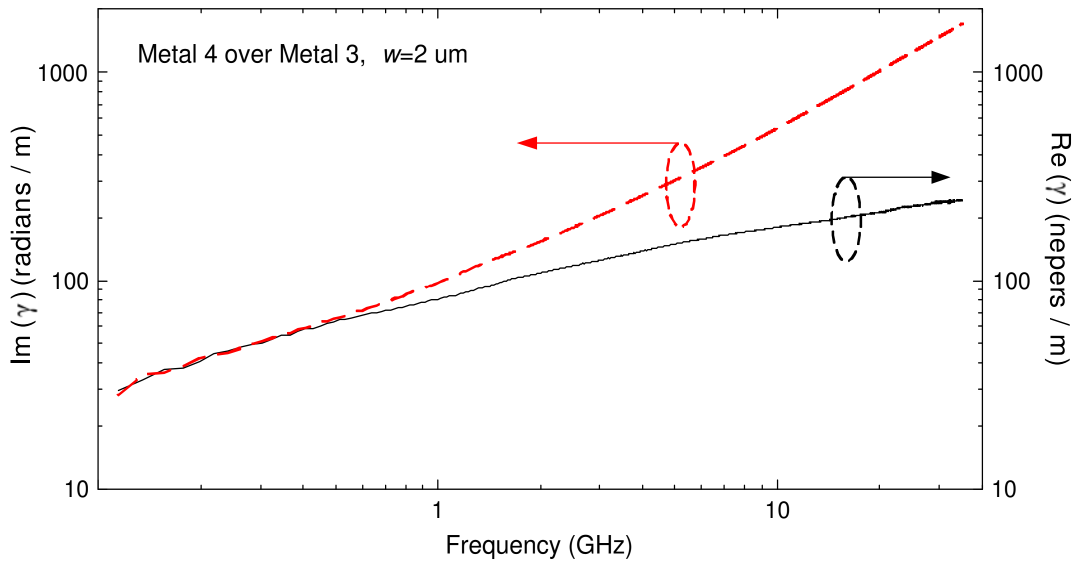


Figure B.2: Experimental propagation constant for the fabricated microstrip line Metal 4 over Metal 3, w=2 μm.

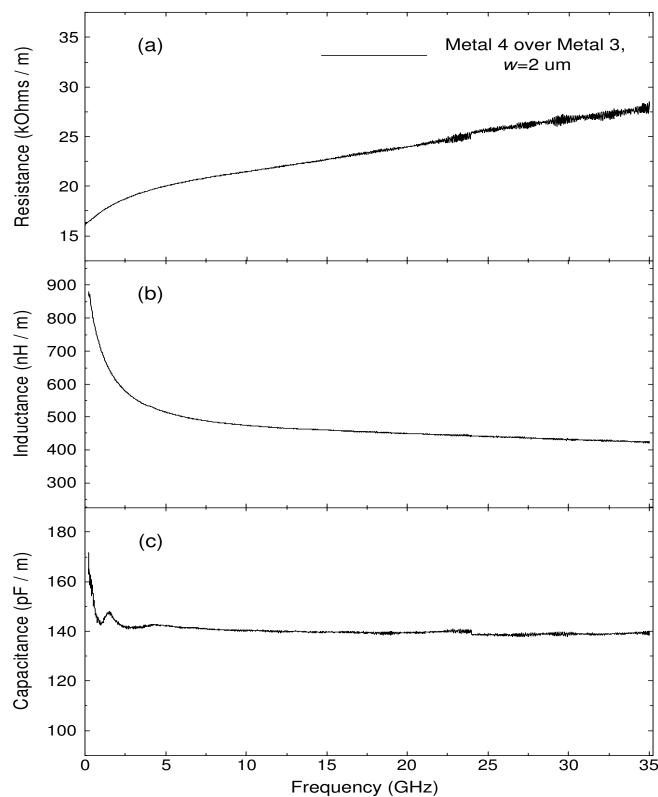


Figure B.3: (a) Resistance, (b) inductance, and (c) capacitance per-unit-length for the fabricated microstrip line Metal 4 over Metal 3, w=2 μm.

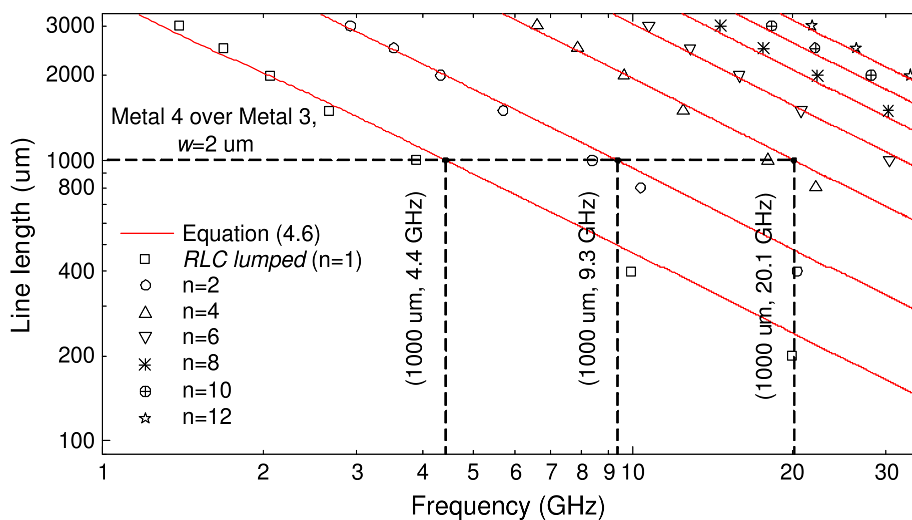


Figure B.4: *RLC lumped* and *RLC distributed* equivalent circuit model regions using 2, 4, 6, 8, 10 and 12 sections for interconnection lines Metal 4 over Metal 3, w=2 μm.

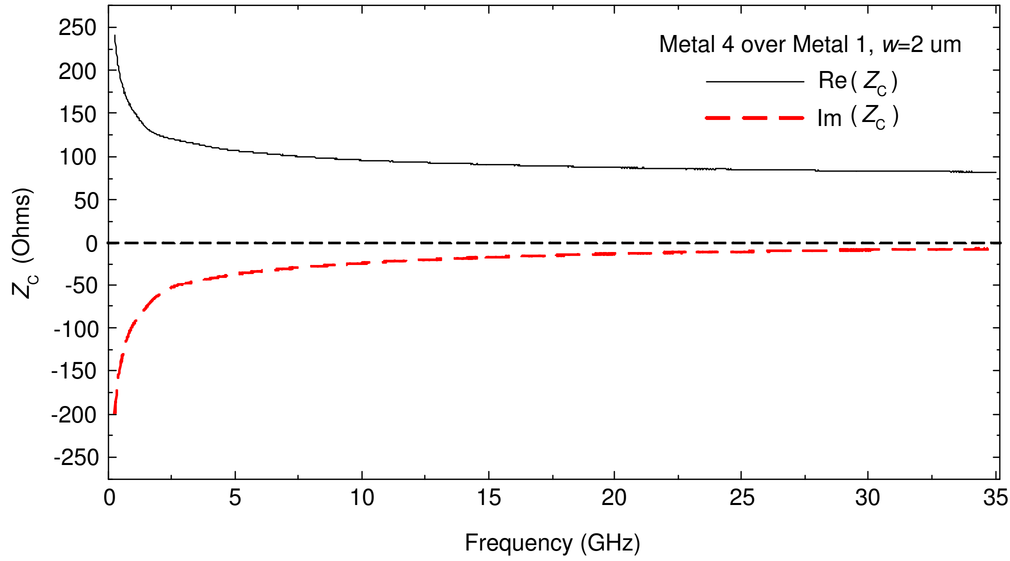


Figure B.5: Experimental characteristic impedance for the fabricated microstrip line Metal 4 over Metal 1, w=2 μm.

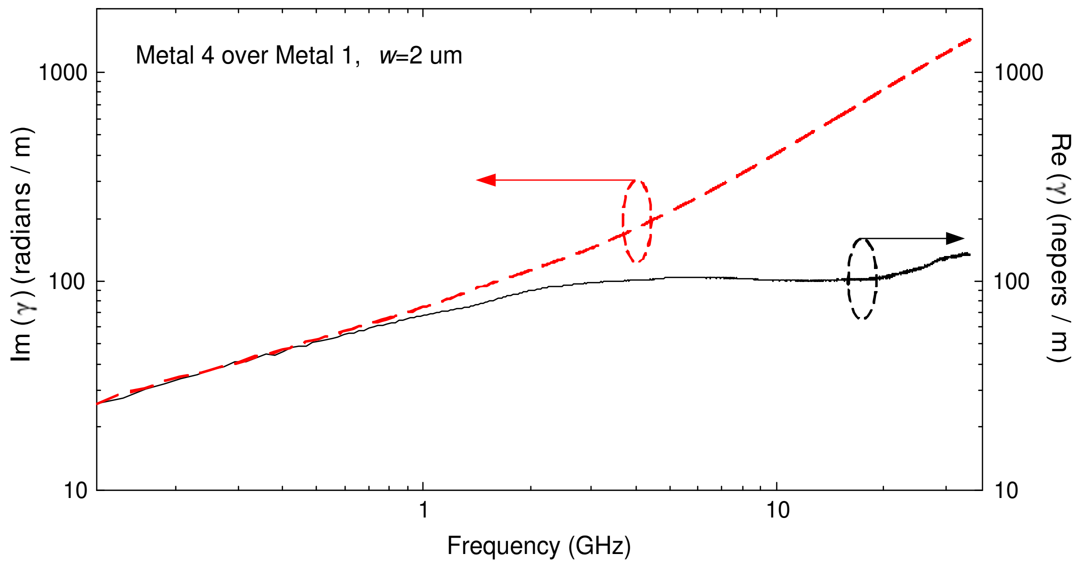


Figure B.6: Experimental propagation constant for the fabricated microstrip line Metal 4 over Metal 1, w=2 μm.

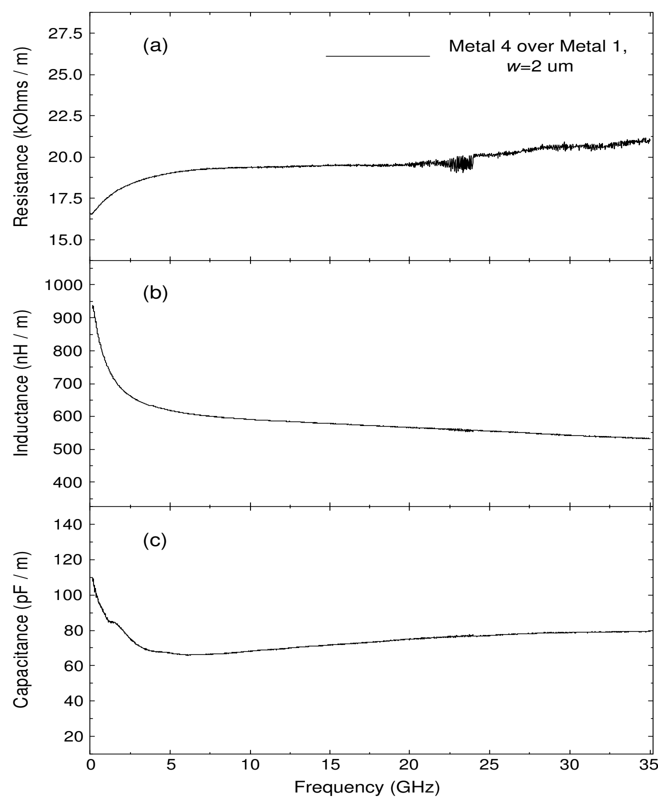


Figure B.7: (a) Resistance, (b) inductance, and (c) capacitance per-unit-length for the fabricated microstrip line Metal 4 over Metal 1, w=2 μm.

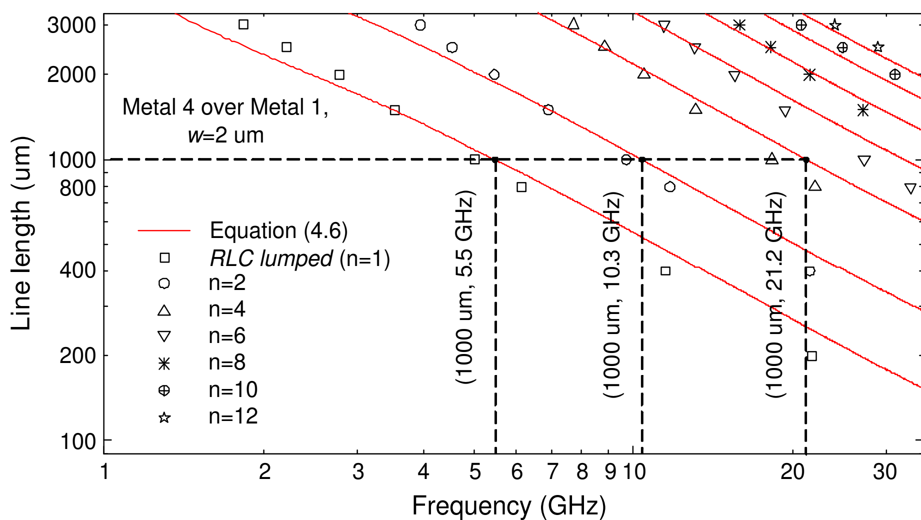


Figure B.8: *RLC lumped* and *RLC distributed* equivalent circuit model regions using 2, 4, 6, 8, 10 and 12 sections for interconnection lines Metal 4 over Metal 1, w=2 μm.

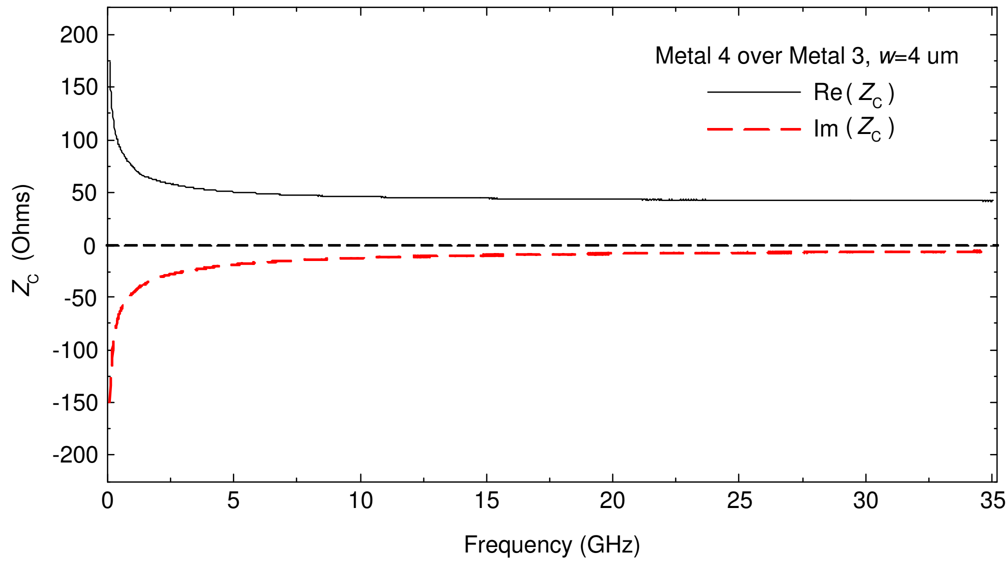


Figure B.9: Experimental characteristic impedance for the fabricated microstrip line Metal 4 over Metal 3, w=4 μm.

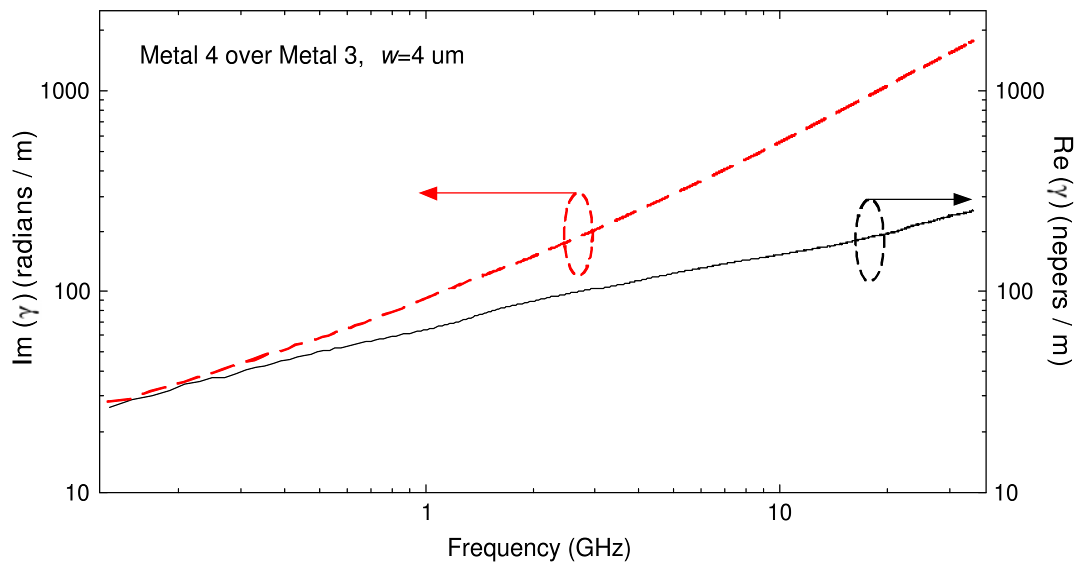


Figure B.10: Experimental propagation constant for the fabricated microstrip line Metal 4 over Metal 3, w=4 μm.

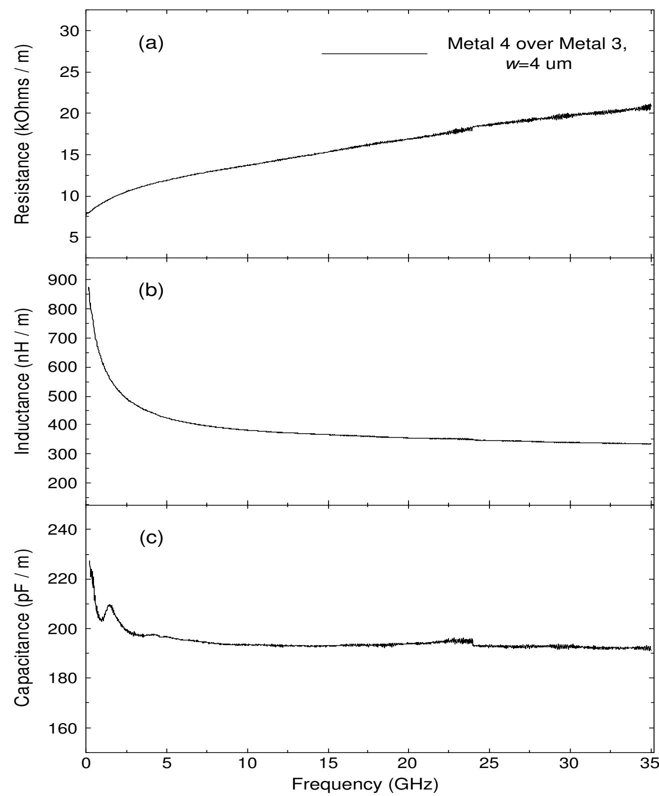


Figure B.11: (a) Resistance, (b) inductance, and (c) capacitance per-unit-length for the fabricated microstrip line Metal 4 over Metal 3, w=4 μm.

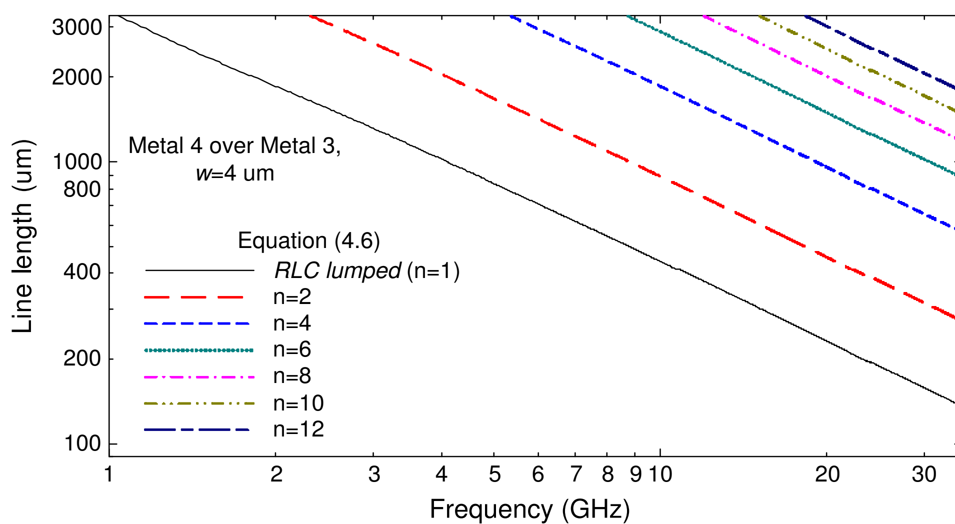


Figure B.12: *RLC lumped* and *RLC distributed* equivalent circuit model regions using 2, 4, 6, 8, 10 and 12 sections for interconnection lines Metal 4 over Metal 3, w=4 μm.

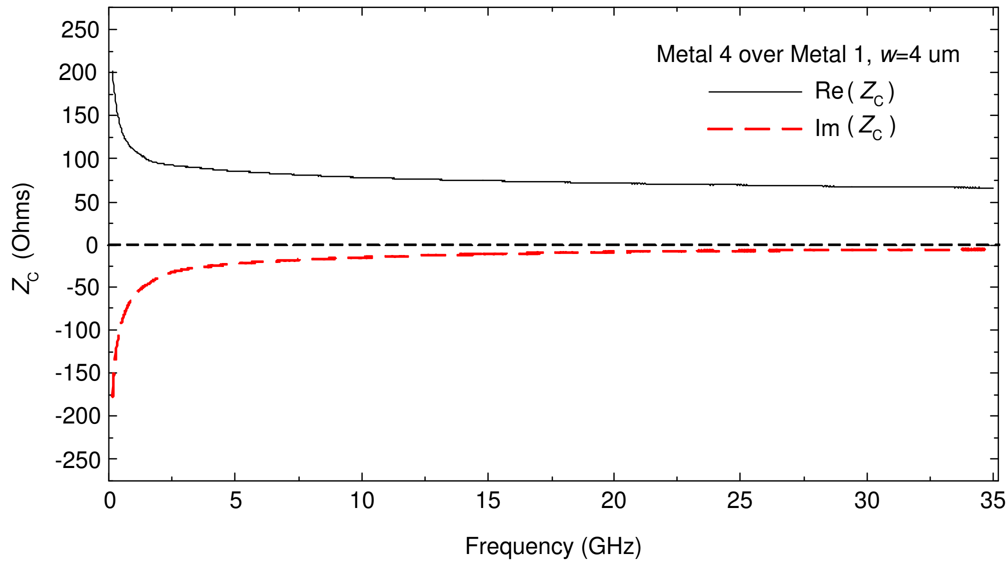


Figure B.13: Experimental characteristic impedance for the fabricated microstrip line Metal 4 over Metal 1, w=4 μm.

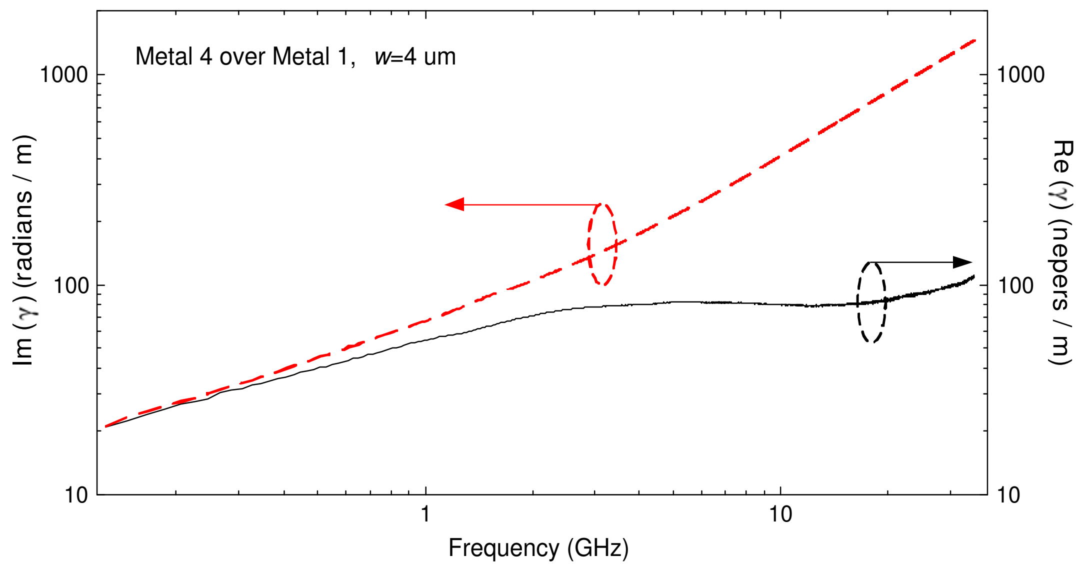


Figure B.14: Experimental propagation constant for the fabricated microstrip line Metal 4 over Metal 1, w=4 μm.

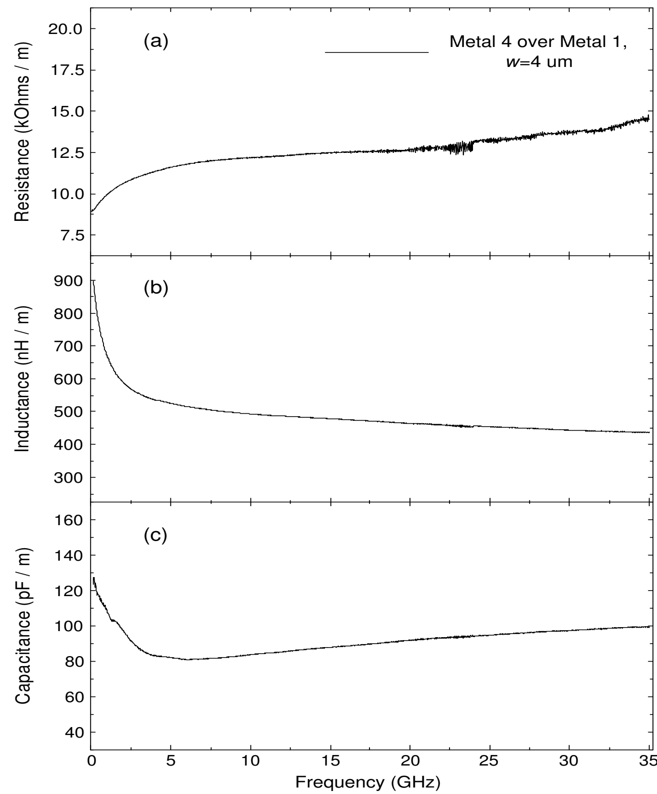


Figure B.15: (a) Resistance, (b) inductance, and (c) capacitance per-unit-length for the fabricated microstrip line Metal 4 over Metal 1, w=4 μm.

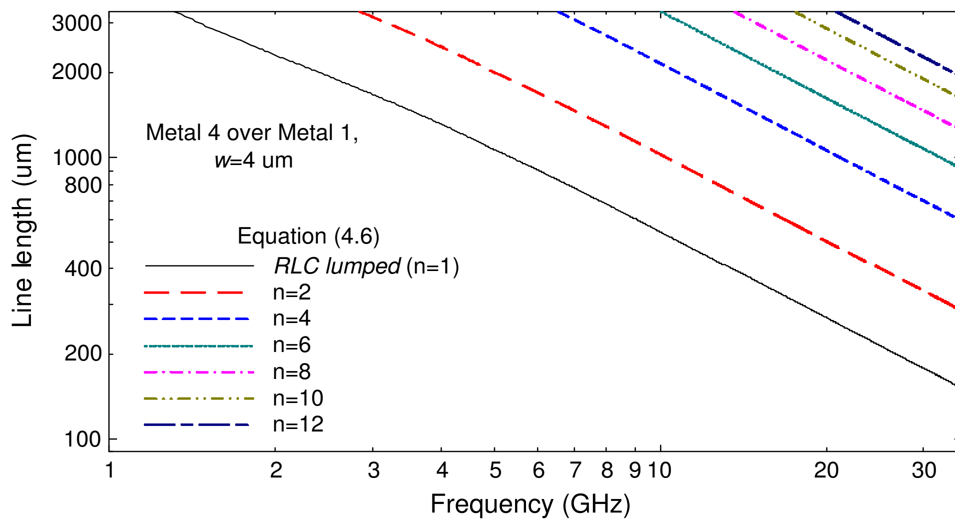


Figure B.16: *RLC lumped* and *RLC distributed* equivalent circuit model regions using 2, 4, 6, 8, 10 and 12 sections for interconnection lines Metal 4 over Metal 1, w=4 μm.

B.1 Technology Scaling

In this section, the interconnect modeling methodology is applied to an interconnection line designed using the 8 Metal TSMC (Taiwan Semiconductor Manufacturing Company) 0.13 μm process. Figure B.17 shows the simplified structure of a microstrip line implemented in the Metal 8 level using the Metal 7 as a ground plane, where w, t and l are the width, thickness, and length of the interconnection, respectively; h and gnd are the thicknesses of the inter-metal dielectric and the ground plane, respectively. Table B.1 shows the thickness for different metal and inter-metal dielectric levels available in TSMC 0.13 μm process.

In order to perform the extraction of R_l, L_l, and C_l parameters associated with the analyzed interconnection line, the corresponding S-parameters are obtained from 0.01 to 35 GHz using an electromagnetic simulator (Advanced Design System), where it is necessary to specify: a) the geometric structure of the interconnection line, inter-metal layer, and ground plane (i.e. width, thickness, length, height, etc.); and b) the properties of the materials used to fabricate the metal and inter-metal layers.

Firstly, from the S-parameters, the values of Z_C and γ are determined using equations 3.21 and 3.22. Figures B.18 and B.19 show the extracted Z_C and γ for a Metal 4 over Metal 3, w=2 μm interconnection line, respectively. Then, after determining Z_C and γ, the values for R_l, L_l, C_l parameters associated with the studied interconnection are directly obtained from equations 3.18, 3.19, 3.20, respectively. Figure B.20 shows the values for R_l, L_l, and C_l for the Metal 8 over Metal 7, w=4 μm interconnection line.

Once that electrical parameters of the interconnect have been obtained, the determination of the minimum number of sections required in the equivalent circuit for accurate representation of interconnects of certain lengths within specific frequency ranges is carried out by applying the modeling procedure described in Chapter 4. Figure B.21 shows the combination of l and f for which the Metal 8 over Metal 7, w=4 μm interconnection can be represented by an *RLC lumped* model and when can be represented by an *RLC distributed* equivalent circuit model implemented

with n=2, 4, 6, 8, and 10 sections. For example, consider an interconnection line with l=1000 μm; this line can be modeled by an *RLC lumped* equivalent circuit only up to about 4.8 GHz as can be seen in Fig. B.21. Now, if the same interconnection is modeled by an *RLC distributed* equivalent circuit implemented with 2 sections, the delay and losses associated with the line can be accurately represented up to 9.8 GHz. Finally, when the same *RLC distributed* equivalent circuit is implemented with 4 sections, the interconnection line under study can be adequately represented up to 20.1 GHz.

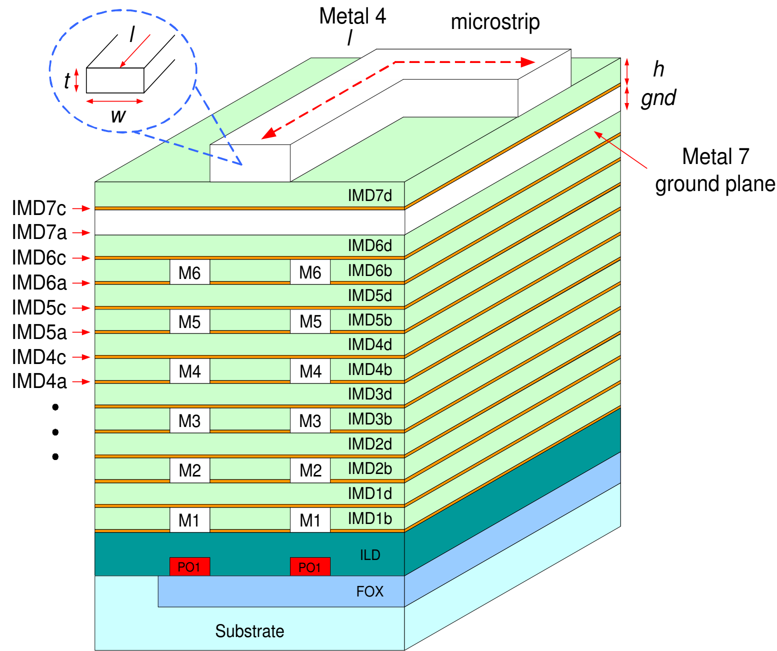


Figure B.17: Simplified structure of a typical on-chip microstrip interconnection implemented in TSMC 0.13 μm process.

Table B.1: TSMC 0.13 μm process parameters.

Parameter	Thickness (nm)	Parameter	Oxide Thickness (nm)
Metal 8	3300	IMD8: a, b	140, 3040
Metal 7	830	IMD7: a, b, c, d	30, 700, 50, 720
Metal 6	370	IMD6: a, b, c, d	30, 250, 50, 720
Metal 5	370	IMD5: a, b, c, d	30, 250, 50, 490
Metal 4	370	IMD4: a, b, c, d	30, 250, 50, 490
Metal 3	370	IMD3: a, b, c, d	30, 250, 50, 490
Metal 2	370	IMD2: a, b, c, d	30, 250, 50, 490
Metal 1	260	IMD1: a, b, c, d	30, 170, 50, 490

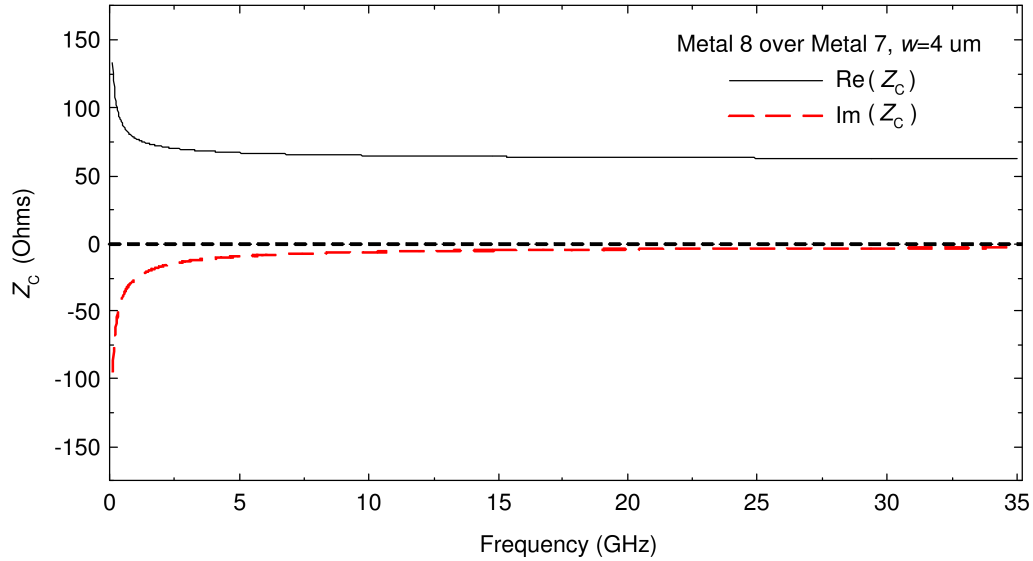


Figure B.18: Simulated characteristic impedance for the microstrip line Metal 8 over Metal 7, w=4 μm.

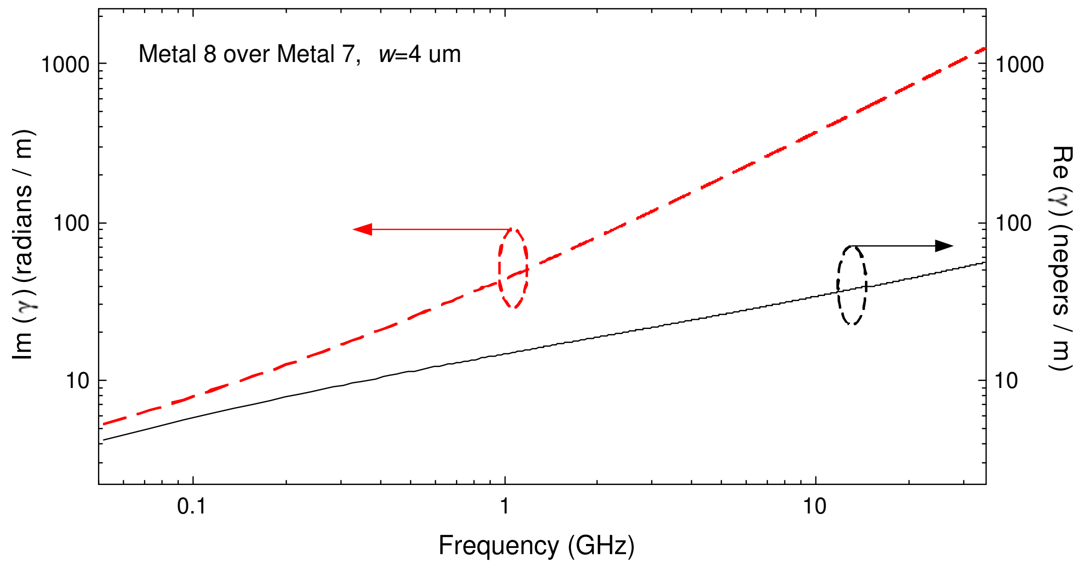


Figure B.19: Simulated propagation constant for the microstrip line Metal 8 over Metal 7, w=4 μm.

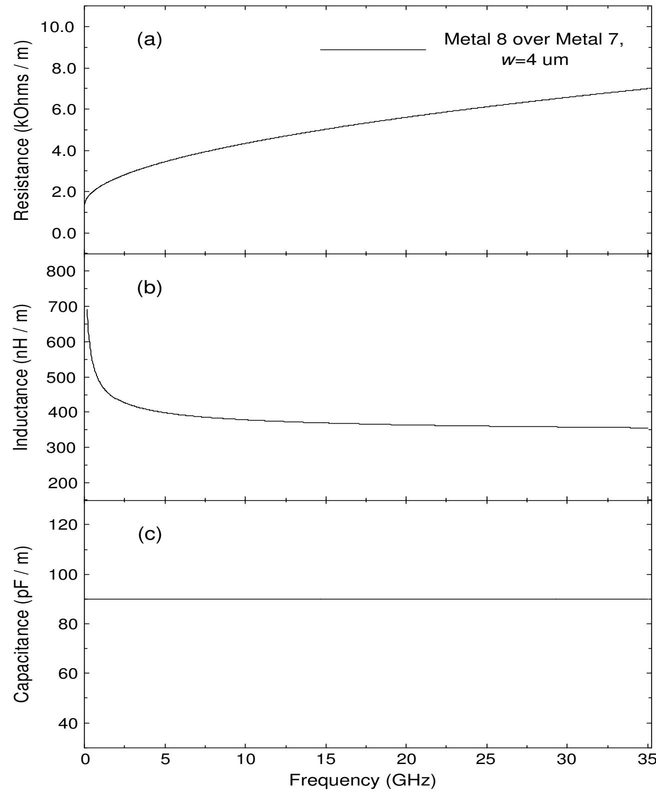


Figure B.20: (a) Resistance, (b) inductance, and (c) capacitance per-unit-length for the microstrip line Metal 8 over Metal 7, w=4 μm.

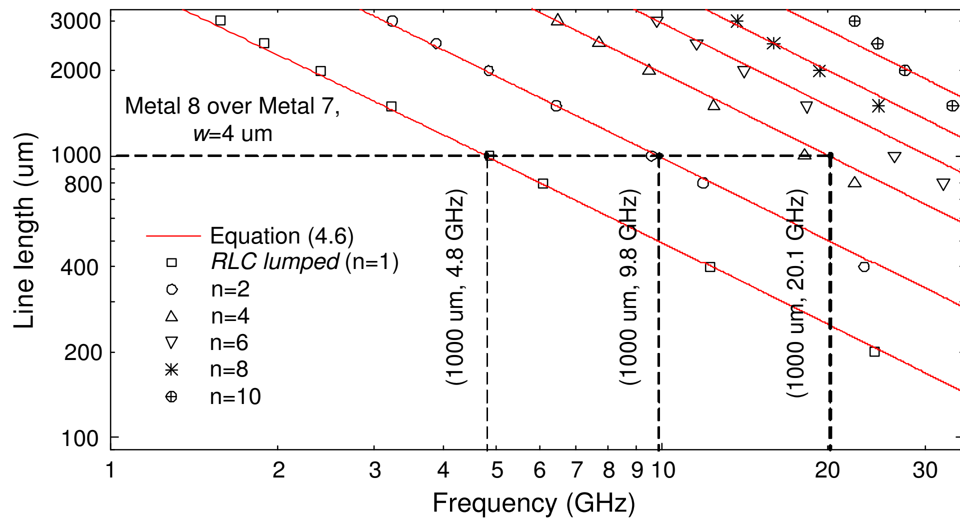


Figure B.21: *RLC lumped* and *RLC distributed* equivalent circuit model regions using 2, 4, 6, 8, and 10 sections for interconnection lines Metal 8 over Metal 7, w=4 μm.

Appendix C

Fabricated Ring Oscillators

In this appendix, a summary of the features and performance of the fabricated three-stage ring oscillators is shown. The oscillators are designed and fabricated using the Austriamicrosystems 0.35 μm process, a power supply of 3.3 V, and the Metal 4 level for the interconnection lines.

For each one of the implemented oscillators, the following items are presented:

- A table containing the performance summary.
- The schematic, layout, and photograph.
- The simulated transient response.
- The experimental *Off-chip* transient response.
- The experimental *On-chip* output spectrum.
- The schematic of the gain stages, dividers, buffers.

Table C.1: Performance summary of the fabricated three-stage ring oscillator using interconnection lines with l=70 μm.

Process Technology	AMS 0.35 μm
Oscillator Type	Single-ended
Power supply voltage (V)	3.3
Interconnection width (μm)	2
Interconnection length (μm) l_1=l_2=l_3	70
Dividers for *Off-chip* measurements	8
Dividers for *On-chip* measurements	1
Operating frequency *OUT* (GHz)	2.58
Output voltage *OUT* (V)	3.06
Power consumption (mW)	33.25
Coverage area (mm x mm)	0.07 x 0.07

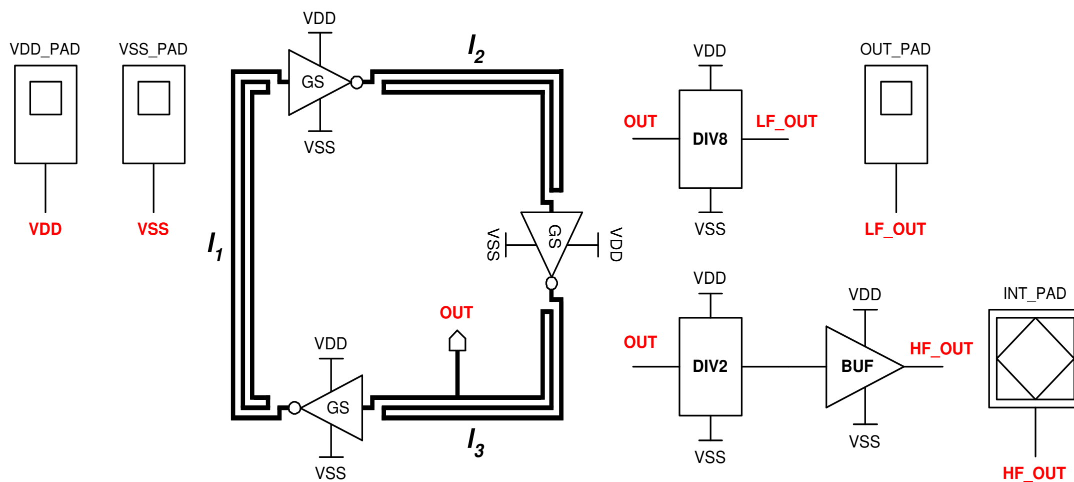


Figure C.1: Schematic of the three-stage ring oscillator using interconnection lines with l=70 μm.

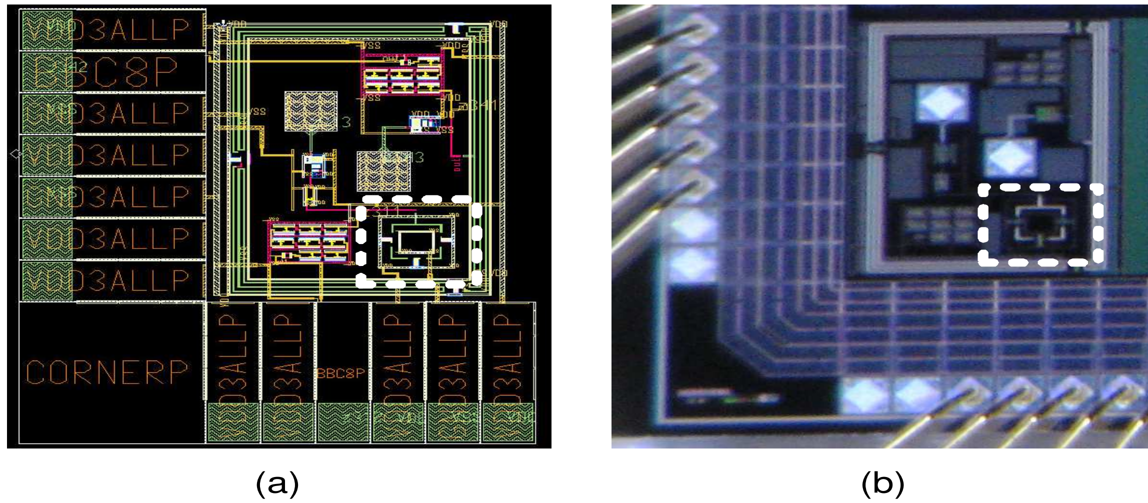


Figure C.2: Three-stage ring oscillator using interconnection lines with l=70 μm: (a) Layout. (b) Photograph.

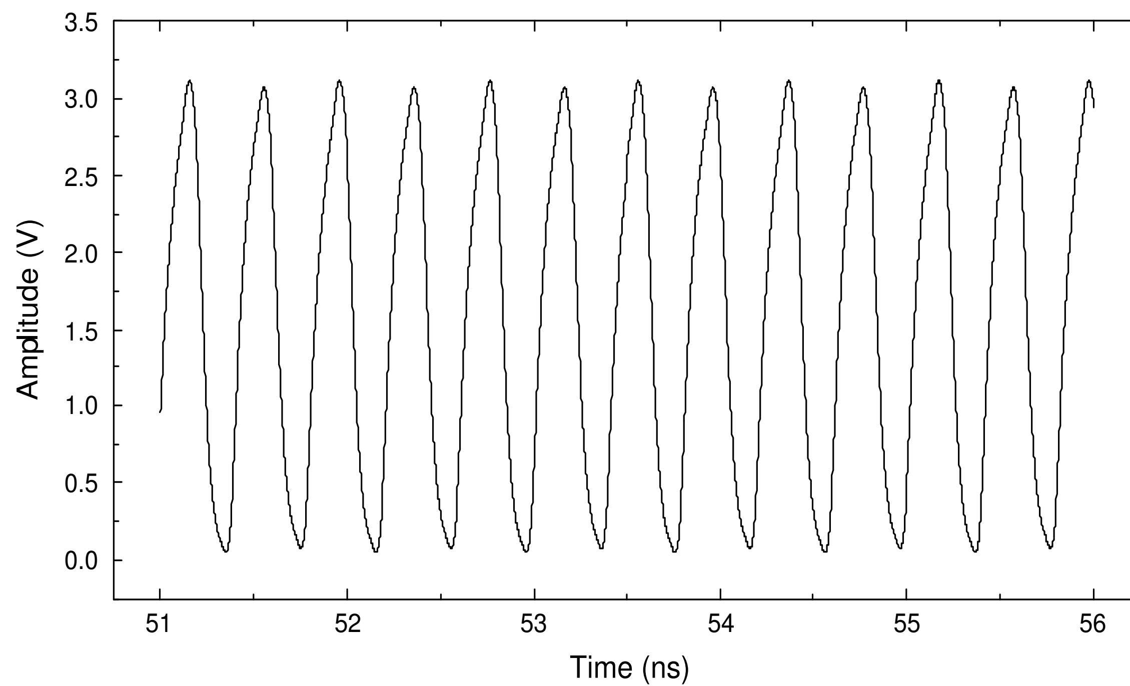


Figure C.3: Simulated transient response of the three-stage ring oscillator using interconnection lines with l=70 μm.

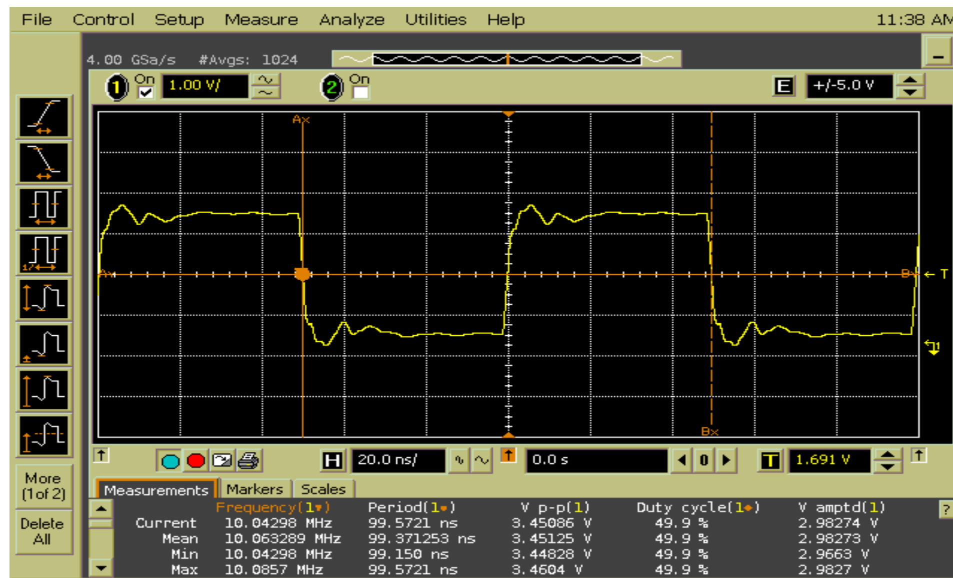


Figure C.4: Measured *Off-chip* transient response of the three-stage ring oscillator using interconnection lines with l=70 μm.

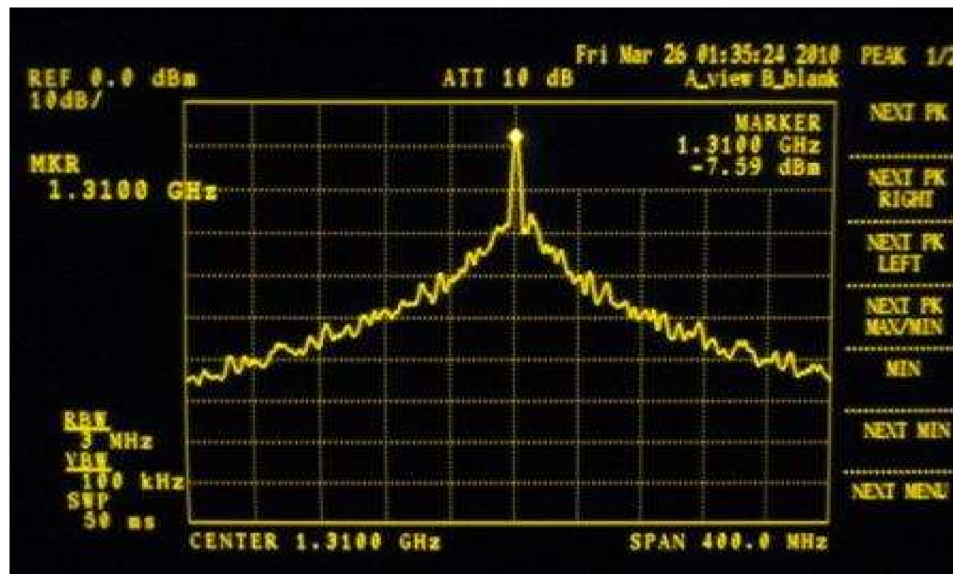


Figure C.5: Measured *On-chip* output spectrum of the three-stage ring oscillator using interconnection lines with l=70 μm.

Table C.2: Performance summary of the fabricated three-stage ring oscillator using interconnection lines with l=1000 μm.

Process Technology	AMS 0.35 μm
Oscillator Type	Single-ended
Power supply voltage (V)	3.3
Interconnection width (μm)	2
Interconnection length (μm) l_1=l_2=l_3	1000
Dividers for *Off-chip* measurements	8
Dividers for *On-chip* measurements	1
Operating frequency *OUT* (GHz)	2.14
Output voltage *OUT* (V)	3.12
Power consumption (mW)	31.34
Coverage area (mm x mm)	0.75 x 0.75

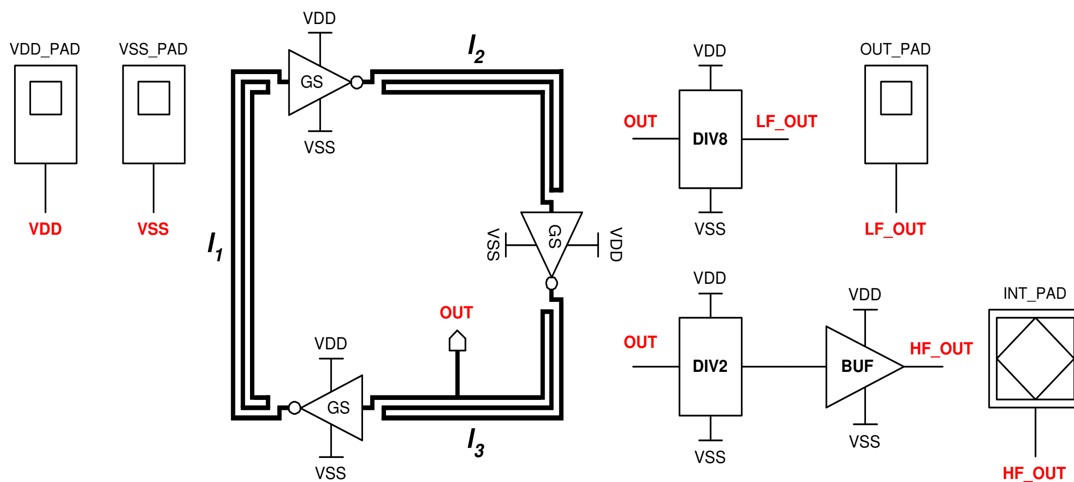


Figure C.6: Schematic of the three-stage ring oscillator using interconnection lines with l=1000 μm.

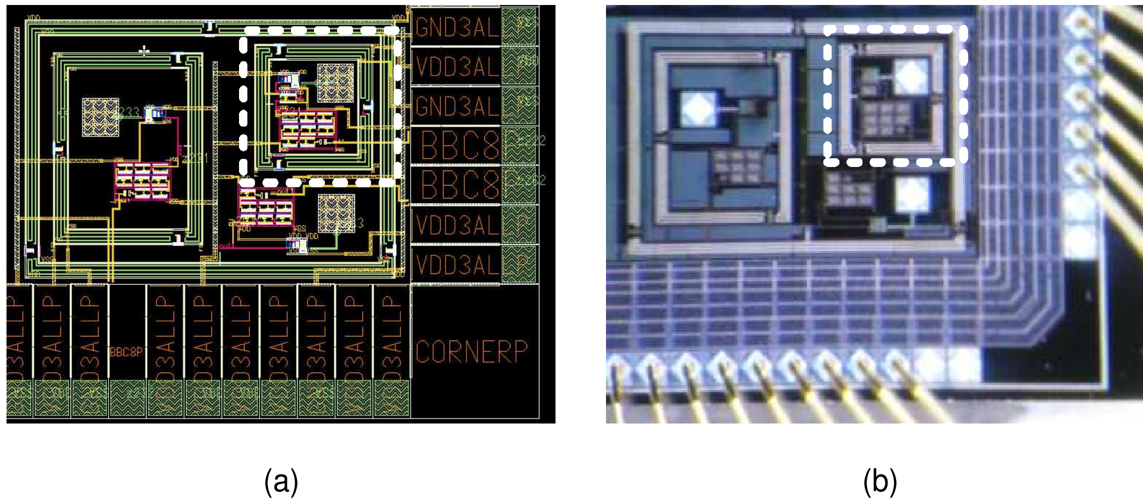


Figure C.7: Three-stage ring oscillator using interconnection lines with l=1000 μm: (a) Layout. (b) Photograph.

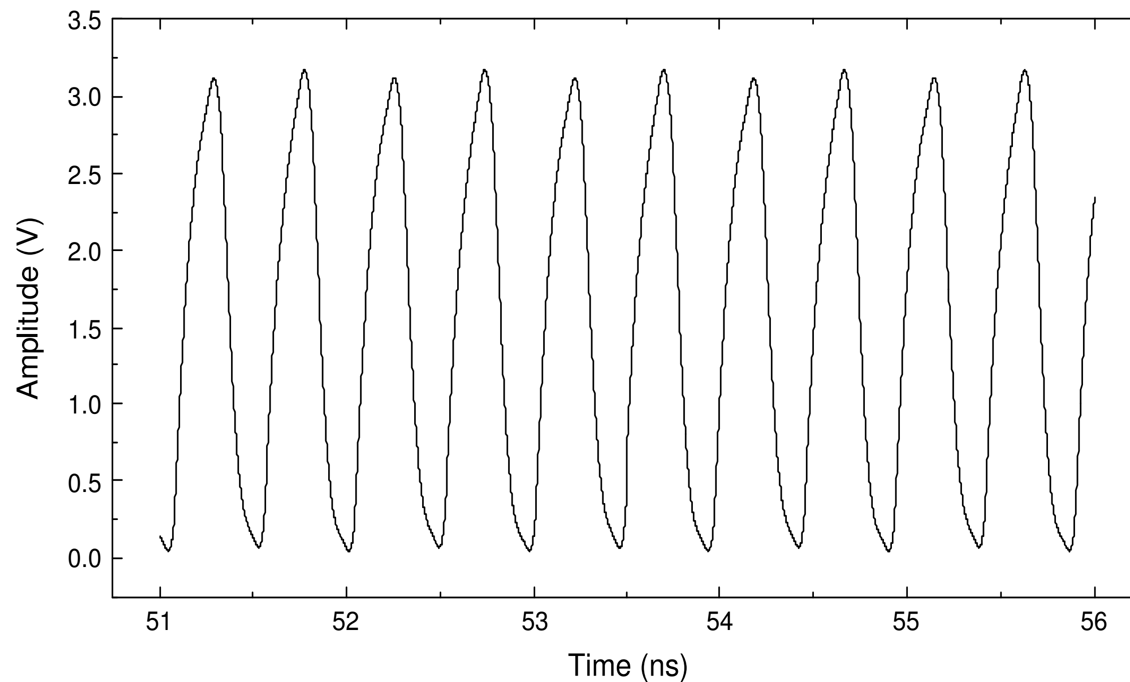


Figure C.8: Simulated transient response of the three-stage ring oscillator using interconnection lines with l=1000 μm.

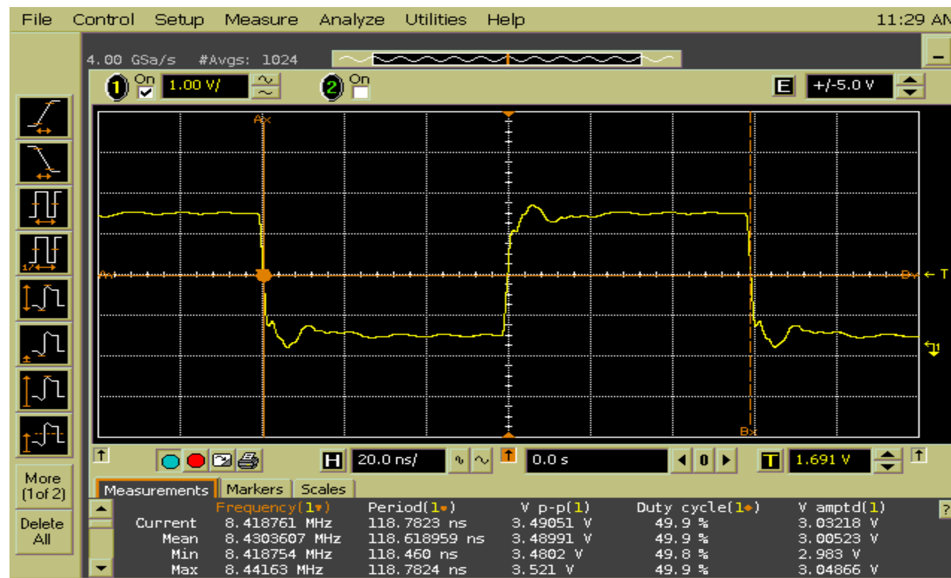


Figure C.9: Measured *Off-chip* transient response of the three-stage ring oscillator using interconnection lines with l=1000 μm.

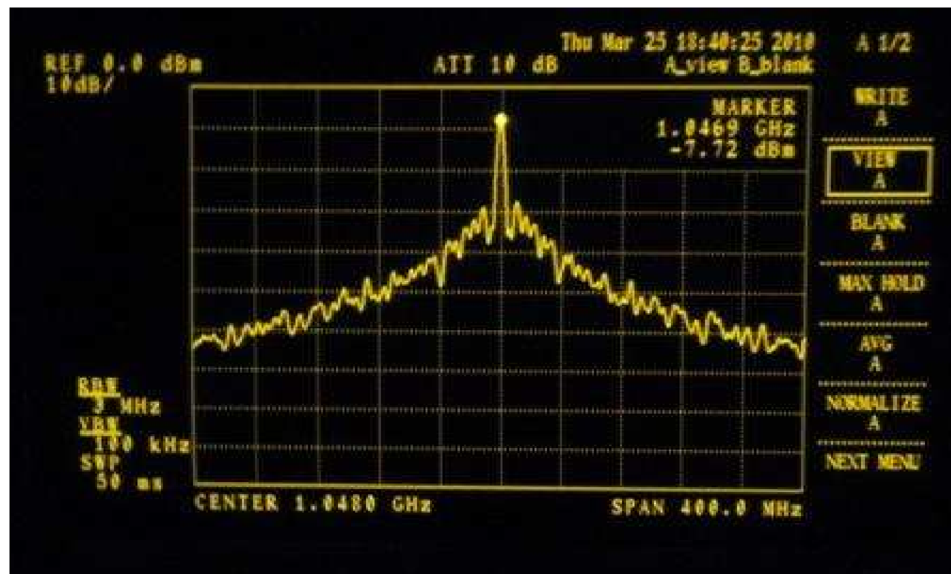


Figure C.10: Measured *On-chip* output spectrum of the three-stage ring oscillator using interconnection lines with l=1000 μm.

Table C.3: Performance summary of the fabricated three-stage ring oscillator using interconnection lines with l=1500 μm.

Process Technology	AMS 0.35 μm
Oscillator Type	Single-ended
Power supply voltage (V)	3.3
Interconnection width (μm)	2
Interconnection length (μm) l_1=l_2=l_3	1500
Dividers for *Off-chip* measurements	8
Dividers for *On-chip* measurements	0
Operating frequency *OUT* (GHz)	2.00
Output voltage *OUT* (V)	3.16
Power consumption (mW)	30.42
Coverage area (mm x mm)	1.125 x 1.125

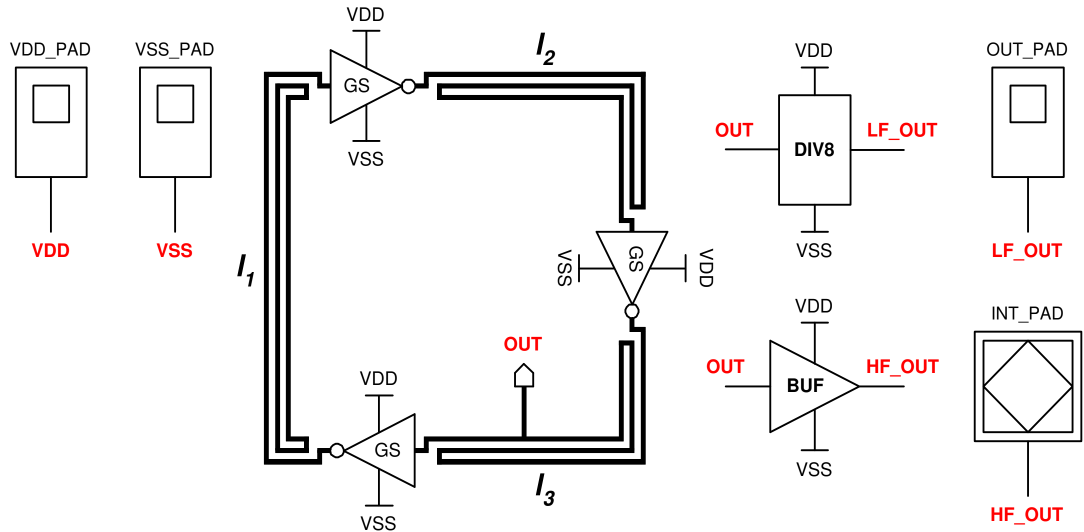


Figure C.11: Schematic of the three-stage ring oscillator using interconnection lines with l=1500 μm.

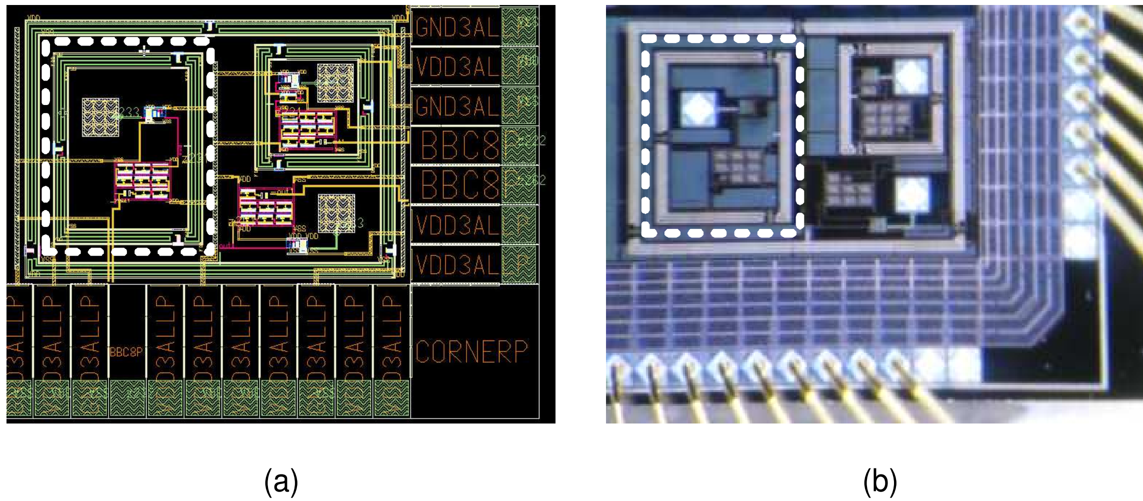


Figure C.12: Three-stage ring oscillator using interconnection lines with l=1500 μm: (a) Layout. (b) Photograph.

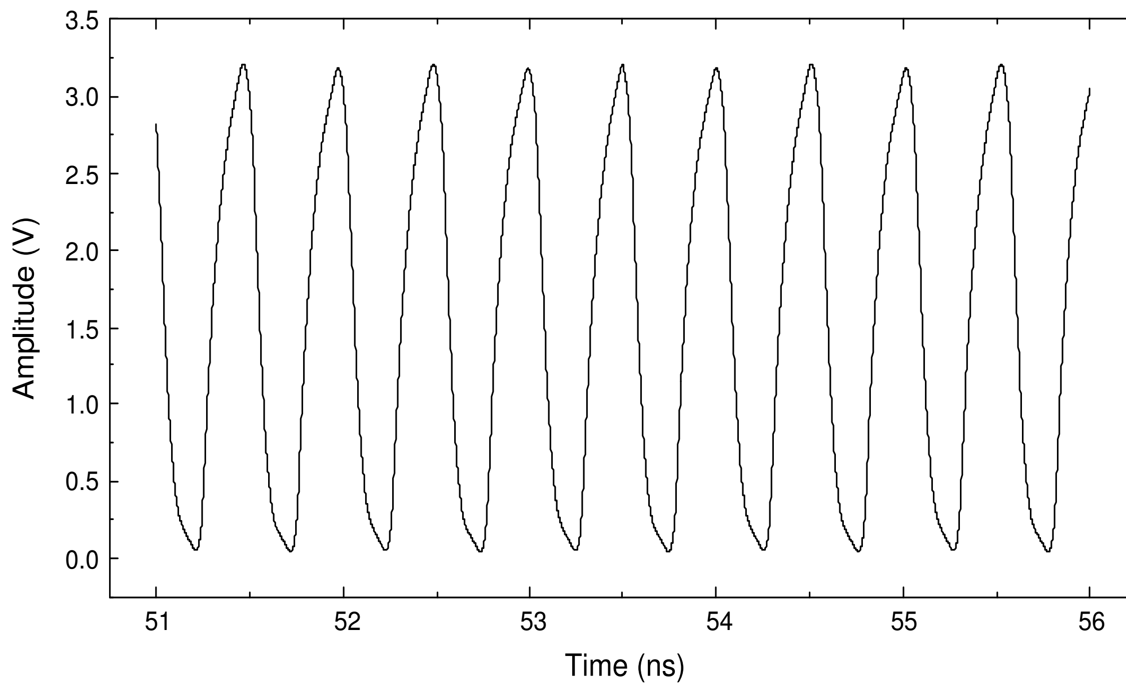


Figure C.13: Simulated transient response of the three-stage ring oscillator using interconnection lines with l=1500 μm.

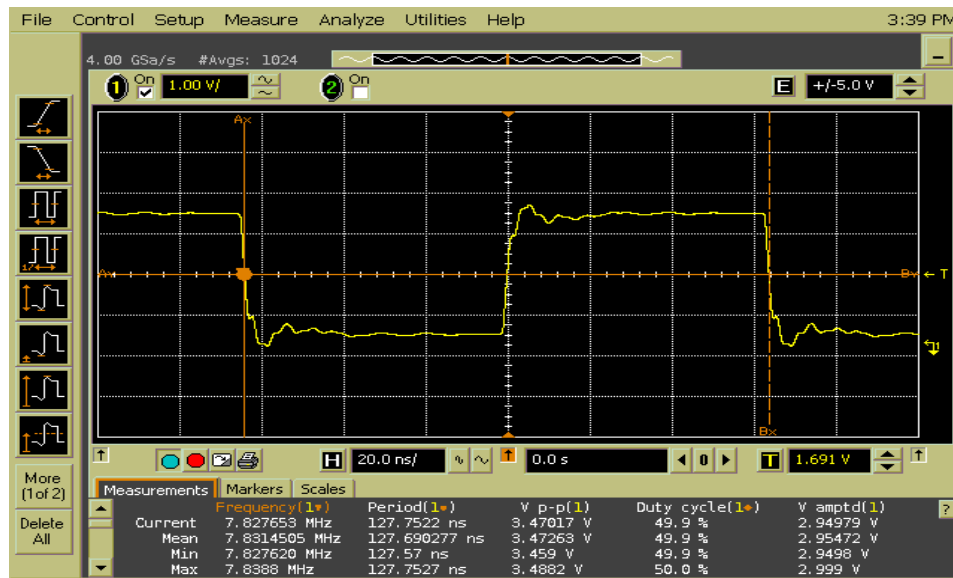


Figure C.14: Measured *Off-chip* transient response of the three-stage ring oscillator using interconnection lines with l=1500 μm.

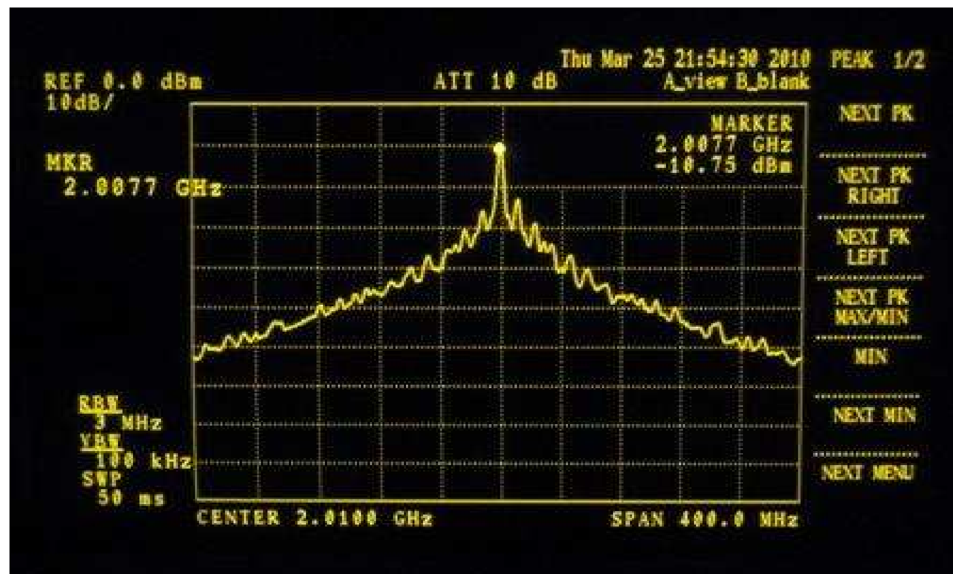


Figure C.15: Measured *On-chip* output spectrum of the three-stage ring oscillator using interconnection lines with l=1500 μm.

Table C.4: Performance summary of the fabricated three-stage ring oscillator using interconnection lines with l=2000 μm.

Process Technology	AMS 0.35 μm
Oscillator Type	Single-ended
Power supply voltage (V)	3.3
Interconnection width (μm)	2
Interconnection length (μm) l_1=l_2=l_3	2000
Dividers for *Off-chip* measurements	7
Dividers for *On-chip* measurements	0
Operating frequency *OUT* (GHz)	1.84
Output voltage *OUT* (V)	3.18
Power consumption (mW)	29.61
Coverage area (mm x mm)	1.5 x 1.5

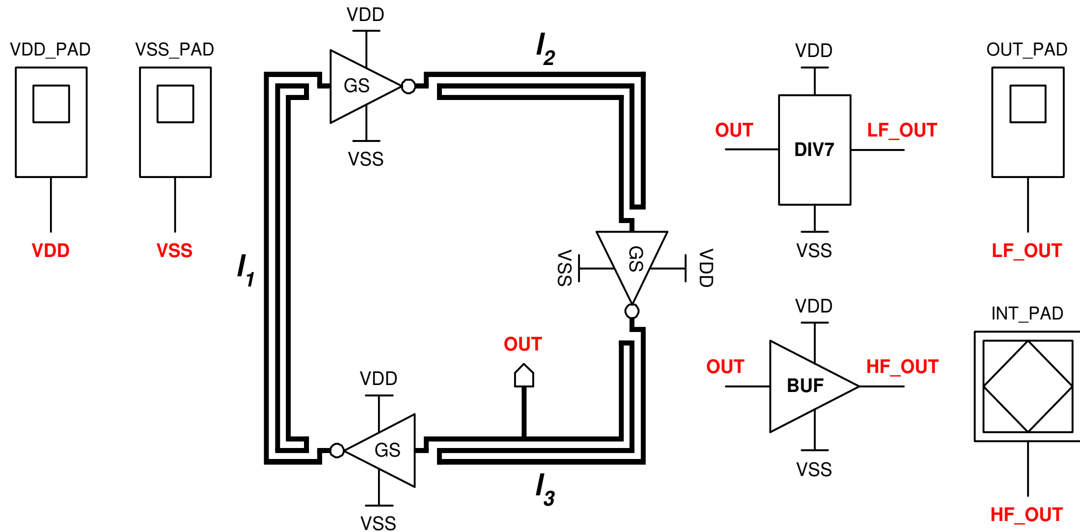


Figure C.16: Schematic of the three-stage ring oscillator using interconnection lines with l=2000 μm.

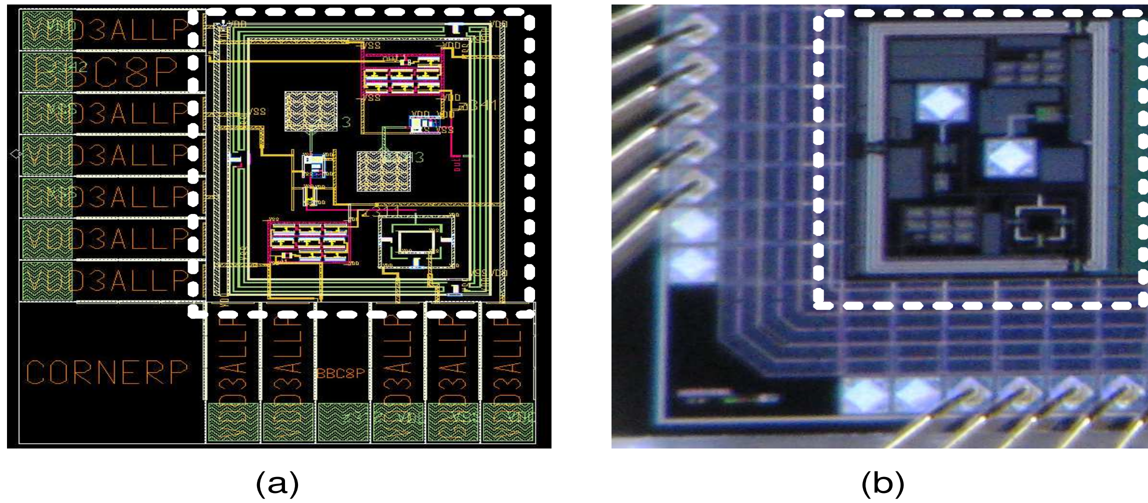


Figure C.17: Three-stage ring oscillator using interconnection lines with l=2000 μm: (a) Layout. (b) Photograph.

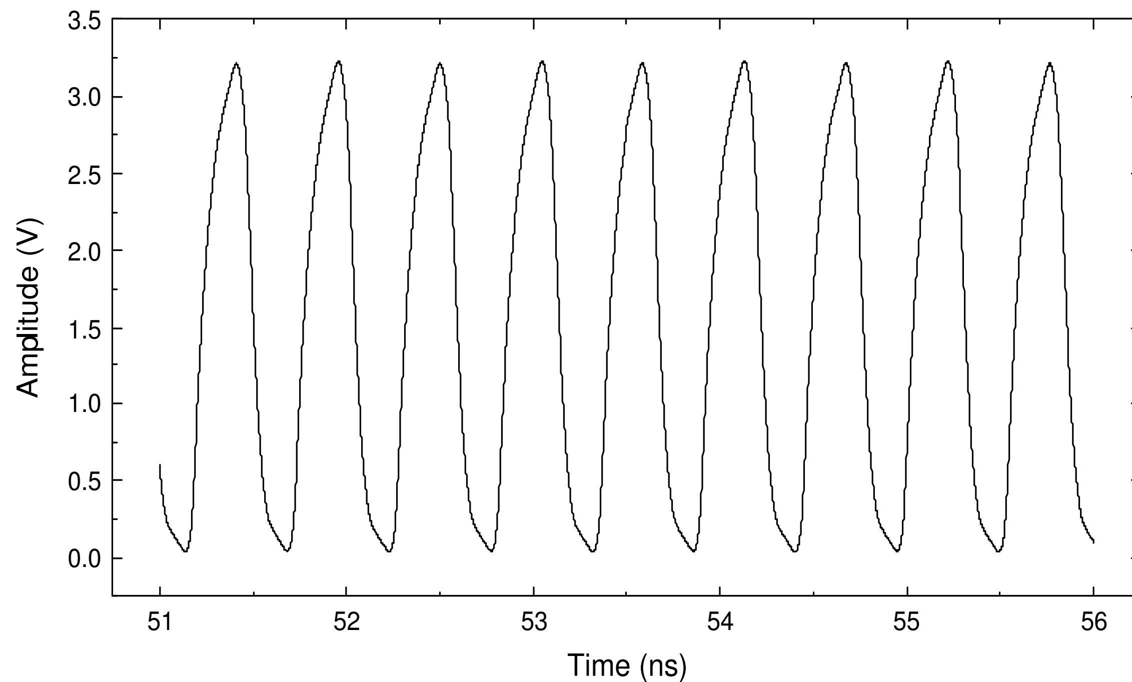


Figure C.18: Simulated transient response of the three-stage ring oscillator using interconnection lines with l=2000 μm.

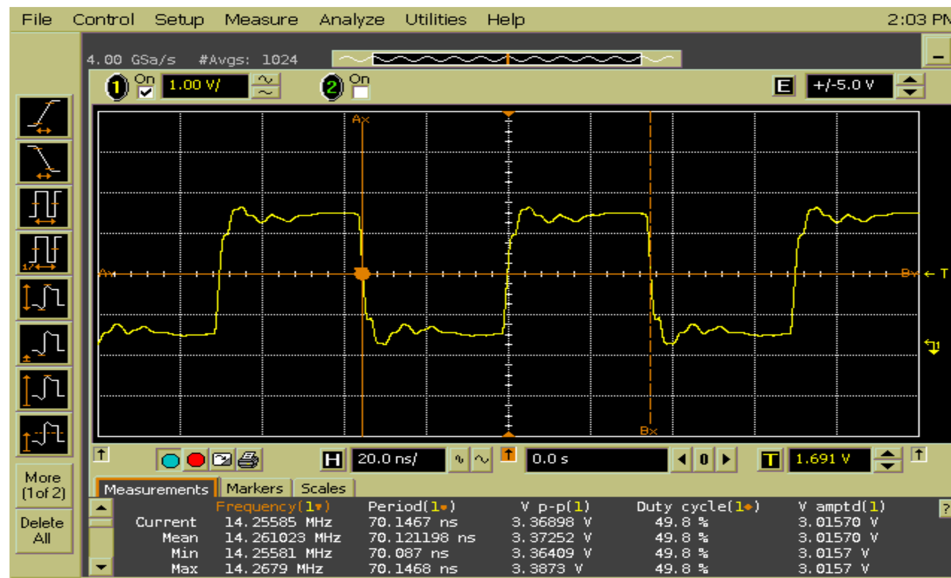


Figure C.19: Measured *Off-chip* transient response of the three-stage ring oscillator using interconnection lines with l=2000 μm.

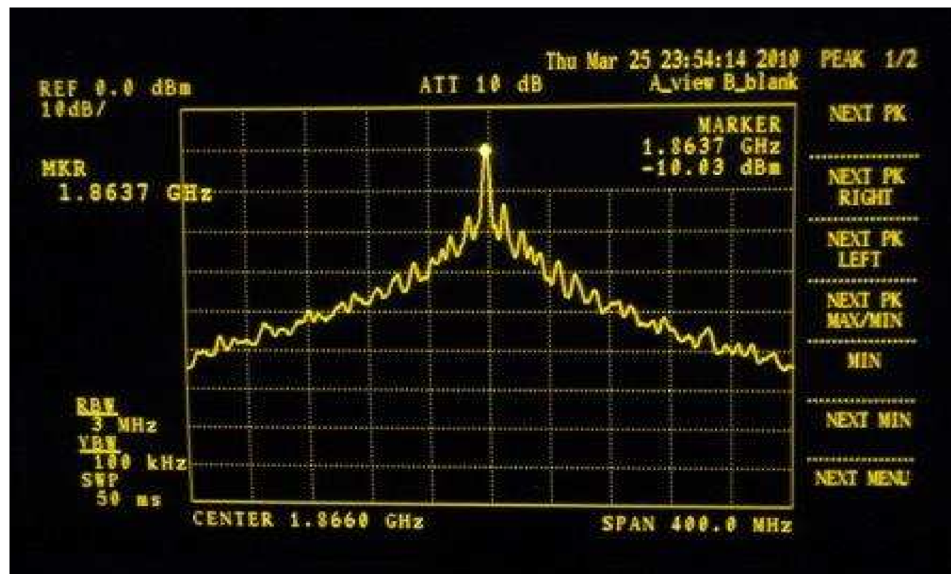


Figure C.20: Measured *On-chip* output spectrum of the three-stage ring oscillator using interconnection lines with l=2000 μm.

Table C.5: Performance summary of the fabricated three-stage ring oscillator using interconnection lines with l=3000 μm.

Process Technology	AMS 0.35 μm
Oscillator Type	Single-ended
Power supply voltage (V)	3.3
Interconnection width (μm)	2
Interconnection length (μm) l_1=l_2=l_3	3000
Dividers for *Off-chip* measurements	7
Dividers for *On-chip* measurements	0
Operating frequency *OUT* (GHz)	1.53
Output voltage *OUT* (V)	3.19
Power consumption (mW)	28.04
Coverage area (mm x mm)	2.25 x 2.25

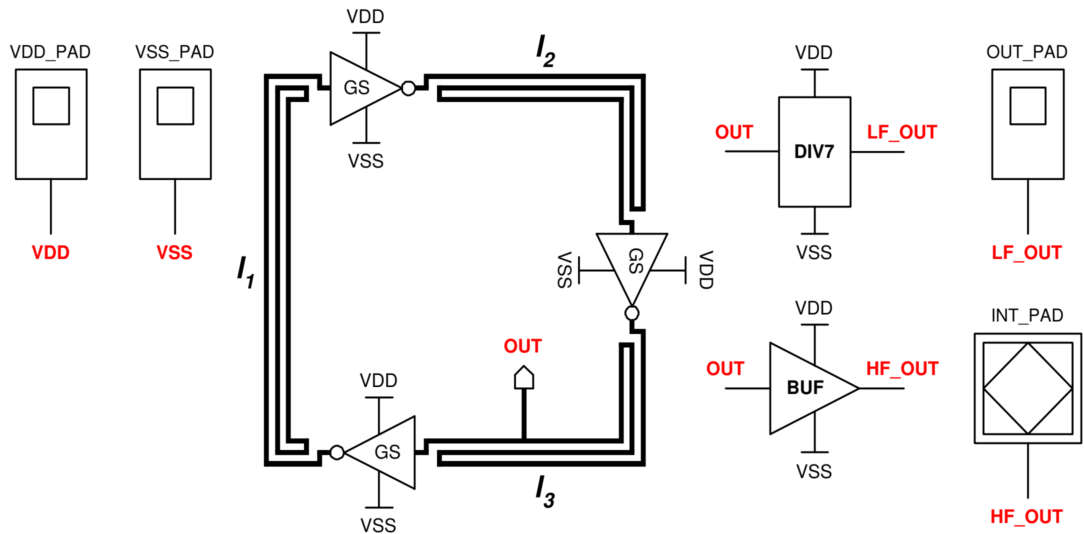


Figure C.21: Schematic of the three-stage ring oscillator using interconnection lines with l=3000 μm.

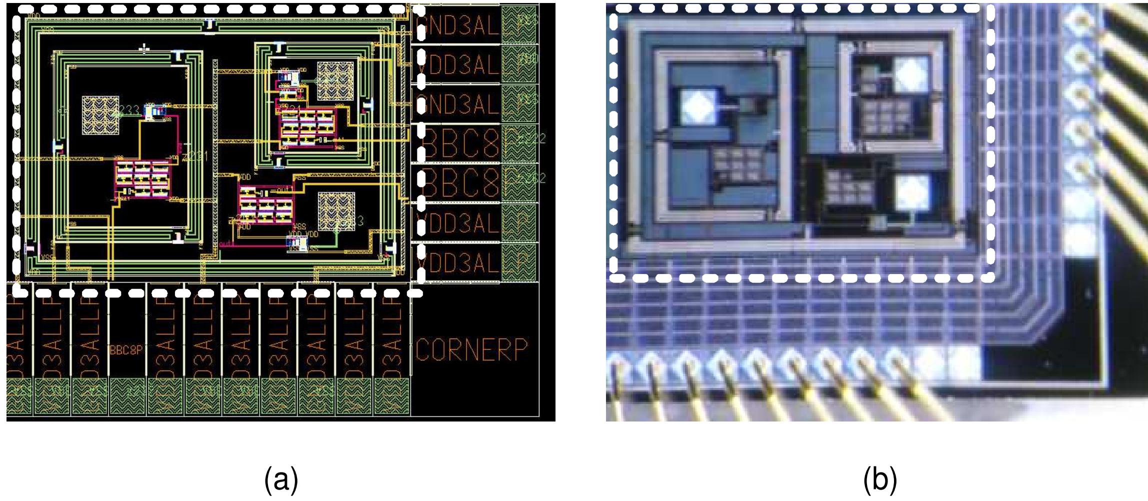


Figure C.22: Three-stage ring oscillator using interconnection lines with l=3000 μm: (a) Layout. (b) Photograph.

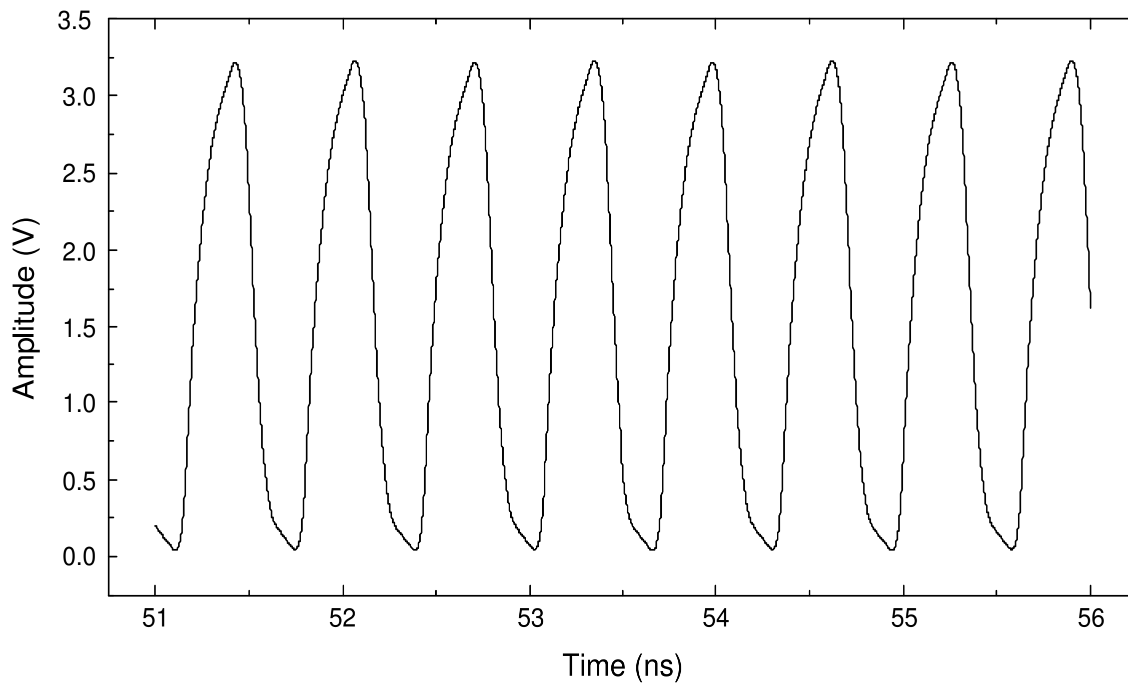


Figure C.23: Simulated transient response of the three-stage ring oscillator using interconnection lines with l=3000 μm.

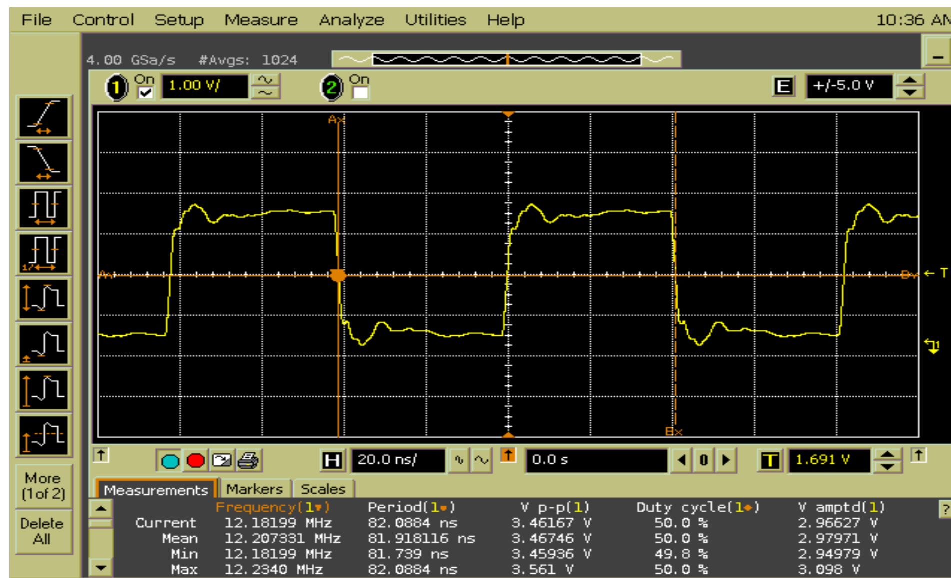


Figure C.24: Measured *Off-chip* transient response of the three-stage ring oscillator using interconnection lines with l=3000 μm.

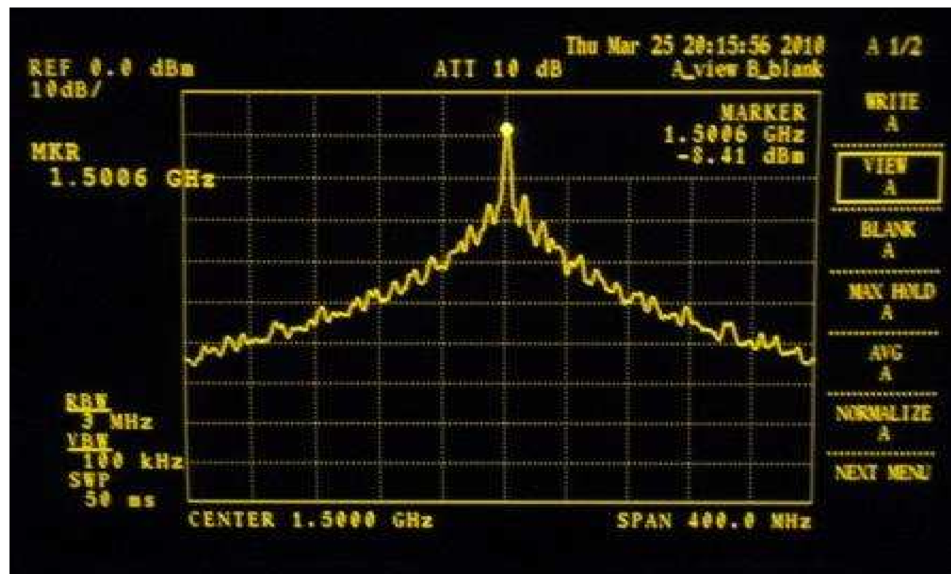
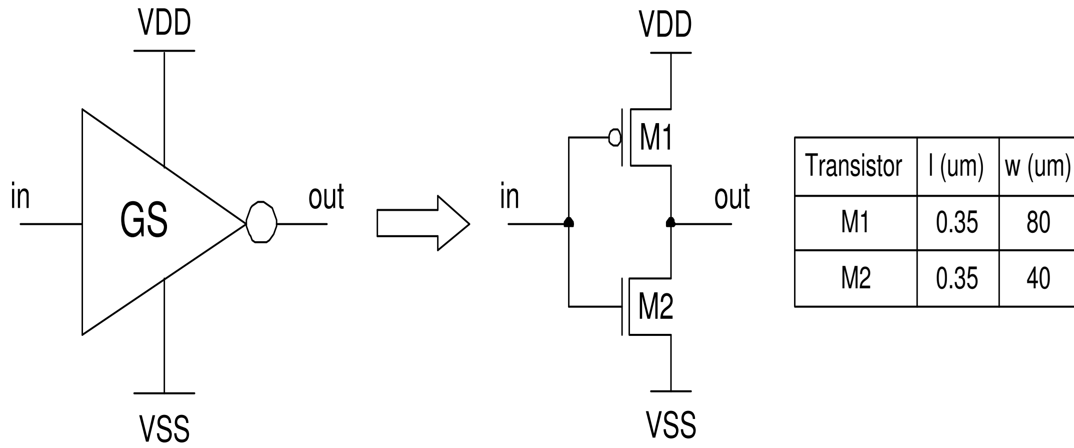
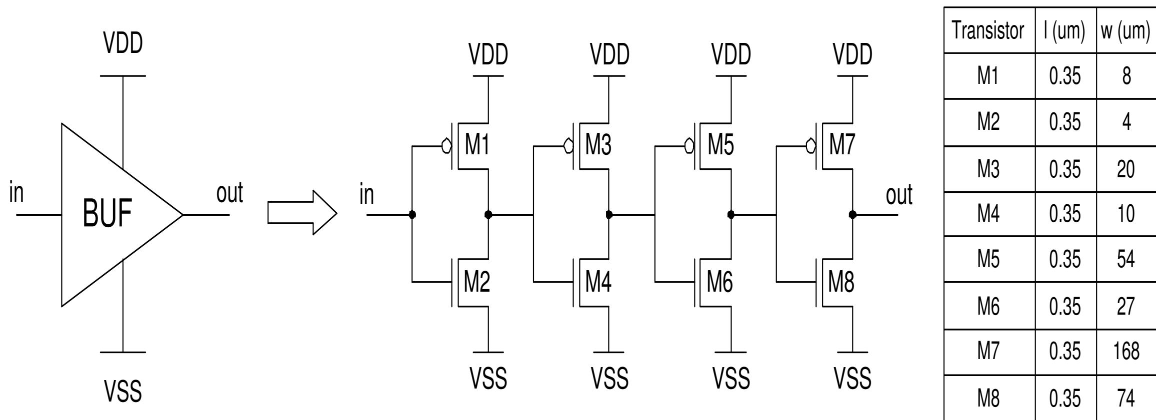


Figure C.25: Measured *On-chip* output spectrum of the three-stage ring oscillator using interconnection lines with l=3000 μm.



Transistor	l (um)	w (um)
M1	0.35	80
M2	0.35	40

Figure C.26: Schematic of the gain stage *GS*.



Transistor	l (um)	w (um)
M1	0.35	8
M2	0.35	4
M3	0.35	20
M4	0.35	10
M5	0.35	54
M6	0.35	27
M7	0.35	168
M8	0.35	74

Figure C.27: Schematic of the high-frequency buffer *BUF*.

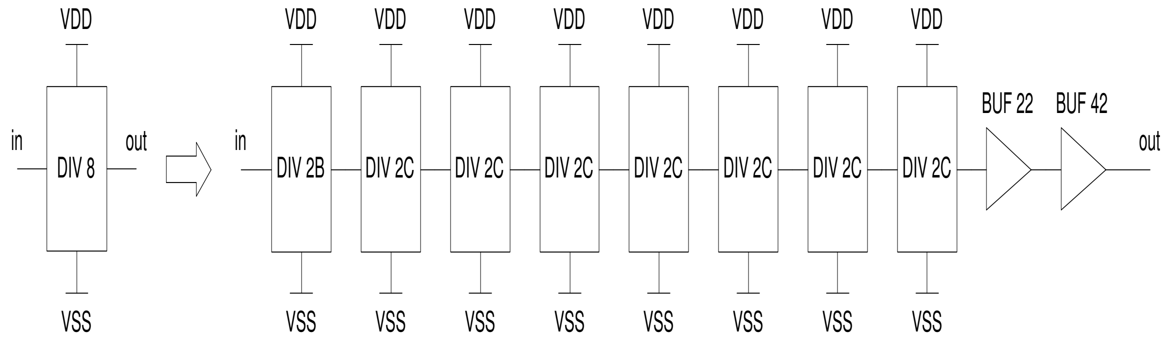


Figure C.28: Schematic of the frequency divider *DIV8*.

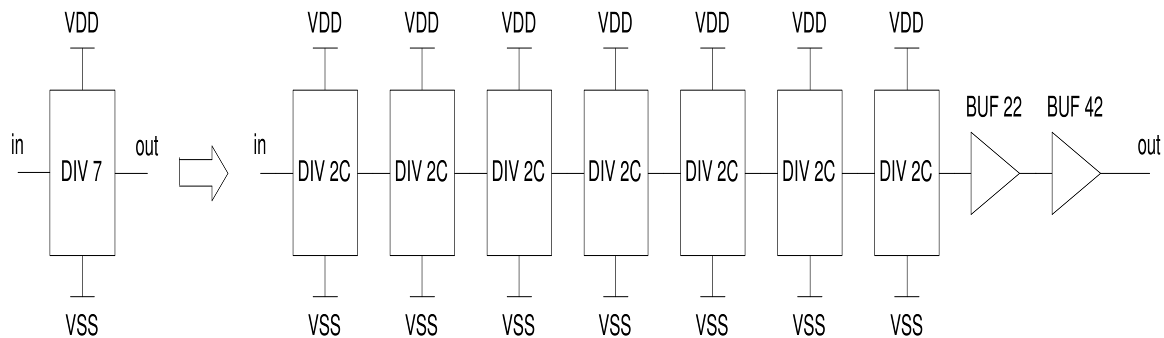
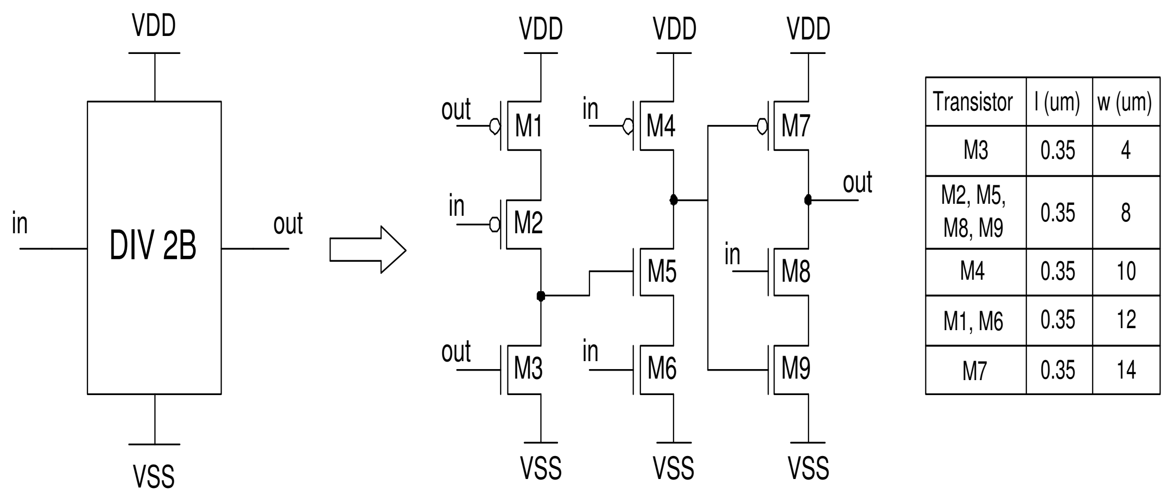
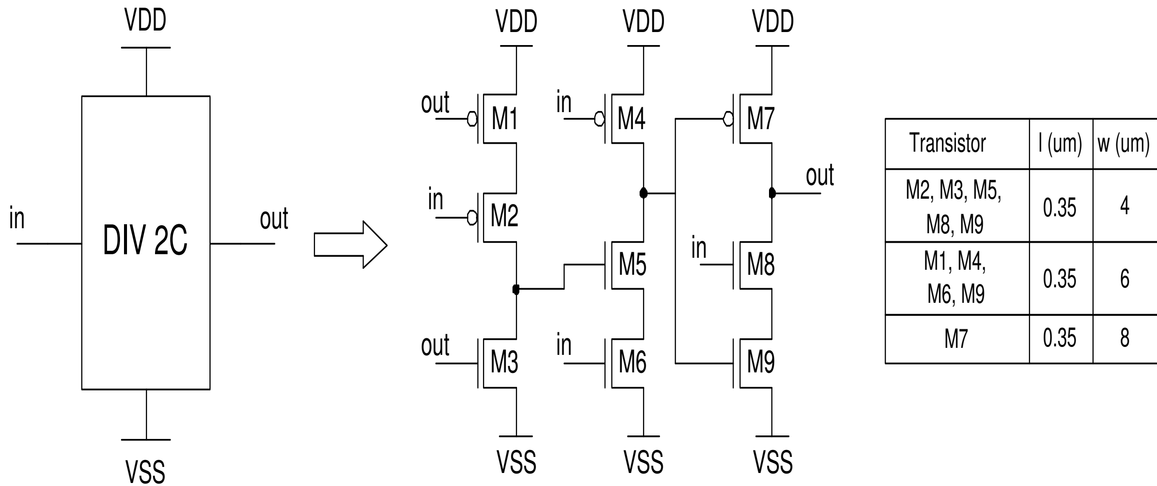


Figure C.29: Schematic of the frequency divider *DIV7*.



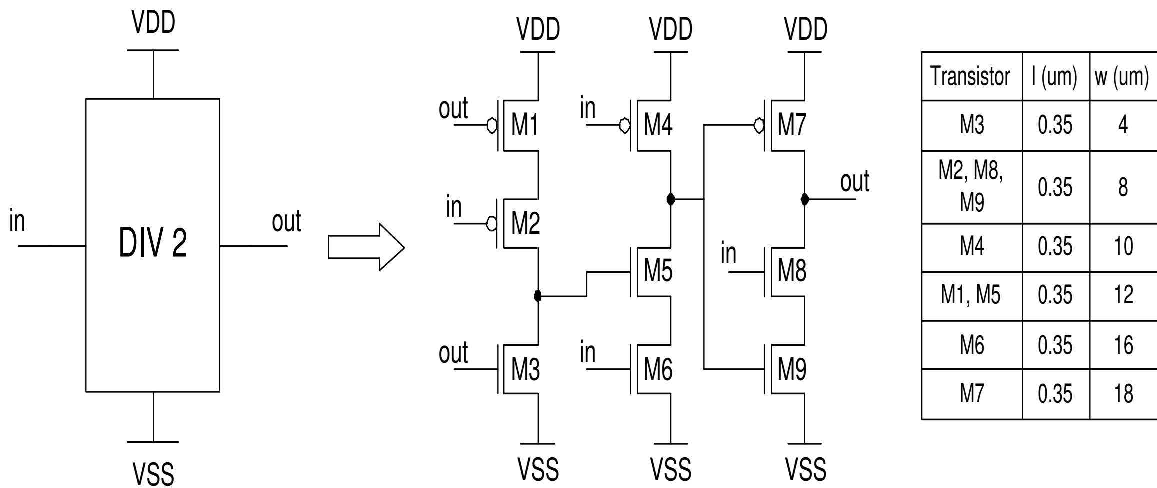
Transistor	l (um)	w (um)
M3	0.35	4
M2, M5, M8, M9	0.35	8
M4	0.35	10
M1, M6	0.35	12
M7	0.35	14

Figure C.30: Schematic of the frequency divider *DIV 2B*.



Transistor	l (um)	w (um)
M2, M3, M5, M8, M9	0.35	4
M1, M4, M6, M9	0.35	6
M7	0.35	8

Figure C.31: Schematic of the frequency divider *DIV 2C*.



Transistor	l (um)	w (um)
M3	0.35	4
M2, M8, M9	0.35	8
M4	0.35	10
M1, M5	0.35	12
M6	0.35	16
M7	0.35	18

Figure C.32: Schematic of the frequency divider *DIV 2*.

Appendix D

Publications

This appendix shows a list of the publications derived from this work.

1. "A Design-Oriented Methodology for Accurate Modeling of On-Chip Interconnects"
   Analog Integrated Circuits and Signal Processing An International Journal.
   Oscar González Diaz, Mónico Linares Aranda, Reydezel Torres Torres.

2. "S-Parameter Measurement-Based Modeling Methodology for On-Chip Interconnects used in High Frequency Systems"
   36th European Solid-State Circuit Conference ESSCIRC 2010.
   Oscar González Díaz, Reydezel Torres Torres, Mónico Linares Aranda.

3. "High-Frequency Interconnect Modeling for Global Signal Networks"
   52nd IEEE International Midwest Symposium on Circuits and Systems MWSCAS 2009.
   Oscar González Diaz, Mónico Linares Aranda, Reydezel Torres Torres.

4. "Redes de Generación y Distribución de Reloj para Sistemas en Chip (SoC): Un Análisis"
   Iberchip XIV Workshop.
   Oscar González Diaz, Mónico Linares Aranda, Reydezel Torres Torres.

5. “Transmission Line Characterization for High Frequency Synchronization System Design”
   20th International Conference on Electronics Communications and Computers CONIELECOMP 2010.
   Oscar González Diaz, Mónico Linares Aranda, Reydezel Torres Torres.

6. “Obtención del Modelo Eléctrico Equivalente RLC de una Línea de Transmisión con Pérdidas utilizando Parámetros S y su Aplicación en la Sincronización de Sistemas Integrados en un Solo Chip”
   XXVII Annual Meeting International Conference on Surfaces, Materials and Vacuum 2007.
   Oscar González Diaz, Mónico Linares Aranda, Reydezel Torres Torres.

7. “Análisis del Modelo Eléctrico Equivalente R, L, C de una Línea de Transmisión con Pérdidas Obtenido a partir de Parámetros Tecnológicos y Parámetros de Dispersión S”
   XXVIII Annual Meeting International Conference on Surfaces, Materials and Vacuum 2008.
   Oscar González Diaz, Mónico Linares Aranda, Reydezel Torres Torres.

8. “Validation of Interconnect Equivalent Model obtained from S-Parameter Measurements and its Application in CMOS Oscillators”
   XXX Annual Meeting International Conference on Surfaces, Materials and Vacuum 2010.
   Oscar González Diaz, Mónico Linares Aranda, Reydezel Torres Torres.

9. “Osciladores Controlados por Voltaje para la Generación y Distribución Simultanea de Señal de Reloj en Sistemas en Chip”
   II Simposio Internacional de Computación y Electrónica: Diseño, Aplicaciones, Técnicas Avanzadas y Retos.
   Oscar González Diaz, Mónico Linares Aranda, Reydezel Torres Torres.

10. “High-Performance Voltage Controlled Oscillators for Local Clock Networks”
    Semana Nacional de Ingeniería Electrónica SENIE 2010.
    Oscar González Díaz, Ramón Baez Alvarez, Mónico Linares Aranda.

Appendix E

Resumen en Extenso

E.1 Introducción

Actualmente, el diseño de microprocesadores de alto desempeño que realicen una gran cantidad de funciones a una alta velocidad y bajo consumo de potencia es muy importante para la implementación de equipos multimedia (e.g. computadoras, teléfonos celulares, juegos de video, video cámaras, reproductores de audio, etc.). En un microprocesador de alto desempeño, una gran cantidad de funciones son llevadas a cabo en una manera digital síncrona; por lo tanto, la incorporación de una red de reloj responsable de generar y distribuir la señal de sincronización (a todos los puntos donde la señal es requerida en el microprocesador) es indispensable.

En los microprocesadores comerciales, la señal de reloj es generada en un solo punto y distribuida a través del circuito integrado (CI) utilizando una red de generación y distribución de reloj global (RGDRG), usualmente implementada por un circuito de amarre de fase (PLL por sus siglas en inglés) y una red de distribución de reloj (RDR) [1]. Sin embargo, debido al continuo escalamiento de la tecnología, el incremento en área de los circuitos integrados, las limitaciones físicas de los materiales de interconexión, las variaciones entre la longitud de las interconexiones, las variaciones del proceso, el acoplamiento electromagnético, las restricciones de carga, la distribución de bloques en los sistemas integrados complejos, etc.; la generación y

distribución de señales de reloj a una alta frecuencia de operación, con baja incertidumbre en el tiempo (i.e. bajo skew y jitter), y bajo consumo de potencia son cada vez más difíciles de llevar a cabo utilizando las redes de reloj globales [2] [3] [4].

Con el fin de resolver los problemas relacionados con las redes globales, actualmente, una de las filosofías de diseño que están bajo estudio son las redes de generación y distribución de reloj locales (RGDRL). En este caso, la señal de reloj es generada en diferentes puntos del CI mediante la interconexión y el acoplamiento de osciladores implementados por líneas de interconexión y etapas de ganancia. Así, el área en la cual la señal de reloj tiene que ser distribuida (i.e. área de cobertura) es reducida; de esta manera es posible generar y distribuir señales de reloj a una alta frecuencia de operación y con una baja incertidumbre en el tiempo [5], [6], [7].

En las redes de reloj globales y locales, las líneas de interconexión (en el chip) en combinación con las etapas de ganancia son utilizadas para generar y distribuir simultáneamente señales de sincronización a una alta frecuencia de operación a través del circuito integrado. En el diseño de este tipo de redes, el modelo eléctrico de circuito equivalente proporciona información importante sobre las características de las interconexiones utilizadas en la implementación; así, con base en esta información, un diseño preciso de las etapas de ganancia, etapas de compensación, y etapas de salida puede ser llevado a cabo. Por lo tanto, un modelado (representación eléctrica) preciso de las interconexiones comúnmente utilizadas en este tipo de sistemas es muy importantes, y representa una importante área de investigación.

Tradicionalmente, las líneas de interconexión han sido modeladas utilizando una capacitancia concentrada C para representar la carga parásita introducida por la línea. Sin embargo, debido al continuo escalamiento de la tecnología, la resistencia finita de las líneas de metal ha tomado importancia limitando el desempeño de las interconexiones (en el chip); por lo tanto, modelos RC han sido utilizados para llevar a cabo la representación correspondiente a relativamente altas frecuencias [8]. Asimismo, en circuitos integrados de alta velocidad los cuales exhiben tiempos de conmutación en el orden de nanosegundos, la inductancia asociada con la línea de metal

así como la conductancia asociada con el material dieléctrico no pueden ser despreciados. Por consiguiente, es necesario considerar modelos de circuito equivalente RLC y $RLGC$ para llevar a cabo una representación precisa de las líneas de interconexión (en el chip) utilizadas en el diseño de sistemas integrados de alta frecuencia.

En trabajos de investigación previamente reportados en el estado del arte del modelado de interconexiones, la representación correspondiente de las líneas de interconexión ha sido llevada a cabo a través de modelos de circuito equivalente RC y RLC distribuidos los cuales incluyen la resistencia, inductancia, y capacitancia total de la interconexión. En estos modelos, los valores de resistencia (R_l), inductancia (L_l), y capacitancia (C_l) por unidad de longitud son obtenidos a partir de expresiones analíticas básicas y parámetros de la tecnología proporcionados por el fabricante (i.e. modelo invariante con la frecuencia) [9], [10], [11]; desafortunadamente, los valores de R_l, L_l, y C_l, son considerados constantes con la frecuencia, lo cual es fundamentalmente incorrecto en el rango de frecuencia de los GHz. Estos modelos son ampliamente utilizados por los diseñadores de circuitos para realizar un estimado rápido del retardo asociado a las diferentes trayectorias presentes en los CI; sin embargo, en el diseño de circuitos integrados operando a una alta frecuencia, los resultados de simulación varían substancialmente de los resultados experimentales debido a un modelado impreciso de las interconexiones.

Con el fin de tomar en consideración la dependencia con la frecuencia de los parámetros de la interconexión para una adecuada representación de las interconexiones operando en el rango de los GHz, los trabajos de investigación [12], [13], [14] llevan a cabo una extracción de parámetros directamente a partir de mediciones de parámetros S. Sin embargo, este procedimiento ha sido raramente utilizado en el diseño de circuitos integrados debido a que los diseñadores asumen que un modelo invariante con la frecuencia es suficiente para representar a las líneas de interconexión. Sin embargo, en el diseño de sistemas de alta velocidad como son las redes de reloj globales y locales, una representación precisa de las líneas de interconexión es esencial; así, una de las contribuciones de esta propuesta es incentivar a los diseñadores

a utilizar modelos de circuito equivalente implementados experimentalmente para la representación de las interconexiones incluso aunque un gran número de autores continúen utilizando el modelo invariante con la frecuencia.

En el diseño de sistemas integrados conteniendo un gran número de interconexiones, otro aspecto que debe ser tomado en cuenta por los diseñadores de circuitos es el número de secciones requeridas en el modelo de circuito equivalente para representar una línea de interconexión, el cual está directamente relacionado con la precisión y el tiempo de computo requerido para llevar a cabo las simulaciones correspondientes. En una gran variedad de trabajos, las líneas de interconexión han sido representadas por un modelo de circuito equivalente distribuido implementado con n secciones, e.g. 20 secciones como se muestra en [15]. Obviamente, utilizando un valor grande para n permite llevar a cabo una representación precisa de una interconexión a mayores frecuencias que cuando se utiliza un valor pequeño para n; desafortunadamente, cuando se utilizan una mayor cantidad de secciones en el modelo de circuito equivalente se incrementa el tiempo de simulación el cual es considerablemente elevado en el diseño de CI conteniendo miles de interconexiones. Por lo tanto, la determinación del número de secciones en las que el modelo de circuito equivalente tiene que ser dividido para una representación precisa de una línea de interconexión con una determinada longitud operando dentro de un rango de frecuencia específico es muy importante; sin embargo, el procedimiento para determinar el número de secciones no ha sido claramente establecido en trabajos de investigación previamente reportados.

La principal contribución de esta propuesta es el establecimiento de una metodología que le permita a los diseñadores de circuitos llevar a cabo una representación precisa de las líneas de interconexión utilizadas en el diseño e implementación de redes de generación y distribución de reloj globales y locales. Esta metodología (desarrollada a partir de la medición de los parámetros S) incluye el procedimiento para la extracción de los parámetros de la interconexión, la selección del modelo de circuito equivalente, y la determinación del número de secciones requeridas en el circuito equivalente para una representación precisa de líneas de interconexión con una determinada longitud

operando dentro de un rango de frecuencia especifico considerando la dependencia con la frecuencia de los parámetros asociados.

En el diseño de sistemas integrados, el diseñador de circuitos es responsable de definir la metodología utilizada para obtener el modelo de circuito equivalente el cual represente a las líneas de interconexión utilizadas en la implementación correspondiente. Sin embargo, en el diseño de redes de reloj actualmente bajo estudio, las líneas de interconexión juegan un papel esencial en la generación y distribución de las señales de reloj; por lo tanto, una representación imprecisa de las interconexiones utilizadas en la implementación de este tipo de redes se reflejará en un funcionamiento inadecuado del sistema. Así, la metodología de modelado propuesta representa una alternativa apropiada para llevar a cabo un diseño más preciso de redes de generación y distribución de reloj globales y locales.

E.2 Redes de Generación y Distribución de Reloj

En este capítulo se muestra un análisis cualitativo de redes de generación y distribución de reloj globales y locales actualmente bajo estudio. En este análisis se resalta la importancia de las interconexiones en el diseño e implementación de redes de reloj actuales y futuras.

E.2.1 Ideas Principales

- En un microprocesador de alto desempeño, una gran cantidad de funciones son llevadas a cabo en una manera digital síncrona; por lo tanto, la incorporación de una red de reloj responsable de generar y distribuir la señal de sincronización (a todos los puntos donde la señal es requerida en el microprocesador) es esencial.

- En los microprocesadores comerciales, la señal de reloj es generada en un solo punto y distribuida a través del circuito integrado utilizando una red de generación y distribución de reloj global.

- Las redes de reloj globales son altamente comprendidas y ampliamente utilizadas para generar y distribuir las señales de sincronización en microprocesadores de alto desempeño. Sin embargo, debido al continuo escalamiento de la tecnología, el incremento en área de los circuitos integrados, las limitaciones físicas de los materiales de interconexión, las variaciones entre la longitud de las interconexiones, las variaciones del proceso, el acoplamiento electromagnético, las restricciones de carga, la distribución de bloques en los sistemas integrados complejos, etc.; el uso de este tipo de redes de reloj está llegando a su límite.

- Las redes de reloj locales implementadas mediante la interconexión y el acoplamiento de osciladores representan una de las principales alternativas para resolver los problemas relacionados con las redes de reloj globales.

- Las métricas de desempeño de las redes de reloj globales y locales (e.g. frecuencia de operación, potencia, voltaje de salida, incertidumbre en el tiempo, etc.) dependen principalmente de las características de las interconexiones utilizadas en su implementación.

- En el diseño e implementación de las redes de generación y distribución de reloj globales y locales, las líneas de interconexión juegan un papel esencial en la generación y distribución de las señales de reloj; por lo tanto, un modelado preciso de las interconexiones utilizadas en este tipo de redes es muy importante.

- Debido a la importancia de las interconexiones en la implementación de las redes de reloj, el flujo de diseño de este tipo de sistemas integrados debe comenzar con el modelado preciso de las interconexiones. Así, con base en esta información, un diseño preciso de las etapas de ganancia, etapas de compensación, y etapas de salida puede ser llevado a cabo.

E.3 Procedimiento para la Extracción de Parámetros de la Interconexión

En este capítulo se muestra la extracción de los parámetros asociados con líneas de interconexión (en el chip) típicamente utilizadas en el diseño e implementación de redes de generación y distribución de reloj globales y locales. En la primer parte de este capítulo, se presenta la descripción de la estructura de las líneas de interconexión (en el chip) utilizadas; después, se presenta el procedimiento para la extracción de los parámetros asociados con una línea de interconexión el cual es desarrollado a partir de la medición de los parámetros S de estructuras de prueba fabricadas.

E.3.1 Ideas Principales

- Un procedimiento de extracción de parámetros preciso es esencial para llevar a cabo un modelado preciso de las interconexiones utilizadas en el diseño e implementación de sistemas integrados (e.g. diseño de redes de generación y distribución de reloj de alto desempeño).

- El procedimiento de extracción de parámetros desarrollado directamente a partir de la medición de los parámetros S permite llevar a cabo una determinación precisa de los parámetros asociados con una línea de interconexión considerando su dependencia con la frecuencia.

- Con el fin de llevar a cabo el procedimiento para la extracción de los parámetros asociados con una línea de interconexión, se requiere el diseño y fabricación de dos líneas de interconexión con las mismas características pero diferente longitud.

- Un procedimiento de des-incrustación es necesario para eliminar la contribución de parásitas introducidas por las discontinuidades de los pads a la línea presentes en el procedimiento de medición.

- Los valores de R_l, L_l, y C_l asociados con una línea de interconexión son determinados a partir de la impedancia característica Z_C y la constante de propagación γ las cuales están directamente relacionadas con el ancho y el espesor de las capas de metal, dieléctrico, y plano de referencia. Por esta razón, el procedimiento para la extracción de parámetros debe ser repetido para líneas de interconexión con diferente Z_C y γ.

E.4 Modelado de la Interconexión

En este capítulo se presenta la metodología para el modelado de interconexiones propuesta. En este capítulo, se lleva a cabo la selección del modelo de circuito equivalente y la determinación del número de secciones requeridas para una representación precisa de líneas de interconexión utilizadas en el diseño de sistemas integrados. Asimismo, se presenta un resumen de los principales pasos requeridos para implementar la metodología de modelado propuesta.

E.4.1 Ideas Principales

- La metodología para el modelado de interconexiones propuesta le permite a los diseñadores de circuitos llevar a cabo la selección del modelo de circuito equivalente y la determinación del mínimo número de secciones requeridas en el circuito equivalente para una representación precisa de líneas de interconexión típicamente utilizadas en el diseño e implementación de redes de generación y distribución de reloj.

- La selección del modelo de circuito equivalente así como la determinación del número de secciones dependen principalmente de la longitud de la línea y la frecuencia de operación.

- Un modelo de circuito equivalente RLC es indispensable para llevar a cabo una representación precisa del retardo y las pérdidas asociadas con líneas de

interconexión (en el chip) operando en el rango de frecuencia de los GHz.

- Para una línea de interconexión determinada existe una combinación de longitud y frecuencia que define cuando la interconexión puede ser representada por un modelo de circuito equivalente *concentrado* y cuando puede ser representada por un modelo *distribuido* implementado con n secciones.

- Las regiones de operación de los modelos de circuito equivalente *concentrado* y *distribuido* son determinadas analíticamente utilizando la ecuación (4.6).

E.5 Aplicación de Diseño

En este capítulo se muestra la aplicación de diseño de la metodología de modelado propuesta. Con el fin de mostrar la precisión y la aplicación de la metodología de modelado propuesta en el diseño e implementación de redes de generación y distribución de reloj, se lleva a cabo el diseño y fabricación de un conjunto de osciladores de anillo expandidos. Además, en este capítulo también se incluye el diseño de redes de reloj locales implementadas mediante la interconexión y el acoplamiento de osciladores de anillo expandidos.

E.5.1 Ideas Principales

- Las líneas de interconexión juegan un papel esencial en el desempeño de las redes de generación y distribución de reloj globales y locales; por lo tanto, la determinación de un modelo de circuito equivalente el cual permita llevar a cabo una representación precisa de las interconexiones utilizadas en este tipo de redes es muy importante.

- En el diseño de redes de generación y distribución de reloj, el modelo de circuito equivalente proporciona información importante sobre las características de las interconexiones utilizadas en la implementación; así, con base en esta información, un diseño preciso de las etapas de ganancia, etapas de compensación,

y etapas de salida puede ser llevado a cabo.

- La metodología para el modelado de interconexiones propuesta le permite a los diseñadores de circuitos llevar a cabo una adecuada selección del modelo de circuito equivalente para una representación precisa de las interconexiones utilizadas en el diseño e implementación de redes de reloj globales y locales.

- Una vez que se obtiene el modelo de circuito equivalente utilizado para representar a las interconexiones, el diseño de sistemas simples y complejos puede ser llevado a cabo en una manera práctica y relativamente simple.

- Para el caso de las redes de reloj locales, se mostró que el desempeño de este tipo de redes depende directamente de las características del oscilador utilizado en la implementación; por lo tanto, un adecuado diseño de el bloque básico de generación y distribución de reloj (e.g. oscilador de anillo, oscilador de onda viajera, oscilador de onda estacionaria) es muy importante.

- En el diseño de bloques básicos de generación y distribución de reloj, se mostró que el porcentaje de error entre la frecuencia de operación experimental y de simulación de los osciladores de anillo expandidos se redujo hasta un 2 % cuando las líneas de interconexión utilizadas en la implementación son representadas con los modelos de circuito equivalente obtenidos mediante la aplicación de la metodología para el modelado de interconexiones propuesta.

- Se mostró que un modelo de circuito equivalente *RLC concentrado* es suficiente para llevar a cabo una representación precisa de las interconexiones utilizadas en la aplicación de diseño presentada en este trabajo.

- La determinación del mínimo número de secciones requeridas en el modelo de circuito equivalente es importante para reducir el tiempo de computo el cual es considerablemente elevado en el diseño de sistemas complejos conteniendo una gran cantidad de interconexiones.

E.6 Conclusiones

En esta tesis se presentó una metodología para el modelado de interconexiones (en el chip) utilizadas en el diseño e implementación de redes de generación y distribución de reloj globales y locales.

Actualmente, el diseño de redes de reloj las cuales simultáneamente generen y distribuyan señales a una alta frecuencia de operación, con baja incertidumbre en el tiempo, y bajo consumo de potencia es esencial para la sincronización de microprocesadores de alto desempeño utilizados en la implementación de equipos multimedia de alta velocidad. En los microprocesadores comerciales, las redes de reloj globales son ampliamente utilizadas para generar y distribuir las señales de sincronización. Sin embargo, debido al continuo escalamiento de la tecnología, el incremento en área de los circuitos integrados, las limitaciones físicas de los materiales de interconexión, las variaciones entre la longitud de las interconexiones, las variaciones del proceso, el acoplamiento electromagnético, las restricciones de carga, la distribución de bloques en los sistemas integrados complejos, etc.; el uso de las redes de reloj globales está llegando a su límite. Por lo tanto, es evidente que un cambio en la generación y distribución de las señales de reloj es inevitable. Así, las redes de generación y distribución de reloj locales implementadas mediante la interconexión y el acoplamiento de osciladores representa una de las alternativas para resolver los problemas relacionados con las redes de reloj globales.

Las tendencias de diseño de redes de reloj actuales y futuras requieren de la implementación de modelos de circuito equivalente precisos para la representación de las interconexiones utilizadas en una determinada aplicación. Entonces, una de las contribuciones de esta propuesta es incentivar a los diseñadores de circuitos a utilizar modelos de circuito equivalente obtenidos directamente a partir de datos experimentales que permitan llevar a cabo una representación precisa de las líneas de interconexión utilizadas en el diseño e implementación de redes de generación y distribución de reloj de alta frecuencia. Por lo tanto, con el fin de proporcionarle al diseñador de circuitos directrices para la implementación de modelos experimentales,

en esta tesis, se presenta el establecimiento de una metodología de modelado desarrollada a partir de la medición de los parámetros S de estructuras fabricadas.

En la metodología de modelado propuesta, se mostró que a través de una apropiada explotación de los parámetros S y $ABCD$ asociados con las líneas de interconexión (en el chip), se puede llevar a cabo la extracción de parámetros, la selección del modelo de circuito equivalente, y la determinación del número de secciones requeridas en el circuito equivalente para una representación precisa de líneas de interconexión con una determinada longitud operando dentro de un rango de frecuencia especifico. Asimismo, es importante mencionar que la selección del modelo de circuito equivalente así como la determinación del mínimo número de secciones dependen principalmente de las características de la línea y la frecuencia de operación. Así, se mostró que un modelo de circuito equivalente RLC es necesario para llevar a cabo una representación precisa de las características (i.e. el retardo y las pérdidas) asociadas con interconexiones (en el chip) operando en el rango de los GHz. Además, se mostró que para una línea de interconexión determinada existe una combinación de longitud y frecuencia que determina cuando la interconexión puede ser representada por un modelo de circuito equivalente *concentrado* y cuando puede ser representada por un modelo *distribuido* implementado con n secciones.

La presente metodología para el modelado de interconexiones desarrollada a partir de la medición de parámetros S de estructuras fabricadas y la aplicación de la teoría de transmisión puede ser utilizada por los diseñadores de circuitos para llevar a cabo una representación eléctrica precisa de líneas de interconexión utilizadas en el diseño de sistemas integrados actuales y futuros fabricados en diferentes tecnologías.

En el diseño de sistemas integrados, el diseñador de circuitos es responsable de definir la metodología utilizada para obtener el modelo de circuito equivalente el cual represente a las líneas de interconexión utilizadas en la implementación correspondiente. Sin embargo, en el diseño de redes de reloj actualmente bajo estudio, las líneas de interconexión juegan un papel esencial en la generación y distribución de las señales de reloj; por lo tanto, una representación imprecisa de las interconexiones

utilizadas en la implementación de este tipo de redes se reflejará en un funcionamiento inadecuado del sistema. Así, la metodología de modelado propuesta representa una alternativa apropiada para llevar a cabo un diseño más preciso de redes de generación y distribución de reloj globales y locales.

Ciertamente, las líneas de interconexión juegan y continuarán jugando un papel importante en el diseño e implementación de redes de generación y distribución de reloj actuales y futuras. Como se mostró en este trabajo, una metodología para el modelado de interconexiones desarrollada a partir de la medición de parámetros S de estructuras fabricadas le permite a los diseñadores de circuitos realizar una representación eléctrica precisa de líneas de interconexión (en el chip) operando en el rango de los GHz. Sin duda alguna, esta metodología desarrollada a partir de datos experimentales es la más precisa y adecuada para llevar a cabo el modelado de interconexiones (en el chip); sin embargo, es importante mencionar que el punto débil de la metodología está relacionado con el diseño y fabricación de estructuras de prueba para líneas de interconexión con diferentes valores de Z_C y γ (i.e. diferente ancho y espesor de las capas de metal, dieléctrico, y/o plano de referencia). Así, una alternativa para resolver este inconveniente es a través de el diseño y fabricación de un conjunto de estructuras de prueba con dimensiones representativas (e.g. interconexiones con diferente ancho, longitud, plano de referencia, etc.); entonces, mediante la aplicación de interpolación/extrapolación, la implementación de un modelo escalable puede ser llevado a cabo. Sin embargo, aunque esta posible solución suena trivial, existe una gran complejidad en el desarrollo de un modelo escalable preciso; por lo tanto, este es un tópico para futuras contribuciones.

E.7 Apéndices

El Apéndice A muestra el prototipo de circuito integrado fabricado y los sistemas de prueba utilizados para realizar las mediciones correspondientes. En la primer parte de este apéndice, se presenta una descripción de las estructuras de prueba de

líneas de interconexión y los osciladores de anillo fabricados. Además, en la segunda parte se muestra una descripción de los sistemas de prueba utilizados para realizar las mediciones de las líneas de interconexión y los osciladores de anillo fabricados.

El Apéndice B muestra la aplicación de la metodología de modelado a un conjunto de líneas de interconexión fabricadas. Primero, se obtienen los valores de Z_C, γ, R_l, L_l, y C_l de las estructuras fabricadas; después, se lleva a cabo la selección del modelo de circuito equivalente y la determinación del número de secciones requeridas para una representación precisa de líneas de interconexión con una determinada longitud operando dentro de un rango de frecuencia especifico.

El Apéndice C presenta un resumen de las principales características y métricas de desempeño de los osciladores de anillo fabricados. En este apéndice, se presenta los resultados de simulación y experimentales de los osciladores de anillo; además, también se incluye los esquemáticos, patrones geométricos, y fotografías de cada uno de los osciladores fabricados.

El Apéndice D presenta una lista de las publicaciones derivadas de este trabajo.

References

[1] N. Ranganathan and N. P. Jouppi, "Evaluating the Potential of Future On-Chip Clock Distribution using Optical Interconnects," *HP Technical Report 2007*, pp. 1–14, Oct. 2007.

[2] S. Tam, S. Rusu, U. Nagarji-Desai, *et al.*, "Clock Generation and Distribution for the First IA-64 Microprocessor," *IEEE J. Solid-State Circuits*, vol. 35, no. 11, pp. 1545–1552, Nov. 2000.

[3] N. A. Kurd, J. S. Barkarullah, R. O. Dizon, *et al.*, "A Multigigahertz Clocking Scheme for the Pentium® 4 Microprocessor," *IEEE J. Solid-State Circuits*, vol. 36, no. 11, pp. 1647–1653, Nov. 2001.

[4] M. Saint-Laurent and M. Swaminathan, "A Multi-PLL Clock Distribution Architecture for Gigascale Integration," in *Proc. of the IEEE Computer Society Workshop on VLSI, 2001*, Apr. 2001, pp. 30–35.

[5] J. Wood, T. C. Edwards, and S. Lipa, "Rotary Traveling-Wave Oscillator Arrays: A New Clock Technology," *IEEE J. Solid-State Circuits*, vol. 36, no. 11, pp. 1654–1664, Nov. 2001.

[6] F. O'Mahony, C. P. Yue, M. A. Horowitz, and S. S. Wong, "A 10-GHz Global Clock Distribution Using Coupled Standing-Wave Oscillators," *IEEE J. Solid-State Circuits*, vol. 38, no. 11, pp. 1813–1820, Nov. 2003.

[7] M. S. Maza, O. Gonzalez-Diaz, and M. Linares-Aranda, “On-chip Clock Network using Interconnected and Coupled Ring Oscillators,” in *Proc. of the 15th IEEE International Conference on Electronics, Circuits and Systems, 2008*, St. Julien’s, Aug. 2008, pp. 518–521.

[8] A. Nalamalpu *et al.*, “Repeater Insertion in Deep Sub-micron CMOS: Ramp-based Analytical Model and Placement Sensitivity Analysis,” in *Proc. of the IEEE Int. Symposium on Circuits and Systems*, Geneva, May 2000, pp. 766–769.

[9] Y. I. Ismail, E. G. Friedman, and J. L. Neves, “Equivalent Elmore Delay for RLC Trees,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 19, no. 1, pp. 83–97, Jan. 2000.

[10] T. C. Chen, S. R. Pan, and Y. W. Chang, “Timing Modeling and Optimization Under the Transmission Line Model,” *IEEE Transaction on Very Large Scale Integration (VLSI) Systems*, vol. 12, no. 1, pp. 28–41, Jan. 2004.

[11] M. Salim-Maza, M. Aguirre-Hernandez, and M. Linares-Aranda, “Fused Timing Analytical Model for Repeater Insertion and Optimization,” in *Proc. of the 48th Midwest Symposium on Circuits and Systems, 2005*, Aug. 2005, pp. 720–723.

[12] W. R. Eisenstadt and Y. Eo, “S-Parameter-Based IC Interconnect Transmission Line Characterization,” *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 15, no. 4, pp. 483–490, Aug. 1992.

[13] Y. Eo and W. R. Eisenstadt, “High-Speed VLSI Interconnect Modeling Based on S-Parameter Measurements,” *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 16, no. 5, pp. 555–562, Aug. 1993.

[14] H. M. Hegazy, “RLC Parasitic Extraction and Circuit Model Optimization for Cu/SiO2-90nm Inductance Structures,” *European Gallium Arsenide and Other Semiconductor Application Symposium, 2005*, pp. 685–688, Oct. 2005.

[15] D. Goren, M. Zelikson, T. C. Galambos, *et al.*, "An Interconnect-Aware Methodology for Analog and Mixed Signal Design, Based on High Bandwidth (over 40 GHz) On-Chip Transmission Line Approach," in *Proceeding Design, Automation and Test in Europe Conference and Exhibition*, Aug. 2002, pp. 804–811.

[16] B. Razavi, *Design of Analog CMOS integrated Circuits.* New York: McGraw-Hill, 2001.

[17] H. Mizuno and K. Ishibashi, "A Noise-Immune GHz-Clock Distribution Scheme using Synchronous Distributed Oscillators," in *Proc. of the IEEE International Solid-State Circuits Conference, 45th ISSCC 1998. Digest of Technical Papers*, San Francisco, CA, Feb. 1998, pp. 404–405.

[18] M. Salim-Maza, "Generación y Distribución de Señal de Reloj para Sistemas en Chip utilizando Anillos Interconectados Acoplados," Ph.D. dissertation, Instituto Nacional de Astrofísica, Óptica, y Electrónica, Tonantzintla, Puebla, June 2005.

[19] R. Wang, C. K. Koh, B. Jung, and W. J. Chappell, "Clock Generation and Distribution Using Traveling-Wave Oscillators with Reflection and Regeneration," in *Proc. of the IEEE Custom Integrated Circuits Conference 2006*, San Jose, CA, Sept. 2006, pp. 781–784.

[20] M. Shiozaki, M. Sasaki, A. Mori, *et al.*, "20 GHz Uniform-Phase Uniform-Amplitude Standing-Wave Clock Distribution," *IEICE Electronics Express*, vol. 3, no. 2, pp. 11–16, Jan. 2006.

[21] A. Rehman *et al.*, "Microstrip Design in a Silicon Technology using Closed Form Analytical Expresions," in *Proc. of the High Frequency Electronics*, Aug. 2005, pp. 720–723.

[22] J. M. Rabaey, *Digital Integrated Circuits: A Design Perspective.* Upper Saddle River, New Jersey: Prentice Hall, 1996.

[23] D. M. Pozar, *Microwave Engineering.* New York: John Wiley & Sons, 1998.

[24] M. T. Thompson, "Inductance Calculation Techniques," *Power Control and Intelligent Motion*, vol. 25, no. 12, pp. 40–45, Dec. 1999.

[25] A. M. Mangan, S. P. Voinigescu, Y. Ming-Ta, and M. Tazlauanu, "De-embedding Transmission Line Measurements for Accurate Modeling of IC Designs," *IEEE Transactions on Electron Devices*, vol. 53, no. 2, pp. 235–241, Feb. 2006.

[26] A. Barger, D. Goren, and A. Kolodny, "Design and Modelling of Network on Chip Interconnects using Transmission Lines," in *Proc. of the 11th IEEE International Conference on Electronics, Circuits and Systems, ICECS 2004*, 2004, pp. 403–406.

[27] J. Zhang *et al.*, "Causal RLGC(f) Models for Transmission Lines From Measured S-Parameters," *IEEE Transactions on Electromagnetic Compatibility*, vol. 52, no. 1, pp. 189–198, Feb. 2010.

[28] R. B. Marks and D. F. Williams, "Characteristic Impedance Determination Using Propagation Constant Measurement," *IEEE Microwave and Guided Wave Letters*, vol. 1, no. 6, pp. 141–143, June 1991.

[29] H. Johnson and M. Graham, *High-Speed Signal Propagation: Advanced Black Magic.* Prentice Hall, 2003.

[30] X. Shi *et al.*, "RF Equivalent-Circuit Model of Interconnect Bends Based on S-Parameter Measurements," *Microwave and Optical Technology Letters*, vol. 45, no. 2, pp. 170–173, Apr. 2005.