Highly-Linear/Highly-Efficient CMOS Power Amplifier for Mobile WiMAX

by:

MSc. Luis Abraham Sánchez Gaspariano

A dissertation submitted to the Academy of Electronics of the National Institute of Astrophysics, Optics and Electronics in partial fulfillment of the requirements for the degree of

Doctor of Science in Electronics

Under the supervision of:

Dr. Alejandro Díaz Sánchez

Dra. Anne-Johan Annema

Tonantzintla, Puebla,

México. June 2011

Acknowledgements

The road to a Ph.D. is an arduous one, but while the degree itself is ultimately a personal goal, the journey to it fortunately does not happen in isolation. If not for the contributions of many people, I would never have made it through to the end, and to these people, I am grateful.

It has been an honour to have had the opportunity to work under the guidance and support of Dr. Ir. Anne-Johan Annema. He has indeed a vast scientific and technical knowledge, but what really impressed the most was his high standards for research. Several times, I wanted to cut one corner or another and he would always discourage doing so; while some of the times left me feeling very deflated with thoughts of how much longer it would take for me to finish everything, looking back in retrospect, the extra time to do things right has been well spent. I am grateful for his keeping me on track.

I would also like to thank Dr Alejandro Díaz Sánchez not only for being my advisor and provide all the support for carrying out my project, but for keeping alive the sense of discovery and enjoyment in circuit design. He always manages to frame technical discussions in a way that somehow avoids the feeling of being enslaved to the external pressures and does not lose sight of learning little things that are interesting for their own sake.

I also thank the members of my dissertation committee. Dr. Jaime Ramírez Ángulo, Dr. José Miguel Rocha Pérez, Dra. María Teresa Sanz Pascual, Dr. Edgar Sánchez Sinencio, and Dr. Miguel Ángel García Andrade. With their remarks, valuable suggestions, and enlightening discussions, the final manuscript improved vastly.

Dr. José Miguel Rocha Pérez and undergraduate student Mauricio Huixtlaca were a great help as I navigated the maze of board fabrication, assembly and testing. Thank you very much for your support.

My experience in the Netherlands have had doubtless a profound impact in my life. I am greatly indebted to Dr. Ir. Bram Nauta for accepting me as a visiting scholar in the ICD group at the University of Twente where he is the head. I am also grateful to Mrs. Gerdien Lammers for providing all the support before and during my stance in Enschede. Staff members at the ICD/SC who I wish to extend my gratitude are Ing. Henk de Vries, Ing. Gerard J.M. Wienk, and Mrs. Annemiek Janssen. Also many fellow students at the ICD/SC who were very kind during my time there and deserve an special mention are Paul Veldhorst, Eric Hoekstra, Kasra Garakoui and Jan-Laurens van der Steen.

Outside of school, I have been lucky of having had the chance to share special moments over the last years with Carlos Muñíz, Mario Alberto García, Miguel Bello, Rosa López, Mario Rojas, Ragnar Kiebach, Iliana Mora, Xicotencatl Adán, Jacobo Salto, Oscar Gónzalez, Ezequiel Molinar, Salvador Arroyo, Tom Griffioen, Henk Jan Mulders, Jos Hoekstra, Karen Mende, Till, Enrique Quiroga, Alina Santillán, Jane Sorensen, Carmen Paleta, Eric Aspnes, Isabel Muñíz, Evelyn Tamaríz, Deniz Anar and Karina Paredes. I will never forget our time together.

In more recent years, Clara Iliana Martínez has been my fortress. I appreciate a lot her love, patience and support to displace my worries and frustrations about many things. One of the most marvelous things about her standing by my side is that now, for those worries and frustrations that refuse to stay displaced, I feel more ease with them. Thanks a lot darling.

Finally, I would never have made it without the patient support, love, and encouragement of my parents, Olga Gaspariano López and José Luis Sánchez Mora. They have done everything in their hands to minimize the things I need to worry about so that I may focus on what I have to do progress in life.

My PhD studies were funded by the National Council of Science and Technology of México through the scholarship number 48352 at the National Institute of Astrophysics, Optics and Electronics (INAOE). To both institution I extend my acknowledgements for providing me the facilities to realize my PhD.

“ Those who forget good and evil and seek only to know the facts are more likely to achieve good than those who view the world through the distorting medium of their own desires.”

- Bertrand Russell

to Mom and Dad

Abstract

The present work is about the design of a power amplification system in CMOS technology which satisfies the demands established by the IEEE802.16e-2005 standard for mobile WiMAX.

The simulation in $CadenceVirtuoso^{®}v$5.0.0. of the complete power amplification stage with the UMC 0.18μm Mixed Mode and RF CMOS technology was carried out. The RF band for which the circuit was tuned to operate was between 2.496GHz and 2.69GHz with an LO signal running from 2.486GHz to 2.68GHz and a BB signal of 10MHz. The power supply for the predriver stage was of 1.8V and 0.9V for the amplification stage. The total power consumption of the circuit was of approximately 26dBm. The peak output power obtained was 23dBm with a drain efficiency, η_D, of 83% and a Power Added Efficiency, PAE, of 61% meanwhile for 12dB of output power back-off the η_D was 33% and the PAE 31%. The harmonic suppression around the carrier in a range of 194MHz at from 2.496GHz to 2.69GHz presents a minimum value of -55dBc. These results indicate that the the proposed multipath polyphase Power Amplifier exhibits both, a high linearity achieving until -60dBc of intermodulation suppression with respect to the frequency of interest, $(\omega_{LO} + \omega_{BB})$, within the mobile WiMAX bandwidth, and a high PAE at peak output power and with 12dB of output power back-off.

In addition, the design and fabrication of the predriver stage was also realized but in a double poly three metal layers 0.5μm CMOS technology from MOSIS foundry. The fabricated prototype area was $0.472\mu m \times 0.148\mu m$. The prototype was characterized with an LO frequency of 80MHz and a BB frequency of 1.6MHz. The power supply was of 3.3V. The tuning control was of 400mV ranging from 1.0V to 1.4V. The maximum power consumption was 14.5dBm and the minimum was 12.6dBm. The maximum output power was 6.5dBm meanwhile the minimum was 0.3dBm. The duty cycle of the prototype was modifiable in a range of 9.3% from 49.4% to 40.1%. Finally, the maximum pulse amplitude of the output signal was 1V and the minimum pulse amplitude covers from 950mV to 200mV. According to these results, we conclude that the behavior of the predriver stage follows the curse anticipated in the synthesis. This is very important since the predriver stage is the key building block to enhance the efficiency of the overall system.

Contents

List of Figures

List of Tables

Chapter 1

The Mobile WiMAX Wireless Technology

1.1 Introduction

Mobile WiMAX (MW) is a relatively novel wireless technology intended for satisfying the emerging need for high data rate applications such as voice over IP, multimedia streaming and broadband mobile internet over large geographic areas. It is based on the IEEE 802.16e-2005 air interface standard, which has been planned to deal with stationary, nomadic and mobile transmission scenarios [1]. Figure 1.1 illustrates the MW environment.

MW supports several key characteristics necessary for delivering mobile broadband services at vehicular speeds up to 120km/h with a quality of service (QoS) comparable to broadband wire line access alternatives. Those features and attributes include [2]:

- Tolerance to multi-path and self-interference with sub-channel orthogonality in both the downlink (DL) and the uplink (UL).
- Scalable channel bandwidths from 1.25 to 20 MHz.
- Hybrid-Automatic Repeat Request (H-ARQ), which provides added robustness with rapidly changing path conditions in high mobility situations.

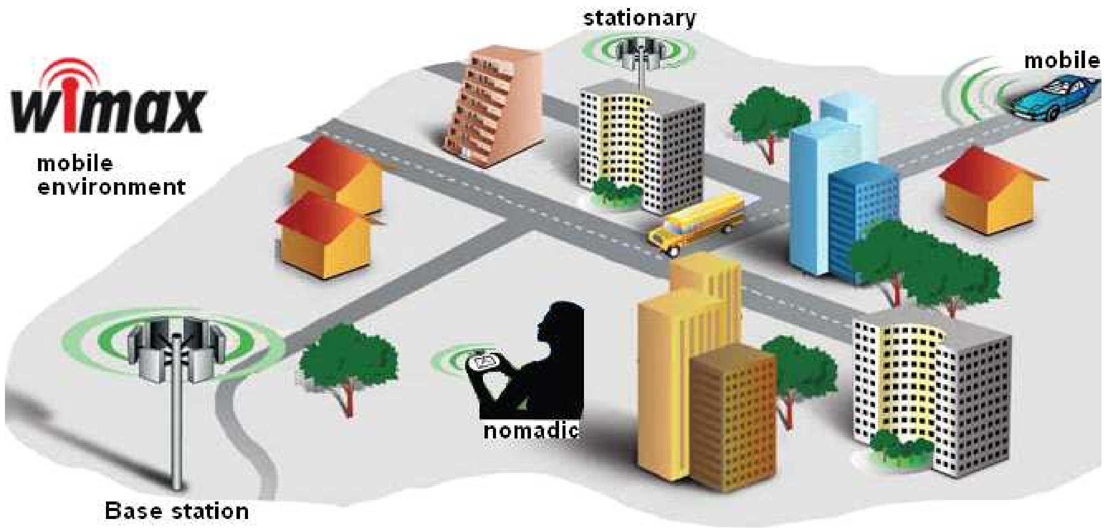

Figure 1.1: *Mobile WiMAX environment.*

- Frequency selective scheduling and sub-channelization with multiple permutation schemes, which gives to MW the ability to optimize the quality of the connection based on relative signals strengths to specific users.

The high throughput, scalability and long-range characteristics of this mobile wireless technology provide the flexibility to fill the broadband coverage gaps and reach millions of new customers worldwide. In fact, MW offers cost-effective broadband access services to both, residential and enterprise customers, and thus, it opens new economically viable market opportunities for operators, wireless Internet service providers and equipment manufacturers. This is, actually, one of the major attractives of this wireless technology. Moreover, MW broadband networks can be built quickly and at relatively low cost, compared with wired systems, by installing just a few wireless base stations mounted on buildings or poles to provide coverage to the surrounding area [3].

Some fixed WiMAX certified products are now commercially available. On the other hand, the deployment of mobile terminals has already began to occur worldwide during 2008. As a matter of fact, the launch of commercial mobile application products took place in Korea during 2007 (WiBro services), and the WiMAX forum have already announced the first MW certified products from the companies POSDATA, Runcom Technologies Ltd, Samsung Electronics Co., LTD

Figure 1.2: *Wireless service providers which have announced WiMAX plans.*

and Sequans Communications [4]. Figure 1.2 shows some of the wireless service providers around the world that have announced WiMAX plans.

1.2 Mobile WiMAX System Overview

Advanced access technologies capable of providing the necessary channel robustness for the support of higher spectral efficiency and higher channel throughput are required in broadband wireless networks. For those purposes, scalable orthogonal frequency division multiple access (*S-OFDMA*) is employed in MW. *S-OFDMA* is based on orthogonal frequency division multiplexing (*OFDM*), in which the data stream is partitioned into multiple narrowband transmissions in the frequency domain by means of sub-carriers that are orthogonal among each other. These sub-carriers are then assembled into frequency channels for their transmission over the air. The specific number of sub-carriers corresponds to the fast fourier transform (*FFT*) size. The 802.16e-2005 standard establishes *FFT*

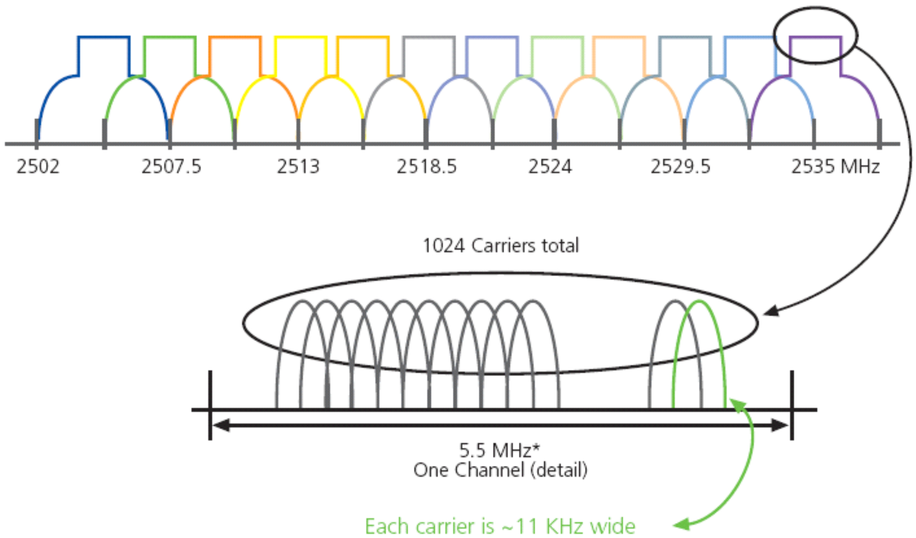

Figure 1.3: *Example of OFDM operation.*

sizes from 128 to 2048 corresponding to channel bandwidths ranging from 1.25 to 20 MHz [1]. Figure 1.3 illustrates the way in which *OFDM* operates [5]. In the example, 5.5MHz channels with 0.5MHz guard band are allocated at 2.5GHz sub-carriers.

In order to make them less sensitive to distortion due to multi-path, the narrowband transmissions employ long-duration symbols in the time domain. By using approximately symbol duration of 100 microseconds with a guard interval of about 11 microseconds, *OFDM* overcomes the effects of multi-path with very low overhead. Moreover, by assigning to the spacing of the sub-carriers the inverse of the symbol duration orthogonality is ensured. Thus, the combination of multiple orthogonal sub-carriers transmitted in parallel with long-duration symbols guarantees the immunity of the overall broadband throughput to constraints related with non-line of sight (*NLOS*) environments and multi-path interference. This is depicted in Figure 1.4 [5].

By means of *OFDMA*, the use of *OFDM* is extended to a large number of users as a multiple access technology. *OFDMA* supports the assignment of individual groups of sub-carriers to specific subscribers, and thus transmissions from several subscribers can occur simultaneously without interfering among them. Each sub-carrier group is denoted as a sub-channel, and each subscriber is provided with one or more sub-channels for transmission based on his specific traf-

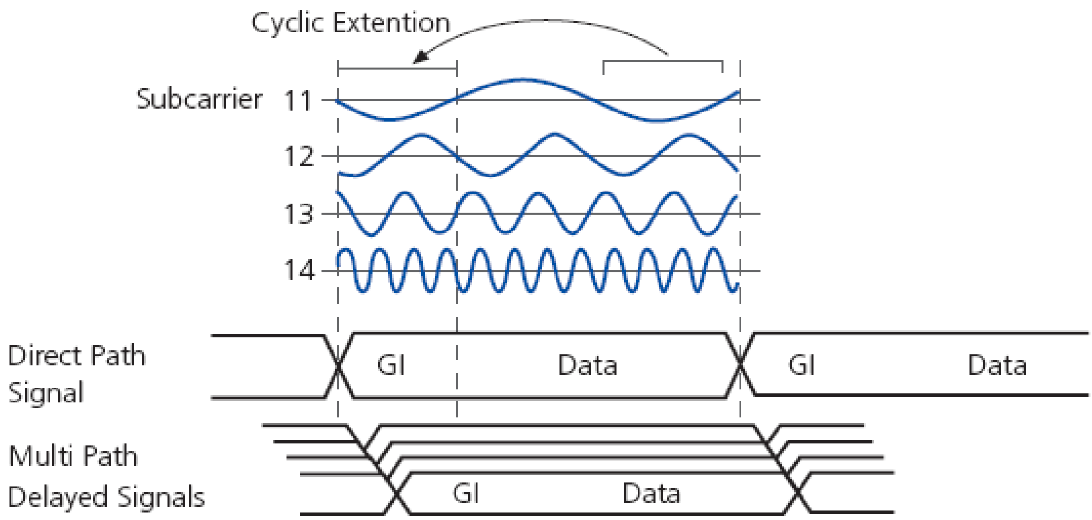

Figure 1.4: *Preservation of symbol integrity from multi-path in OFDM.*

fic requirements. Since sub-channelization enables the concentration of transmit power over reduced number of sub-carriers, an improvement in range and coverage is attained. Figure 1.5 depicts the concept of sub-channelization in *OFDMA* [5].

In order to deal with diverse usage scenarios and the challenges associated with rapidly moving mobile users in a *NLOS* environment, the IEEE 802.16e-2005 standard provides three sub-channel allocation alternatives that can be selected based on the usage scenario as follows [1], [5]:

- **FUSC** - Sub-carriers can be scattered throughout the frequency channel range.
- **PUSC** - Several clusters of sub-carriers can be used to form a sub-channel.
- **AMC** - Sub-channels can be composed of contiguous groups of sub-carriers.

In general terms, **FUSC** and **PUSC** are the best alternatives for mobile applications, whereas **AMC** is the most favorable for stationary, portable, and low mobility applications.

On the other hand, considering that regulators assign varying amounts of spectrum to different service providers, it is convenient that the *OFDMA* parameters can be optimized in proportion to the bandwidth granted to a specific service provider. *S-OFDMA* provides the ability to adjust *OFDMA* in accordance

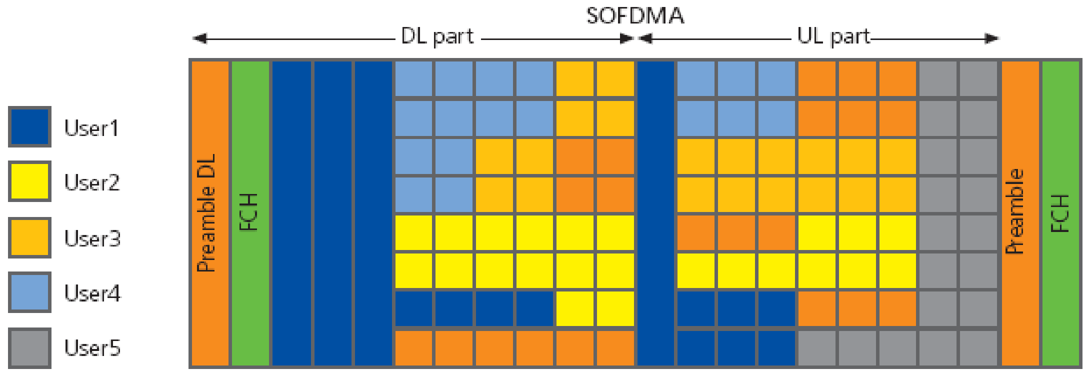

Figure 1.5: *Sub-channelization in OFDMA.*

Table 1.1: *Initial MW profiles.*

Channel Bandwidth	**2.3-2.4 GHz**	**2.305-2.32 2.345-2.36 GHz**	**2.496-2.69 GHz**	**3.3-3.4 GHz**	**3.4-3.8 GHz**
1.25MHz					
5MHz	**TDD**	**TDD**	**TDD**	**TDD**	**TDD**
7MHz				**TDD**	**TDD**
8.75MHz	**TDD**				
10MHz	**TDD**	**TDD**	**TDD**	**TDD**	**TDD**
20MHz					

with the bandwidth of the channel being used. The frequency bands and channel bandwidths considered for the initial MW profiles are summarized in table 1.1. As can be seen, the MW release-1 profiles only cover the 5, 7, 8.75 and 10 MHz channel bandwidths for licensed worldwide spectrum allocations in the 2.3, 2.5, 3.3, and 3.5 GHz frequency bands in a time division duplex (TDD) mode. Other bands, channel bandwidths, and frequency division duplex (FDD) mode will be considered for future profiles based on specific market opportunities [6].

The 2.5GHz band is of particular interest since it corresponds to the radio spectrum allocation assigned to many countries in south, central, and North America, including the United States. According to table 1.1, a TDD mode of operation and channel bandwidths of 5 and 10 MHz are considered as the initial

Table 1.2: *MW scalability parameters.*

Parameters	Value
System Channel Bandwidth [MHz]	**1.25, 5, 10, 20**
Number of Sub-channels	**2, 8, 16, 32**
Sub-carrier Frequency Spacing [KHz]	**10.94**
Useful Symbol Time $(T_b = 1/f)$ $[\mu sec]$	**91.4**
Guard Time $(T_g = T_b/8)$ $[\mu sec]$	**11.4**
OFDMA Symbol Duration $(T_s = T_b + T_g)$ $[\mu sec]$	**102.9**
Frame Duration [msec]	**5**
Number of OFDMA Sysmbols (5msec Frame)	**48**

Table 1.3: *Supported Code and Modulations.*

Modulation scheme	Code Rate CCT	Code Rate CCT	Repetition
UL:*QPSK, 16QAM, 64QAM**	$\frac{1}{2}, \frac{2}{3}, \frac{3}{4}, \frac{5}{6}$	$\frac{1}{2}, \frac{2}{3}, \frac{3}{4}, \frac{5}{6}$	**x2, x4, x6**
DL:*QPSK, 16QAM, 64QAM*	$\frac{1}{2}, \frac{2}{3}, \frac{3}{4}, \frac{5}{6}$	$\frac{1}{2}, \frac{2}{3}, \frac{3}{4}, \frac{5}{6}$	**x2, x4, x6**

$*$ Not mandatory but optional

profiles for this band. Some important parameters related to the bandwidths for the release-1 profiles are compiled in table 1.2.

Support for *QPSK*, *16QAM* and *64QAM* modulation schemes is mandatory for the DL whereas the 64QAM modulation is optional in the UL. Both Convolutional Code (CC) and Convolutional Turbo Code (CTC) with variable code rate are aided as well. Block Turbo Code and Low Density Check Code are supported as optional features. Table 1.3 summarizes the coding and modulation schemes assisted in the MW profile [1], [7]. The combination of various modulations and code rates provide a fine resolution of data rates.

Since the signal to be transmitted is formed by several sub-carriers mod-

Table 1.4: *Transmission parameters.*

Parameters	**5MHz & 10MHz BW**[1]	**5MHz & 10MHz BW**[2]
ACPR [dB]	≥ 30	≥ 44
PAPR [dB]	12	12
Output Power [dBm]	≤ 23	≤ 23

Table 1.5: *Transmission parameters.*

Burst type	**EVM [dB]**
QPSK $\frac{1}{2}$	**15**
QPSK $\frac{3}{4}$	**18**
16QAM $\frac{1}{2}$	**20.5**
16QAM $\frac{3}{4}$	**24**
64QAM $\frac{1}{2}$	**26**
64QAM $\frac{2}{3}$	**28**
64QAM $\frac{3}{4}$	**30**

ulated at different frequencies, then its amplitude varies with time. At certain instants, those sub-carriers overlap in such a way that the amplitude of the envelope is higher than the average value. The peak-to-average power ratio (PAPR) established for MW is defined considering a probability of 10^{-3} that the peak excursions exceed the average power of the signal [8], [9]. On the other hand, the nonlinearities associated with the PA produce an spectral regrowth into the adjacent frequency bands. Hence, a spectral mask is defined to set a limit upon the leakage power allowed into the adjacent channels. That limit is the adjacent channel power ratio (ACPR), which is the ratio between the power within the transmission band and the power within the adjacent band. National regulatory bodies and network service providers set ACPR performance. Unwanted emission characteristics for *OFDMA* TDD wireless metropolitan area network (WMAN) mobile terminals in the United States have been recommended by the International Telecommunication Union (ITU) [10]. Table 1.4 summarizes the values for the ACPR, PAPR, and output power for MW.

Another important parameter in the transmitter chain is the error vector magnitude (EVM). It is employed to quantify the performance of the transmitter. According to the WiMAX standard, the EVM varies depending on the transmission burst type [1], [7], [8]. Table 1.5 summarizes the diverse values of the EVM for MW.

1.3 Performance Demands of Mobile WiMAX on the Transmitter

A major drawback of *S-OFDMA* is the high PAPR attained. A high PAPR establishes constraints on the linearity of the transmitter, specially on the Power Amplifier (PA) since it has to include the high peak power value in its amplification range. Furthermore, the requirement of the maximum output power at the load is an event that rarely occurs. Instead, the average output power is more frequently demanded. The maximum output power required by MW is 23dBm ($\approx$ 200mW) and the output power back-off established by the standard is 12dB (table 1.4). That means that the average output power is 11dBm ($\approx$ 12.6mW). Hence, both of those extreme values must be delivered by the PA with a limit on the amount of distortion allowed in the adjacent bands. That limit is settled by the ACPR. As can be seen in table 1.4, the standard have resolved an ACPR for MW of 44dB. That is, the power within the transmission band must be around 25120 times higher than the power of the spectral regrowth generated within the adjacent bands. Therefore, a highly linear performance in the PA is mandatory.

Reducing the PAPR is desirable. In fact, there are a lot of publications with many types of PAPR reduction techniques [11]. Most of these approaches are applied to the baseband signal in the digital domain. It is difficult to establish a unified criterion to compare all of those PAPR reduction methods since each of them presents advantages over the rest in certain situations. For instance, *clipping without clipping noise reduction* is the simplest approach but with a poor bit error rate (BER) performance. On the other hand, coding methods such as *the Reed Muller coding* are more complex and require bandwidth expansion. However, they exhibit the largest PAPR reduction and the best BER performance [12].

Nonetheless the existence of PAPR reduction methodologies, the *OFDM* signal to be transmitted still faces the nonlinearity of the PA to various extents depending on different tolerable performance degradations, e.g. the ACPR, and the desired efficiency of the amplifier.

Efficiency is also an important issue. It must be taken into account that the standard has been planned for MW, i.e. it is intended for portable terminals. Typically, portable terminals are biased with batteries and, in that case, long duration working times are preferable. Most frequently, the PA is the most power-hungry block in the transmitter. Therefore, the more efficient it is, the more adequate use of the energy it presents. Consequently, a highly-efficient PA will have a better impact on the battery consume of the terminal.

1.4 Conclusions

The salient features of MW are highlighted as follows:

- The support of cost-effective broadband access services over large geographic areas with mobile transmission scenarios.
- High data rates.
- Improved multipath performance in *NLOS* environments.
- The capability to operate in scalable channel bandwidths to comply with various spectrum allocations worldwide.
- QoS.

In order to provide the necessary channel robustness for the support of a high spectral efficiency, MW employs *S-OFDMA*. Unfortunately, the use of *S-OFDMA* results in a high PAPR, which imposes stringent requirements on the transmitter, specially on the linearity of the PA, which has to include the high peak power value in its amplification range. Moreover, the ACPR established for MW tolerates an spectral regrowth of, maximum, -44dBc. On the other hand, since MW has been planned for being used in portable terminals, it is preferable to make use of an efficient PA to extend the duration of the battery which provides the power supply to the terminal. Therefore, a linear and efficient PA is demanded.

Chapter 2

Power Amplifier Fundamentals

2.1 Introduction

There are some systems where electrical signals are weak enough such that those are not able to transfer the adequate amount of energy required by a determined load. Therefore, there is the need to reinforce somehow such signals. The amplifier is one of the most important building blocks in the electronics field. As its name suggests, it has the ability to produce an strengthened replica at its output of the signal fed at its input. In particular, a **Power Amplifier (PA)** is intended to provide some power gain between its input and output ports.

PAs are commonly associated with audio systems, driving loudspeakers. However, this is just one of the numerous PA applications. In the wireless communication (RF) world, PAs are used to hand over the sufficient energy to the antenna for transmission. Figure 2.1 shows the general scheme of a conventional RF PA. As can be seen, it consists of an active device, usually a transistor of some kind (BJT, HBT, MESFET, MOSFET, LDMOS), which provides the amplification mechanism; an RF choke inductor, that fixes the DC value at the drain/collector terminal; a matching network, whose labor is to match the impedances between the load and the amplifier as well as tuning the amplifier at the frequency of interest; and finally a load, which normally corresponds to the load of the antenna.

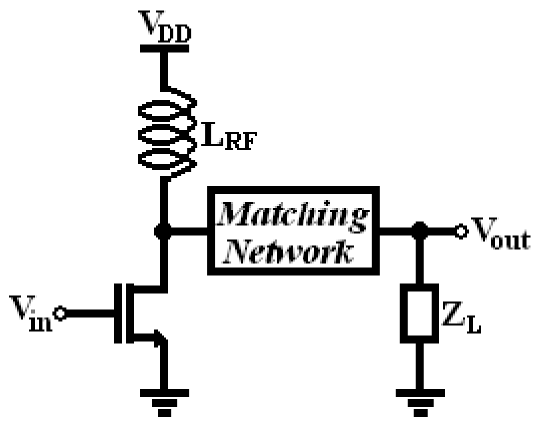

Figure 2.1: *General scheme of a conventional RF PA.*

2.2 Power Amplifier Performance Metrics

There are some metrics which characterize the performance of an RF PA. Those are: the *power capacity (PC)*, the *linearity*, and the *efficiency*. The PC is a measure of the amount of output power that can be delivered by the PA when its active device operates under the maximum reliability limits of the technology. It is defined by [13]:

$$PC = \frac{P_{out}}{I_{max} \cdot V_{max}} \tag{2.1}$$

where P_{out} is the output power delivered to the load and I_{max}, V_{max}, are the maximum current limit and the maximum voltage limit of the device, respectively.

The linearity of a PA can be estimated in different ways. One possibility is by means of the two-tone test. In case that a two-tone signal with a small frequency separation between the tones is fed to the input of the PA, then, at the output, the n-th order intermodulation (IM) products will appear at n times the frequency spacing of the input tones. Thus, if we plot on a logarithmic scale the output power versus the input power, diverse curves are obtained; one of those curves corresponds to the spectrum of the desired signal and the rest belong to the IM products caused by the non-linearity of the PA. By extrapolating the linear part of these graphs, diverse intercept points are obtained. Such intercept points give a measure of the non-linearity of the amplifier. Figure 2.2(a) depicts the third order intercept point (IP3) of a nonlinear PA produced by the third order

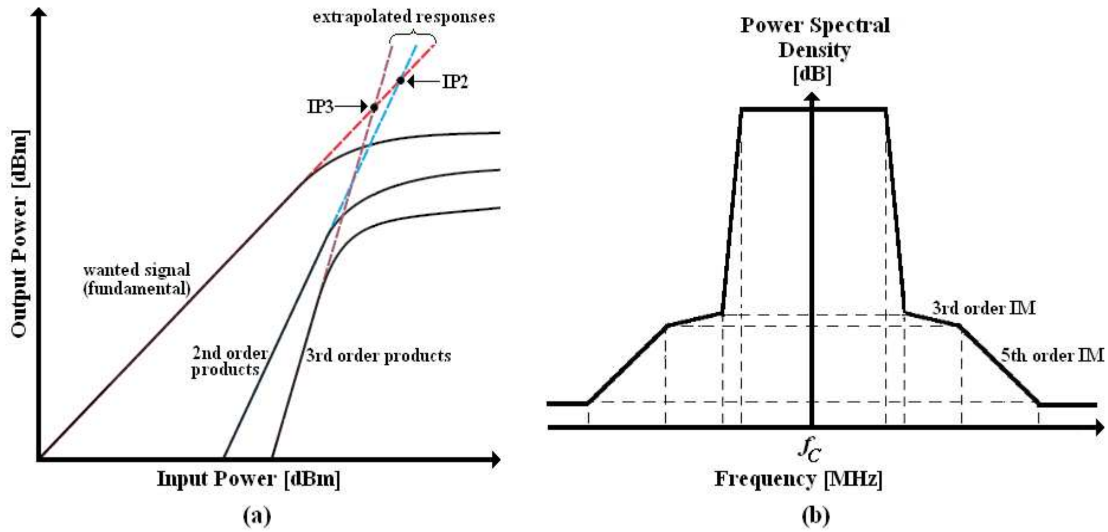

Figure 2.2: *Estimation of the linearity of an RF PA: (a) the two-tones test, and (b) spectral mask.*

distortion level when applying the two-tone test. Another manner to assess the linearity of a PA is by defining a spectral mask. In this case, the input signal to the PA is codified under a given modulation scheme. The spectral mask establishes an upper bound about how much power can be transmitted at frequencies close to the RF carrier. Figure 2.2(b) shows the spectral mask defined for mobile WiMAX.

The efficiency measures the ability of the PA to deliver power to the load by converting the DC power from the power supply into AC signal at the output of the amplifier without wasting so much energy in the process. Three definitions are commonly used in the literature: the drain efficiency (η_D), the power added efficiency (PAE), and the overall efficiency ($\eta_{overall}$). The η_D of a PA is defined as [13]:

$$\eta_D = \frac{P_{out}}{P_{DC}} \tag{2.2}$$

where P_{out} is the output power transferred to the antenna and P_{DC} is the power drawn from the DC power supply.

The PAE is defined as [13]:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{2.3}$$

where P_{in} is the power delivered at the input of the PA.

Finally, the $\eta_{overall}$ is defined as [13]:

$$\eta_{overall} = \frac{P_{out}}{P_{DC} + P_{in}} \tag{2.4}$$

According to expressions (2.2), (2.3), and (2.4), we can see that the η_D does not consider the power delivered by the input signal. The effect of the P_{in} can be ignored if the power gain of the PA is high or if its input impedance is predominately reactive. If neither of those circumstances happens, then, P_{in} may become a substantial portion of the output power. In that case, the PAE and the $\eta_{overall}$ provide a more accurate estimation about the efficiency performance of the PA. Actually, since the total dissipated power is a function of the P_{out} and the P_{DC} [14], the $\eta_{overall}$ is the most significative quantity from a thermodynamic point of view. Nonetheless, the PAE is still the most popular measure in industry.

2.3 Classification of Power Amplifiers

Figure 2.1 shows the general scheme of a conventional RF PA. Based on the utilization of the active device, conventional PAs can be primarily classified into two groups: transconductance PAs, which employs the transistor as a transconductor, and switched PAs, where the transistor is occupied as a switch. Amplifiers labeled as classes A, AB, B, and C belong to the first group while amplifiers classes D, E and S reside in the second group. There are some classes of operation where the transistor is driven in both ways, as a transconductor and as a switch, e.g. class F PA. Furthermore, there are some other classes of operation where the device is employed as a transconductor but it also has switches which switch the bias supplies when necessary, e.g. classes G and H PAs.

Transconductance PAs present a higher linearity whereas switched PAs exhibit a better efficiency. Generally speaking, in conventional PAs, when the linearity rises the efficiency drops. Hence, there is a linearity-efficiency trade-off in these type of PAs.

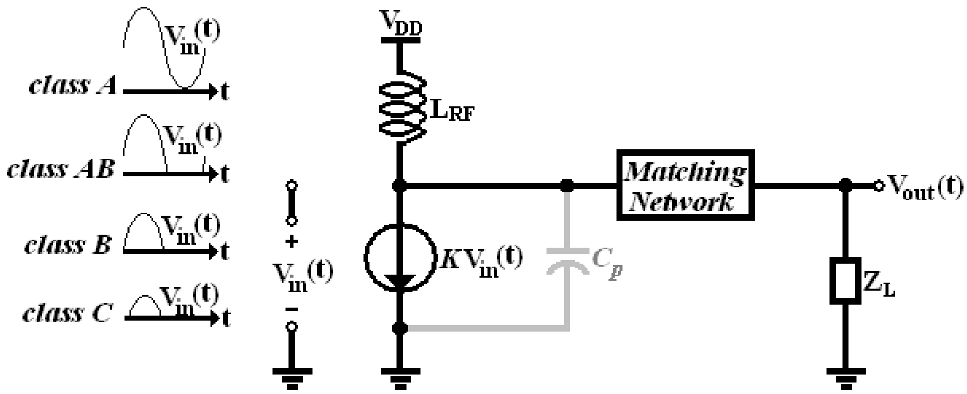

Figure 2.3: *Configuration of a typical transconductance PA.*

Table 2.1: *Ideal linearity-efficiency characteristics of transconductance PAs.*

PA	Linearity	Efficiency
Class A	High	25%-50%
Class AB	High-Moderate	Variable(ϕ)
Class B	Moderate	50%-78.5%
Class C	Moderate-Low	Variable(ϕ)

ϕ is the conduction angle

2.3.1 Transconductance Power Amplifiers

As mentioned above, PA classes A, AB, B, and C correspond to transconductance Power Amplifiers. They all have a similar circuit configuration distinguished essentially by biasing conditions. Figure 2.3 illustrates this concept. The principle of operation of a class A PA is similar to that of a small-signal amplifier. It works over the entire cycle of the input signal and generates, at its output, an amplified replica of the input, ideally without clipping. Since the transistor is biased to amplify over the entire input cycle, it wastes much power even if it is not necessary, i.e. in the absence of an input signal. Therefore, the efficiency of a class A PA is rather poor. In order to enhance the efficiency, the technique of amplifying a signal with a reduced conduction angle is used. This approach consists of biasing the active device such that its input signal turn it on only for part of the input cycle. As the conduction angle becomes smaller, the PA moves from class AB, to class B and eventually class C. As a result, the efficiency rises

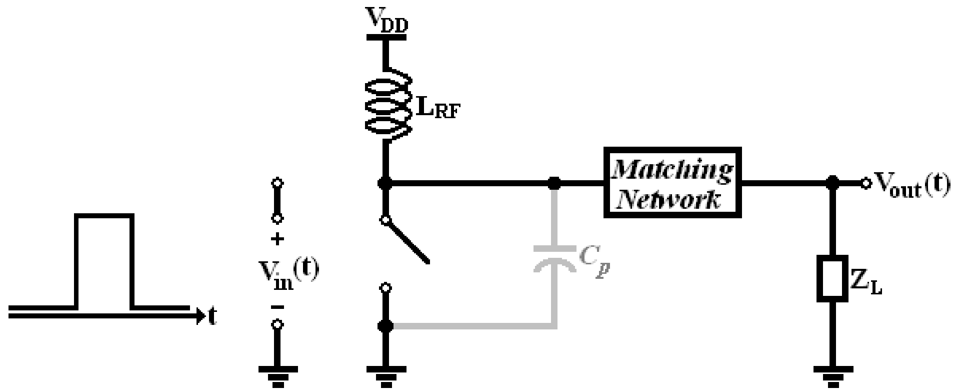

Figure 2.4: *Configuration of a typical switched PA.*

but also linearity drops. A common practice to improve the linearity of the output signal to some extend is to place a matching network which resonates with the parasitic capacitance of the transistor at the frequency of interest. Table 2.1 shows the ideal linearity-efficiency characteristics of transconductance PAs [15].

2.3.2 Switched Power Amplifiers

In PA classes *D*, *E* and *S* the transistor is driven as a switch. In general terms, there is no current flowing through an ideal switch when it is open and, on the other hand, there is no a voltage drop between the terminals of an ideal switch if it is closed. Therefore, the efficiency of a switched PA is, theoretically, 100%. In reality, however, there are no ideal switches and some losses are present in the circuit leading to a lower efficiency. Nevertheless, the efficiency exhibited by a switched PA is higher than that attained by a transconductance PA. The high efficiency reached by a switched PA is obtained at the expense of a non-linear output signal. Thus, switched PAs are known also as non-linear PAs. Figure 2.4 shows the configuration of a typical switched PA.

A class *D* PA consists of a voltage controlled switch and a matching network which is tuned to the fundamental frequency. Hence, it has a negligible impedance at the frequency of the fundamental and a high impedance at harmonic frequencies. The class *S* PA works in a similar way to the class D with the difference that the input signal to a class D has a duty cycle of 50% whereas the input waveform to the class *S* amplifier has a variable duty-cycle [14]. Thus, the different pulse widths produce different average outputs to form the desired waveform. On the other hand, in a class E PA the parasitic capacitances of the transistor are absorbed into a wave-shaping/matching network. During operation, the waveforms of the drain current and the voltage are shaped such that they do not overlap. Moreover, the voltage decreases gradually to zero before the transistor is turned on. This avoids to charge and discharge the capacitor at the drain, which improves the efficiency. Nonetheless, the class E PA has the drawback of exhibit a high peak voltage, which may cause damage to the active device.

2.4 Conclusions

A high linearity and a good efficiency are difficult, if not impossible, to get with conventional PAs. On one hand, the linearity of transconductance PAs decreases as the conduction angle of the input signal is reduced, but at the same time, the efficiency rises. On the other hand, switched PAs are essentially non-linear amplifiers, yet, their efficiency is better when compared to that attained with their transconductance counterparts.

The election of a particular class of operation depends on the needs of the system where the amplifier is going to be placed. If both, linearity and efficiency are wanted, then, a transconductance PA with a good trade-off between those figures of merit can be preferred. For instance, a class B or class C amplifer. However, if the linearity demands are stringent, then, the non-linearity introduced by such amplifiers may be inadmissible. Even though classes of operation such as AB and A are, in theory, more linear, in practice, however, the active devices employed in PAs have non-linearities that produce detrimental effects into the system. Therefore, there is the need to improve the linearity of conventional PAs. Specially when the demands of the system where they are used are strict, e.g. the mobile WiMAX technology.

Chapter 3

Power Amplifier Linearization Techniques

3.1 Introduction

In electronics, a Power Amplifier (PA) refers to an amplifier which provides some power gain to a signal in order to deliver the adequate amount of energy required by a determined load. Generally speaking, linear PAs are those which satisfy the superposition principle. In the frequency domain, this implies that the response of a linear, time-invariant PA, includes only those frequencies present at its input, i.e. the amplifer does not generate new frequencies at its output (distortion). On the other hand, non-linear PAs generate a number of new frequency components at their output. Depending on the system in which the PA is going to be employed, some of those new frequency elements may be unwanted due to the pernicious effects they introduce into the system. This is the case of some wireless communication transmitters, like those envisaged for mobile WiMAX terminals, where the spreading of the transmitted spectrum, so-called spectral regrowth, can be tolerated only at some level within a confined bandwidth in order to avoid interfering with other transmissions. Figure 3.1 illustrates these concepts.

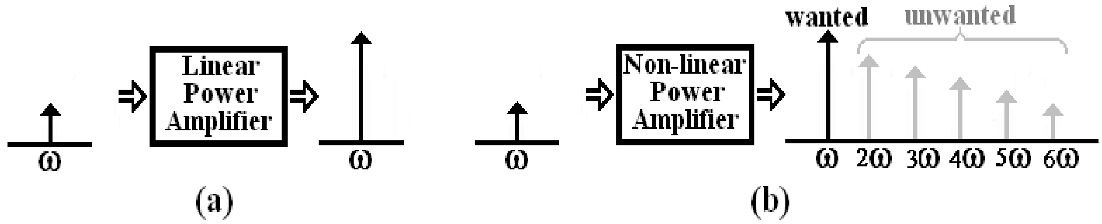

Figure 3.1: *Frequency response of a PA with a single tone signal at its input: (a) Linear PA, (b) Non-linear PA.*

3.2 Non-linear Effects in RF Power Amplifiers

In practice, however, the devices used in PAs, such as transistors, have nonlinearities that produce an output signal with new frequency components to some extent. The non-linear transfer characteristic of an amplifier can be modeled in several ways, e.g. power series or Volterra series can be used to describe the non-linearity of weakly non-linear PAs [16]. Even though polynomial modeling does not describe with adequate accuracy the input-output characteristic of strongly non-linear amplifiers [17], it allows an easy calculation of the spectral components and provides a more comprehensible perspective about the problem of generating distortion. Hence, it is an useful tool in the design of PAs. An standard power series formulation for a PA can be written as [18]:

$$v_0 = a_0 + a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + a_4 v_i^4 + a_5 v_i^5 + \dots \tag{3.1}$$

where v_i and v_0 are the input and output voltages of the amplifier, respectively, and the coefficients a_i describe the non-linear characteristic of it.

Based on this formulation and relying upon the characteristics of the input signal, v_i, different distortion types arise [19], [20]: harmonic distortion, which occurs when v_i consists of a single tone signal; intermodulation (IM) distortion, present when v_i is compound of a two-tones signal; cross modulation (XM) distortion, which takes place when v_i is composite by a two-tones signal and one of those is modulated; and spectral regrowth, which appears when v_i is a more complex modulated signal, e.g. a digital modulated signal. Thus, in the case of RF PAs, the modulation scheme used for transmission will produce a determined distortion type. In particular, for mobile WiMAX terminals, the modulation schemes

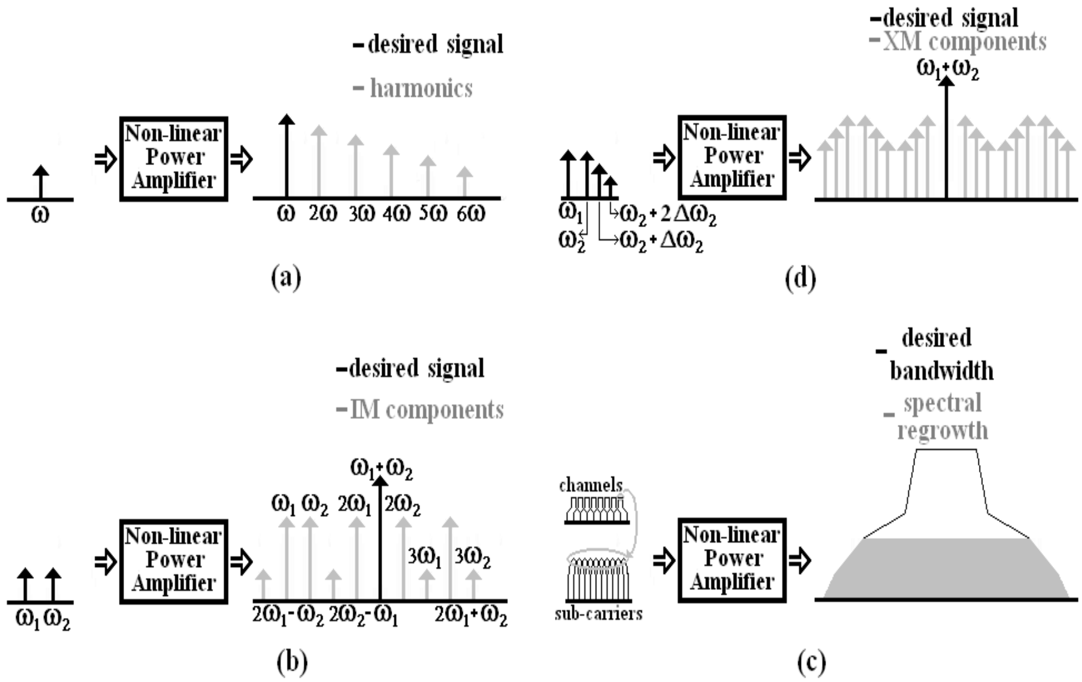

Figure 3.2: *Different distortion types produced by a non-linear PA: (a) harmonic distortion, (b) IM distortion, (c) XM distortion, and (d) spectral regrowth.*

employed for transmission are *QPSK* and *16QAM*, therefore, a spectral regrowth over a continuous band of frequencies will be present at the output of the PA. Figure 3.2 depicts the different distortion types.

In order to quantify the linearity of PAs there are some linearity metrics commonly used. One of those is the adjacent channel power ratio (ACPR), which is an important test parameter for characterizing the spectral regrowth of PAs and the likelihood that a given PA may cause interference with a neighbor communication channel [21]. Many wireless communication systems specify the minimum ACPR for an explicit bandwidth at a given channel separation. For mobile WiMAX, the minimum ACPR is -44dB for a 10MHz bandwidth with a channel separation of 10Mhz. This means that the output power within a transmission channel of 10MHz must be, at least, about 160 times larger than the power generated by the spectral regrowth in a 10MHz vicinity. Consequently, the linearity demands of the systems are quite stringent. Figure 3.3 shows the spectral mask established for mobile WiMAX.

Since there are no perfect linear PAs, and the linearity requirements of some

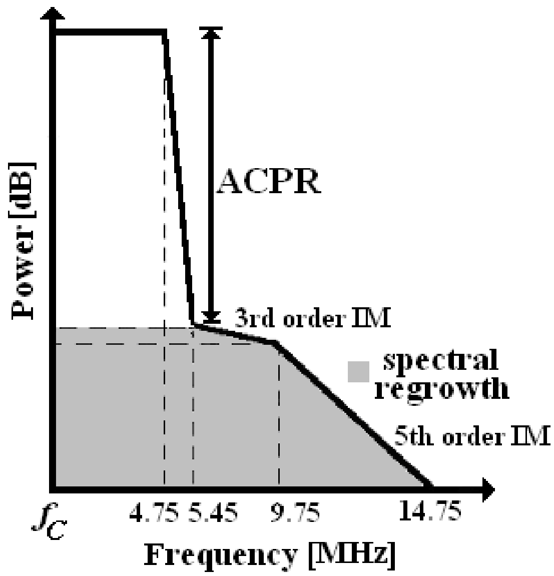

Figure 3.3: *Spectral mask for mobile WiMAX.*

wireless technologies are rather severe, as in the case of mobile WiMAX, then, some form for linearizing PAs is necessary. In fact, diverse approaches have been proposed in order to improve the linearity of RF PAs.

3.3 Linearization Techniques

Typically, our interest focuses on the distortion produced by the PA onto its input signal. Hence, it makes sense to use the input signal as the reference with which to compare the distorted output signal, and thus to generate the appropriate corrections. Since there are only two signals present in the system, at the input and at the output, then, the corrections can be applied to either. A first distinction among PA linearization techniques can be done based on the way the signal correction is applied [18]. If correction is accomplished at the input, then, two major groups of linearization approaches can be distinguished: *feedback* and *predistortion*. On the other hand, if the signal correction is performed at the output, then, another group of linearizers is obtained: *feedforward*. In the following subsections, a brief description of some of the most important linearization methods is presented.

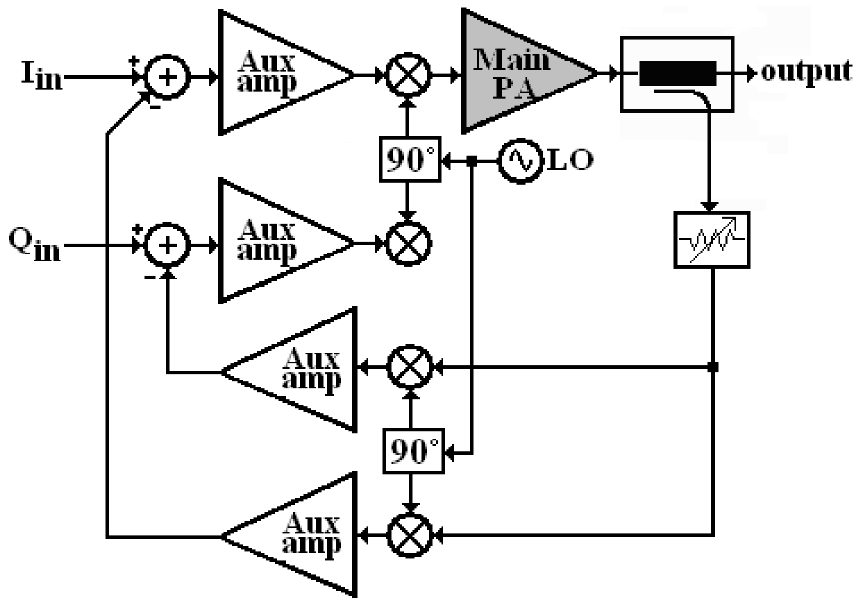

Figure 3.4: *Cartesian loop feedback PA.*

3.3.1 Feedback

Regardless its effective use in many different electronic systems, the utilization of feedback for the linearization of RF PAs has not yet been successfully applied due to the problematic of having a considerable time delay of the propagating signal through the PA in comparison to the timescale on which the signal itself is changing [18]. This, in turn, will lead to a conditional stability of the feedback circuit, which must be achieved under a wide range of conditions.

An alternative for making use of a feedback loop to improve the linearity of an RF PA consists of providing the feedback at lower frequencies by downconverting the amplified signal to either, IF or baseband frequencies. One possibility to accomplish this is by means of a cartesian loop, which is, by far, the widespread feedback technique used for linearizing RF PAs [22]. Figure 3.4 illustrates the block diagram of a cartesian loop feedback PA. The technique is specially suited for modulation schemes that use both amplitude and phase to convey information. By bringing into play the in-phase and quadrature components of the input and output signals, a cartesian loop feedback PA corrects the errors present in the amplitude and the phase.

The cancellation performance achieved by means of the Cartesian feedback

PA is good. Nevertheless, the bandwidth in which the system can work without running into stability issues is rather narrow, making the technique inappropriate for very wideband systems. Diverse experimental cartesian loop feedback PAs have been reported operating at frequencies ranging from a few Megahertz to a couple of Gigahertz with modulation bandwidths of up to 500kHz [23]. Distortion suppression varies from 20dBc up to 50dBc.

A potential problem for Cartesian feedback transmitters is the fact that the non-linear characteristics of the PA degrade the gain and phase margins of the loop. Moreover, the phase shift that occurs in the loop when, for example, changing the carrier frequency, obligates to add a phase adjuster into the system in order to fix automatically the phase and thus preserve the stability of the overall system. This, eventually, increases vastly the complexity of a practical cartesian feedback transmitter.

3.3.2 Predistortion

If it were possible to predistort the input signal to the PA with the inverse of the PA non-linearity, then the overall effect of the non-linearity could be cancelled out. Based on this idea, several methods have been developed in order to realize the predistorter which modifies the input signal. Such approaches, invariably, fall into either of the following categories: analog (RF) predistorters or digital (baseband) predistorters.

- **Analog predistortion**. Figure 3.5 depicts the block diagram of an analog predistorted PA. As can be seen, one or more non-linear devices are placed between the input signal and the main amplifier. The non-linear transfer characteristic of the predistortion stage must be exactly opposite to the non-linear transfer function of the main amplifier. As a result, the total distortion gain will be 0dB. This technique uses constant predistortion factors, thus the transfer function of the main amplifier must be thoroughly characterized. Analog predistortion suffers from several practical drawbacks [19]. It is very difficult to precisely track the effects of temperature, process, and power supply variations on the non-linear characteristics of the PA. This is a serious drawback, because the amount of acceptable distortion in a typical

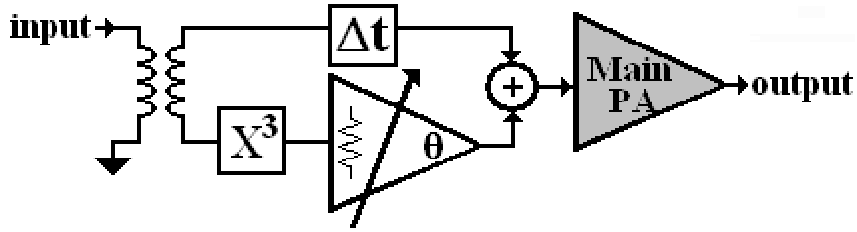

Figure 3.5: *Analog predistorted PA.*

2G or 3G system, to name some examples, is very low, and a small offset in the characteristics of the power amplifier and the predistortion circuit can create substantial out-of-band interference. The use of polynomial functions and a simple adaptation scheme based on out-of-band power measurements offers low cost and complexity. However, a low-order polynomial is capable of canceling only weak non-linearities. For PAs with a more severe non-linearity, more dedicated schemes based on digital signal processing (DSP) techniques and look-up tables have been developed.

- **Digital predistortion**. The rapid progress in DSP technology has brought new resources for improving the linearity of transmitters. In fact, digital predistorted PAs has been one of the most active research areas in the linearizers development. One of the key factors for such advance is the possibility of modifying digitally the baseband signal which, in upconverted format, is fed to the PA at any given time. Diverse digital predistorted PA architectures have been proposed [24], Figure 3.6 puts on view some of the most widespread.

  Originally, the digital predistortion approach used a look-up table (LUT) with curve fitting to realize an adaptive predistorter PA. Unfortunately, this have the disadvantage that transmission must be interrupted to realize the adaptation process. An alternative solution is offered by the Mapping predistortion technique (Figure 3.6a), which by means of using a two-dimensional LUT is capable to map into a new constellation any complex input signal represented by its cartesian components. Hence, any distortion present in the conversion process can be cancelled online. The major drawback of such procedure is the size of the two-dimensional LUT, which results in long

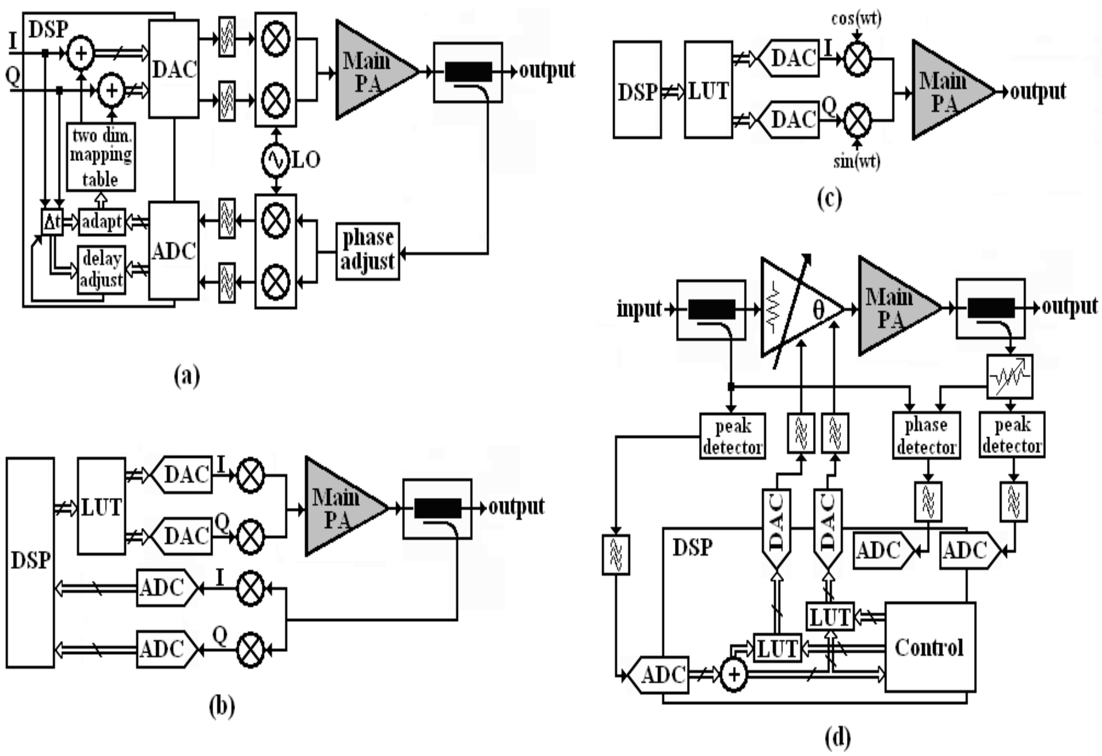

Figure 3.6: *Digital predistorted PA.*

adaptation times.

On the other hand, polar predistorted PAs (Figure 3.6b) take advantage of two one-dimensional LUTs containing magnitude gain and phase rotation. Since the adaptation process is based on polar coordinates, the technique requires a large quantity of operations to predistort the signal. This leads to a substantially larger computational load compared with the mapping predistorter PA. However, the table size in the polar predistorter is much smaller than in the mapping predistorter. As a result, the adaptation time is rather short. In spite of this, the modulation bandwidth is pretty narrow. The complex gain predistorted PA (Figure 3.6c) has a LUT which contains complex-valued gain factors given in cartesian form. The address to the table is calculated as the squared magnitude of the input signal, which gives a uniform distribution of power in the table entries. Furthermore, the input signal is predistorted by a single complex multiplication. The adaptation scheme of this approach is multiplicative in contrast to the mapping predistorter, which is additive. Consequently, the complex gain predistorter PA is not sensitive to the phase of the feedback signal, as is the case for the mapping predistorter. This solution assumes a phase-invariant characteristic which depends heavily on the use of perfect quadrature modulators and demodulators.

An alternative to digitally predistort the input signal to the PA is via vector modulation (Figure 3.6d). In such methodology, the RF-predistortion is carried out by transforming the analog PA input signal by analog means controlled by digital signals. The phase and envelope of the input and output signals are detected by analog means and then converted to digital format. The result is provided to a DSP that retrieves phase and amplitude correction values corresponding to the input envelope value from a LUT. The limiting factors in the vector modulation technique are mainly related to the analog parts of the circuit. The envelope detection process generates signals that have a higher bandwidth than the original modulation bandwidth of the RF signal. Therefore, the vector modulation approach is mainly suitable for narrowband systems.

In general terms, one of the problems that the digital predistorted PAs face is the fact that the transfer characteristics of the predistorter exhibits memory effects, and therefore, the algorithm performing the predistortion must be periodically updated [24].

Digital predistorted PAs are more efficient to cancel distortion components than their analog counterparts [19]. However, their effectiveness depends on the availability of the system to provide both, a priori knowledge of the signal modulation in digital form, and a phase coherent sample of the RF carrier used to perform the downconversion [18]. There are some wireless communication systems where neither of those requisites can be met.

3.3.3 Feedforward

In the feedback technique, the error is detected and subtracted at the input of the amplifier. Oppositely, the error is subtracted from a delayed version of the output in the feedforward approach. Some benefits of feedforward PAs are:

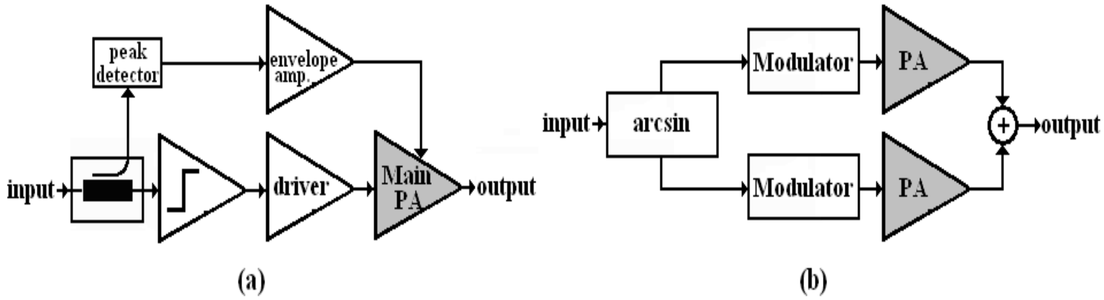

Figure 3.7: *Feedforward predistorted PAs: (a) EER PA, and (b) LINC PA.*

the gain-bandwidth is preserved within the band of interest; linearization are not sensitive to the PA delays; the method is unconditionally stable; the correction is not attempted based on past events, unlike in systems which employ feedback. Figure 3.7 show the most commonly used feedforward PAs.

Envelope elimination and restoration technique (EER) is a technique which attempts to linearize the PA by varying its power supply. The basic EER PA architecture (Figure 3.7a) combines a high efficiency non-linear PA with an envelope amplifier. It consists of a peak detector that subtracts the amplitude modulation and a limiter which takes the phase modulation from the carrier signal, respectively. The resulting phase modulated signal is amplified with any of the high efficiency amplification techniques. Finally, the original modulation is restored with an RF amplifier-modulator device. The major disadvantage of the EER PA is the phase mismatch introduced between the paths of the amplitude and phase processing stages [23].

The linear amplification using non-linear components (LINC), also known as outphasing PA (Figure 3.7b), basically improves the amplitude distortion without considering the phase distortion. It is based on the equivalence between an amplitude/phase modulated signal and two phase modulated signals [22]. Thus, the information to be transmitted is now phase modulated in two envelope constant signals. High efficient amplifiers can be used without linearity restrictions. Both phase-modulated signals are combined at the output. Some of the problematic related to LINC are the implementation of the signal separator at RF frequencies, which is extremely complex, and the signal combination at the output which is complicated since the signals are not in phase. Besides losses are introduced

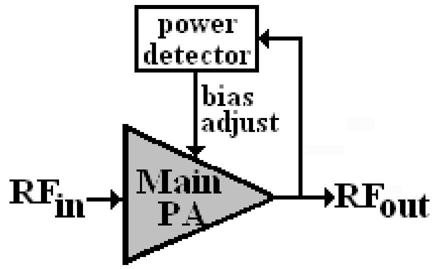

Figure 3.8: *Block diagram of a PA with bias adaptation.*

by the power combiner. These practical challenges become worse as the carrier frequency of the RF PA increases.

Generally speaking, Feedforward PAs suffer from a number of drawbacks that make them less popular than feedback amplifiers. Some of those shortcomings are [21]: the variations in the characteristics of the device with time and temperature are not compensated; the matching between the circuit elements in both amplitude and phase must be upheld to a very high degree over the correction bandwidth of interest; the circuit complexity is generally greater than that of a feedback system, especially with the demand of a second amplifier, which eventually leads to a greater cost and size.

3.3.4 Other linearization methods

In the previous subsections the foremost features of some linearization approaches were described. As mentioned earlier, those methodologies can be grouped into two of the following categories: linearizers based on signal correction performed at the input of the PA, and linearizers based on signal amendment applied at the output of the amplifier. A third possibility to increase the linearity of a PA lies on the modification of the attributes of the amplifier. There are not many techniques that employ this course. One of such schemes which adjust dynamically the traits of the PA is the bias adaptation procedure [18]. Figure 3.8 depicts the block diagram of a PA with bias adaptation. As can be seen, a power detector senses the output power and according with the detected level it modifies the bias of the main amplifier. Bias adaptation attempts to enhance both linearity and efficiency. Nevertheless, its effectiveness for cancelling distortion components is

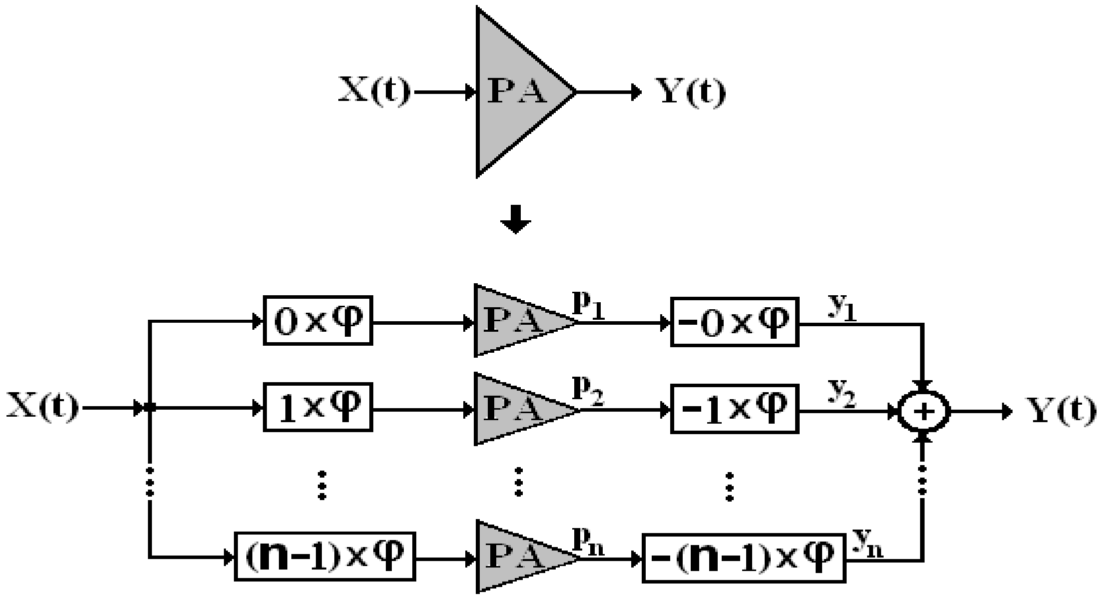

Figure 3.9: *Distortion cancellation with the multipath-polyphase scheme.*

rather low. Yet, it improves the efficiency of the PA at output power back-off [25].

Another approach which modifies the features of the amplifier in order to ameliorate its linearity is the multipath-polyphase technique [26]. Figure 3.9 shows the basic principle of distortion cancellation in a PA by means of the multipath-polyphase scheme. It can be appreciated that the non-linear PA is divided into n equal smaller amplifiers. Then, at the input of each stage, a phase shift is performed. Additionally, at the output of each amplifier, a similar but opposite phase shift is also accomplished. The magnitude of the phase shift depends on the number of stages employed. By adding all the signals from the amplifiers, the cancellation of diverse distortion components can be attained. The effectiveness of the cancellation performance lies on the number of phases used. The larger the number of phases is, the more linear the PA becomes [27]. Thus, the multipath-polyphase PA exhibits a high flexibility with regard to the linearity it can achieve. Moreover, the technique is well suited for broadband multi-carrier systems [28].

The main disadvantage of the multipath-polyphase procedure is the fact that it is sensitive to the phase mismatch among the signals on the different paths. However, a careful design can alleviate this problem [27].

Table 3.1: *Comparison of different linearized PAs.*

Approach	**Linearization performance**	**Bandwidth**	**Efficiency**	**Complexity**	**Capacity for multicarrier**
Cartesian Feedback	⋆⋆⋆	⋆	⋆⋆	⋆⋆	⋆
Analog Predistortion	⋆	⋆⋆	⋆⋆⋆	⋆	⋆⋆
Digital Predistortion	⋆⋆	⋆⋆	⋆⋆	⋆⋆⋆	⋆⋆
Feedforward EER	⋆⋆	⋆⋆	⋆⋆⋆	⋆⋆⋆	⋆⋆
Feedforward LINC	⋆⋆	⋆⋆	⋆⋆	⋆⋆⋆	⋆⋆
Bias Adaptation	⋆	⋆⋆	⋆⋆⋆	⋆⋆	⋆⋆
Multipath-Polyphase	⋆⋆⋆	⋆⋆⋆	⋆	⋆⋆	⋆⋆⋆

⋆⋆⋆ = high/wide, ⋆⋆ = moderate, ⋆ = low/narrow

3.4 Conclusions

Table 3.1 shows a comparison among the different linearization techniques formerly described. The linearization performance of the cartesian feedback is good. Besides, it presents moderated efficiency and complexity. Nonetheless, its narrow bandwidth and low capacity for multicarrier make it impractical for mobile WiMAX. On the other hand, the low capability for cancelling distortion components with analog predistortion and bias adaptation, make them also inappropriate for systems where the linearity claims are demanding. However, those approaches offer a high efficiency. A moderate linearization effect, medium bandwidth and middling efficiency are appealing characteristics of the digital predistortion, EER and LINC linearizers. Notwithstanding, their high complexity is a drawback which may be difficult to overcome, specially in a system such as mobile WiMAX, with very stringent performance requirements. Finally, the multipath-polyphase PA posses very attractive features: a high linearization performance with a wide bandwidth and a moderate complexity. Unfortunately, the efficiency attained with the PA proposed in [27] is quite low. Anyhow, the system was not intended to exhibit a high efficiency, therefore, there is the possibility to conceive a new design with a better power conversion ability.

Chapter 4

The Multipath-Polyphase Linearizer

4.1 Introduction

One of the difficulties to deal with in the implementation of mobile WiMAX transmitters is to establish a procedure that overcomes the difficulty of cancelling the distortion components produced by the non-linearities of the Power Amplifier (PA). This problem is severe due to the linearity requirements demanded by the standard.

An effective method for solving complex tasks is the so called *Divide and Conquer Principle*. It has been applied successfully in a wide variety of problems [29]. The main idea behind this principle is to break up a given complex task appropriately into a reasonable number or less complicated assignments so that by putting properly all of those solutions together some or even all solutions of the original complex task can be found.

The multipath-polyphase technique makes use of that principle to cancel, to some extent, the distortion components generated by a non-linear system. In theory, the quantity of distortion components that the technique is able to cancel depends on the number of phases employed. Therefore, the procedure offers a high flexibility, a wide bandwidth, and a high capacity for operating in multicarrier transmitters.

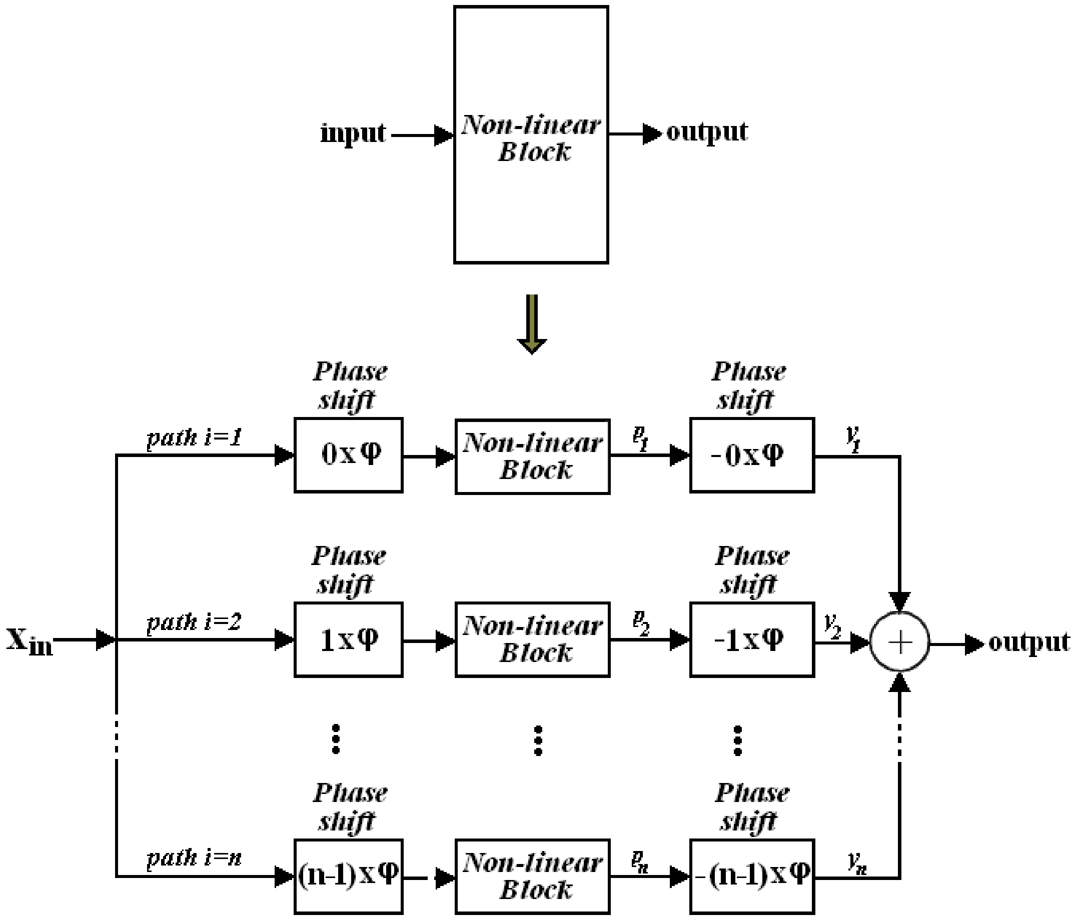

Figure 4.1: *The multipath-polyphase principle.*

4.2 The Multipath-Polyphase Technique

Figure 4.1 depicts the use of the multipath-polyphase approach to cancel the non-linearities produced by a non-linear system. As can be appreciated, the principle of cancelling distortion components lies on the basis of dividing the non-linear block into n smaller identical non-linear blocks placed on n different signal paths. Diverse phase shifts must be applied to the input signal on each path before it reaches the non-linear blocks. As a result, the signals from those blocks will present different phases for the fundamentals and the distortion components. Another phase shift must be executed at the output of the non-linear blocks. By doing this, the phases of the fundamentals are aligned and the phases of the distortion components are ordered such that their addition will cancel distortion.

Let the input signal in Figure 4.1 equal to $Acos(\omega t)$. Assuming that the transfer characteristic of the non-linear block in the time domain can be modeled as in the case of a memoryless weakly non-linear system, then, at the output of the non-linear block on the ith path we will have

$$p_i = \sum_{k=0}^{m} C_k (x_{in})^k = C_0 + C_1 Acos[\omega t + (i-1)\varphi] + \ldots + C_m A^m cos[m\omega t + m(i-1)\varphi] \tag{4.1}$$

where the C_k terms are constant coefficients from the power series and φ is the phase shift.

Afterwards this signal passes through the second phase shift, we will obtain

$$y_i = C_0 + C_1 Acos[\omega t] + \ldots + C_m A^m cos[m\omega t + (m-1)(i-1)\varphi] \tag{4.2}$$

Note that the phase of the fundamental component in this expression is identical for all the paths, but the phases of the harmonics are different for each path. Thus, by making $\varphi = 2\pi/n$, where n is the number of paths, the output signal will contain the fundamental term and, at the same time, will cancel the higher harmonics components with the exception of those who satisfy the following condition [26]

$$k = jn + 1 \tag{4.3}$$

where $j = 0, 1, 2, 3, \ldots$

Hence, if $n = 2$, then $k = 1, 3, 5, 7, \ldots$, i.e., only the odd harmonics components appear, as in the case of a differential amplifier. If $n = 3$, then $k = 1, 4, 7, 10, \ldots$, i.e., the second, third, fifth, sixth, eighth, ninth, and some other higher harmonics disappear. Theoretically, as n approaches to infinite, all the distortion components are completely cancelled [26]. Figure 4.2 illustrates the harmonics cancellation in a six paths six phases system.

It is important to assess the results attained with the technique when the input is a two-tone signal. If we make the input equal to $A_1cos(\omega_1 t) + A_2cos(\omega_2 t)$, besides harmonics the non-linear blocks will also produce intermodulation products (IM) at frequencies $\omega = p\omega_1 + q\omega_2$, where p and q identify harmonics of ω_1

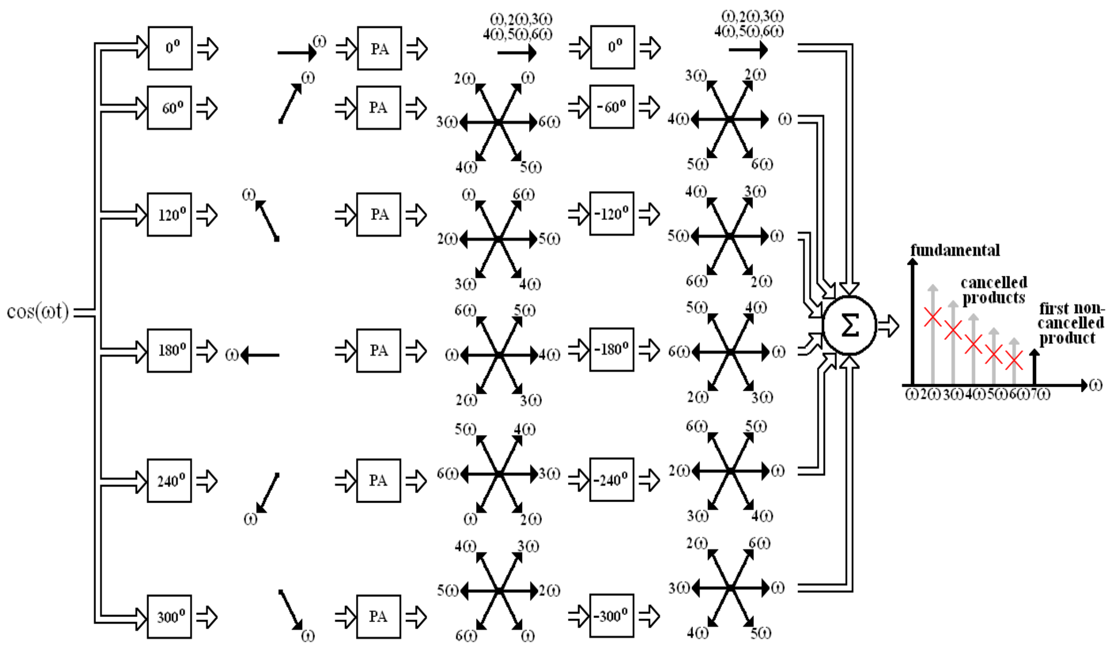

Figure 4.2: *Harmonics cancellation in a six paths six phases system.*

and ω_2, respectively, and can be positive or negative numbers. Equation (4.2) establishes that the phase shift of the kth harmonic at the end of the ith path is given by $(k-1)(i-1)\varphi$ in case of a single-tone input. Similarly, for a two-tone signal, the phase shift of the IM products at the output of the path will be given by $(p+q-1)(i-1)\varphi$. Thus, the IM products which satisfy

$$p + q = jn + 1 \tag{4.4}$$

where $j = 0, 1, 2, 3, \ldots$, are not cancelled [27].

In particular, the third order IM components, $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$, satisfy this condition for $j = 0$. Therefore, these products always appear in phase at the output of each path and hence, they are not cancelled. In general, if $p + q = k$, the kth harmonic is cancelled, thus $p\omega_1 + q\omega_2$ is also cancelled.

4.3 The Phase Shifter

One of the key factors in the multipath-polyphase technique is the phase shifter placed before and afterwards the non-linear block. It is important to

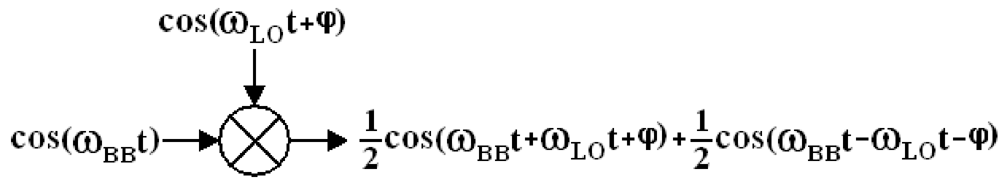

Figure 4.3: *Mixer as a phase shifter.*

consider that those phase shifters have to exhibit a constant phase shift over all the relevant frequencies involved in the cancellation process [27]. However, to implement a phase shifter with a constant phase shift over a wide bandwidth at high frequencies is a difficult task. On the other hand, at lower signal frequencies, e.g. baseband frequencies, digital signal processing techniques can be exploited to realize highly-precise phase shifts before the digital-to-analog conversion and the non-linear block. Therefore, an alternative can be to pass the phase generation problem to the digital domain.

Another possibility in the analog domain is to use a mixer as a very wideband phase shifter [27]. Figure 4.3 depicts the action of a mixer on the baseband (BB) signal $cos(\omega_{BB}t)$, which is at low frequency, and the local oscillator (LO) signal $cos(\omega_{LO}t + \varphi)$, which is at high frequency. As can be seen, at the output of the mixer there are simultaneously up-conversion of the BB signal and the phase shift, φ, set by the LO signal. Mathematically, whatever phase φ is added to the LO signal, it will appear at the output of the mixer. This also holds for higher harmonics of both, the BB and the LO signals, as long as speed limitations in the mixer play no significant role. Therefore, it is possible to set the input signal of Figure 4.1 as the BB signal and replace the second group of phase shifters by mixers. The first set of phase shifters can be implemented in the digital domain or by means of polyphase filters, which exhibit an acceptable accuracy at low frequencies [30].

Figure 4.4 illustrates the new block diagram of the multipath-polyphase approach with a mixer as phase shifter. Usually, active mixers employed in RF transmitters circuits are preferably implemented using "hard switching" via a large LO signal [31]. Mathematically, this corresponds to the multiplication of the BB signal with a square LO wave, instead of a sinusoidal signal. Therefore, the output spectrum at the output of the mixer will contain a forest of harmonics

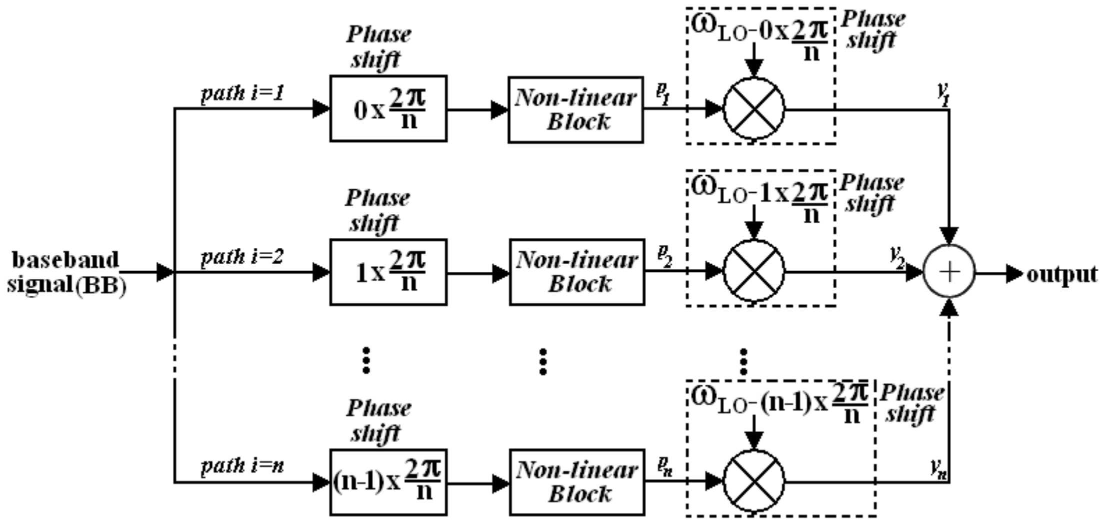

Figure 4.4: *The multipath-polyphase approach with a mixer as phase shifter.*

and sidebands at frequencies $K_{LO}\omega_{LO} \pm m\omega_{BB}$, where k_{LO} and m are integers, due to the multiplication of the square LO wave with the distorted BB signal from the non-linear blocks. The new conditions for non-cancelled distortion components is given by

$$k_{LO} = jn + m \tag{4.5}$$

where $j = 0, 1, 2, 3, \ldots$, and m is a positive or negative integer [27].

The most important distortion components that remain uncancelled are [27]: $3\omega_{LO} + 3\omega_{BB}$, $5\omega_{LO} + 5\omega_{BB}$, $7\omega_{LO} + 7\omega_{BB}$, for $j = 0$, and $15\omega_{LO} - 3\omega_{BB}$, $13\omega_{LO} - 5\omega_{BB}$, when $j = 1$. From those, the third order distortion component, $3\omega_{LO} + 3\omega_{BB}$, is troublesome since it is close to the desired signa, $\omega_{LO} + \omega_{BB}$, and it is usually stronger than higher order distortion products [32]. An alternative to get rid of the third order distortion product is to modify the duty cycle of the LO signal to one third [27]. By doing so, the $2b + 1$ harmonic terms, where $b = 1, 2, 3, \ldots$, disappear from the Fourier series expansion of the square LO wave, and consequently, the $3\omega_{LO} + 3\omega_{BB}$ and $15\omega_{LO} - 3\omega_{BB}$ terms also dissolve. Nevertheless, to do this also implies to produce harmonics components with even coefficients like $2\omega_{LO}$, $4\omega_{LO}$, etcetera. Hence, other distortion products such as $2\omega_{LO} + 2\omega BB$, $4\omega_{LO} + 4\omega BB$, $14\omega_{LO} - 4\omega BB$, and $16\omega_{LO} - 2\omega BB$ will appear at the output of the system. Fortunately, it is possible to cancel those distortion com-

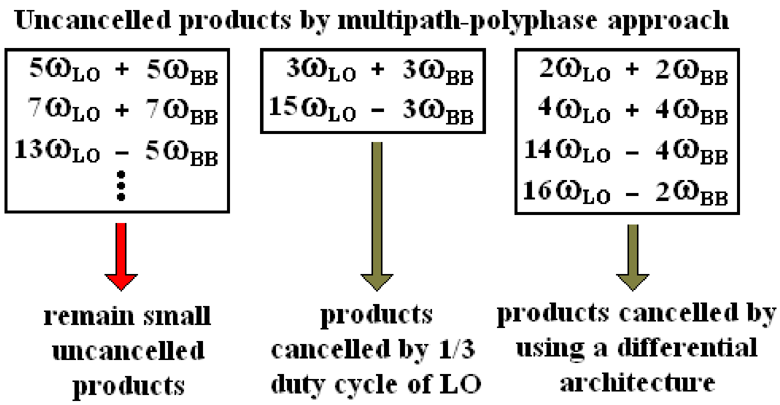

Figure 4.5: *Overview of solutions for the uncancelled products.*

ponents by using a differential architecture, which is desired anyway in order to reject common-mode interference like substrate and supply bounce [27]. Figure 4.5 shows the techniques applied to cancel the most important distortion components that remain uncancelled afterwards the use of the multipath-polyphase approach with a mixer as a phase shifter.

4.4 The Effects of Mismatch

In the previous analysis it has been assumed that all the n smaller non-linear blocks are identical as well as the phase shifters and the paths on which those are placed. Nevertheless, the materials employed to implement transistors and interconnection lines exhibit properties that vary randomly. As a result, mismatch between the blocks and paths is present in a real multipath-polyphase system. Therefore, it is necessary to analyze the effects of mismatch on the cancellation of distortion components.

Figure 4.6 depicts a multipath-polyphase system considering a phase mismatch in the first group of phase shifters, represented by θ, a different phase mismatch in the second group of phase shifters, i.e. the mixers, delineated by δ, and a mismatch in the coefficient of the power series from the non-linear blocks described by ε. The variables θ, δ and ε are considered uncorrelated random variables of either polarity. Note that also the LO signal has been taken as a square wave signal and it is represented by its Fourier series expansion. Under these

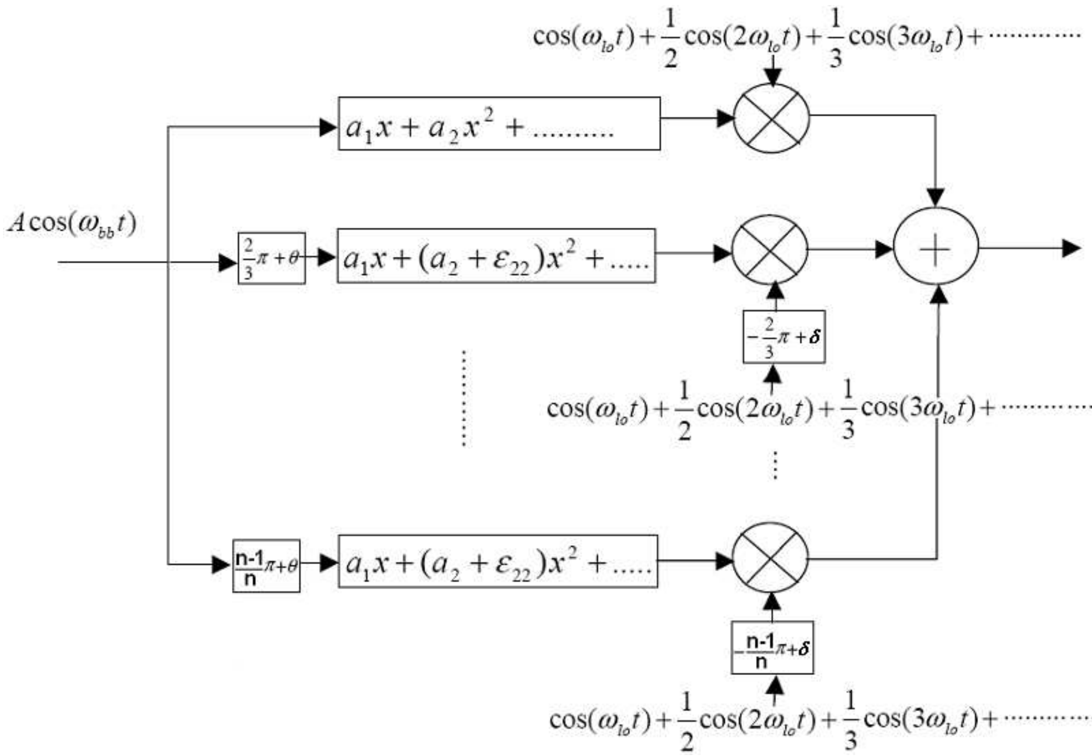

Figure 4.6: *Mismatch in the multipath-polyphase technique.*

considerations, the distortion components produced by the system at frequencies $k_{LO}\omega_{LO} \pm m\omega_{LO}$ are not cancelled completely but suppressed to some extent. The suppression of those unwanted products is given by the ratio of the total power of the distortion components produced in the absence of mismatch and without the use of the multipath-polyphase technique, and the total power of the same distortion components, but produced by the multipath-polyphase system in the presence of mismatch. Mathematically, this can be expressed as [26]

$$E(sup) = \frac{P_{k,m,reference}}{P_{k,m,rejected}} = \frac{N^2}{(N-1)\left(\dfrac{\sigma_\varepsilon^2}{a_n^2} + k_{LO}^2\sigma_\theta^2 + m^2\sigma_\delta^2\right)} \tag{4.6}$$

where σ_θ^2, σ_δ^2 and σ_ε^2 are the variances of the stochastic variables θ, δ, and ε, respectively, and $E()$ is the expectation operator. Equation (4.6) predicts that the effect of phase mismatch is higher for higher order distortion components due to the terms k_{LO}^2 and m^2. However, those harmonics are relatively weak and more distant with respect to the desired signal. It is notable to see that, according to this expression, a higher number of paths is beneficial to suppress the harmonics more effectively in the presence of mismatch. Finally, equation (4.6) also shows that the effect of ε mismatch is constant for all the harmonics. Since the ε mismatch comes from the non-linear blocks and these are, in the case of our interest, power amplifiers which are typically implemented with large transistors in order to produce sufficient output power, then, the ε mismatch term tends to be less important than the mismatch of the phases θ and δ.

4.5 Conclusions

The principle of operation for linearizing non-linear systems by means of the multipath-polyphase technique has been described. It consists of dividing the non-linear block into smaller identical non-linear blocks with phase shifts before and after them. Depending on the number of paths and phases employed the non-linearities can be cancelled to some extent. This characteristic provides a high flexibility to the technique, and hence, it suits to different wireless technologies with diverse linearity requirements.

When the input signal is compound by more than a single tone, harmonics and IM distortion are produced. Moreover, since the last phase shifts in the system are performed with a mixer and one of the inputs to the mixer is a square wave signal, then cross modulation is also present. From those distortion components, the third order products are not cancelled regardless the number of paths and phases occupied. A solution for cancelling this troublesome non-linearities is to modify the duty cycle of the square wave signal to 1/3. However, by doing this, new even harmonics are produced. Fortunately, a differential architecture can be used to cancel this new unwanted products.

In a real multipath-polyphase linearizer mismatch plays a significant role. Perfect cancellation of distortion components is only possible if all the paths and blocks are identical. Unfortunately, this is not possible due to the fact that the materials employed to implement transistors and interconnection lines exhibit properties that vary randomly. As a result, distortion is not completely cancelled but suppressed to some extent. In general terms, the phase mismatch in the system is more crucial than the mismatch from the power gain among the non-linear blocks. The larger the number of paths and phases is the more effective the harmonics suppression is accomplished.

Chapter 5

Efficiency Analysis of the Multipath-Polyphase Power Amplifier

5.1 Introduction

By definition, standalone Power Amplifier (PA) circuits exhibit certain degree of linearity at the expense of efficiency. The more linear the PA behaves, the more inefficient it becomes. Unfortunately, there are some systems which demand PAs with both figures of merit. Thus, a good trade-off between linearity and efficiency is needed. Mobile WiMAX is not the exception. On one hand, the linearity requirements are rather stringent, but, on the other hand, the mobile terminals are intended to operate with batteries, and therefore, a more efficient use of the energy is also desired.

Different linearization strategies can be adopted in order to achieve the spectral mask established by the standard. The multipath-polyphase technique is a good option due to both, its linearization performance and its wide bandwidth. However, the analysis related with its efficiency needs to be done in order to understand the mechanisms involved in the way the energy is transformed in the system towards the synthesis of a linear multipath-polyphase PA with high efficiency.

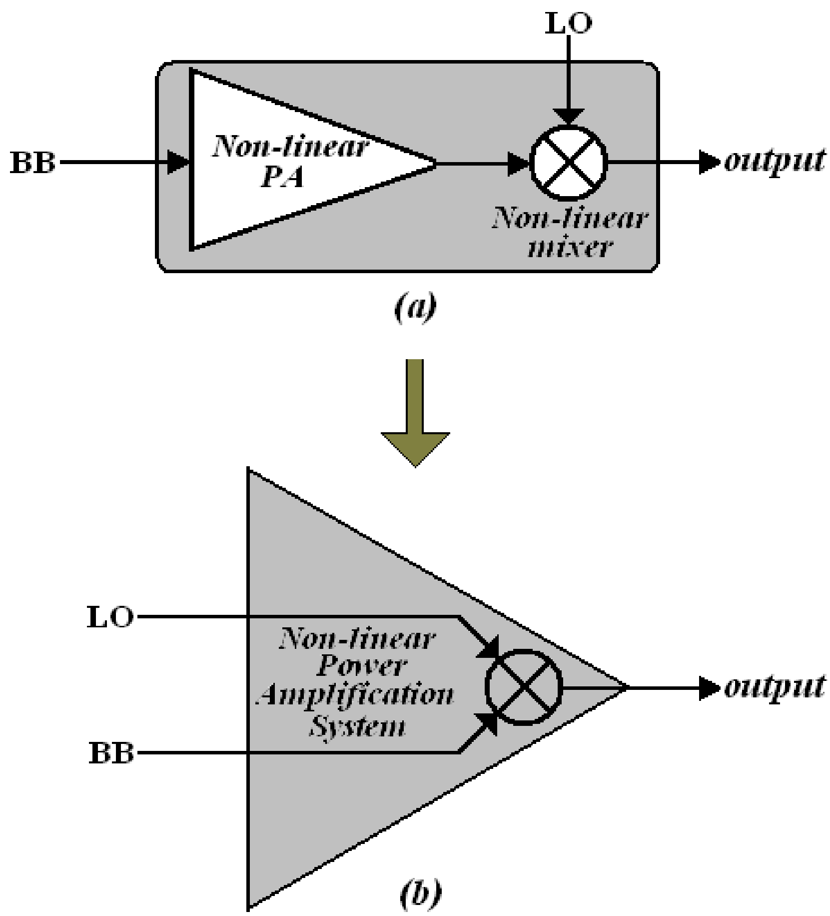

Figure 5.1: *Equivalent circuit of the multipath-polyphase PA.*

5.2 The Efficiency of the Power Upconverter

Figure 5.1 (a) shows the equivalent circuit of the multipath polyphase PA before it is divided into n smaller blocks with n different signal paths and phases. As can be seen, the system is compounded by two non-linear circuits, the PA and the mixer which acts as a phase shifter. Such a system can be conceived as a single non-linear power amplification system with two inputs and one output, as depicted in Figure 5.1 (b). The assignments of this non-linear power amplification system consist of: 1) realizing the upconversion of the baseband signal (BB) at the frequency of the local oscillator (LO); 2) to provide some power gain between the input and output ports; and finally, 3) to perform the phase shift required to cancel the distortion components produced by the non-linearities of the system.

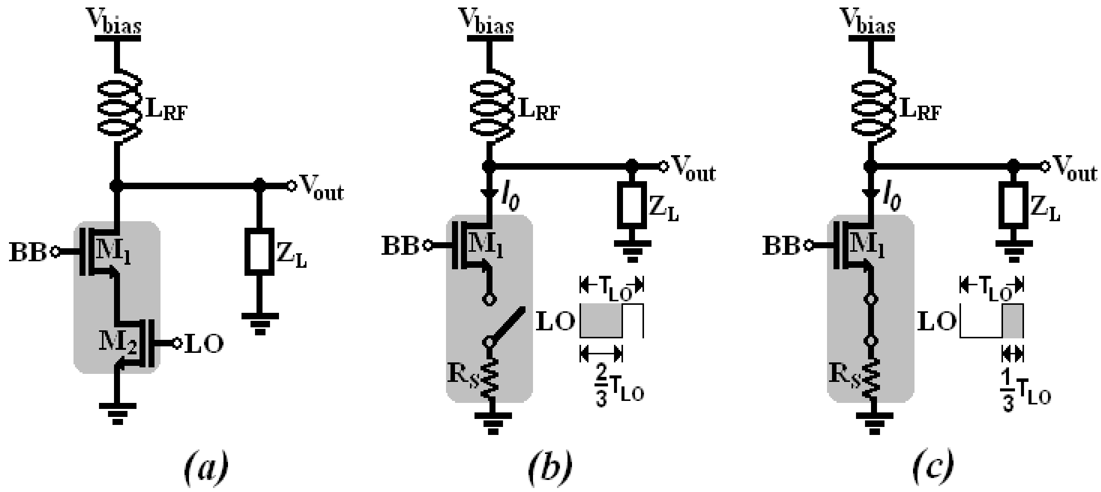

Figure 5.2: *CMOS Power upconverter.*

We are interested in knowing how much energy is occupied to perform those tasks. In order to make an estimation, we first analyze the power amplification system based on the multipath-polyphase approach proposed in [27]. Figure 5.2 (a) shows the circuit of the basic power upconverter employed. As can be seen, it consists of a NAND function block formed by the series connection of transistors M_1 and M_2. Transistor M_2 is driven as a hard switch by the square LO wave whereas transistor M_1 is driven as a transconductor by the BB and biased to operate in saturation. One third duty cycle of the LO is chosen to eliminate, among others, the third harmonic term from the Fourier series of the square wave [26]. Figure 5.2 (b) depicts the action of the circuit when the LO is at a 'low' value whereas Figure 5.2 (c) illustrates its action when the LO is at a 'high' value. According to this, the resistance of the switch within the circuit can be expressed as [33]

$$R_S = \begin{cases} \infty & \text{for } 0 < t < \frac{2}{3}T_{LO} \\ \dfrac{1}{\mu_n C_{OX} \dfrac{W_2}{L}(V_{LO} - V_{TH})} & \text{for } \frac{2}{3}T_{LO} < t < T_{LO} \end{cases} \quad (5.1)$$

where μ_n, C_{OX}, and V_{TH} are the mobility of the carriers, the oxide capacitance, and the threshold voltage of the device, respectively; V_{LO} is the voltage value of the LO; W_2 and L are the width and the length of transistor M_2.

When the switch is open, there are no current flowing through the NAND function block. On the other hand, since M_1 operates in saturation, the current flowing through the circuit, I_0, when the switch is closed is given by [33]

$$I_0 = \frac{1}{2}\mu_n C_{OX}\frac{W_1}{L}(V_{BB} - R_S I_0 - V_{TH})^2$$

where W_1 and L are the width and the length of transistor M_1, respectively; V_{BB} is the voltage value of the BB at the gate of the device; the product $R_S I_0$, is the voltage drop at the source terminal of M_1, and V_{TH} is the threshold voltage of the transistor. As can be appreciated, the feedback mechanism established by the resistor R_S during the time $\frac{2}{3}T_{LO} < t < T_{LO}$ and illustrated in Figure 5.2 (c), sets the equation of the current to be a quadratic formulation. It can be found that the solution for the current I_0 is given by

$$I_0 = \begin{cases} 0 & \text{for } 0 < t < \frac{2}{3}T_{LO} \\ \dfrac{1 + \mu_n C_{OX}\frac{W_1}{L}(V_{BB} - V_{TH})R_S}{\mu_n C_{OX}\frac{W_1}{L}R_S^2} - \dfrac{\sqrt{1 + 2\mu_n C_{OX}\frac{W_1}{L}(V_{BB} - V_{TH})R_S}}{\mu_n C_{OX}\frac{W_1}{L}R_S^2} & \text{for } \frac{2}{3}T_{LO} < t < T_{LO} \end{cases}$$

Combining this expression with equation (5.1) we obtain

$$I_0 = \begin{cases} 0 & \text{for } 0 < t < \frac{2}{3}T_{LO} \\ \dfrac{1 + \left(\frac{W_1}{W_2}\right)\left(\frac{V_{BB} - V_{TH}}{V_{LO} - V_{TH}}\right)}{\frac{LW_1}{W_2^2}\frac{1}{\mu_n C_{OX}(V_{LO} - V_{TH})^2}} - \dfrac{\sqrt{1 + 2\left(\frac{W_1}{W_2}\right)\left(\frac{V_{BB} - V_{TH}}{V_{LO} - V_{TH}}\right)}}{\frac{LW_1}{W_2^2}\frac{1}{\mu_n C_{OX}(V_{LO} - V_{TH})^2}} & \text{for } \frac{2}{3}T_{LO} < t < T_{LO} \end{cases} \tag{5.2}$$

On the other hand, transistor M_1 is intended to operate in class A [27]. Thus, the output power of the upconverter is given by $P_{OUT} = v_0^2/2R_L$, where v_0 is the peak value of the voltage swing at the output of the NAND function block and R_L the real part of the load, Z_L. The voltage swing, v_0, is given by the product of the transconductance of the circuit, gm, by the real part of the load, R_L, and the voltage swing at the input of transistor M_1, v_{bb}, i.e. $v_0 = -gmR_Lv_{bb}$ [35]. Consequently, it is needed to obtain the transconductance of the circuit. This can be done by deriving I_0 with respect to V_{BB}, by doing so, we attain

$$gm = \begin{cases} 0 & \text{for } 0 < t < \frac{2}{3}T_{LO} \\ \left\{1 - \dfrac{1}{\sqrt{2\left(\dfrac{W_1}{W_2}\right)\left(\dfrac{V_{BB}-V_{TH}}{V_{LO}-V_{TH}}\right)+1}}\right\}\times & \\ \qquad \times\mu_n C_{OX}\left(\dfrac{W_2}{L}\right)(V_{LO}-V_{TH}) & \text{for } \frac{2}{3}T_{LO} < t < T_{LO} \end{cases} \tag{5.3}$$

Figure 5.3 shows the graph of gm as a function of these widths. In order to compute those values, parameters of the UMC 0.18μm Mixed Mode and RF CMOS technology were used. Transistor M_1 was consider to operate with $V_{BB} =$ 1V, $V_{bias} = 0.9$V, and transistor M_2 with $V_{LO} = 1.8$V. According to this plot, the maximum transconductance is achieved when $W_1 = W_2$. In this manner, a good practice would be to keep both transistors the same size in order to design the power upconverter to hand over the maximum possible output power. Finally, in terms of the parameters of the transistors, the output power can be expressed as

$$P_{out} = \begin{cases} 0 & \text{for } 0 < t < \frac{2}{3}T_{LO} \\ \left[\mu_n C_{OX}\dfrac{W_2}{L}v_{bb}\right]^2 R_L\left\{\dfrac{1+\dfrac{W_1}{W_2}\left(\dfrac{V_{BB}-V_{TH}}{V_{LO}-V_{TH}}\right)}{1+2\dfrac{W_1}{W_2}\left(\dfrac{V_{BB}-V_{TH}}{V_{LO}-V_{TH}}\right)}-\right. & \\ \left.-\dfrac{1}{\sqrt{1+2\dfrac{W_1}{W_2}\left(\dfrac{V_{BB}-V_{TH}}{V_{LO}-V_{TH}}\right)}}\right\}(V_{LO}-V_{TH})^2 & \text{for } \frac{2}{3}T_{LO} < t < T_{LO} \end{cases} \tag{5.4}$$

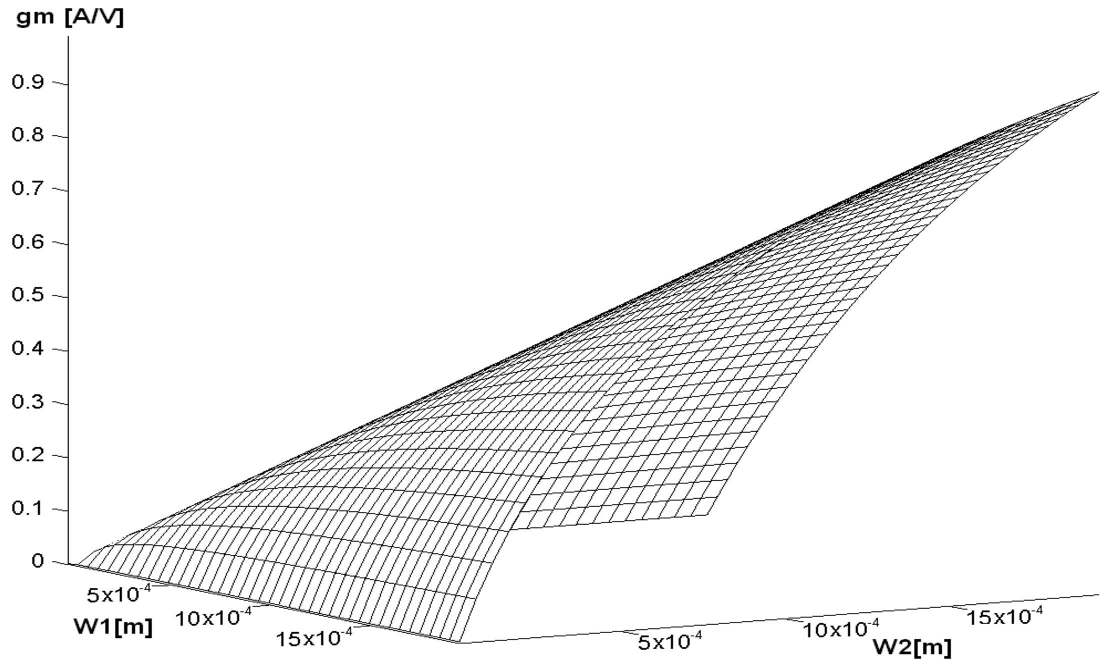

Figure 5.3: *Transconductance of the power upconverter, gm, as a function of the widths of transistors M_1 and M_2.*

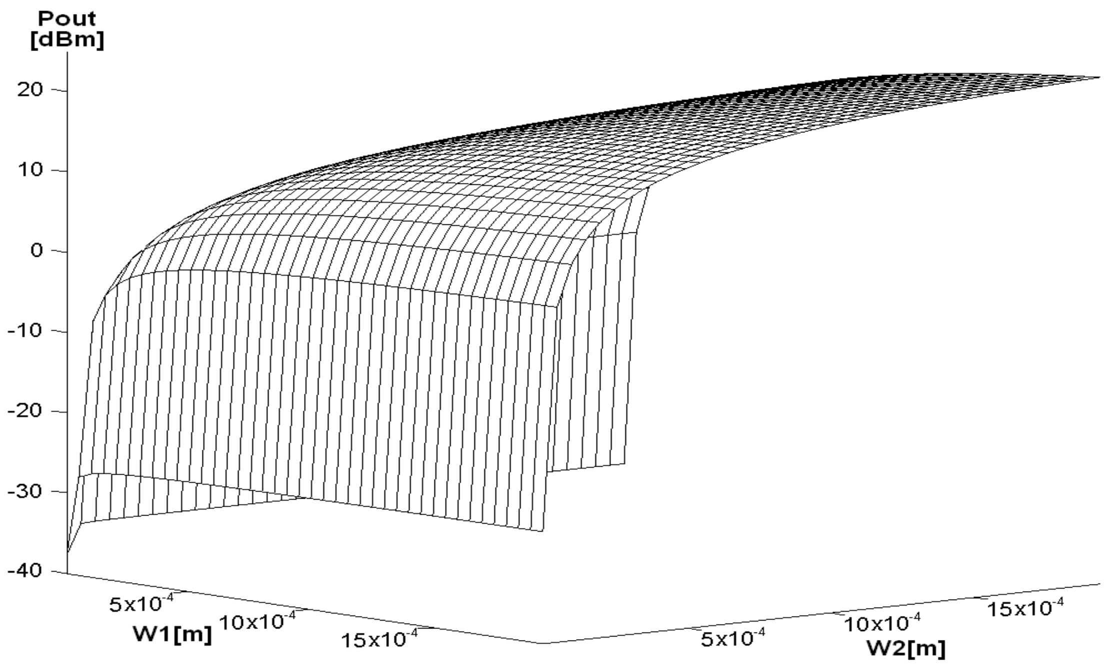

Figure 5.4: *Output power of the power upconverter, P_{OUT}, as a function of the widths of transistors M_1 and M_2.*

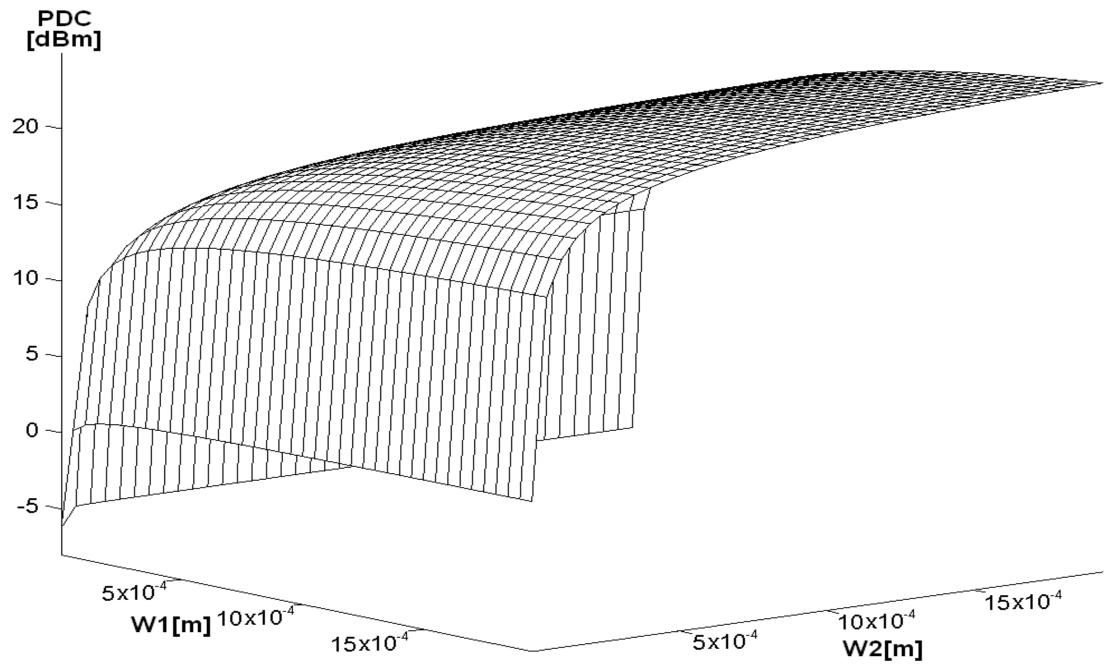

Figure 5.5: *DC power of the power upconverter, P_{DC}, as a function of the widths of transistors M_1 and M_2.*

Figure 5.4 shows the graph of P_{OUT}. As expected, it reaches its maximum value when $W_1 = W_2$. A peak value of 300mV from the voltage swing at the input, v_{bb}, and an R_L of 5Ω were considered.

The power drawn from the DC power supply, P_{DC}, is also an important parameter. This can be obtained by the multiplying the current flowing through the circuit, I_0, by the value of the power supply, V_{bias}. In so doing, we get

$$P_{DC} = \begin{cases} 0 & \text{for } 0 < t < \frac{2}{3}T_{LO} \\ V_{bias}\left\{ \dfrac{1 + \left(\dfrac{W_1}{W_2}\right)\left(\dfrac{V_{BB} - V_{TH}}{V_{LO} - V_{TH}}\right)}{\dfrac{LW_1}{W_2^2}\dfrac{1}{\mu_n C_{OX}(V_{LO} - V_{TH})^2}} - \right. \\ \qquad \left. - \dfrac{\sqrt{1 + 2\left(\dfrac{W_1}{W_2}\right)\left(\dfrac{V_{BB} - V_{TH}}{V_{LO} - V_{TH}}\right)}}{\dfrac{LW_1}{W_2^2}\dfrac{1}{\mu_n C_{OX}(V_{LO} - V_{TH})^2}} \right\} & \text{for } \frac{2}{3}T_{LO} < t < T_{LO} \end{cases} \tag{5.5}$$

Figure 5.5 shows the graph of P_{DC}. As can be appreciated, the maximum DC power consumption is also achieved when both transistors are equal in size. However, when comparing this plot with that obtained for P_{OUT}, it can be seen that the lowest values of P_{DC} are larger than those attained for the output power. This has a negative impact in the efficiency of the circuit.

Now it is possible to estimate the drain efficiency, η_D, of the circuit, which is defined as the ratio between the output power and the DC power [13]. Since P_{OUT} and P_{DC} equal zero for the time $0 < t < \frac{2}{3}T_{LO}$, then $\eta_D = 100\%$ during this time. On the other hand, for the time $\frac{2}{3}T_{LO} < t < T_{LO}$, η_D is given by

$$\eta_D = \left\{ \frac{\dfrac{1+\left(\frac{W_1}{W_2}\right)\left(\frac{V_{BB}-V_{TH}}{V_{LO}-V_{TH}}\right)}{1+2\left(\frac{W_1}{W_2}\right)\left(\frac{V_{BB}-V_{TH}}{V_{LO}-V_{TH}}\right)} - \dfrac{1}{\sqrt{1+2\left(\frac{W_1}{W_2}\right)\left(\frac{V_{BB}-V_{TH}}{V_{LO}-V_{TH}}\right)}}}{\dfrac{1+\left(\frac{W_1}{W_2}\right)\left(\frac{V_{BB}-V_{TH}}{V_{LO}-V_{TH}}\right) - \sqrt{1+2\left(\frac{W_1}{W_2}\right)\left(\frac{V_{BB}-V_{TH}}{V_{LO}-V_{TH}}\right)}}{\frac{LW_1}{(W_2)^2}}} \right\} \times \frac{R_L v_{bb}^2 \mu_n C_{OX}}{V_{bias}} \left(\frac{W_2}{L}\right)^2 \tag{5.6}$$

Figure 5.6 shows the graph of η_D as a function of the widths of transistors M_1 and M_2. According to this plot, the largest value of η_D is achieved when $W_1 = W_2$. It can be noticed that conforming those widths become larger, η_D also increases. Thus, while the output power is large, the power upconverter exhibits a high efficiency. It is important to remark that the results obtained in the analysis do not take into account some effects present in the system such as the diverse loss mechanisms which cause a detriment of the efficiency [25].

Since η_D is larger when the transistors are the same size, it is interesting to see what happens with the efficiency of the circuit under this consideration at output power back-off. Figure 5.7 depicts the plot of η_D when $W_1 = W_2$ in function of the output power, P_{OUT}. As can be seen, at a large output power back-off the drain efficiency decreases severely. This is very inconvenient for wireless communication systems such as mobile WiMAX, which demands most of the time

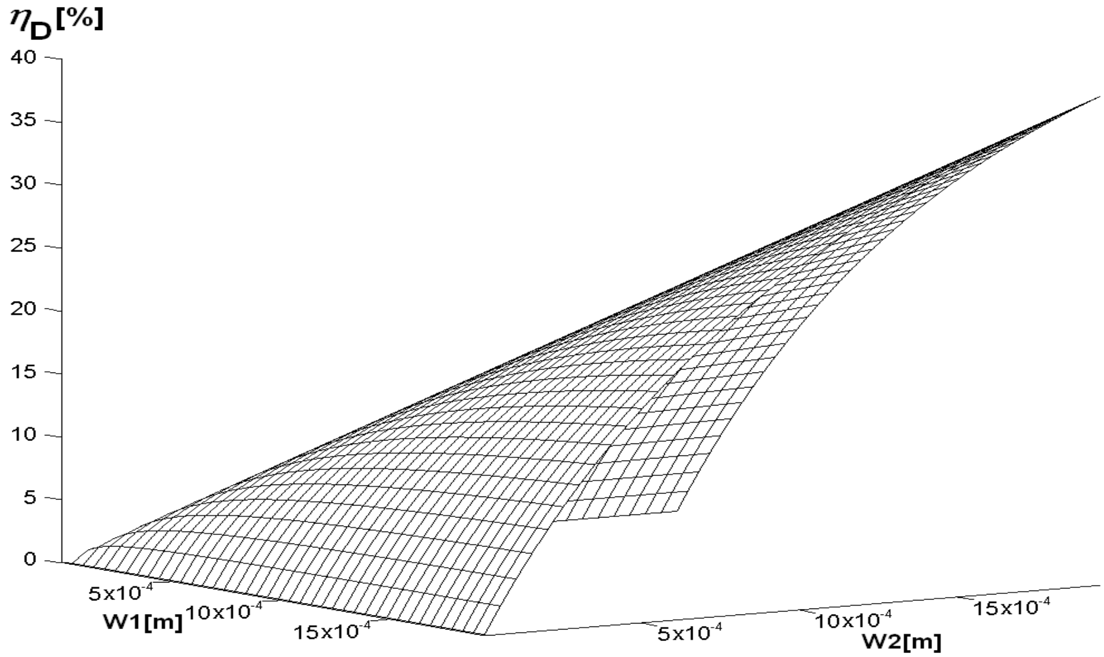

Figure 5.6: *Drain efficiency of the power upconverter, η_D, as a function of the widths of transistors M_1 and M_2.*

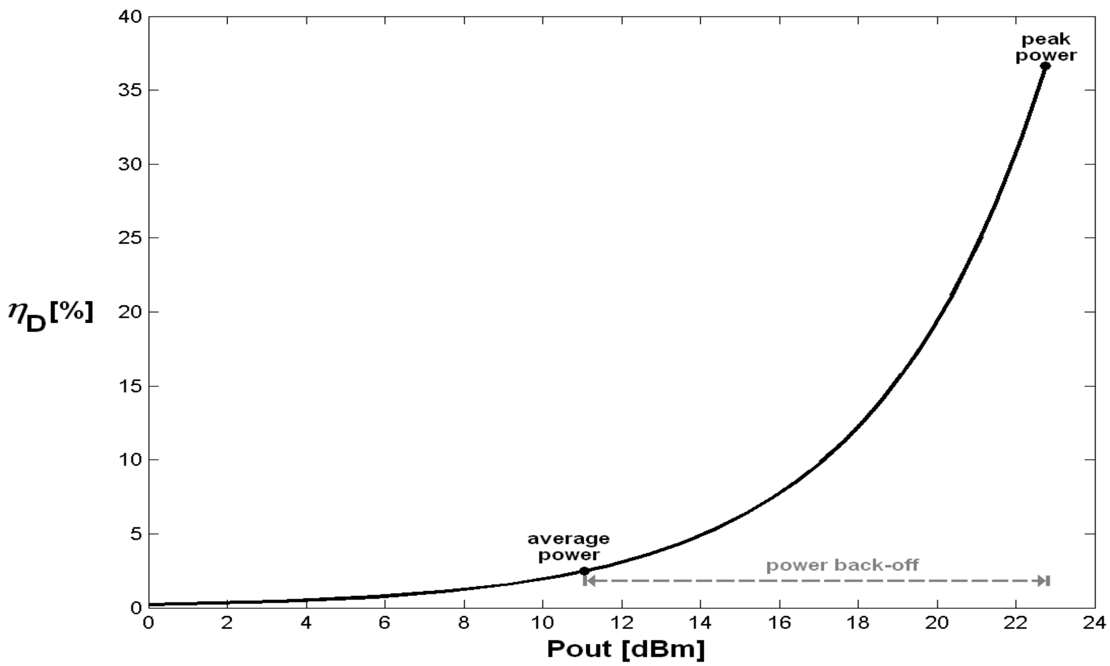

Figure 5.7: *η_D of the power upconverter at power back-off when transistors M_1 and M_2 are equal in size.*

the average output power rather than the maximum output power value.

Another important parameter which must be assessed is the input power of the circuit, P_{IN}. In order to evaluate P_{IN}, we focus on the circuit of the power upconverter showed in Figure 5.8 (a). As can be seen, the parasitic capacitances of transistors M_1 and M_2 are depicted. As mentioned earlier, transistor M_2 is driven as a hard switch by the square LO wave which runs at RF frequency whereas transistor M_1 is driven as a transconductor by the BB. Since BB runs slower than LO, the voltage at the gate of M_1, V_{BB}, can be considered to have a constant value during a switching period, T_{LO}, where $T_{LO} = \frac{1}{f_{LO}}$. Therefore, when the switch is open, for the time $0 < t < \frac{2}{3}T_{LO}$, which corresponds to a voltage value of $V_{LO} = 0V$, the capacitors highlighted in Figure 5.8 (b) are charged by V_{BB}. The open switch implicates that both, transistor M_1 and M_2 are off. Therefore, the highlighted capacitors are given by [33]

$$
\begin{aligned}
C_{DB2} &= W_2 E C_j + 2(W_2 + E)C_{jsw} \quad \text{for } 0 < t < \frac{2}{3}T_{LO} \\
C_{SB1} &= W_1 E C_j + 2(W_1 + E)C_{jsw} \quad \text{for } 0 < t < \frac{2}{3}T_{LO} \\
C_{GD2} &= W_2 C_{OV} \quad \text{for } 0 < t < \frac{2}{3}T_{LO} \\
C_{GS1} &= W_1 C_{OV} \quad \text{for } 0 < t < \frac{2}{3}T_{LO} \\
C_{GB1} &= \frac{W_1 L C_{OX} C_d}{W_1 L C_{OX} + C_d} \quad \text{for } 0 < t < \frac{2}{3}T_{LO} \\
C_{GD1} &= W_1 C_{OV} \quad \text{for } 0 < t < \frac{2}{3}T_{LO}
\end{aligned} \tag{5.7}
$$

where C_{OV} and C_{OX} are the overlap and the oxide capacitances, respectively; C_j and C_{jsw} are the junction capacitance between the drain/source area and sidewall capacitance due to the perimeter of the union, respectively; E is the length of the diffusion; and C_d is the depletion capacitance. Note that there is a series connection of capacitor C_{GS1} and capacitor $C_{DB2} + C_{SB1} + C_{GD2}$, and this series connection is in parallel with C_{GB1}. Then, the equivalent capacitance at the gate of M_1, C_{eq}, can be written as

$$
C_{eq} = C_{GB1} + \frac{C_{GS1}\big(C_{DB2} + C_{SB1} + C_{GD2}\big)}{C_{GS1} + C_{DB2} + C_{SB1} + C_{GD2}} \tag{5.8}
$$

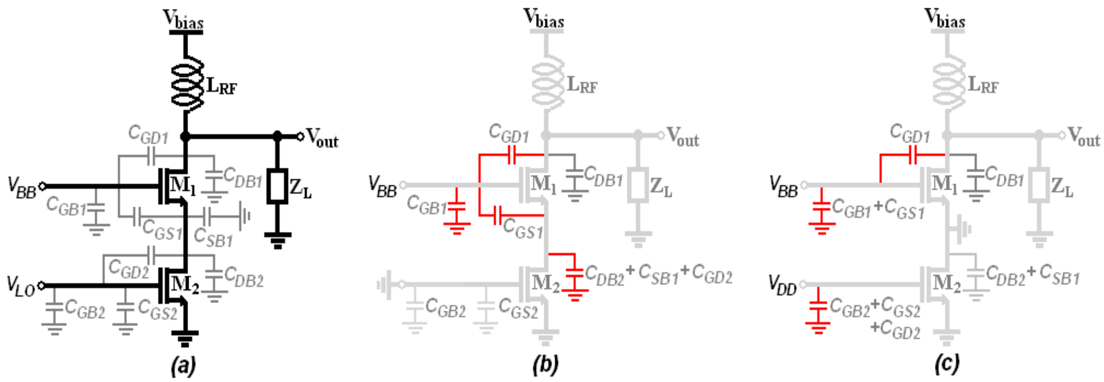

Figure 5.8: *Power Upconverter and (a) its parasitic capacitances. (b) Capacitances charged when the switch is open. (c) Capacitances charged when the switch is closed.*

Thus, capacitor C_{eq} is charged by V_{BB} and capacitor C_{GD1} is charged by the voltage difference $V_{BB} - V_{bias}$. This causes a charge $q = C_{eq}V_{BB}$ to flow through C_{eq} and a charge $q = C_{GD1}(V_{BB} - V_{bias})$ to flow through capacitor C_{GD1}. Since this action is repeated once every T_{LO} seconds, the average current through capacitor C_{eq} is [34]

$$i_{avceq} = \frac{\big[(W_1+W_2)EC_j + 2(W_1+W_2+2E)C_{jsw} + W_2C_{OV}\big]W_1C_{OV}}{(W_1+W_2)EC_j + 2(W_1+W_2+2E)C_{jsw} + (W_1+W_2)C_{OV}}V_{BB}f_{LO} + \frac{W_1LC_{OX}C_d}{W_1LC_{OX}+C_d}V_{BB}f_{LO} \quad (5.9)$$

whereas the current through capacitor C_{GD1} is

$$i_{avcdg1} = W_1C_{OV}\big(V_{BB} - V_{bias}\big)f_{LO} \quad (5.10)$$

The average power caused by those currents is obtained by multiplying (5.9) by V_{BB}, which is the voltage at capacitor C_{eq}, and (5.10) by $(V_{BB} - V_{bias})$, which is the drop voltage through capacitor C_{GD1}. In this form, we have that the average power when the switch is open, P_{avswop}, for the time $0 < t < \frac{2}{3}T_{LO}$, is

$$P_{avswop} = \frac{\big[(W_1+W_2)EC_j + 2(W_1+W_2+2E)C_{jsw} + W_2C_{OV}\big]W_1C_{OV}}{(W_1+W_2)EC_j + 2(W_1+W_2+2E)C_{jsw} + (W_1+W_2)C_{OV}}V_{BB}^2f_{LO} + \frac{W_1LC_{OX}C_d}{W_1LC_{OX}+C_d}V_{BB}^2f_{LO} \quad (5.11)$$

On the other hand, when the switch is closed, for the time $\frac{2}{3}T_{LO} < t < T_{LO}$, the capacitors highlighted in Figure 5.8 (c) are charged by V_{BB}. The closed switch implicates that device M_2 is in triode meanwhile transistor M_1 is in saturation. Thus, the highlighted capacitors are given by [33]

$$
\begin{aligned}
C_{GD1} &= W_1 C_{OV} \quad \text{for } \tfrac{2}{3}T_{LO} < t < T_{LO} \\
C_{GS1} &= \frac{2}{3} W_1 L_{eff} C_{OX} + W_1 C_{OV} \quad \text{for } \tfrac{2}{3}T_{LO} < t < T_{LO} \\
C_{GS2} &= \frac{W_2 L}{2} C_{OX} + W_2 C_{OV} \quad \text{for } \tfrac{2}{3}T_{LO} < t < T_{LO} \\
C_{GD2} &= \frac{W_2 L}{2} C_{OX} + W_2 C_{OV} \quad \text{for } \tfrac{2}{3}T_{LO} < t < T_{LO}
\end{aligned}
\tag{5.12}
$$

where L_{eff} is the effective length of the channel of the transistor. It is important to remark that C_{GB1} and C_{GB2} were not considered since tha gate-bulk capacitance is usually neglected in saturation and triode regions because the inversion layer acts as a shield between the gate and the bulk [33]. Note that capacitor $C_{GB1} + C_{GS1}$ is charged by V_{BB} whereas capacitor C_{GD1} is charged by $V_{BB} - V_{bias}$. On the other hand, capacitor $C_{GB2} + C_{GS2} + C_{GD2}$ is charged by V_{DD}. Thus, by doing a similar procedure like that we made previously for the case when the switch is open, it can be obtained that the average power of the circuit when the switch is closed, P_{avswcl}, for the time $\frac{2}{3}T_{LO} < t < T_{LO}$, is

$$
\begin{aligned}
P_{avswcl} &= \left(\frac{2}{3} W_1 L_{eff} C_{OX} + W_1 C_{OV} \right) V_{BB}^2 f_{LO} + \left(W_2 L C_{OX} + 2 W_2 C_{OV} \right) V_{DD}^2 f_{LO} \\
&\quad + W_1 C_{OV} (V_{BB} - V_{bias})^2 f_{LO}
\end{aligned}
\tag{5.13}
$$

Figure 5.9 (a) and (b) show the graphs of P_{avswop} and P_{avswcl}, respectively as a function of the widths of transistors M_1 and M_2. As can be seen, for the case when the switch is open, the power increments conforming the size of M_1 rises. This makes sense since most of the parasitic capacitors which are charged during this period belong to M_1. On the other hand, when the switch is closed, we can see that the dependence of the power is stronger on the size of device M_2. This is due to the fact that the average power at this node corresponds to the dynamic power of the LO since its voltage swing ranges from $0V$ to V_{DD}. In general terms,

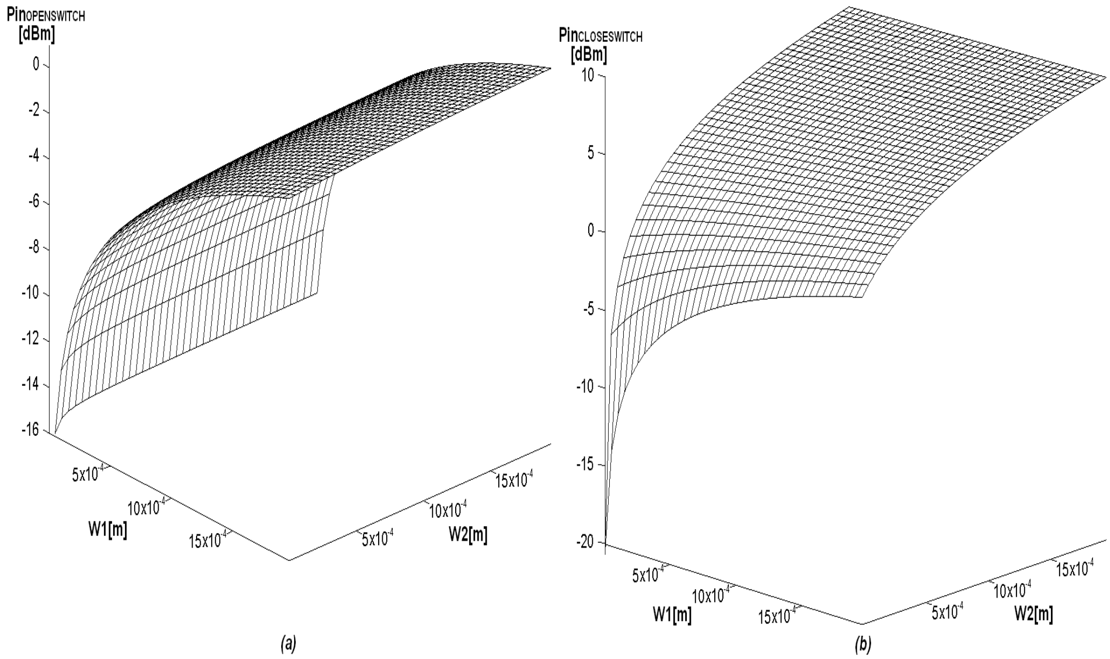

Figure 5.9: *Input power components of the power upconverter as a function of the widths of transistors M_1 and M_2: (a) P_{avswop} and (b) P_{avswcl}.*

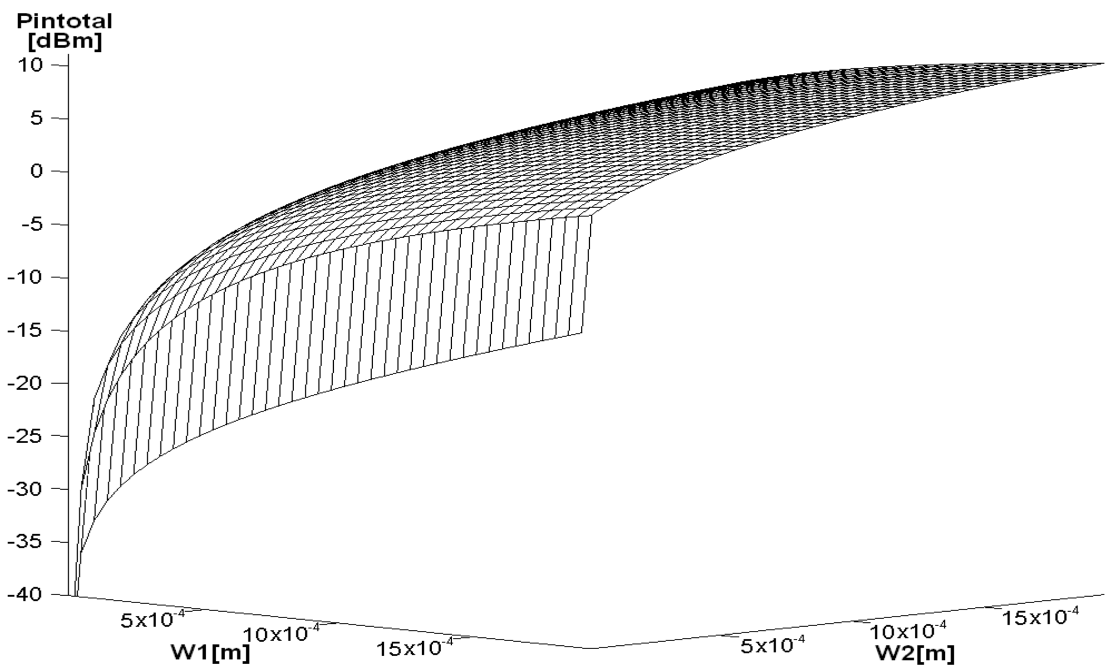

Figure 5.10: *Total input power of the power upconverter as a function of the widths of transistors M_1 and M_2.*

we can appreciate that the power in the circuit is higher when the switch is closed than when it is open.

Figure 5.10 depicts the graph of the total power produced at the input of the power upconverter due to the switching activity. In accordance with this result, it can be appreciated that the major contribution to the power is conferred by device M_2. Again, in order to compute those values showed in the graphs, parameters of the UMC 0.18μm Mixed Mode and RF CMOS technology were used. Transistor M_1 was considered to operate with $V_{BB} = 1V$, $V_{bias} = 0.9V$, and transistor M_2 with $0V \leq V_{LO} \leq 1.8V$. The frequency of the LO was taken of 2.69GHz, which is the highest frequency for mobile WiMAX in America [5].

With the expressions for the output and input power, it is possible to estimate the power gain (A_P) of the power upconverter, which is given by the ratio $A_P = \frac{P_{OUT}}{P_{intotal}}$. Since $P_{OUT} = 0$ for the time $0 < t < \frac{2}{3}T_{LO}$, then A_P is zero during this period. For the time $\frac{2}{3}T_{LO} < t < T_{LO}$, A_P is different to zero. Figure 5.11 shows the power gain obtained, for that interval, as a function of the widths of transistors $M1$ and M_2. As can be appreciated, A_P increases more rapidly when the width of transistor M_1 becomes large than when the width of transistor M_2 grows. However, there is not much gain between the output and the input power. Generally speaking, the maximum gain is achieved when the sizes of M_1 and M_2 are equal and large. Another important characteristic that must be analyzed is the Power-Added-Efficiency (PAE), which is the most popular measure of the efficiency in PAs in industry. The PAE can be defined as [13]:

$$PAE = \eta_D(1 - \frac{1}{A_P}) \qquad (5.14)$$

Employing the results obtained for the output power, the input power and the drain efficiency, it is possible to evaluate the PAE of the circuit. Since the $A_P = 0$ for $0 < t < \frac{2}{3}T_{LO}$, then, for this time $PAE = -\infty$, which means that no output power is produced when there is input power in the circuit. This makes sense since $P_{OUT} = 0$ for that period. On the other hand, Figure 5.12 depicts the graph of the PAE as a function of the widths of transistors M_1 and M_2, for the interval $\frac{2}{3}T_{LO} < t < T_{LO}$. In general terms, this plot indicates that the PAE is high when the widths of M_1 and M_2 are large. If any of those becomes smaller

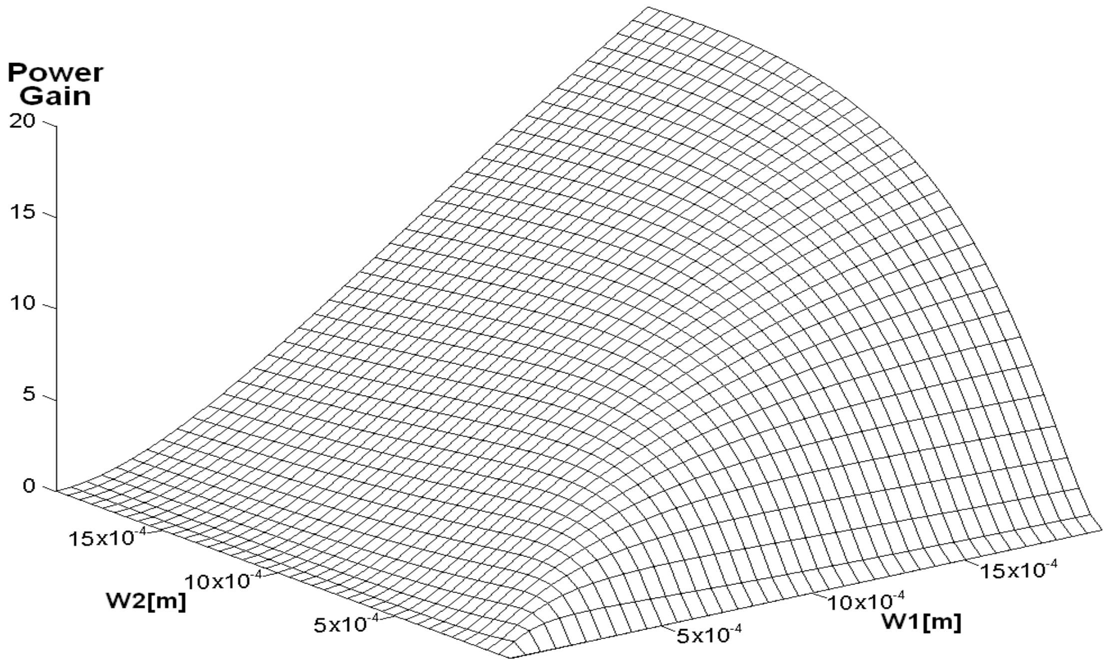

Figure 5.11: *Power gain of the power upconverter, AP, as a function of the widths of transistors M_1 and M_2.*

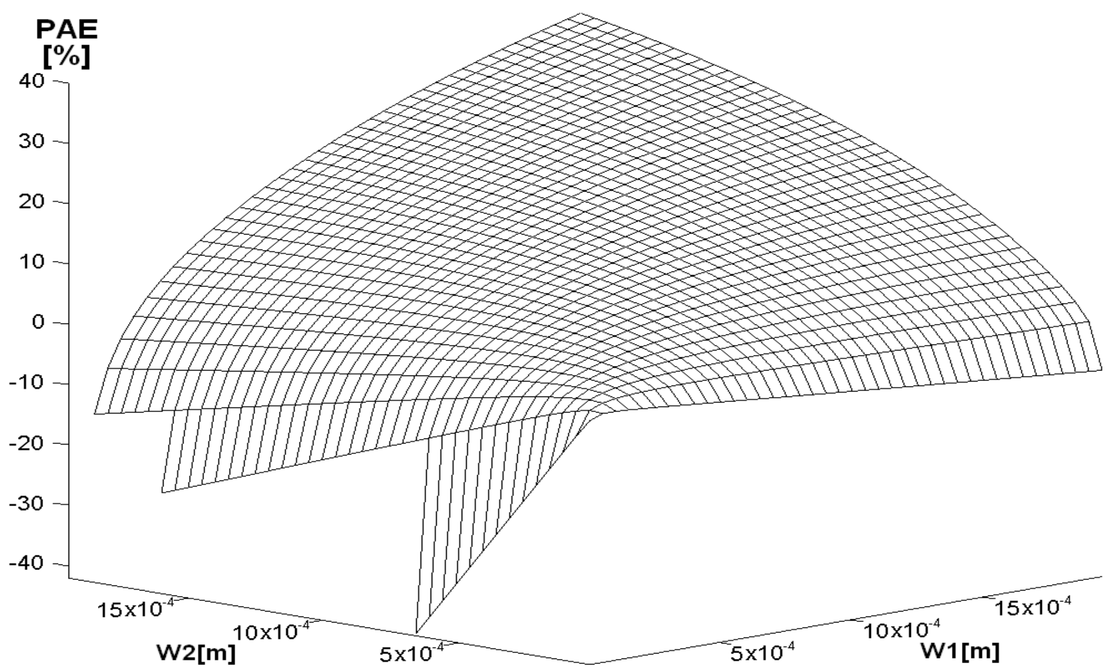

Figure 5.12: *Power Added Efficiency of the power upconverter, PAE, as a function of the widths of transistors M_1 and M_2.*

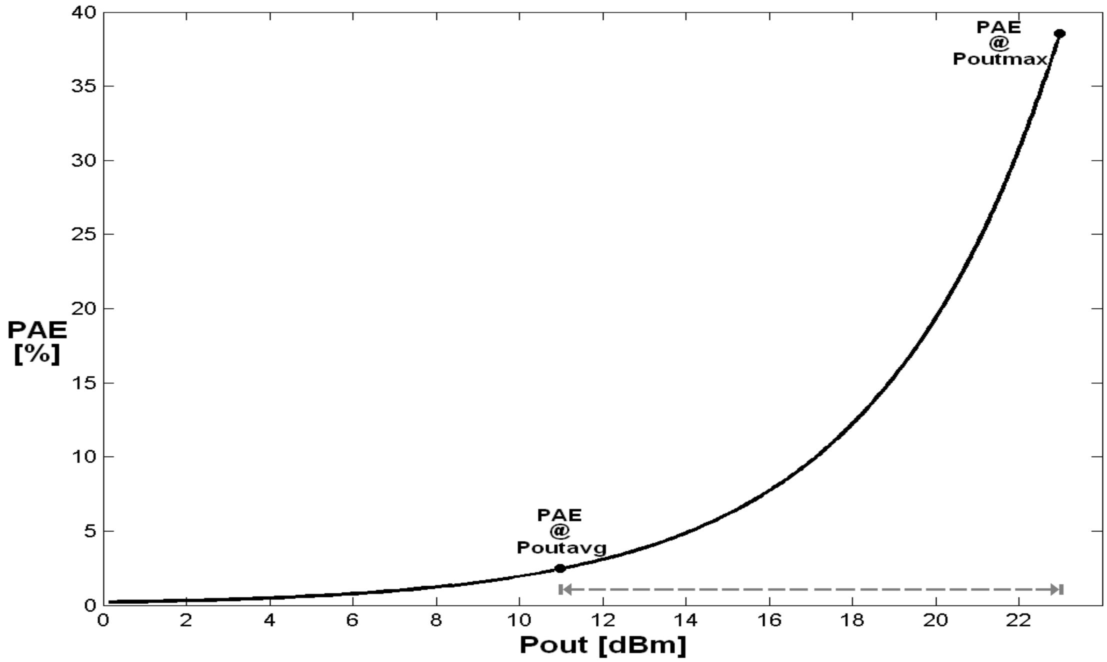

Figure 5.13: *PAE of the power upconverter at power back-off when transistors M_1 and M_2 are equal in size.*

respect each other, there will be a decay in the PAE of the circuit.

Considering that in order to transfer the maximum possible output power to the load is convenient to size transistors M_1 and M_2 equal, then, it is interesting to assess the PAE when both devices present the same dimensions and at output power back-off. Figure 5.13 illustrates this situation.

As can be perceived, at peak output power, the PAE exhibits its highest value. To the contrary, with a large power back-off at average output power, the PAE presents its minimum value. The drop of the efficiency is dramatic. This is a problem since the terminal operates most of the time at average output power and the PAE at this point is very low, which yields in an effective circuit from the point of view of efficiency.

5.3 Key Factors in the Efficiency of the System

From the results obtained in the previous section associated with the analysis of the efficiency of the power upconverter proposed in [27] as an alternative to implement a linearized multipath polyphase PA, the following set of conclusions can be established:

- The drain efficiency in the system, η_D, without considering any loss mechanism in the circuit, depends entirely on the conduction angle of the BB which drives transistor M_1.
- The power added efficiency, PAE, attained is rather ineffective for the whole range of output power considered (12dB PAPR). This is due to the inability of the circuit to provide a larger power gain, A_P.
- According to the formulation for the PAE (equation 5.14), it can be improved if both, η_D and A_P are increased.

It is important to delve into the second item. By inspecting the plots for P_{out} and $P_{intotal}$, one can appreciate that the output power is larger than the input power when the sizes of transistors M_1 and M_2 are big. Conforming the widths of the devices decrease, the output and input power become comparable. Both graphs were computed under the same assumptions and with equal parameter values. The problem with the low output power when the transistors are not so big lies in the fact that the load resistance, R_L, is small. Remember that if a high output power value is required by the load, then a large voltage swing is desired at the output. Furthermore, the voltage swing at the output is bounded by the maximum voltage value allowed by the technology that is employed. Typically, in submicrometric CMOS technologies, that value is around one or two Volts as much. Consequently, the value of the resistive load seen by the PA must be lower than 50Ω, which is normally the resistive value of the antenna, and the use of a matching network is necessary. Thus, the effect of R_L in the power gain is not considerable. On the other hand, we can see in Figure 5.9 that the total input power depends more on the size of transistor M_2. Unfortunately, it is not possible to keep that device small since its function is to act as a switch at the LO speed, and due to the fact that the LO runs at RF, the switch must be fast enough to be charged and discharged quickly. This implies a low RC time constant which means a low resistive value between the terminals of the switch and therefore a large transistor M_2.

5.4 Conclusions

The efficiency analysis of the linearized multipath polyphase power upconverter circuit has been introduced. The results obtained indicate that the circuit is inefficient at output power back-off. The cause of this drawback is the failure of the circuit to provide some power gain, which originates a deficient PAE. The proposed architecture of the power upconverter is such that the larger portion of the input power is proportional to the aspect ratio of the big transistor that performs as a hard switch driven by the fast LO. Consequently, the energy investment to mix the BB and LO by means of that topology is excessive.

Linear PAs for wireless communication systems which are considered to operate in portable terminals are preferable to exhibit a high efficiency in order to extend the battery duration. Since mobile WiMAX belongs to this class of transmission systems, a linear and efficient PA is preferred. Therefore, the design and implementation of a linearized multipath PA with improved efficiency is an assignment that must be addressed.

Chapter 6

Synthesis of a Multipath Polyphase Power Amplifier with Improved Efficiency

6.1 Introduction

The multipath polyphase approach allows the possibility to suppress to some extend, depending on the number of phases used and their precision, the distortion components produced by non-linear circuits such as Power Amplifiers (PAs). Thus, with the application of this technique is possible to fulfill the linearity requirements demanded for transmission by a particular wireless communication standard.

In the case of PAs employed in wireless portable terminals, efficiency is also an issue. Therefore, the design of a linearized multipath polyphase PA with an adequate use of the energy is crucial for systems where both, linearity and efficiency are mandatory. Forasmuch as the only multipath polyphase PA implemented has a poor power conversion ability, the conception of a new circuit with improved Power Added Efficiency (PAE) is necessary.

6.2 The Essential Aspects for Power Saving

There are three parameters which play an important role in the efficiency of any PA: the input power, P_{IN}; the output power, P_{OUT}; and the DC power consumption, P_{DC}. The ratio between P_{OUT} and P_{IN} defines the drain efficiency, η_D, whereas the ratio between the difference of P_{OUT} minus P_{IN} and P_{DC} defines the power added efficiency, PAE, which is the most popular measure in industry. An alternative manner to express the PAE is as a function directly proportional to η_D and inversely proportional to the power gain, A_P, i.e.

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}} = \frac{P_{OUT}}{P_{DC}}\left(1 - \frac{P_{IN}}{P_{OUT}}\right) = \eta_D\left(1 - \frac{1}{A_P}\right)$$

Hence, η_D and A_P are relevant for a high efficiency performance. In terms of the conduction angle, the η_D for transconductance PAs is given by [15]

$$\eta_D = \frac{\phi - \sin(\phi)\cos(\phi)}{2\sin(\phi) - 2\phi\cos(\phi)} \tag{6.1}$$

For switched PAs, the η_D can be expressed as [18]

$$\eta_D = \frac{2\sin^2(\phi)}{\phi(\pi - \phi)} \tag{6.2}$$

In both cases, ϕ is half the total conduction angle, 2ϕ, of the driving signal, which is considered a sine wave for transconductance PAs and a squarewave for switched PAs. Figures 6.1 and 6.2 depicts the η_D of both, transconductance and switched PAs, respectively, as a function of 2ϕ. As can be seen, for the case of transconductance PAs, the drain efficiency increases monotonically with the decrease of the conduction angle. The theoretical efficiency is 50% at Class A operation, 78.5% at Class B and it approaches 100% as the conduction angle shrinks towards zero. However, the high efficiency at the Class C operation is at the expense of diminishing the output power deliver at the load. In general, reducing the conduction angle limits the amount of charge injected into the load network and thus reduces the deliverable output power. On the other hand, for the case of switched PAs, we can appreciate that the maximum η_D, about 81%, is achieved at the symmetrical squarewave case, which corresponds to the generation of a maximum proportion of energy at the fundamental. As 2ϕ departs from π

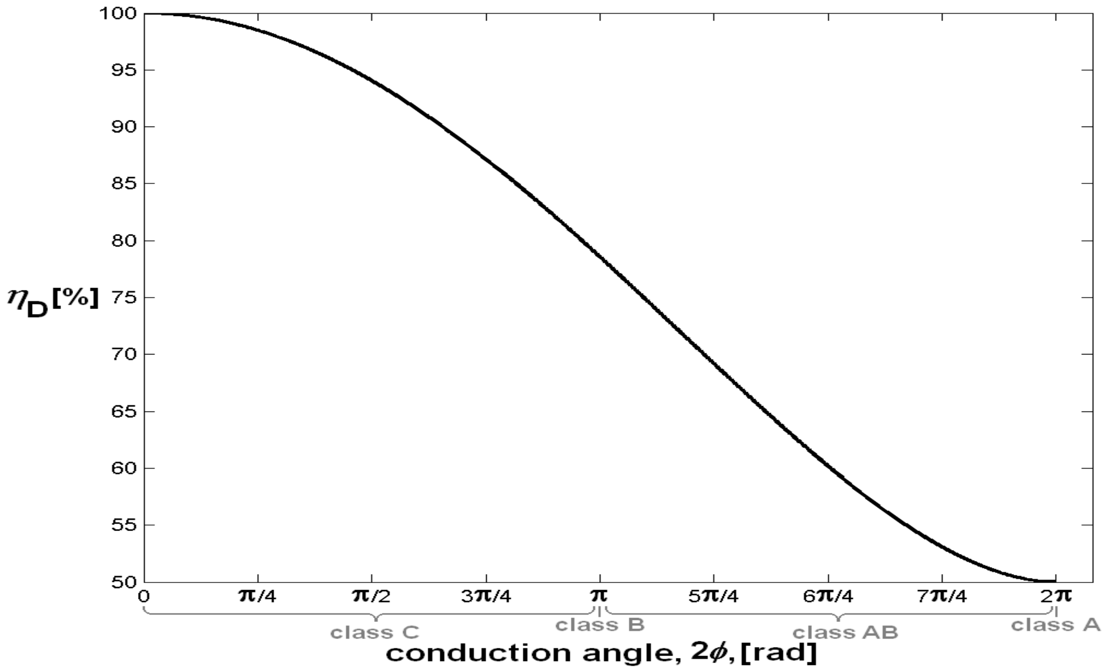

Figure 6.1: *Drain efficiency of transconductance PAs vs conduction angle.*

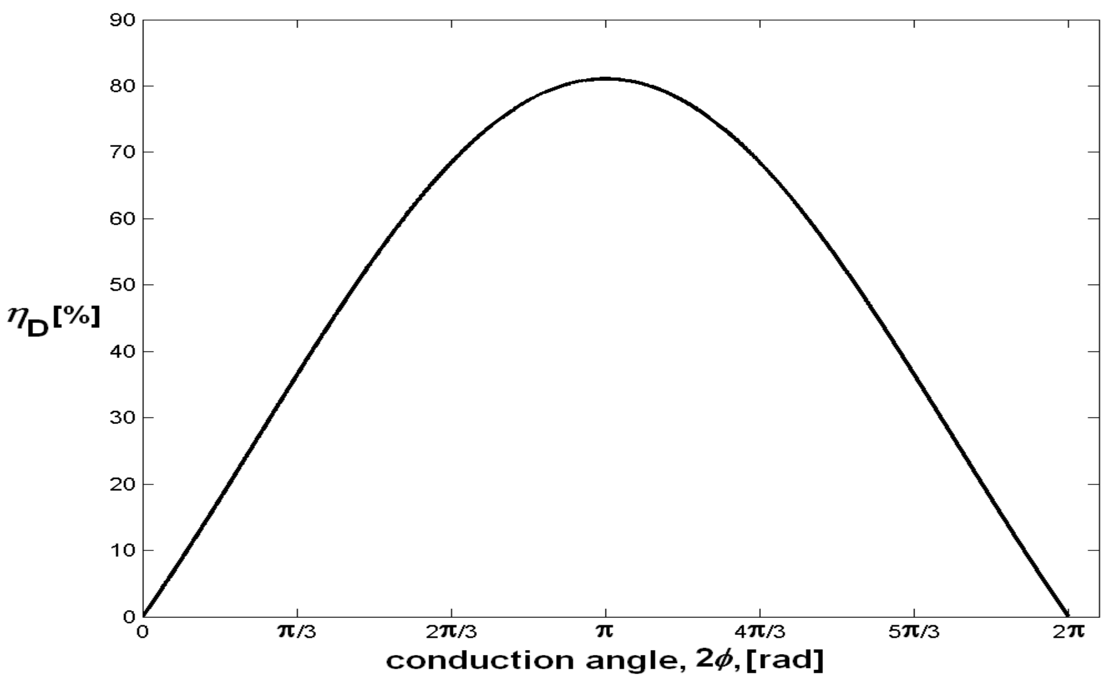

Figure 6.2: *Drain efficiency of switched PAs vs conduction angle.*

at both, left and right sides, η_D decreases monotonically approaching zero at conduction angles of 0 and 2π, respectively. The reason because of the η_D does not reach the maximum 100% value is due to the fact that some power is wasted in the generation of harmonics in the switched PAs [18].

The efficiency analysis in the previous chapter revealed that the A_P of the power upconverter proposed in [27] is rather ineffective. This is due to the fact that the power at the input of the circuit employed to mix the baseband signal (BB) and the RF local oscillator signal (LO) is high. Probably, one of the simplest manners in which the A_P can be enlarged is to reduce the P_{IN}. Figure 6.3 (a) shows the power scheme of the power up-converter. As can be seen, both, the BB and the LO provide power at the input of the power amplification system. Once in the power amplification stage, those signals are mixed and the resulting power from the mixed signal is delivered to the load. Hence, the mixer is basically the intermediary between the input signals and the load. Because of the high speed at which transistor M_2 in the power upcoventer is switched, the power at the gate of this device, P_{avswcl}, is considerable high. In fact, P_{avswcl} is the major contributor to the total input power. Therefore, to place the mixer in the power amplification stage is not convenient for power efficiency. Consequently, a more effective way to mix the BB and the LO and provide some power gain to the mixed signal must be applied. Figure 6.3 (b) shows the power scheme of a direct-conversion transmitter. As can be seen, the mixer is at the back driving the power amplification stage. In such a way, the power transference of this stage to the load can be improved by modulating the power delivered by the mixer, i.e. the input power of the PA. Besides, if the mixed signal is fed into the PA such that it is capable of modifying the conduction angle of the amplifier, then also the η_D can be controlled. Moreover, the power demands on the BB can be relaxed. In sum, the allocation of the mixer out of the power amplification stage is more convenient for power efficiency.

There is no novelty on the direct conversion diagram of Figure 6.3 (b). Typically, in a zero-IF transmitter, the mixer is allocated behind the PA. However, the usual metrics to evaluate the performance of a mixer are: conversion gain/loss, noise figure, port isolations, linearity, and power consumption [37]. From those, noise figure and port isolations are of major concern in case that the mixer is

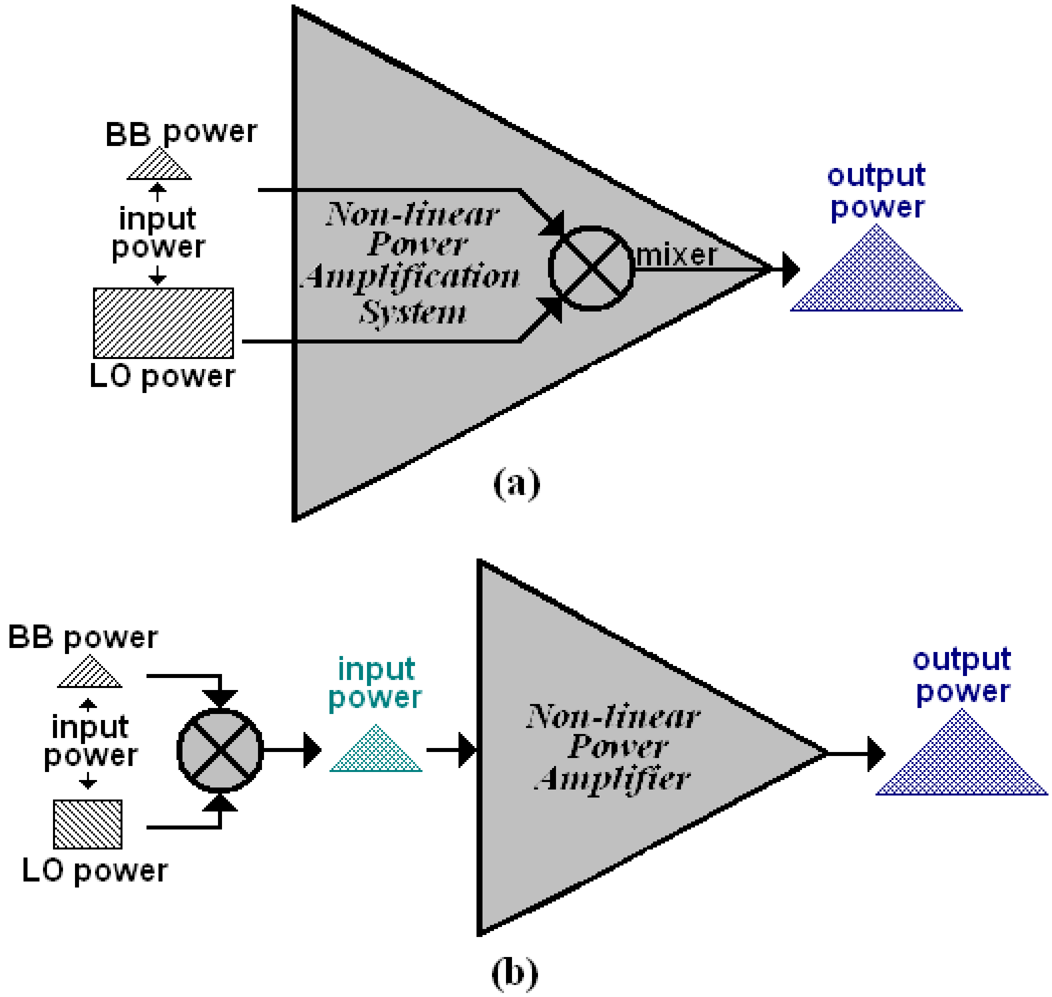

Figure 6.3: *Power scheme of: (a) the power up-converter proposed in [27] and (b) a direct-conversion transmitter.*

intended to be used in a receiver circuit. In addition, with the use of the multipath polyphase technique, linearity is, in principle, not a major issue. Instead, the demands on the performance of the mixer used as a predriver stage just like depicted in Figure 6.3 (b) in a multipath polyphase architecture with improved efficiency can focus in the following aspects:

- Output power modulation.

- Capability of modifying the conduction angle of its output signal, i.e. the driving signal of the PA.

From the many mixer architectures available, it is difficult to find one which exhibits those features. Therefore, we have to synthesize a new circuit which translates the BB up to RF by the LO and, at the same time, capable of modulating its output power and modifying the conduction angle of its output signal.

6.3 The Predriver Stage

As mentioned previously in section 6.2, the predriver stage consists of a mixer which performs the up conversion of the BB to RF by the LO. There are basically two ways to accomplish the frequency translation of two signals. The first method is by means of a non-linear circuit whose non-linearities generate harmonics and IM products, and the second possibility is with the use of a time variant circuit. Time variant circuits undergo response variation with a strong dependence on time, such as switching circuits. The use of large signal swings with abrupt transition between their maximum and minimum values to change the state of switches from closed to open and viceversa yields in a combination of the many frequency components of the large signal swing with the signal passing through the switch. Switching circuits known as harmonic mixers are used in transceivers to down convert and up convert either, the RF and IF signals, respectively [37]. Since harmonic mixers possess a low self-mixing DC offset, these result attractive for zero-IF transmitters, with the drawback of having a conversion gain usually small [38]. Therefore, a starting point in the fulfillment of the predriver stage may be set with the analysis of a simple time variant circuit.

Figure 6.4 depicts the action of a simple switching circuit with two switches, S_1 and S_2, and one capacitor, C. The LO signal controls the action of S_1 and S_2 such that they operate in turn. When LO is at a high value S_2 is open and S_1 is closed leading to the charge of capacitor C at voltage V_{BB} which is provided by the voltage source on the left. Assuming there is some resistance value between the terminals of S_1 when it is closed then there is an RC circuit given by the series connection of C and the resistive value of the switch. The time constant of the RC circuit establishes a rise time, t_r, in which C is charged at approximately V_{BB}. On the other hand, when LO is at a low value S_1 is open meanwhile S_2 is closed. Again, assuming there is an RC circuit given by the resistive value between the

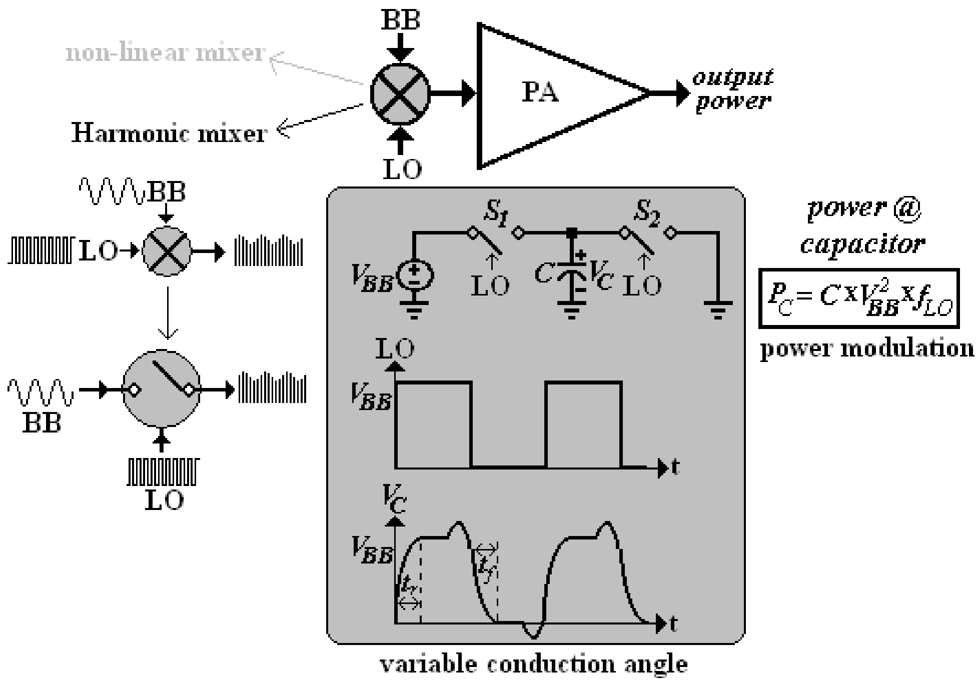

Figure 6.4: *Switching circuit used as a mixer.*

terminals of S_2 when it is closed and the capacitor C, the time constant given by this RC circuit establishes a fall time, t_f, in which C is discharged completely. Note that if there are different rise and fall times in the circuit, it is possible to alter the duty cycle of the resulting signal. In other words, we can modify the conduction angle of the signal at the output by changing the time constants in the circuit, which can be done easily by changing the resistive value of the switches. Moreover, the power at the output of circuit such as the one depicted in Figure 6.4 is given by [36]

$$P_C = CV_{BB}^2 f_{LO} \tag{6.3}$$

where f_{LO} is the frequency of the LO. According with this expression, the output power is proportional to the quadratic value of voltage V_{BB}. Thus, the output power can be controlled by changing the value of V_{BB}. Therefore, it is convenient to use a switched RC network as a pre-driver mixer for the PA stage in a multipath polyphase transmitter since it allows to modulate the power at its output and to change the duty cycle of the output waveform, which are the two aspects desired

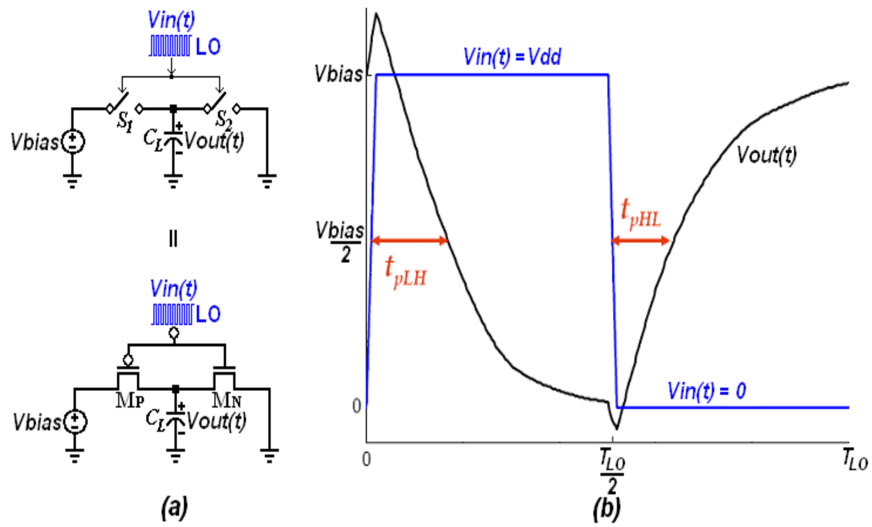

Figure 6.5: *CMOS inverter: (a) schematic diagram and (b) input and output waveforms.*

on the performance of the predriver in order to improve the efficiency of the circuit.

Now that we have deduced why a switched RC predriver is convenient for our purposes, the next step in the synthesis is to determine how to built it in CMOS technology. Figure 6.5 (a) shows the circuit diagram with transistors M_P and M_N of the harmonic mixer previously analyzed. Now the voltage source which charges the load capacitor, C_L, has been labeled as V_{bias}, meanwhile the LO has been also marked as $V_{in}(t)$. Since devices M_P and M_N are complementary, they work in turn controlled by the LO. Thus, when $V_{in}(t) = 0V$, M_P is closed and M_N is open, with the consequent charge of C_L. On the other hand, when $V_{in}(t) = V_{dd}$, where V_{dd} is the maximum biasing voltage allowed, M_P is open and M_N is closed, granting the discharge of C_L. This is not other circuit than a CMOS inverter gate whose input and output waveforms are depicted in Figure 6.5 (b). As can be seen, there is some delay in the output voltage at both transitions, when the signal goes from V_{bias} to zero and vice versa. These propagation delays are labeled as t_{pHL} and t_{pLH}, respectively, and can be expressed as [36]

$$t_{pHL} = \frac{C_L V_{bias}}{\left(\frac{W_N}{L}\right)\mu_n C_{OX}(V_{dd} - V_{THN})^2} \tag{6.4}$$

$$t_{pLH} = \frac{C_L V_{bias}}{\left(\frac{W_P}{L}\right)\mu_p C_{OX}(-V_{bias} - |V_{THP}|)^2} \tag{6.5}$$

where C_{OX} is the oxide capacitance; μ_n is the mobility of the electrons and μ_p the mobility of the holes; L is the length of the devices; W_N and W_P are the respective widths of the NMOS and PMOS transistors whereas V_{THN} and V_{THP} are their corresponding threshold voltages.

According to (6.4), the propagation delay t_{pHL} is directly proportional to the supply voltage, V_{bias}. On the other hand, expression (6.5) indicates that the propagation delay t_{pLH} decreases inversely with the quadratic increment of V_{bias}. Figure 6.6 illustrates the variations on the propagation delays as a function of V_{bias} and the width of the transistors. In order to compute those values, parameters of the UMC 0.18um Mixed Mode and RF CMOS technology were used and a load capacitance, C_L, of 1pF was considered. As can be seen, both propagation delays decrease with the increasing size of transistors and t_{pLH} exhibits a larger variation than t_{pHL} in function of both variables, the width and V_{bias}. In general, the value of t_{pLH} is higher than the value of t_{pHL}.

The variations on the propagation delays will change the pulse width of the output signal, dt_{out}, in function of the supply voltage, V_{bias}. By inspection of Figure 6.5 (b), it can be inferred that the duty cycle of $V_{out}(t)$ in terms of t_{pHL} and t_{pLH} is given by

$$dt_{out} = T_{in} - dT_{in} + (t_{pHL} - t_{pLH}) \tag{6.6}$$

where T_{in} and dT_{in} are the period and the pulse width of the input signal, $V_{in}(t)$, respectively.

Figure 6.7 shows the graphic of the duty cycle of $V_{out}(t)$ as a function of the supply voltage, V_{bias} and the width of transistors. In this case, the input signal was considered to present two third duty cycle, i.e. $d.t._{in} = 66.66\%$ [1]. Since the value of t_{pLH} is higher than the value of t_{pHL}, the width of transistor M_P was taken three times smaller than the width of transistor M_N. As can be

[1]Two third duty cycle was taken into account in order to have one third duty cycle at the output of the inverter since that is the pulse width used by the multipath-polyphase technique to get rid of the troublesome third order distortion components.

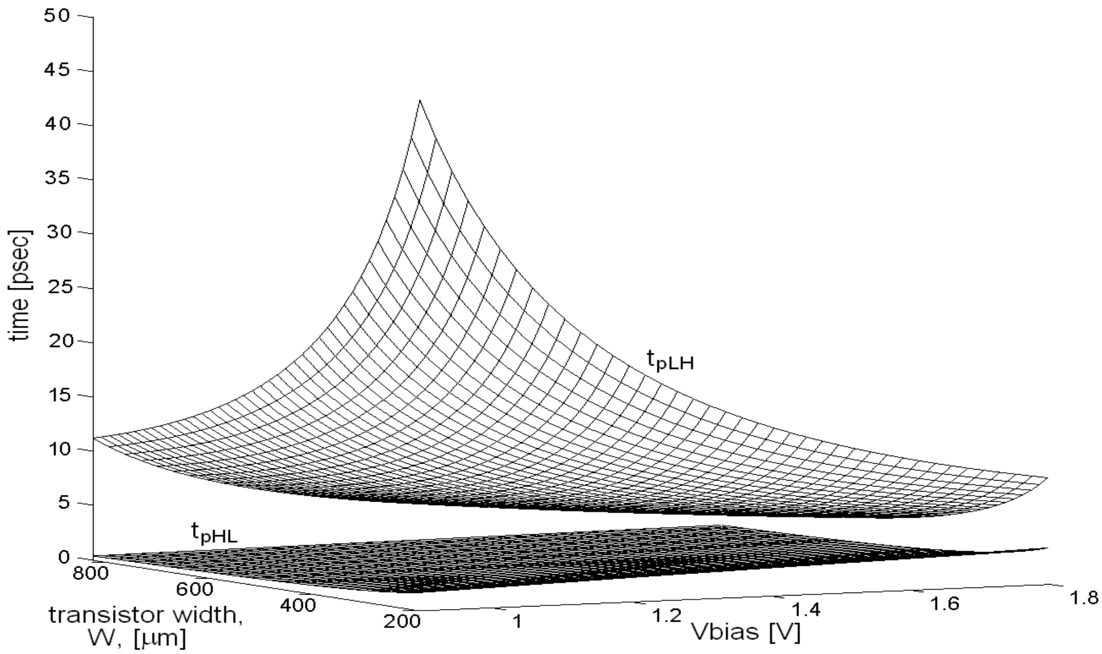

Figure 6.6: *Propagation delays t_{pHL} and t_{pLH} of the inverter as a function of the supply voltage, V_{bias}, and the width of the corresponding transistor, W_P and W_N.*

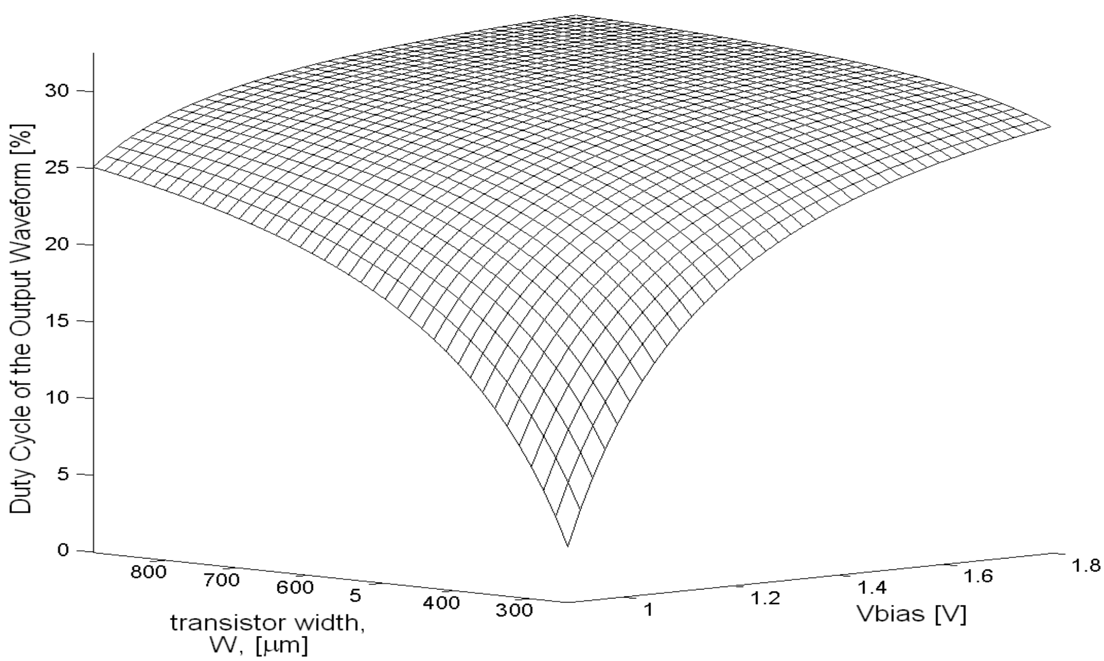

Figure 6.7: *Duty Cycle of the output waveform as a function of the supply voltage, V_{bias}, and the width of the corresponding transistor, W_P and W_N.*

seen, for the case of the maximum transistor width, when V_{bias} equals V_{dd} (1.8V), $d.t._{out}$ exhibits approximately the expected one third duty cycle (33%). As V_{bias} decreases, $d.t._{out}$ also becomes smaller. When V_{bias} equals half V_{dd} (0.9V), $d.t._{out}$ is reduced at about one quarter duty cycle (25%). On the other hand, conforming the width of the transistors decrease, the reduction of the duty cycle in proportion with V_{bias} becomes even larger. Therefore, there is a variation on the width of the output pulse of the inverter in function of the supply voltage, V_{bias}, and thus, the conduction angle of $V_{out}(t)$ can be modified.

Now that we have verified how the conduction angle at the output of the inverter can be changed, we have to analyze the way in which this circuit mixes the BB and LO signals. As can be seen in Figure 6.8(a), the LO is placed at the input of the inverter meanwhile the BB is fed through a current source connected between the power supply, V_{bias}, and the supply terminal of the inverter. The resistor R_m represents the output resistance of the current source and capacitor C_L is the load at the output of the gate. In order to facilitate the analysis, the equivalent circuit in Figure 6.8 (b) is used. The inverter is modeled as the series connection of two switches controlled by the LO with their respective ON resistors, R_P and R_N. We consider, first, the case when the LO is at a 'low' logic value at one third duty cycle. According to Figure 6.8 (c), when that happens the upper switch is closed allowing the interconnection of the current source, I_{bb}, with the series connection of resistor, R_P, and capacitor, C_L. In this form, the current I_{bb} produces a voltage drop, v_{out}, between the terminals of C_L. On the other hand, when the LO is at a 'high' logic value around two third duty cycle, the situation depicted in Figure 6.8 (d) occurs. In this case, the voltage v_{out}, stored in capacitor C_L, is discharged through resistor R_N. By means of circuit analysis and assuming that the current I_{bb} is a sinusoidal signal of the form $I_{bb} = I_{bias} + i_{bb}cos(\omega_{bb}t)$, where I_{bias} is the DC component, i_{bb} the amplitude of the current and w_{bb} the frequency of the BB, it is found that

$$v_x = V_{bias} + R_m I_{bias} + R_m i_{bb} \cos(\omega_{bb} t) \tag{6.7}$$

and

$$v_{out} \approx v_x[1 - v_{in}(t)] \tag{6.8}$$

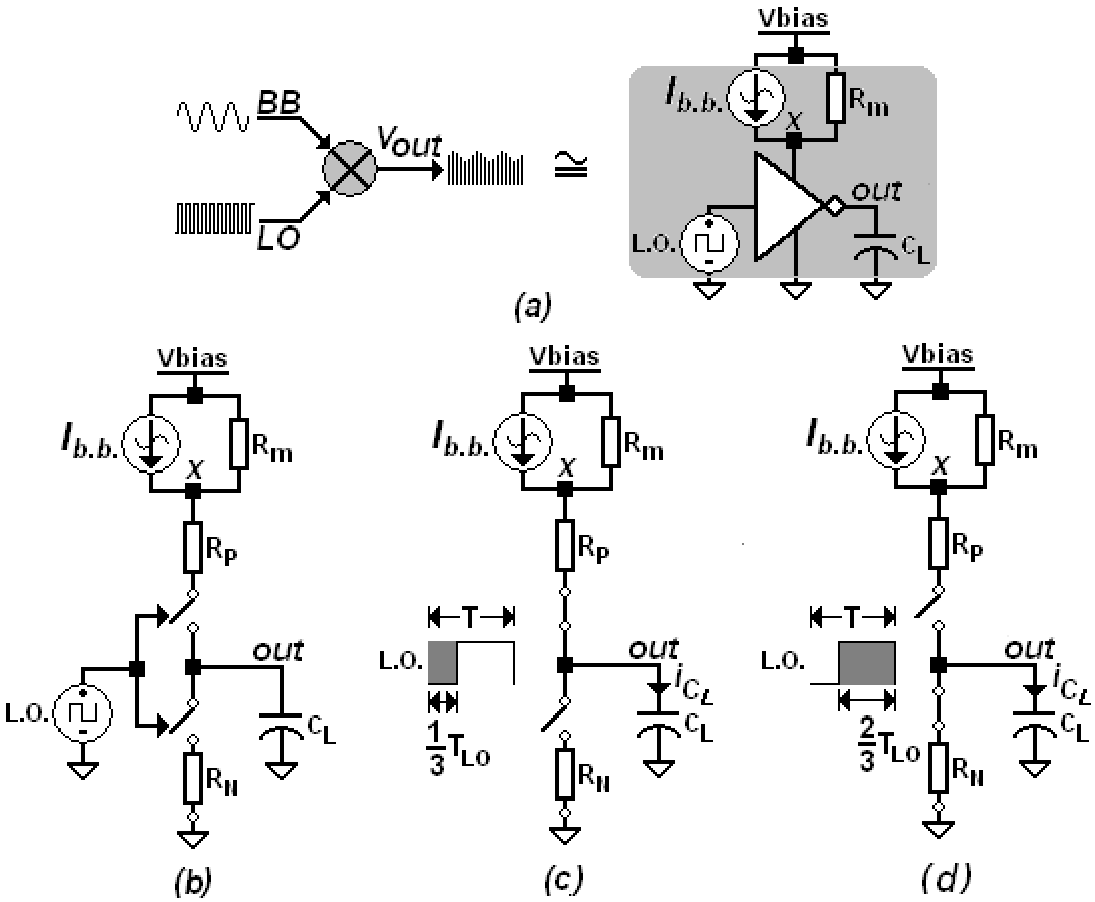

Figure 6.8: *The proposed mixer: (a) schematic diagram, (b) equivalent circuit, (c)equivalent circuit when LO is 'low', and (d) equivalent circuit when LO is 'high'.*

where $v_{in}(t)$ is the input signal, which corresponds to the square wave from the LO and that can be mathematically expressed as

$$v_{in}(t) = \begin{cases} 0 & \text{for } 0 < t < \dfrac{T_{LO}}{3} \\ 1 & \text{for } \dfrac{T_{LO}}{3} < t < T_{LO} \end{cases} \tag{6.9}$$

and T_{LO} is the period of the LO.

Figure 6.9 depicts the square wave of the LO, $v_{in}(t)$, in expression (6.9). If we expand $v_{in}(t)$ into its Fourier series, then the term $1 - v_{in}(t)$ in expression (6.8) can be re-written as

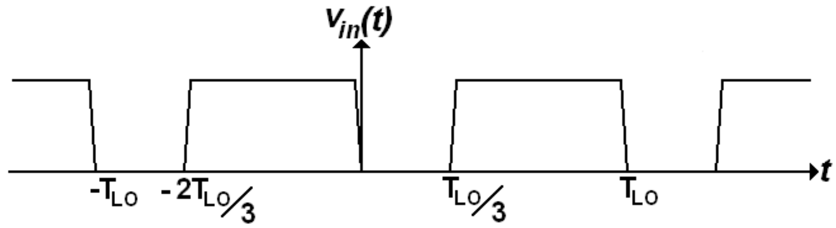

Figure 6.9: *LO square wave, $v_{in}(t)$.*

$$\begin{aligned} 1 - v_{in}(t) &= \frac{2}{3} - \frac{\sqrt{3}}{\pi}\cos\omega_{LO}t + \frac{\sqrt{3}}{2\pi}\cos 2\omega_{LO}t - \frac{\sqrt{3}}{4\pi}\cos 4\omega_{LO}t + \\ &\quad + \frac{3}{5\pi}\cos 5\omega_{LO} - \frac{\sqrt{3}}{7\pi}\cos 7\omega_{LO}t + \frac{\sqrt{3}}{8\pi}\cos 8\omega_{LO}t - \cdots \end{aligned} \tag{6.10}$$

and hence, the output voltage, v_{out}, is given by

$$\begin{aligned} v_{out} &\approx \{V_{bias} + R_m I_{bias}\}\Big\{\frac{2}{3} - \frac{\sqrt{3}}{\pi}\cos\omega_{LO}t + \frac{\sqrt{3}}{2\pi}\cos 2\omega_{LO}t - \\ &\quad -\frac{\sqrt{3}}{4\pi}\cos 4\omega_{LO}t + \frac{3}{5\pi}\cos 5\omega_{LO} - \frac{\sqrt{3}}{7\pi}\cos 7\omega_{LO}t + \frac{\sqrt{3}}{8\pi}\cos 8\omega_{LO}t - \cdots\Big\} \\ &\quad -\frac{i_{bb}R_m\cos\omega_{bb}t}{\pi} - \frac{\sqrt{3}}{2\pi}i_{bb}R_m[\cos(\omega_{LO}+\omega_{bb})t + \cos(\omega_{LO}-\omega_{bb})t] + \\ &\quad +\frac{\sqrt{3}}{4\pi}i_{bb}R_m[\cos(2\omega_{LO}+\omega_{bb})t + \cos(2\omega_{LO}-\omega_{bb})t] - \\ &\quad -\frac{\sqrt{3}}{8\pi}i_{bb}R_m[\cos(4\omega_{LO}+\omega_{bb})t + \cos(4\omega_{LO}-\omega_{bb})t] + \\ &\quad +\frac{\sqrt{3}}{10\pi}i_{bb}R_m[\cos(5\omega_{LO}+\omega_{bb})t + \cos(5\omega_{LO}-\omega_{bb})t] - \\ &\quad -\frac{\sqrt{3}}{14\pi}i_{bb}R_m[\cos(7\omega_{LO}+\omega_{bb})t + \cos(7\omega_{LO}-\omega_{bb})t] + \\ &\quad +\frac{\sqrt{3}}{16\pi}i_{bb}R_m[\cos(8\omega_{LO}+\omega_{bb})t + \cos(8\omega_{LO}-\omega_{bb})t] - \cdots \end{aligned} \tag{6.11}$$

From this result, we can see that the term of interest, $\omega_{LO} + \omega_{bb}$, appears at the output of the inverter and thus, it produces the desired signal along with

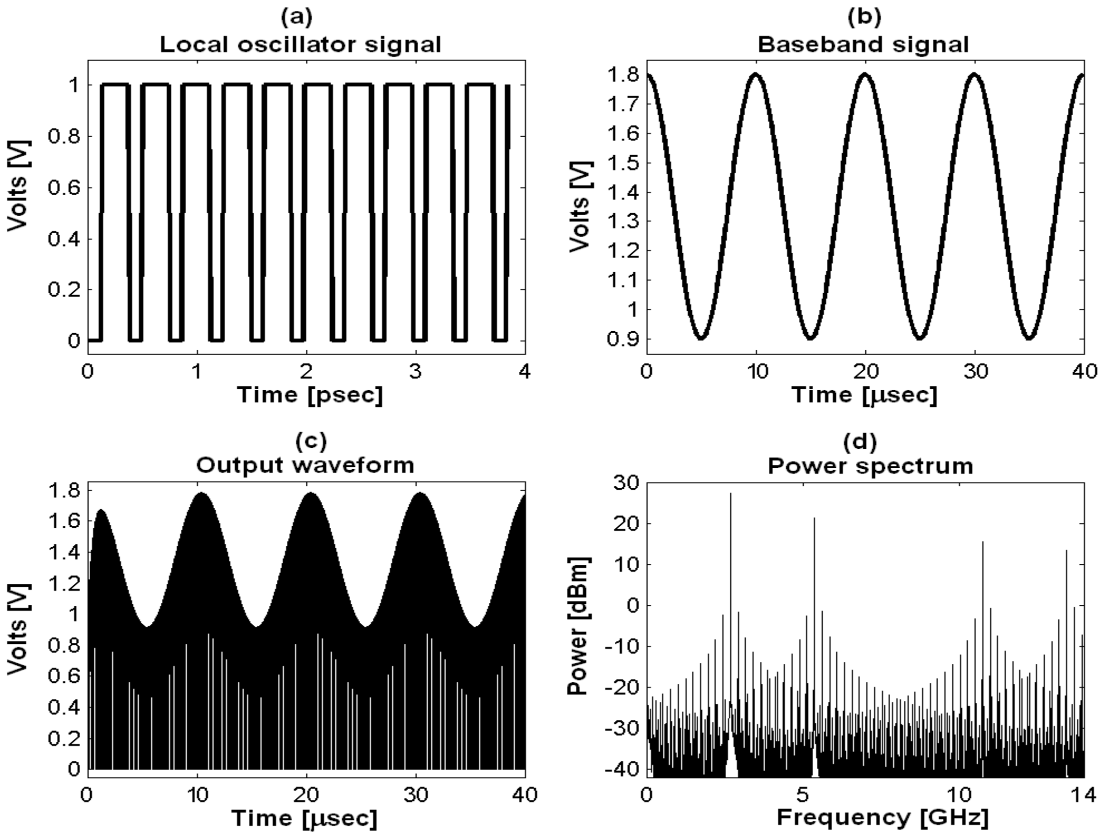

Figure 6.10: *Input and output waveforms of the mixer: (a) the LO, (b) the BB, (c) v_{out} in time domain, and (d) v_{out} in frequency domain.*

harmonics components and intermodulation products. Therefore, the circuit realizes the frequency translation of the BB towards RF given by the LO. Figure 6.10 illustrates the input and output waveforms of the mixer in both, time and frequency domain. These graphs were computed considering an LO frequency of 2.69GHz and a BB frequency of 10MHz. Figure 6.11 shows a zoom of v_{out} in the frequency domain around the frequency components $\omega_{LO} - \omega_{bb}$, ω_{LO}, and $\omega_{LO} + \omega_{bb}$.

Thus, the generation of new frequency components at the output of the circuit further than ω_{bb} and ω_{LO} comes from the time variant characteristic of the inverter gate, which is provided by the LO. Table 6.1 shows some of the effective voltage values from diverse frequency components produced by the mixer. Since one third duty cycle is present at the output signal, then the harmonics 3rd, 6th, 9th, 12th, and so on, do not appear. Note that if a fully differential architecture

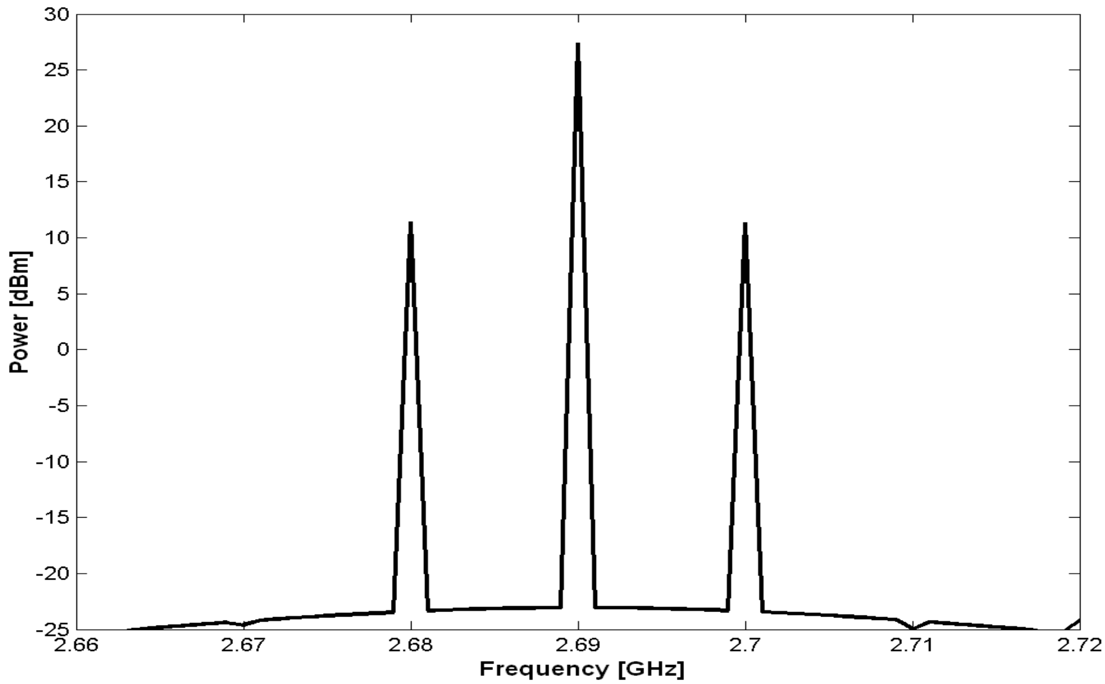

Figure 6.11: *v_{out} in frequency domain around the frequency components $\omega_{LO} - \omega_{bb}$, ω_{LO}, and $\omega_{LO} + \omega_{bb}$.*

is adopted, then the harmonics 2nd, 4th, 8th, 10th, and etcetera, are cancelled. Hence, the closer harmonic to the frequency of interest is the 5th. Depending on the frequency ω_{LO}, that harmonic can be far enough from the band of interest and consequently the linearity exhibited by the mixer may be acceptable.

It is important to analyze the power generated by the circuit since this corresponds to the power delivered to the input of the power amplification stage. Forasmuch as the leakage power contributes only in a small portion to the total power consumption and the short-circuit dissipation becomes smaller when the load capacitance increases [39], then we will analyze only the dynamic power case. First, we examine the energy provided by the sources, V_{bias} and I_{bb}, at node x in the circuit of Figure 6.8 (c) and (d), which is given by

$$E_S = \int_{t_0}^{t_1} P_x \, dt = \int_{t_0}^{t_1} i_{C_L} v_x \, dt \tag{6.12}$$

where t_0 and t_1 are the initial and final time, respectively, when either the PMOS or the NMOS switches in the inverter are closed. Note that for the time $\dfrac{T_{LO}}{3} < t <$

Table 6.1: *Some of the effective voltage values from diverse frequency components produced by the mixer.*

Frec. Component	**Coefficient [V]**	**Frec. Component**	**Coefficient [V]**
DC	$\frac{2(V_{bias}+I_{bias}R_m)}{3}$	$9\omega_{LO}$	0
ω_{bb}	$-\frac{R_m i_{bb}}{\pi\sqrt{2}}$	$\omega_{LO}+\omega_{bb}$,$\omega_{LO}-\omega_{bb}$	$-\sqrt{\frac{3}{2}}\left(\frac{i_{bb}R_m}{2\pi}\right)$
ω_{LO}	$-\sqrt{\frac{3}{2}}\left(\frac{V_{bias}+I_{bias}R_m}{\pi}\right)$	$2\omega_{LO}+\omega_{bb}$,$2\omega_{LO}-\omega_{bb}$	$\sqrt{\frac{3}{2}}\left(\frac{i_{bb}R_m}{4\pi}\right)$
$2\omega_{LO}$	$\sqrt{\frac{3}{2}}\left(\frac{V_{bias}+I_{bias}R_m}{2\pi}\right)$	$\mathbf{3}\omega_{LO}+\omega_{bb}$,$3\omega_{LO}-\omega_{bb}$	0
$3\omega_{LO}$	0	$\mathbf{4}\omega_{LO}+\omega_{bb}$,$4\omega_{LO}-\omega_{bb}$	$-\sqrt{\frac{3}{2}}\left(\frac{i_{bb}R_m}{8\pi}\right)$
$4\omega_{LO}$	$-\sqrt{\frac{3}{2}}\left(\frac{V_{bias}+I_{bias}R_m}{4\pi}\right)$	$5\omega_{LO}+\omega_{bb}$,$5\omega_{LO}-\omega_{bb}$	$\sqrt{\frac{3}{2}}\left(\frac{i_{bb}R_m}{10\pi}\right)$
$5\omega_{LO}$	$\sqrt{\frac{3}{2}}\left(\frac{V_{bias}+I_{bias}R_m}{5\pi}\right)$	$6\omega_{LO}+\omega_{bb}$,$6\omega_{LO}-\omega_{bb}$	0
$6\omega_{LO}$	0	$\mathbf{7}\omega_{LO}+\omega_{bb}$,$7\omega_{LO}-\omega_{bb}$	$-\sqrt{\frac{3}{2}}\left(\frac{i_{bb}R_m}{14\pi}\right)$
$7\omega_{LO}$	$-\sqrt{\frac{3}{2}}\left(\frac{V_{bias}+I_{bias}R_m}{7\pi}\right)$	$8\omega_{LO}+\omega_{bb}$,$8\omega_{LO}-\omega_{bb}$	$\sqrt{\frac{3}{2}}\left(\frac{i_{bb}R_m}{16\pi}\right)$
$8\omega_{LO}$	$\sqrt{\frac{3}{2}}\left(\frac{V_{bias}+I_{bias}R_m}{8\pi}\right)$	$9\omega_{LO}+\omega_{bb}$,$9\omega_{LO}-\omega_{bb}$	0

T_{LO}, $i_{C_L}=0$. On the other hand, during the time $0<t<\frac{T_{LO}}{3}$, $i_{CL}=C_L\frac{dv_{out}}{dt}$. Hence, we obtain

$$E_S \approx \begin{cases} C_L\left(V_{bias}+R_mI_{bias}+\frac{R_m i_{bb}}{\sqrt{2}}\right)^2 & \text{for } 0<t<\frac{T_{LO}}{3} \\ 0 & \text{for } \frac{T_{LO}}{3}<t<T_{LO} \end{cases} \tag{6.13}$$

Part of this energy is dissipated by the PMOS and NMOS transistors in the inverter and the resistor R_m associated with the current source, I_{bb}. Only a fraction is transferred to the load, C_L. It can be found that the energy stored in the capacitor C_L is given by

$$E_{C_L} = \begin{cases} \frac{C_L}{2}\left(V_{bias}+R_mI_{bias}+\frac{R_m i_{bb}}{\sqrt{2}}\right)^2 & \text{for } 0<t<\frac{T_{LO}}{3} \\ 0 & \text{for } \frac{T_{LO}}{3}<t<T_{LO} \end{cases} \tag{6.14}$$

Similarly, the energy dissipated by resistor R_m is

$$E_{R_m} = R_m\left(\frac{2}{3}I_{bias}^2 + \frac{4}{3\sqrt{2}}i_{bb}I_{bias} + \frac{i_{bb}^2}{3}\right)T_{LO} \quad \text{for } 0 < t < T_{LO} \tag{6.15}$$

During the time $\frac{T_{LO}}{3} < t < T_{LO}$, there is no energy dissipated by the PMOS transistor. However, for the time $0 < t < \frac{T_{LO}}{3}$, the energy dissipated is given by the energy provided by the sources V_{bias} and I_{bb}, E_S, minus the energy transferred to the load, E_{C_L}, and the energy dissipated by resistor R_m, E_{R_m}, i.e. $E_{PMOS} = E_S - E_{C_L} - E_{R_m}$. Thus

$$E_{PMOS} = \begin{cases} \frac{C_L}{2}\left(V_{bias} + R_m I_{bias} + \frac{R_m i_{bb}}{\sqrt{2}}\right)^2 - \\ -R_m\left(\frac{I_{bias}^2}{3} + \frac{2}{3\sqrt{2}}i_{bb}I_{bias} + \frac{i_{bb}^2}{6}\right)T_{LO} & \text{for } 0 < t < \frac{T_{LO}}{3} \\ 0 & \text{for } \frac{T_{LO}}{3} < t < T_{LO} \end{cases} \tag{6.16}$$

On the other hand, we have that during the time $0 < t < \frac{T_{LO}}{3}$, there is no energy dissipation by the NMOS device. Nevertheless, for the time $\frac{T_{LO}}{3} < t < T_{LO}$, the energy stored in the load is dissipated by the ON resistor of the NMOS transistor, R_N. In this manner, we get

$$E_{NMOS} = \begin{cases} 0 & \text{for } 0 < t < \frac{T_{LO}}{3} \\ \frac{C_L}{2}\left(V_{bias} + R_m I_{bias} + \frac{R_m i_{bb}}{\sqrt{2}}\right)^2 & \text{for } \frac{T_{LO}}{3} < t < T_{LO} \end{cases} \tag{6.17}$$

Finally, the energy dissipated and the energy transferred in a complete cycle are given by the summation of the the correspondent contributions in each element. In this way, considering that a complete switching cycle takes place every f_{LO} times per second, where f_{LO} is the frequency of the LO, we get that the total output power transferred to the load is expressed as

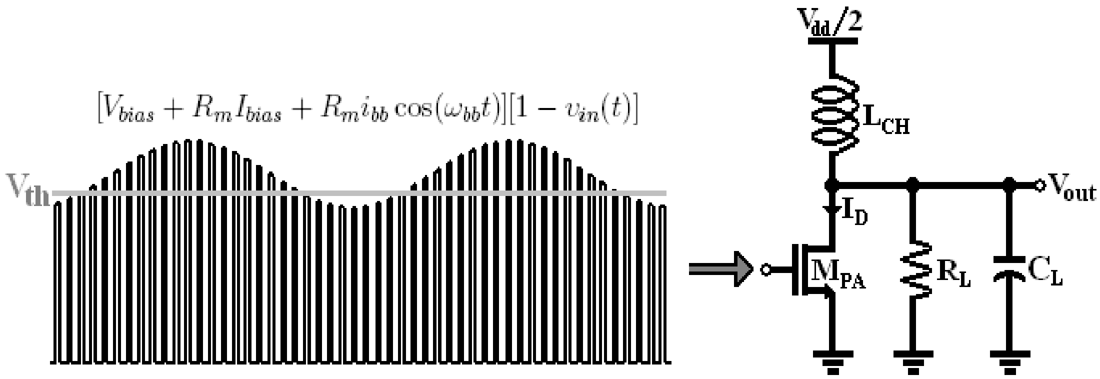

Figure 6.12: *Power Amplifier and its input voltage signal from the pre-driver stage.*

$$P_{OUT} = \frac{C_L}{2}\left(V_{bias} + R_m I_{bias} + \frac{R_m i_{bb}}{\sqrt{2}}\right)^2 f_{LO} \tag{6.18}$$

the total input power at node x is given by

$$P_{IN} = C_L\left(V_{bias} + R_m I_{bias} + \frac{R_m i_{bb}}{\sqrt{2}}\right)^2 f_{LO} \tag{6.19}$$

and the total power dissipated by the circuit is

$$P_D = C_L\left(V_{bias} + R_m I_{bias} + \frac{R_m i_{bb}}{\sqrt{2}}\right)^2 f_{LO} \tag{6.20}$$

Therefore, in a cycle, only one half of the input power provided by the sources V_{bias} and I_{bb} is transferred to the output. The power dissipated by the circuit is equal to the input power, one part is consumed when $v_{in}(t) = 0$ by the PMOS transistor and resistor R_m and the rest is dispelled when $v_{in}(t) = 1$ by the NMOS transistor and resistor R_m.

6.4 The Power Amplification Stage

Figure 6.12 shows the Power Amplifier (PA) which is fed with the output voltage from the pre-driver stage. When that signal is below the threshold voltage, V_{TH}, of transistor M_{PA}, the device is turned off and no current signal flows on the drain terminal. As soon as the voltage surpasses V_{TH} the transistor is turned on and there is a current signal flowing to the load. Since the amplitude of the pulse

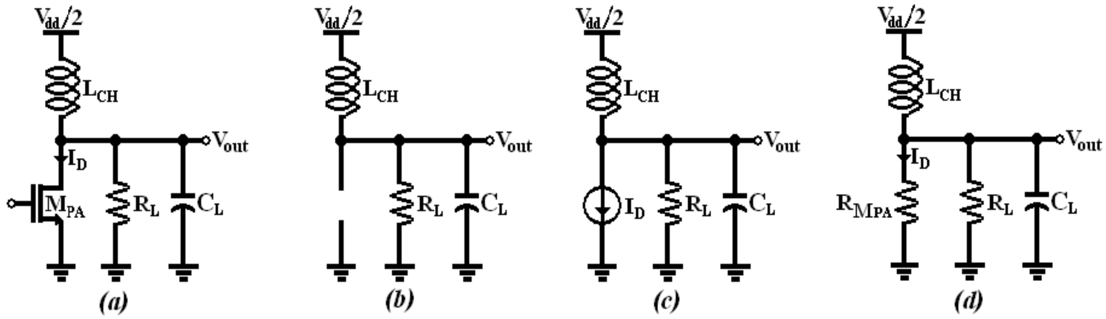

Figure 6.13: *Power Amplifier in different modes of operation: (a)circuit diagram, (b)M_{PA} as an open switch, (c)M_{PA} in saturation, and (d)M_{PA} as a closed switch.*

train is variable, then the PA cannot be considered to be driven as a switched PA. Switch-mode PAs work by switching the voltage across the load between the supply and ground. However, in the case depicted in Figure 6.12, the amplitude of the driver pulse some times is large enough (when the voltage swing from the pre-driver equals V_{dd}) so that the overdrive voltage at the input, $V_{GS} - V_{TH}$, is larger than the voltage at the drain terminal of the transistor, $V_{dd}/2$, and thus, the transistor acts as a closed switch. On the other hand, when the swing of the driver signal becomes smaller and consequently the overdrive voltage decreases so that $V_{GS} - V_{TH} < V_{dd}/2$, the transistor is in saturation mode. Therefore, the PA is driven as a mixed mode class C PA where the active device presents different modes of operation depending on the magnitude of its input voltage [42]. Thus, the analysis of what happens in every case must be done.

Figure 6.13 depicts the equivalent circuit of the PA in its different modes of operation determined by the output signal from the pre-driver stage. R_L represents the resistive load provided by either the antenna or a matching network; C_L is the capacitive load compound by the parasitic capacitance of M_{PA} and L_{CH} is the choke inductor which fixes the DC at the drain terminal of M_{PA}. Assuming that initially the device is in the cut-off region, then the transistor acts as an open switch, as shown in Figure 6.13(b), and the voltage at the output is given by $V_{out} = V_{dd}/2$, meanwhile the current through R_L is expressed as $I_{R_L} = V_{dd}/2R_L$. Then, when the output signal from the pre-driver stage surpasses the threshold voltage and the overdrive voltage is smaller than the output voltage, the device is in saturation and now the transistors behaves as a voltage-controlled current

Table 6.2: *Some of the distortion components produced when M_{PA} is in saturation.*

Frec. Component	**Coefficient [A]**
DC	$\mu_n C_{OX}\left(\frac{W}{L}\right)\left\{0.65\left[(V_{dc})^2+\frac{(V_{ac})^2}{2}\right]-1.34V_{dc}V_{TH}+(V_{TH})^2\right\}$
ω_{bb}	$\mu_n C_{OX}\left(\frac{W}{L}\right)\left[V_{ac}(1.3V_{dc}-1.33V_{TH})\right]$
$2\omega_{bb}$	$\mu_n C_{OX}\left(\frac{W}{L}\right)0.325(V_{ac})^2$
ω_{LO}	$\mu_n C_{OX}\left(\frac{W}{L}\right)\left\{-0.9\left[(V_{dc})^2+\frac{(V_{ac})^2}{2}\right]+1.1V_{dc}V_{TH}\right\}$
$2\omega_{LO}$	$\mu_n C_{OX}\left(\frac{W}{L}\right)\left\{0.5\left[(V_{dc})^2+\frac{(V_{ac})^2}{2}\right]-0.55V_{dc}V_{TH}\right\}$
$3\omega_{LO}$	$\mu_n C_{OX}\left(\frac{W}{L}\right)0.05\left[(V_{dc})^2+\frac{(V_{ac})^2}{2}\right]$
$4\omega_{LO}$	$\mu_n C_{OX}\left(\frac{W}{L}\right)\left\{-0.2\left[(V_{dc})^2+\frac{(V_{ac})^2}{2}\right]+0.28V_{dc}V_{TH}\right\}$
$5\omega_{LO}$	$\mu_n C_{OX}\left(\frac{W}{L}\right)\left\{0.2\left[(V_{dc})^2+\frac{(V_{ac})^2}{2}\right]+0.22V_{dc}V_{TH}\right\}$
$\omega_{LO}\pm\omega_{bb}$	$\mu_n C_{OX}\left(\frac{W}{L}\right)(-0.9V_{dc}V_{ac}+0.55V_{ac}V_{TH})$
$\omega_{LO}\pm 2\omega_{bb}$	$\mu_n C_{OX}\left(\frac{W}{L}\right)[-0.225(V_{ac})^2]$
$2\omega_{LO}\pm\omega_{bb}$	$\mu_n C_{OX}\left(\frac{W}{L}\right)(0.5V_{dc}V_{ac}-0.275V_{ac}V_{TH})$
$2\omega_{LO}\pm 2\omega_{bb}$	$\mu_n C_{OX}\left(\frac{W}{L}\right)0.125(V_{ac})^2$
$3\omega_{LO}\pm\omega_{bb}$	$\mu_n C_{OX}\left(\frac{W}{L}\right)0.05V_{dc}V_{ac}$
$3\omega_{LO}\pm 2\omega_{bb}$	$\mu_n C_{OX}\left(\frac{W}{L}\right)0.0125(V_{ac})^2$
$4\omega_{LO}\pm\omega_{bb}$	$\mu_n C_{OX}\left(\frac{W}{L}\right)(-0.2V_{dc}V_{ac}+0.137V_{ac}V_{TH})$
$4\omega_{LO}\pm 2\omega_{bb}$	$\mu_n C_{OX}\left(\frac{W}{L}\right)[-0.05(V_{ac})^2]$
$5\omega_{LO}\pm\omega_{bb}$	$\mu_n C_{OX}\left(\frac{W}{L}\right)(0.2V_{dc}V_{ac}-0.11V_{ac}V_{TH})$
$5\omega_{LO}\pm 2\omega_{bb}$	$\mu_n C_{OX}\left(\frac{W}{L}\right)0.05(V_{ac})^2$

$V_{dc}=V_{bias}+I_{bias}R_m,\ V_{ac}=i_{bb}R_m$

source, just like in Figure 6.13(c). The current provided by the device, I_D, is approximately given by

$$I_D=\mu_n C_{OX}\frac{W}{L}(V_{in}-V_{TH})^2 \tag{6.21}$$

where μ_n and C_{OX} are the mobility of the carriers and the oxide capacitance, respectively; W is the width of the transistor and L its length; V_{TH} is the threshold voltage and V_{in} the one third duty cycle square wave from the predriver stage whose Fourier expansion is expressed in equation (6.11). If we combine this equation with expression (6.21), many different harmonics and intermodulation products appear in the current of the transistor. Table 6.2 shows the coefficient of some of those distortion components. For the time being, we are interested in the frequency term $\omega_{LO} + \omega_{bb}$, which corresponds to the up-converted signal we want to transmit. Thus, we do not take into account the effect of the distortion components and consider that the current I_D can be expressed approximately as

$$I_D \approx \mu_n C_{OX} \frac{W}{L} \cos(\omega_{LO}+\omega_{bb})t[-0.9(V_{bias}+I_{bias}R_m)i_{bb}R_m+0.5i_{bb}R_mV_{TH}] \quad (6.22)$$

In this way, by applying the Kirchoff's current law to the node V_{out} of the equivalent circuit depicted in Figure 6.13(c), we get

$$\frac{dV_{out}^2}{dt^2} + \frac{1}{C_L R_L}\frac{dV_{out}}{dt} - \frac{V_{out}}{C_L L_{CH}} = -\frac{1}{C_L}\frac{dI_D}{dt} \quad (6.23)$$

If $2R_LC_L < \sqrt{L_{CH}C_L}$, which is not difficult to satisfy considering that the value of L_{CH} is around 3 or 4 nanoHenries in case that the choke inductor is established by means of a bondwire and since the typical R_L value is 50Ω (or less if a matching network is employed) and the value of C_L of some picoFarads, then the natural response of the network, V_{outn}, is of the form $V_{outn} = A_1e^{S_1t} + A_2e^{S_2t}$. By means of circuit analysis the values of the coefficients A_1 and A_2 can be found and finally obtain

$$V_{outn} = \frac{V_{dd}}{2(S_2 - S_1)}\left[\left(\frac{2}{R_LC_L} + S_2\right)e^{S_1t} - \left(\frac{2}{R_LC_L} + S_1\right)e^{S_2t}\right] \quad (6.24)$$

where

$$S_{1,2} = -\frac{1}{2R_LC_L} \pm \sqrt{\frac{1}{4R_L^2C_L^2} - \frac{1}{L_{CH}C_L}}$$

On the other hand, to obtain the forced response of the network, we first solve dI_D/dt and use the result in expression (6.23). By doing this, we get

$$
\begin{aligned}
V_{outf} \quad = \quad & \frac{R_L L_{CH}^2(\omega_{LO}+\omega_{bb})^2}{R_L^2 L_{CH}^2 C_L^2(\omega_{LO}+\omega_{bb})^4+(2R_L^2 C_L+L_{CH})(\omega_{LO}+\omega_{bb})^2 L_{CH}+R_L^2} \\
& \times \mu_n C_{OX}\frac{W}{L}\big[0.9(V_{bias}+I_{bias}R_m)i_{bb}R_m-0.55i_{bb}R_m V_{TH}\big] \\
& \times\left\{\frac{R_L C_L}{(\omega_{LO}+\omega_{bb})}\left[\frac{1}{L_{CH}C_L}+(\omega_{LO}+\omega_{bb})^2\right]\sin(\omega_{LO}+\omega_{bb})t\right. \\
& \left. +\cos(\omega_{LO}+\omega_{bb})t\right\}
\end{aligned} \tag{6.25}
$$

and by adding (6.24) and (6.25), we attain the output voltage of the PA when the transistor is in saturation, V_{outsat}, which is

$$
\begin{aligned}
V_{outsat} \quad = \quad & \frac{V_{dd}}{2(S_2-S_1)}\left[\left(\frac{2}{R_L C_L}+S_2\right)e^{S_1 t}-\left(\frac{2}{R_L C_L}+S_1\right)e^{S_2 t}\right]+\mu_n C_{OX}\frac{W}{L} \\
& \times\big[0.9(V_{bias}+I_{bias}R_m)i_{bb}R_m-0.55i_{bb}R_m V_{TH}\big]\times \\
& \frac{R_L L_{CH}^2(\omega_{LO}+\omega_{bb})^2}{R_L^2 L_{CH}^2 C_L^2(\omega_{LO}+\omega_{bb})^4+(2R_L^2 C_L+L_{CH})(\omega_{LO}+\omega_{bb})^2 L_{CH}+R_L^2} \\
& \times\left\{\frac{R_L C_L}{(\omega_{LO}+\omega_{bb})}\left[\frac{1}{L_{CH}C_L}+(\omega_{LO}+\omega_{bb})^2\right]\sin(\omega_{LO}+\omega_{bb})t\right. \\
& \left. +\cos(\omega_{LO}+\omega_{bb})t\right\}
\end{aligned} \tag{6.26}
$$

It is possible to determine the current signal through L_{CH} by means of the Kirchhoff's current law applied to the node V_{out} in Figure 6.13(c). By doing this, we see that

$$
i_{L_{CH}} = i_D(t) + \frac{V_{out}}{R_L} + C_L\frac{dV_{out}}{dt}
$$

Employing (6.26) in the above equation , L_{CH} is expressed as

$$
\begin{aligned}
i_{L_{CH}} \;=\; & \frac{V_{dd}}{2(S_2 - S_1)}\left\{\left(\frac{2}{R_L C_L} + S_2\right)\left(C_L S_1 + \frac{1}{R_L}\right)e^{S_1 t} - \left(\frac{2}{R_L C_L} + S_1\right)\right. \\
& \left.\times\left(C_L S_2 + \frac{1}{R_L}\right)e^{S_2 t}\right\} + \mu_n C_{OX}\frac{W}{L}\big[0.9(V_{bias} + I_{bias}R_m)i_{bb}R_m \\
& -0.55 i_{bb}R_m V_{TH}\big]\cos(\omega_{LO} + \omega_{bb})t\left\{\frac{num}{den}\left[\frac{1}{L_{CH}C_L} + (\omega_{LO} + \omega_{bb})^2\right]\right. \\
& \left.\times R_L C_L^2 + \frac{num}{den}\frac{1}{R_L} - 1\right\} + \mu_n C_{OX}\frac{W}{L}\frac{num}{den}\big[0.9(V_{bias} + I_{bias}R_m) \\
& \times i_{bb}R_m - 0.55 i_{bb}R_m V_{TH}\big]\sin(\omega_{LO} + \omega_{bb})t\left\{\frac{C_L}{(\omega_{LO} + \omega_{bb})}\left[\frac{1}{L_{CH}C_L}\right.\right. \\
& \left.\left. + (\omega_{LO} + \omega_{bb})^2\right] - C_L(\omega_{LO} + \omega_{bb})\right\}
\end{aligned}
$$

where

$$\frac{num}{den} = \frac{R_L L_{CH}^2(\omega_{LO} + \omega_{bb})^2}{R_L^2 L_{CH}^2 C_L^2(\omega_{LO} + \omega_{bb})^4 + (2R_L^2 C_L + L_{CH})(\omega_{LO} + \omega_{bb})^2 L_{CH} + R_L^2}$$

Furthermore, when the voltage swing at the gate of transistor M_{PA} equals V_{dd} and the output voltage is smaller than the overdrive voltage, the device is in the triode region and it behaves as a closed switch whose ON resistance, $R_{M_{PA}}$, is given by

$$R_{M_{PA}} = \frac{1}{\mu_n C_{OX}\frac{W}{L}(V_{in} - V_{TH})}$$

Afterwards transition, the current value of the choke inductor, L_{CH}, and the voltage value of the load capacitor, C_L, are preserved. Those values are given by $i_{L_{CH}}$ and V_{outsat}, respectively. Then, conforming time runs and the device still is in the triode region, the equivalent circuit of the PA is like the one depicted in Figure 6.13(d). As can be seen, it is a parallel RLC circuit. If we apply circuit analysis to the network, and taking into account that $i_{L_{CH}}$ and V_{outsat} are the initial values of the circuit, it can be found that the natural response of it when the transistor is in the linear region, V_{outlin}, is

$$
\begin{aligned}
V_{outlin} \quad = \quad & \frac{1}{(S_{22}-S_{11})}\Bigg\{V_{dd}\bigg(\frac{1}{R_L C_L}+\frac{S_{22}}{2}\bigg)+\frac{num}{den}\mu_n C_{OX}\frac{W}{L}\big[0.9(V_{bias}+I_{bias}\times \\
& R_m)i_{bb}R_m - 0.55 i_{bb}R_m V_{TH}\big]\bigg[\frac{R_L}{L_{CH}}+(\omega_{LO}+\omega_{bb})^2 R_L C_L + S_{22}\bigg]\Bigg\}e^{S_{11}t} \\
& +\frac{1}{(S_{22}-S_{11})}\Bigg\{-V_{dd}\bigg(\frac{1}{R_L C_L}+\frac{S_{11}}{2}\bigg)+\frac{num}{den}\mu_n C_{OX}\frac{W}{L}\big[0.9(V_{bias}+ \\
& I_{bias}R_m)i_{bb}R_m - 0.55 i_{bb}R_m V_{TH}\big]\bigg[\frac{R_L}{L_{CH}}+(\omega_{LO}+\omega_{bb})^2 R_L C_L - S_{11}\bigg]\Bigg\}e^{S_{22}t}
\end{aligned} \tag{6.27}
$$

where

$$
S_{11,22} = -\frac{1}{2C_L(R_L\|R_{ON})} \pm \sqrt{\frac{1}{4C_L^2(R_L\|R_{ON})^2}-\frac{1}{L_{CH}C_L}}
$$

Then, the voltage swing at the gate of transistor M_{PA} decreases and at certain moment it occurs that the overdrive voltage is, again, smaller than the output voltage and once more the device is in saturation. However, since the natural response of the circuit has been modified, this time the output voltage of the PA in saturation, V_{outsat}, is expressed as

$$
\begin{aligned}
V_{outsat} \quad = \quad & \frac{e^{S_{11}t}}{(S_{22}-S_{11})}\Bigg\{V_{dd}\bigg(\frac{1}{R_L C_L}+\frac{S_{22}}{2}\bigg)+\frac{num}{den}\mu_n C_{OX}\frac{W}{L}\big[0.9(V_{bias}+I_{bias} \\
& R_m)i_{bb}R_m - 0.55 i_{bb}R_m V_{TH}\big]\bigg[\frac{R_L}{L_{CH}}+(\omega_{LO}+\omega_{bb})^2 R_L C_L + S_{22}\bigg]\Bigg\} + \\
& \frac{e^{S_{22}t}}{(S_{22}-S_{11})}\Bigg\{-V_{dd}\bigg(\frac{1}{R_L C_L}+\frac{S_{11}}{2}\bigg)+\frac{num}{den}\mu_n C_{OX}\frac{W}{L}\big[0.9(V_{bias}+ \\
& I_{bias}R_m)i_{bb}R_m - 0.55 i_{bb}R_m V_{TH}\big]\bigg[\frac{R_L}{L_{CH}}+(\omega_{LO}+\omega_{bb})^2 R_L C_L - S_{11}\bigg]\Bigg\} \\
& +\frac{num}{den}\big[0.9(V_{bias}+I_{bias}R_m)i_{bb}R_m - 0.55 i_{bb}R_m V_{TH}\big]\mu_n C_{OX}\frac{W}{L}\times \\
& \Bigg\{\cos(\omega_{LO}+\omega_{bb})t+\bigg[\frac{R_L C_L}{L_{CH}C_L(\omega_{int})}+R_L C_L(\omega_{LO}+\omega_{bb})\bigg]\sin(\omega_{int})t\Bigg\}
\end{aligned} \tag{6.28}
$$

where $\omega_{int} = \omega_{LO} + \omega_{BB}$.

Conforming the voltage swing at the gate of the transistor M_{PA} continues decreasing, there is moment at which $V_{in} < V_{TH}$, and then the device is turned-off once more.

The whole process of moving from a turned-off state to saturation mode and then to the linear region realized by M_{PA} repeats over and over as long as the PA is working. Thus, is more convenient to express the output voltage, V_{out}, in a more general form for feasibility. Generally speaking, the natural response of the amplifier is of the form

$$V_{outn} = V_1 e^{S_1 t} + V_2 e^{S_2 t} \tag{6.29}$$

where V_1, V_2 vary their values since the initial conditions of the circuit change constantly, and

$$S_{1,2} = \begin{cases} -\dfrac{1}{2R_L C_L} \pm \sqrt{\dfrac{1}{4R_L^2 C_L^2} - \dfrac{1}{L_{CH} C_L}} & M_{PA} \text{ turned-off} \\ -\dfrac{1}{2(R_L \| R_{ON}) C_L} \pm \sqrt{\dfrac{1}{4(R_L \| R_{ON})^2 C_L^2} - \dfrac{1}{L_{CH} C_L}} & M_{PA} \text{ in triode} \end{cases} \tag{6.30}$$

Furthermore, the forced response of the circuit when the transistor is in saturation is given by

$$\begin{aligned} V_{outf} = {} & \frac{R_L L_{CH}^2 (\omega_{LO} + \omega_{bb})^2}{R_L^2 L_{CH}^2 C_L^2 (\omega_{LO} + \omega_{bb})^4 + (2R_L^2 C_L + L_{CH})(\omega_{LO} + \omega_{bb})^2 L_{CH} + R_L^2} \\ & \times \left[0.9(V_{bias} + I_{bias} R_m) i_{bb} R_m - 0.55 i_{bb} R_m V_{TH}\right] \mu_n C_{OX} \frac{W}{L} \times \\ & \left\{ \frac{R_L C_L}{(\omega_{LO} + \omega_{bb})} \left[\frac{1}{L_{CH} C_L} + (\omega_{LO} + \omega_{bb})^2 \right] \sin(\omega_{LO} + \omega_{bb}) t + \right. \\ & \left. \cos(\omega_{LO} + \omega_{bb}) t \right\} \end{aligned} \tag{6.31}$$

Therefore, the total voltage at the output of the amplifier considering just the frequency term of interest $\omega_{LO} + \omega_{bb}$ can be written as

$$
\begin{aligned}
V_{out} \;=\; & \frac{R_L L_{CH}^2(\omega_{LO}+\omega_{bb})^2}{R_L^2 L_{CH}^2 C_L^2(\omega_{LO}+\omega_{bb})^4+(2R_L^2C_L+L_{CH})(\omega_{LO}+\omega_{bb})^2 L_{CH}+R_L^2} \\
& \times\big[0.9(V_{bias}+I_{bias}R_m)i_{bb}R_m-0.55i_{bb}R_mV_{TH}\big]\mu_n C_{OX}\frac{W}{L}\times \\
& \left\{\frac{R_LC_L}{(\omega_{LO}+\omega_{bb})}\left[\frac{1}{L_{CH}C_L}+(\omega_{LO}+\omega_{bb})^2\right]\sin(\omega_{LO}+\omega_{bb})t+\right. \\
& \left.\cos(\omega_{LO}+\omega_{bb})t\right\}+V_1e^{S_1t}+V_2e^{S_2t}
\end{aligned}
\tag{6.32}
$$

and consequently, the power at the output produced by this voltage signal is

$$
\begin{aligned}
P_{out} \;=\; & \frac{1}{R_L}\left\{\frac{\big[0.9(V_{bias}+I_{bias}R_m)i_{bb}R_m-0.55i_{bb}R_mV_{TH}\big]^2}{2}\mu_n^2C_{OX}^2\left(\frac{W}{L}\right)^2\times\right. \\
& \frac{[R_LL_{CH}^2(\omega_{LO}+\omega_{bb})^2]^2}{[R_L^2L_{CH}^2C_L^2(\omega_{LO}+\omega_{bb})^4+(2R_L^2C_L+L_{CH})(\omega_{LO}+\omega_{bb})^2L_{CH}+R_L^2]^2} \\
& \left.\times\left[\frac{(R_LC_L)^2}{(\omega_{LO}+\omega_{bb})^2}\left(\frac{1}{L_{CH}C_L}+(\omega_{LO}+\omega_{bb})^2\right)^2+1\right]+V_1^2+V_2^2\right\}
\end{aligned}
\tag{6.33}
$$

It is possible to assess the power gain, A_P, of the PA if we accomplish the ratio between the output power in (6.33) and the power delivered by the mixer at the input of the amplification stage, given by (6.18). However, it is important to recall that the output power expressed by (6.33) involves only the frequency term $\omega_{LO}+\omega_{bb}$, and thus, the power produced at different harmonics and IM products is not considered. Nevertheless, if we carry out this ratio, an estimation about the power added efficiency, PAE, of the PA can be done by employing (5.14). Figure 6.14 shows the graphic of the PAE attained at both, peak output power and average output power. As can be seen, for a large power back-off (12dB) the PAE does not decrease dramatically as it used to with the use of the power up-converter discussed in the previous chapter. In fact, the PAE is closer to the η_D. This makes sense since the output power in (6.47) is in direct proportion with the quadratic value of the aspect ratio of the transistor M_{PA}, (W/L), meanwhile the

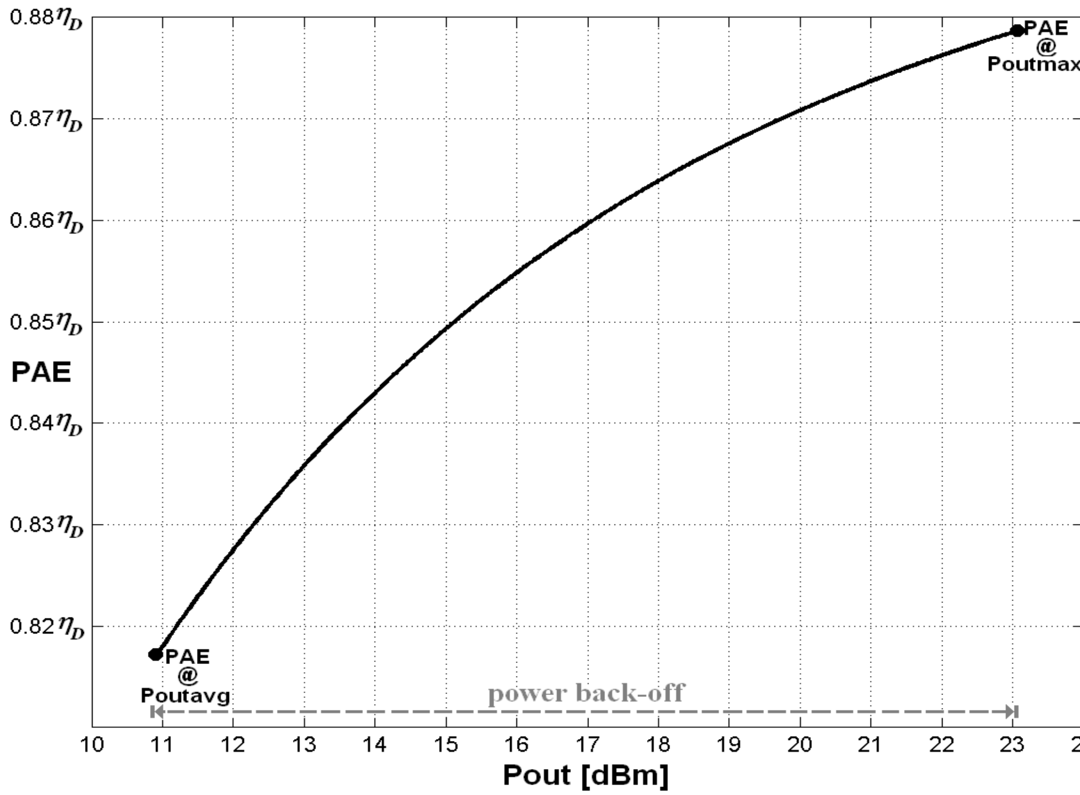

Figure 6.14: *PAE of the PA in function of the η_D at both, peak output power and average output power.*

power delivered by the mixer to the PA exhibits a direct linear proportion with the size of the width, W, of M_{PA} (the load capacitance in (6.18), C_L, depends on the size of W, among other parameters). Thus, the power gain of the PA does not change in a considerable proportion at large output power back-off. In both expressions, (6.18) and (6.33), there is a quadratic dependence of the power with respect to the DC current and voltage of the BB, I_{bias} and V_{bias}, respectively, and the peak current of the BB, i_{bb}. In order to compute the results displayed in Figure 6.14, the same values of I_{bias}, V_{bias} and i_{bb} were considerer in (6.18) and (6.33), with an LO frequency of 2.69GHz and a load resistance, R_L, of 5Ω.

It can be appreciated in Figure 6.14 that the PAE is depicted in terms of the drain efficiency of the PA, η_D, just like expressed in equation (5.14). Considering that the drain efficiency of the amplifier corresponds to that of a class C, and without taking into account any loss mechanism in the circuit [18], then the PAE of the PA may range from 40% at average output power to 80% at peak output power with a conduction angle of $\pi/3$, which corresponds to one third duty cycle of the driving signal from the mixer. Therefore, the efficiency of the proposed PA is preserved at large power back-off. This is a desirable characteristic in systems where the circuits are biased with batteries. However, the estimation of a $40-80\%$ PAE is rather an optimistic value. The loss mechanisms present in the circuit were not considered in the estimation accomplished and these will play their role putting the PAE at a lower amount. Nevertheless, the interesting result in the performance of the proposed PA lies on its capability to keep the A_P almost unmovable at a large power back-off which yields in a more efficient behavior.

6.5 The Linearity of the Overall System

Figure 6.15 shows the block diagram of the proposed multipath polyphase PA with improved efficiency. As can be seen, it is based on the multipath polyphase principle depicted in Figure 4.1. Nevertheless, the new system accomplishes the phase shifts at the predriver stage and the final block corresponds to the mixed mode class C PA. Since the phase shift is now performed at the time variant mixer and then this up-converted signal is amplified by the nonlinear PA, the harmonics and IM products at the output of each path are different from those expressed in (4.2). Therefore, in order to know the new spectrum at the output of the proposed architecture, we must first determine the distortion components of each path. According to (6.11), the output of the predriver stage at each ith path, P_i, is given by

$$\begin{aligned} P_i &= \sum_{k=0}^{\infty} \big\{ a_k \cos(k\omega_{LO}t - k\varphi) + b_k \cos[(k\omega_{LO} + \omega_{bb})t - (k-1)\varphi] \\ &\quad + b_{k+1} \cos[((k+1)\omega_{LO} - \omega_{bb})t + k\varphi] \big\} \end{aligned} \tag{6.34}$$

where a_k, b_k and b_{k+1} are the coefficients of the different frequency components at the output of the mixer; φ is the phase shift at the BB meanwhile $-\varphi$ is the phase shift at the LO; ω_{LO} and ω_{bb} are the LO and BB frequencies, respectively.

On the other hand, based on the distortion components showed in Table 6.2, which are produced by the PA when it is in saturation mode, we can derive an expression for the output of the mixed mode class C PA at each ith path, Y_i:

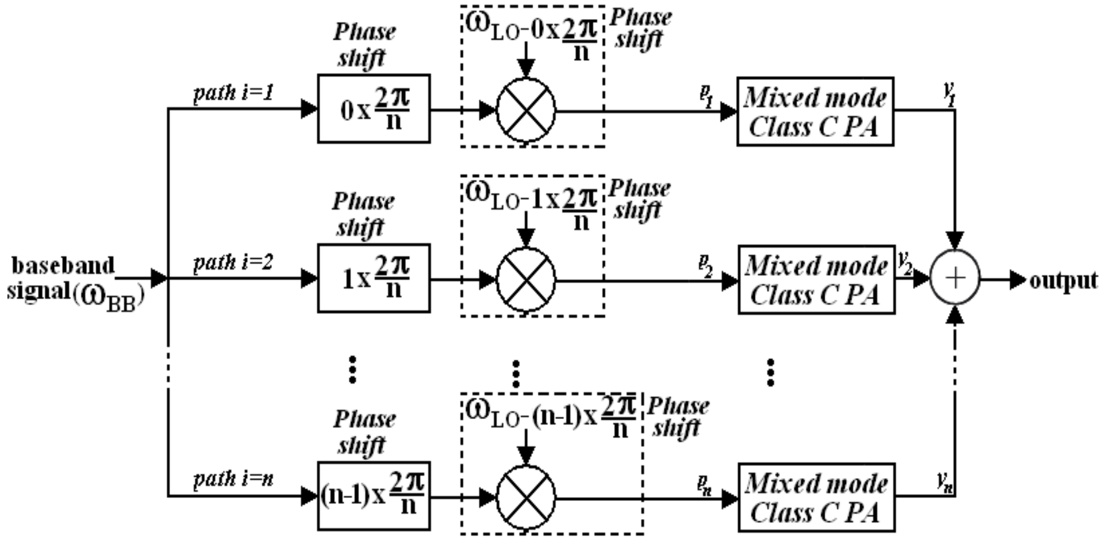

Figure 6.15: *The proposed multipath polyphase PA with improved efficiency.*

$$\begin{aligned} Y_i \;=\; & \sum_{k=0}^{\infty} \{ c_k \cos(k\omega_{LO}t - k\varphi) + d_k \cos[(k\omega_{LO} + \omega_{bb})t - (k-1)\varphi] \\ & + d_{k+1} \cos[((k+1)\omega_{LO} - \omega_{bb})t + k\varphi] + e_k cos[(k\omega_{LO} + 2\omega_{bb})t \\ & -(k-1)\varphi] + e_{k+1} \cos[((k+1)\omega_{LO} - \omega_{bb})t + k\varphi] \} \end{aligned} \tag{6.35}$$

where c_k, d_k, d_{k+1}, e_k and e_{k+1} are the coefficients of the different frequency components at the output of the PA; again, φ and $-\varphi$ are the phase shift at the BB and LO, respectively; ω_{LO} is the LO frequency meanwhile ω_{bb} is the BB frequency.

Let $\varphi = i2\pi/n$, where i is the ith path and n is the total number of paths. By adding all the signals from the PAs, we find that the output of the system is

$$\begin{aligned} output \;=\; & \sum_{i=0}^{n-1} \Big\{ \sum_{k=0}^{\infty} \Big\{ c_k \cos\big(k\omega_{LO}t - ki\frac{2\pi}{n}\big) + d_k \cos\big[(k\omega_{LO} + \omega_{bb})t \\ & -(k-1)i\frac{2\pi}{n}\big] + d_{k+1} \cos\big[((k+1)\omega_{LO} - \omega_{bb})t + ki\frac{2\pi}{n}\big] \\ & + e_k cos\big[(k\omega_{LO} + 2\omega_{bb})t - (k-1)i\frac{2\pi}{n}\big] + e_{k+1} \cos\big[((k+1) \\ & (\omega_{LO} - \omega_{bb})t + ki\frac{2\pi}{n}\big]\Big\}\Big\} \end{aligned} \tag{6.36}$$

Table 6.3: *Some of the frequency components cancelled in the proposed multipath polyphase PA in function of the number of paths employed.*

Number of paths	**Frequency Components Cancelled**
2	$2\omega_{LO}, 3\omega_{LO} \pm 2\omega_{bb}, 3\omega_{LO} \pm \omega_{bb}, 6\omega_{LO}, 7\omega_{LO} \pm 2\omega_{bb}, 7\omega_{LO} \pm \omega_{bb}$ $10\omega_{LO}, 11\omega_{LO} \pm 2\omega_{bb}, 11\omega_{LO} \pm \omega_{bb}, 14\omega_{LO}, 15\omega_{LO} \pm 2\omega_{bb}, 15\omega_{LO} \pm \omega_{bb}$ $18\omega_{LO}, 19\omega_{LO} \pm 2\omega_{bb}, 19\omega_{LO} \pm \omega_{bb}, 22\omega_{LO}, 23\omega_{LO} \pm 2\omega_{bb}, 23\omega_{LO} \pm \omega_{bb}$
3	$2\omega_{LO}, 3\omega_{LO} \pm 2\omega_{bb}, 3\omega_{LO} \pm \omega_{bb}, 4\omega_{LO}, 5\omega_{LO} \pm 2\omega_{bb}, 5\omega_{LO} \pm \omega_{bb}$ $8\omega_{LO}, 9\omega_{LO} \pm 2\omega_{bb}, 9\omega_{LO} \pm \omega_{bb}, 10\omega_{LO}, 11\omega_{LO} \pm 2\omega_{bb}, 11\omega_{LO} \pm \omega_{bb}$ $14\omega_{LO}, 15\omega_{LO} \pm 2\omega_{bb}, 15\omega_{LO} \pm \omega_{bb}, 16\omega_{LO}, 17\omega_{LO} \pm 2\omega_{bb}, 17\omega_{LO} \pm \omega_{bb}$ $20\omega_{LO}, 21\omega_{LO} \pm 2\omega_{bb}, 21\omega_{LO} \pm \omega_{bb}, 22\omega_{LO}, 23\omega_{LO} \pm 2\omega_{bb}, 23\omega_{LO} \pm \omega_{bb}$
4	$2\omega_{LO}, 3\omega_{LO} \pm 2\omega_{bb}, 3\omega_{LO} \pm \omega_{bb}, 4\omega_{LO}, 5\omega_{LO} \pm 2\omega_{bb}, 5\omega_{LO} \pm \omega_{bb}$ $6\omega_{LO}, 7\omega_{LO} \pm 2\omega_{bb}, 7\omega_{LO} \pm \omega_{bb}, 10\omega_{LO}, 11\omega_{LO} \pm 2\omega_{bb}, 11\omega_{LO} \pm \omega_{bb}$ $12\omega_{LO}, 13\omega_{LO} \pm 2\omega_{bb}, 13\omega_{LO} \pm \omega_{bb}, 14\omega_{LO}, 15\omega_{LO} \pm 2\omega_{bb}, 15\omega_{LO} \pm \omega_{bb}$ $18\omega_{LO}, 19\omega_{LO} \pm 2\omega_{bb}, 19\omega_{LO} \pm \omega_{bb}, 20\omega_{LO}, 21\omega_{LO} \pm 2\omega_{bb}, 21\omega_{LO} \pm \omega_{bb}$ $22\omega_{LO}, 23\omega_{LO} \pm 2\omega_{bb}, 23\omega_{LO} \pm \omega_{bb}$
5	$2\omega_{LO}, 3\omega_{LO} \pm 2\omega_{bb}, 3\omega_{LO} \pm \omega_{bb}, 4\omega_{LO}, 5\omega_{LO} \pm 2\omega_{bb}, 5\omega_{LO} \pm \omega_{bb}$ $6\omega_{LO}, 7\omega_{LO} \pm 2\omega_{bb}, 7\omega_{LO} \pm \omega_{bb}, 8\omega_{LO}, 9\omega_{LO} \pm 2\omega_{bb}, 9\omega_{LO} \pm \omega_{bb}$ $12\omega_{LO}, 13\omega_{LO} \pm 2\omega_{bb}, 13\omega_{LO} \pm \omega_{bb}, 14\omega_{LO}, 15\omega_{LO} \pm 2\omega_{bb}, 15\omega_{LO} \pm \omega_{bb}$ $16\omega_{LO}, 17\omega_{LO} \pm 2\omega_{bb}, 17\omega_{LO} \pm \omega_{bb}, 18\omega_{LO}, 19\omega_{LO} \pm 2\omega_{bb}, 19\omega_{LO} \pm \omega_{bb}$ $22\omega_{LO}, 23\omega_{LO} \pm 2\omega_{bb}, 23\omega_{LO} \pm \omega_{bb}, 24\omega_{LO}$
6	$2\omega_{LO}, 3\omega_{LO} \pm 2\omega_{bb}, 3\omega_{LO} \pm \omega_{bb}, 4\omega_{LO}, 5\omega_{LO} \pm 2\omega_{bb}, 5\omega_{LO} \pm \omega_{bb}$ $6\omega_{LO}, 7\omega_{LO} \pm 2\omega_{bb}, 7\omega_{LO} \pm \omega_{bb}, 8\omega_{LO}, 9\omega_{LO} \pm 2\omega_{bb}, 9\omega_{LO} \pm \omega_{bb}$ $10\omega_{LO}, 11\omega_{LO} \pm 2\omega_{bb}, 11\omega_{LO} \pm \omega_{bb}, 14\omega_{LO}, 15\omega_{LO} \pm 2\omega_{bb}, 15\omega_{LO} \pm \omega_{bb}$ $16\omega_{LO}, 17\omega_{LO} \pm 2\omega_{bb}, 17\omega_{LO} \pm \omega_{bb}, 18\omega_{LO}, 19\omega_{LO} \pm 2\omega_{bb}, 19\omega_{LO} \pm \omega_{bb}$ $20\omega_{LO}, 21\omega_{LO} \pm 2\omega_{bb}, 21\omega_{LO} \pm \omega_{bb}, 22\omega_{LO}, 23\omega_{LO} \pm 2\omega_{bb}, 23\omega_{LO} \pm \omega_{bb}$
7	$2\omega_{LO}, 3\omega_{LO} \pm 2\omega_{bb}, 3\omega_{LO} \pm \omega_{bb}, 4\omega_{LO}, 5\omega_{LO} \pm 2\omega_{bb}, 5\omega_{LO} \pm \omega_{bb}$ $6\omega_{LO}, 7\omega_{LO} \pm 2\omega_{bb}, 7\omega_{LO} \pm \omega_{bb}, 8\omega_{LO}, 9\omega_{LO} \pm 2\omega_{bb}, 9\omega_{LO} \pm \omega_{bb}$ $10\omega_{LO}, 11\omega_{LO} \pm 2\omega_{bb}, 11\omega_{LO} \pm \omega_{bb}, 12\omega_{LO}, 13\omega_{LO} \pm 2\omega_{bb}, 13\omega_{LO} \pm \omega_{bb}$ $16\omega_{LO}, 17\omega_{LO} \pm 2\omega_{bb}, 17\omega_{LO} \pm \omega_{bb}, 18\omega_{LO}, 19\omega_{LO} \pm 2\omega_{bb}, 19\omega_{LO} \pm \omega_{bb}$ $20\omega_{LO}, 21\omega_{LO} \pm 2\omega_{bb}, 21\omega_{LO} \pm \omega_{bb}, 22\omega_{LO}, 23\omega_{LO} \pm 2\omega_{bb}, 23\omega_{LO} \pm \omega_{bb}, 24\omega_{LO}$

Table 6.4: *Some of the frequency components cancelled in the proposed multipath polyphase PA in function of the number of paths employed (continued).*

Number of paths	**Frequency Components Cancelled**
8	$2\omega_{LO}, 3\omega_{LO} \pm 2\omega_{bb}, 3\omega_{LO} \pm \omega_{bb}, 4\omega_{LO}, 5\omega_{LO} \pm 2\omega_{bb}, 5\omega_{LO} \pm \omega_{bb}$
	$6\omega_{LO}, 7\omega_{LO} \pm 2\omega_{bb}, 7\omega_{LO} \pm \omega_{bb}, 8\omega_{LO}, 9\omega_{LO} \pm 2\omega_{bb}, 9\omega_{LO} \pm \omega_{bb}$
	$10\omega_{LO}, 11\omega_{LO} \pm 2\omega_{bb}, 11\omega_{LO} \pm \omega_{bb}, 12\omega_{LO}, 13\omega_{LO} \pm 2\omega_{bb}, 13\omega_{LO} \pm \omega_{bb}$
	$14\omega_{LO}, 15\omega_{LO} \pm 2\omega_{bb}, 15\omega_{LO} \pm \omega_{bb}, 18\omega_{LO}, 19\omega_{LO} \pm 2\omega_{bb}, 19\omega_{LO} \pm \omega_{bb}$
	$20\omega_{LO}, 21\omega_{LO} \pm 2\omega_{bb}, 21\omega_{LO} \pm \omega_{bb}, 22\omega_{LO}, 23\omega_{LO} \pm 2\omega_{bb}, 23\omega_{LO} \pm \omega_{bb}, 24\omega_{LO}$
9	$2\omega_{LO}, 3\omega_{LO} \pm 2\omega_{bb}, 3\omega_{LO} \pm \omega_{bb}, 4\omega_{LO}, 5\omega_{LO} \pm 2\omega_{bb}, 5\omega_{LO} \pm \omega_{bb}$
	$6\omega_{LO}, 7\omega_{LO} \pm 2\omega_{bb}, 7\omega_{LO} \pm \omega_{bb}, 8\omega_{LO}, 9\omega_{LO} \pm 2\omega_{bb}, 9\omega_{LO} \pm \omega_{bb}$
	$10\omega_{LO}, 11\omega_{LO} \pm 2\omega_{bb}, 11\omega_{LO} \pm \omega_{bb}, 12\omega_{LO}, 13\omega_{LO} \pm 2\omega_{bb}, 13\omega_{LO} \pm \omega_{bb}$
	$14\omega_{LO}, 15\omega_{LO} \pm 2\omega_{bb}, 15\omega_{LO} \pm \omega_{bb}, 16\omega_{LO}, 17\omega_{LO} \pm 2\omega_{bb}, 17\omega_{LO} \pm \omega_{bb}$
	$20\omega_{LO}, 21\omega_{LO} \pm 2\omega_{bb}, 21\omega_{LO} \pm \omega_{bb}, 22\omega_{LO}, 23\omega_{LO} \pm 2\omega_{bb}, 23\omega_{LO} \pm \omega_{bb}, 24\omega_{LO}$
10	$2\omega_{LO}, 3\omega_{LO} \pm 2\omega_{bb}, 3\omega_{LO} \pm \omega_{bb}, 4\omega_{LO}, 5\omega_{LO} \pm 2\omega_{bb}, 5\omega_{LO} \pm \omega_{bb}$
	$6\omega_{LO}, 7\omega_{LO} \pm 2\omega_{bb}, 7\omega_{LO} \pm \omega_{bb}, 8\omega_{LO}, 9\omega_{LO} \pm 2\omega_{bb}, 9\omega_{LO} \pm \omega_{bb}$
	$10\omega_{LO}, 11\omega_{LO} \pm 2\omega_{bb}, 11\omega_{LO} \pm \omega_{bb}, 12\omega_{LO}, 13\omega_{LO} \pm 2\omega_{bb}, 13\omega_{LO} \pm \omega_{bb}$
	$14\omega_{LO}, 15\omega_{LO} \pm 2\omega_{bb}, 15\omega_{LO} \pm \omega_{bb}, 16\omega_{LO}, 17\omega_{LO} \pm 2\omega_{bb}, 17\omega_{LO} \pm \omega_{bb}$
	$18\omega_{LO}, 19\omega_{LO} \pm 2\omega_{bb}, 19\omega_{LO} \pm \omega_{bb}, 22\omega_{LO}, 23\omega_{LO} \pm 2\omega_{bb}, 23\omega_{LO} \pm \omega_{bb}, 24\omega_{LO}$

According to (6.36), there will be some cancelled distortion components in function of the number of paths employed in the system. Tables 6.3 and 6.4 summarize some of those frequency components for a number of paths ranging from 2 to 10. If it is desired to suppress a larger number of high order harmonics and IM products, it is possible to use a differential mode approach. By doing this, the even frequency components which are preserved in the single mode architecture will be erased.

It can be noticed from the results showed in tables 6.3 and 6.4 that the carrier, ω_{LO}, and the lower side band, $\omega_{LO} - \omega_{bb}$, are not cancelled by the system. Since those components are close to the frequency of interest, $\omega_{LO} + \omega_{bb}$, it may be necessary to use a bandpass filter at the output of the system to suppress to some extent such components. Thus, the separation between ω_{LO} and ω_{bb} must be chosen taking into account this fact in order to relax the filter requirements.

The price we pay by employing a filter at the output of the system is a decrement in the efficiency due to the losses in the filter. Thus, a trade-off between linearity and efficiency must be done if the new multipath polyphase PA is adopted.

6.6 Conclusions

The synthesis of a new multipath polyphase power amplifier with improved efficiency have been introduced. Since the key factors for power saving in the PA lie on its power gain and the conduction angle at which the amplifier is driven, then the allocation of the up-converter at the amplification stage, as it was proposed originally, has been changed. Instead, the up-converter is now allocated behind the PA as a predriver stage whose functions are: to modify the conduction angle at which the PA is driven and, at the same time, to regulate the power it delivers to the amplifier. The use of a CMOS inverter gate with the inclusion of a current mirror has been proved to be useful as a time variant mixer at high frequency capable of regulating its output power and the duty cycle of its output signal, i.e. the conduction angle of the signal which drives the PA. By doing this, the amplification stage becomes now a mixed mode class C PA whose PAE is high at both, peak output power and average output power even in the presence of a large power back-off. The suppression of many distortion components in function of the number of paths used still is preserved in the new multipath polyphase architecture. However, the carrier, ω_{LO}, as well as the lower side band, $\omega_{LO} - \omega_{bb}$, are not cancelled and therefore the inclusion of a bandpass filter at the output of the system to suppress to some extent such components may be necessary depending on the linearity requirements of the wireless technology where the technique is going to be applied. If the use of a bandpass filter is necessary, then the separation between ω_{LO} and ω_{bb} must be chosen taking into account this fact in order to relax the demands of the filter. The price paid by employing a filter is reduction in the efficiency due to the loss mechanisms present on the filter. Thus, a trade-off between linearity and efficiency must be done if the new multipath polyphase PA is adopted.

Chapter 7

Linear and Efficient CMOS Power Amplifier for Mobile WiMAX

7.1 Introduction

The previous chapters describe in detail the multipath polyphase technique and how by means of this approach the harmonics and intermodulation (IM) products produced by a non-linear Power Amplifier (PA) can be suppressed. Moreover, the synthesis of a new multipath polyphase PA with improved efficiency have been introduced. Thus, linearity is achieved without dismissing efficiency. Since the goal is to build such PA in CMOS technology for mobile WiMAX transmitters, then it is necessary to establish a methodology to design the new power amplification system in such technology.

This chapter covers the design of the complete multipath polyphase PA with improved efficiency in CMOS technology. First, a review of the specifications for mobile WiMAX will be discussed followed by the design procedure.

7.2 Power Amplifier Specification

In this work, a mixed mode class C PA with multiple paths and phases is intended to satisfy the requirements of the IEEE802.16e-2005 standard for mobile WiMAX. As stated earlier in chapter one, the peak output power is 23 dBm ($\approx 200mW$) at the antenna, and a large output power back-off (or peak to average power ratio -PAPR) of 12dB is present in the system being 11dBm ($\approx 12.6mW$) the average output power. Hence, both of those extreme values must be delivered by the PA with a limit on the amount of distortion allowed in the adjacent bands. That limit is settled by the adjacent channel power ratio (ACPR), which has a minimum value of value of 44dB. On the other hand, the transmit band is between 2.496 and 2.69GHz, with channel bandwidths of 5 and 10MHz in south, central, and North America, including the United States. Even though efficiency is not specified by the standard, it is also an important issue. It must be taken into account that mobile WiMAX is intended for portable terminals. Typically, such type of terminals are biased with batteries and, in that case, long duration working times are preferable. Therefore, the more efficient the PA is, the more adequate use of the energy it exhibits.

7.3 Circuit Design

Before starting with the design of the full output stage, the inclusion of an output impedance transformation network must be considered. This network will present the optimum resistance, R_{OPT}, seen by the PA by transforming the real load impedance from the antenna to the adequate resistance value for the amplifier, which is limited by the available voltage swing in the circuit, $V_{outpeak}$, to

$$R_{OPT} = \frac{V_{outpeak}^2}{2P_{outpeak}} \tag{7.1}$$

Where $P_{outpeak}$ is the peak output power provided by the PA. It is important to consider the losses introduced by the matching network and the choke inductors from the amplifier. It is possible than around the 40% of the output swing would be lost before achieving the antenna [42]. Thus, a larger peak output power than that imposed by the standard must be taking into account.

The matching network is typically compound by the combination of some passive components interconnected in a given form. A simple output network which has been successfully employed in the implementation of a Class C PA is shown in Figure 7.1 [42]. As can be seen, it consists of a step-down network with a parallel LC tank formed by the drain-bulk junction capacitor of the transistor

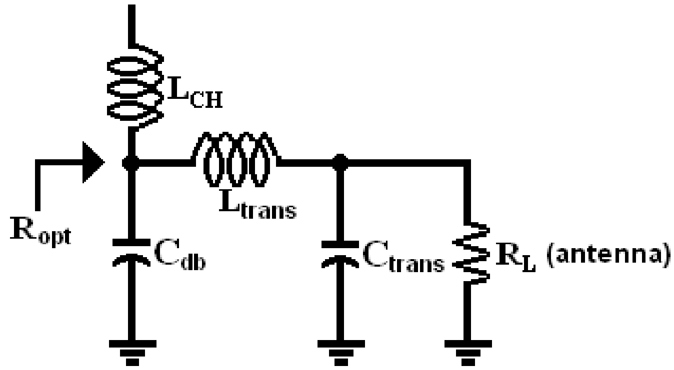

Figure 7.1: *Down-step network for matching the antenna with the PA.*

from the PA, C_{db}, and the choke inductor, L_{CH}, of the amplifier. On the other hand, the impedance transformation network is composite by capacitor C_{Trans} and inductor L_{Trans}. Finally, R_L is the resistive value of the load, which in this case belongs to the antenna. Since the impedance of the antenna (whose reactance equals zero typically) and R_{OPT} are known, the values of L_{Trans} and C_{Trans} can be determined easily from the system of equations obtained when making R_{OPT} equal to the real part of the step-down network and the imaginary part equal to zero.

By inspection of expression (7.1), we realize that the output power is proportional to the voltage swing available at the output of the amplifier. Therefore, by designing the amplifier in a differential mode, the voltage swing usable is twice the voltage swing present in the single-ended case. Moreover, the differential topology in the design of amplifiers prevails for good reasons: inasmuch as it is ideally immune to common mode signals and interference as well as it cancels the even order harmonics components at the output, it offers an attractive solution. However, when designing PAs, the true-differential pair is not appropriate because it limits the linearity performance under large input signal [14]. An alternative is to use a pseudo-differential pair as shown in Figure 7.2, where each device has its source grounded. Some benefits which are achieved by using a pseudo-differential pair in the design of a PA include [14]: the fundamental frequency components as well as the odd-order harmonics of the current from the two devices will be equal in amplitude and opposite in phase, this in turn creates a low-loss on-chip AC-ground at the common source node and the supply node, which significantly minimizes

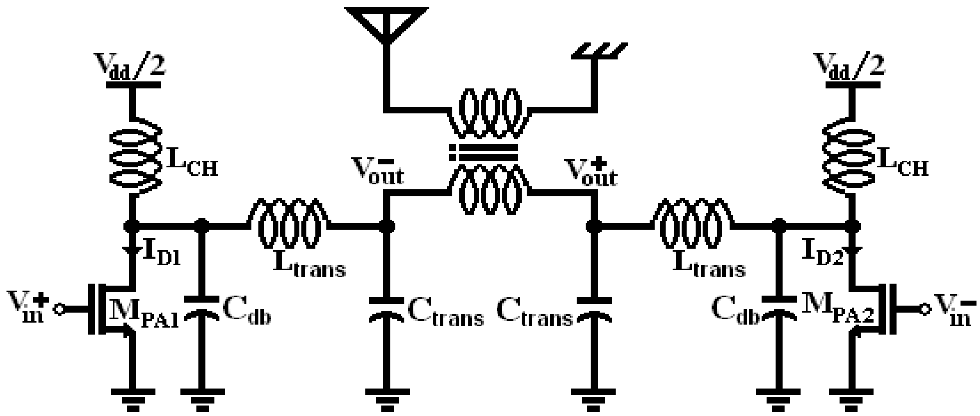

Figure 7.2: *Pseudo-differential PA with matching network.*

the impact of package parasitics on the performance of the amplifier; under typical conditions, the output is taken differentially so that even-order harmonics are suppressed. Hence, this relaxes the filtering requirements at the output to meet stringent spurious tone emission specifications; in addition, signals injected into the substrate are even order harmonics, therefore, the impact on the performance of other circuit blocks that are on the same chip is substantially reduced. Nevertheless, the most important benefit, in the context of the PA design, is doubling the voltage swing at the output. In fact, a pseudo-differential amplifier is equivalent to a 2-way power combined amplifier.

We now proceed to size the transistors from the pseudo-differential PA. For this purpose we use expression (6.33) from which it can be found that the aspect ratio of the device M_{PA} is expressed as

$$\begin{aligned}\left(\frac{W}{L}\right) &= \frac{1}{\mu_n C_{OX}}\sqrt{\frac{2[P_{outpeak}R_{OPT} - V_1^2 - V_2^2]}{R_{OPT}^2[1+(\omega_{LO}+\omega_{bb})^2 L_{CH}C_{db}]^2 + (\omega_{LO}+\omega_{bb})^2 L_{CH}^2}} \\ &\quad \times\left\{\frac{R_{OPT}^2 L_{CH}^2 C_{db}^2(\omega_{LO}+\omega_{bb})^4 + R_{OPT}^2}{[0.9(V_{bias}+I_{bias}R_m)i_{bb}R_m - 0.55 i_{bb}R_m V_{TH}]R_{OPT}L_{CH}(\omega_{LO}+\omega_{bb})}\right. \\ &\quad \left. + \frac{(2R_{OPT}^2 C_{db} + L_{CH})(\omega_{LO}+\omega_{bb})^2 L_{CH}}{[0.9(V_{bias}+I_{bias}R_m)i_{bb}R_m - 0.55 i_{bb}R_m V_{TH}]R_{OPT}L_{CH}(\omega_{LO}+\omega_{bb})}\right\} \end{aligned} \tag{7.2}$$

Where R_{OPT} is the optimum resistance value seen by the PA and determined previously in equation (7.1); L_{CH} is the inductance of the choke inductor of the amplifier; C_{db} is the drain-bulk capacitor from the transistor M_{PA}; $\omega_{LO}+\omega_{bb}$ is the frequency of interest for transmission; V_{bias} is the voltage employed for biasing the predriver stage; I_{bias} is the DC current from the current source of the predriver stage; R_m is the resistive value of the device which delivers the control current of the mixer; i_{bb} is the peak value of the BB signal; V_{TH} is the threshold voltage of the device; μ_n and C_{OX} are the mobility of the carriers and the oxide capacitance of the MOS transistor, respectively; $P_{outpeak}$ is the peak output power of the PA; finally, V_1 and V_2 are the voltages given by the natural response of the amplifier. As can be seen, both, parameters from the amplifier and the predriver are involved to size the power amplification stage. It is important to remark that expression (6.33) neglects other frequency terms present in the amplifier. Thus, expression (7.2) provides an initial estimate to determine the size of the transistor of the PA. However, the power produced at the frequency of interest is the one which must be strong enough at the antenna and therefore (7.2) is useful.

Since (7.2) determines the size of the device at peak power, the values chosen for I_{bias} and i_{bb} for the case of the mixer are the maximum peak and DC currents flowing through the predriver. Moreover, the size of transistor M_{PA} determines the value of its parasitic capacitances and thus, the magnitude of the load seen by the amplifier, C_L, which is compound by the capacitors related to the gate of the device: C_{GD}, C_{GS} and C_{GB}. These are, in turn proportional to the width of the transistors [33].

Expressions (6.4) and (6.5) are now used to size the inverter from the predriver stage. Figure 7.3 shows the circuit diagram of the power amplification system. Transistors M_N and M_P are the devices from the predriver. The aspect ratio of such elements can be determined by means of

$$\left(\frac{W}{L}\right)_N = \frac{t_{PHL}\mu_n C_{OX}(V_{dd}-V_{THN})^2}{C_L V_{bias}} \tag{7.3}$$

$$\left(\frac{W}{L}\right)_P = \frac{t_{PLH}\mu_p C_{OX}(-V_{bias}-\mid V_{THP}\mid)^2}{C_L V_{bias}} \tag{7.4}$$

Where t_{PHL} and t_{PLH} are the propagation times of the inverter from high-to-low and low-to-high, respectively; μ_p is the mobility of the wholes; V_{THN} and V_{THP} are the threshold voltages from the P and N MOSFETs, respectively; V_{dd} is the bias

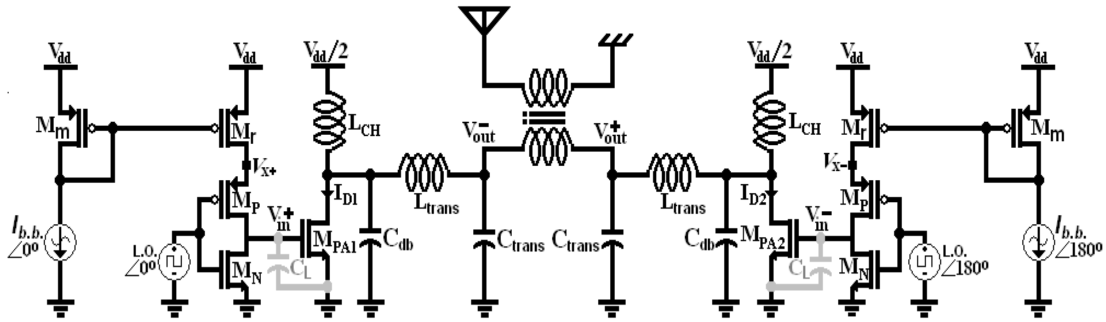

Figure 7.3: *Pseudo-differential power amplification system with predriver stage.*

voltage employed meanwhile V_{bias} is the DC voltage at node V_x in the predriver; finally, C_L is the load capacitance seen by the mixer, which is compound by the self load of the circuit, the capacitance of the interconnection line between the mixer and the PA and the capacitance at the input of the amplifier. A helpful practice is to consider, as an initial procedure just the capacitance at the input of the PA. On the other hand, t_{PHL} and t_{PLH} ca be selected in function of the speed of the square wave at the input of the mixer and the duty cycle desired at the output of this block. The rest of the parameters are known and depend on the CMOS technology that is going to be use to build the system. It is important to recall that, according with the analysis of the predriver in chapter six, it is convenient to size the N transistor larger than the P device in order to obtain similar propagation delays and in this way to control better the duty cycle of the output waveform.

Finally, transistors labelled as M_r and M_m can be sized in function of the current which is intended to be delivered to the mixer. If these devices are planned to remain in saturation for the whole range of operation, which in turn determines the power at the input of the PA and thus the power gain of the amplifier as well as the conduction angle of the signal which drives the PA, then the quadratic model for the drain current can be used to determine the aspect ratio of those transistors.

At this point, we have determined the value of the passive elements in the PA and size all the transistors involved. Now we still have to assess the number of paths and phases in which we are going to divide the system. In order to decide which number of phases is more convenient we must consider two aspects of the system: bandwidth and channelization; the former refers to the entire spectrum in which the users of mobile WiMAX are allowed to communicate (from 2.496GHz to 2.69GHz in America) whereas the latter refers to the bandwidth of one user in the system (5MHz and 10MHz). The IEEE 802.16e-2005 standard establishes the in-band requirements for rejecting out-of-channel interferers (44dBc for 10MHz channel bandwidth and 33dBc for 5MHz channel bandwidth). However, since the wireless environment includes the spectrum allocation of diverse wireless communication technologies ranging from a few Megahertz (HF band)to several tens of Gigahertz (EHF band) [43], it is beneficial to cancel as many harmonics and IM products as possible. Notwithstanding, the more paths and phases we use the more complex the realization of the system becomes. Therefore, a trade-off between complexity and linearity must be established when setting the number of paths and phases in the circuit. According to the results attained related to the linearity of the overall system in the previous chapter, the minimum number of paths and phases that theoretically are able to cancel harmonics and IM products from the UHF to the EHF band is six. This considering that the LO signal is in the middle of the RF spectrum for mobile WiMAX ($\approx 2.6GHz$). On the other hand, in the original analysis of the linearity of the overall system realized previously, we had considered a single-ended amplifier and in this case the lower side band, $\omega_{LO} - \omega_{bb}$, as well as the carrier, ω_{LO}, appear in the spectrum of the output waveform. However, in the case of a pseudo-differential amplifier, it always cancels the image components. Generally speaking, when two groups of signals having either the positive or the negative balanced phase sequences are mixed, then the image signals are cancelled. This means that the frequency components at the output of the pseudo-differential PA will be of the single sideband kind. Moreover, since the opposite balanced phase sequences are multiplied by the predriver stage and then amplified by the PA, the output will contain only the upper-sideband component, $\omega_{LO} + \omega_{bb}$ [44]. Thus, theoretically, there is no need to filter the output signal to achieve the channel linearity requirements.

Figure 7.4 shows the complete circuit diagram of a six phases PA with high linearity and good efficiency for mobile WiMAX in CMOS technology. As can be appreciated, it consists of six differential mixers which drive six pseudo-differential PAs in a six path parallel architecture with a matching network at the output. The

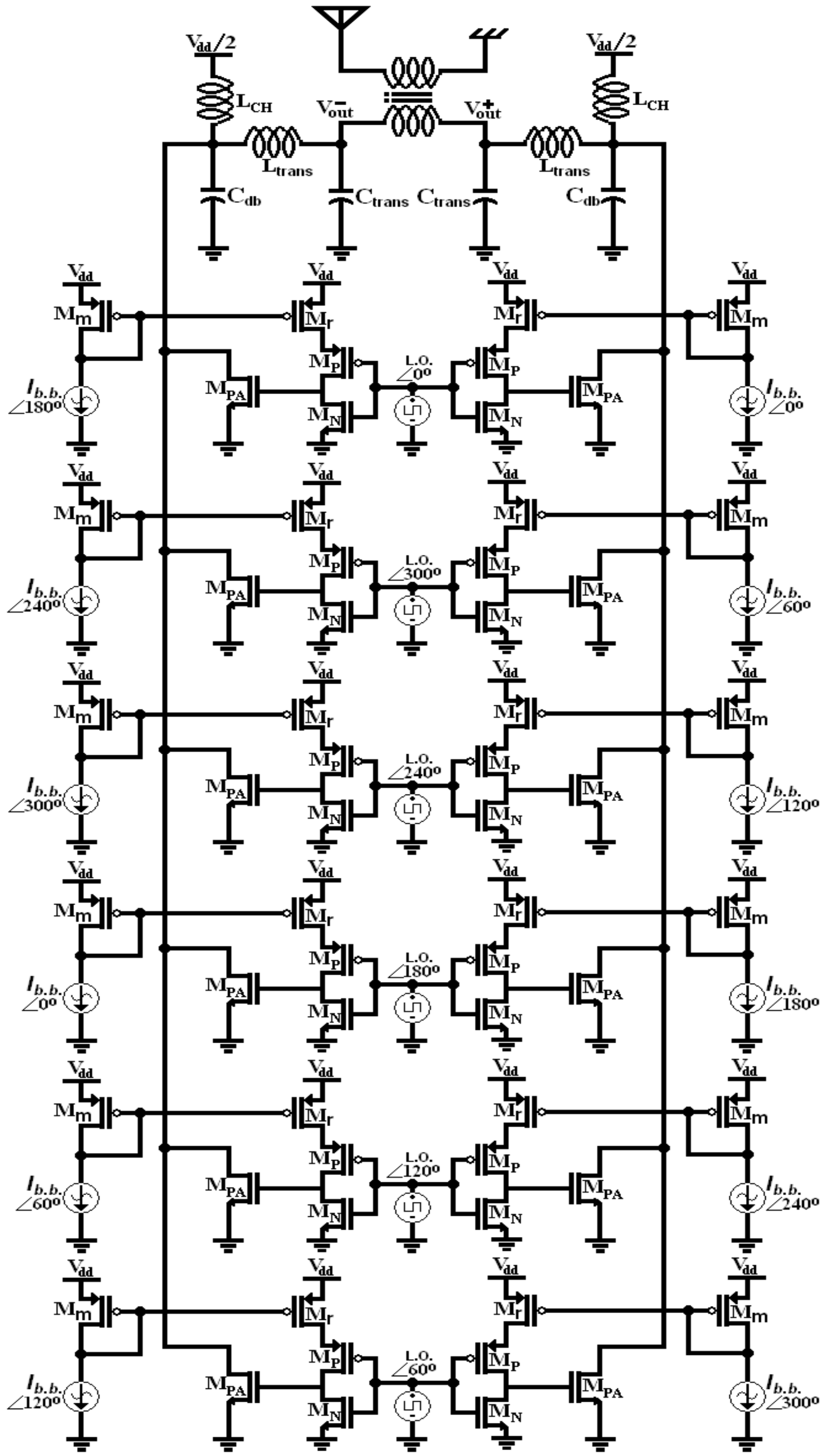

Figure 7.4: *The complete circuit diagram of a six phases PA with high linearity and good efficiency for mobile WiMAX in CMOS technology.*

inclusion of a balun between the differential output and the antenna is necessary to convert the output signal to a single-ended signal. Then, it is necessary to consider the losses introduced by the balun and its corresponding effects in both: the power from the amplifier delivered to the antenna and the efficiency of the overall system.

7.4 Conclusions

The design of a complete pseudo-differential power amplification system for mobile WiMAX in CMOS technology have been presented. The new PA is intended to exhibit a high linearity which considers the cancellation of both: out-of-channel interferers established by the IEEE802.16e-2005 standard and high order harmonics and IM products which appear along the UHF and EHF bands. In addition, the proposed topology is also intended to present a high efficiency since the inclusion of a mixer with the ability of modifying its output power and conduction angle as the predriver stage of the amplifier have been employed. The inclusion of a step-down network to modify the impedance seen by the PA and thus deliver the adequate power to the antenna have been also addressed.

Finally, equations for sizing the transistors involved in the system and important considerations in the design procedure have been also introduced.

Chapter 8

Results

8.1 Introduction

This chapter summarizes both, simulation and measurements that were performed to the power amplification system. The goal of the simulations is to determine if the in-band linearity requirements of mobile WiMAX were satisfied by the proposed system as well as to verify if the cancelled harmonics correspond to those anticipated in the analysis. Moreover, efficiency assessments are also of major interest in order to verify if the system exhibits the energy saving as predicted in the analysis. On the other hand, the measurements reported correspond to the predriver stage. Since the predriver stage is the key building block to enhance the efficiency performance of the amplifier, then it is of interest to evaluate its effectiveness to modulate its output power as well as to modify the conduction angle of the output waveform.

Simulations of the complete power amplification stage were carried out with parameters of the UMC $0.18\mu m$ Mixed Mode and RF CMOS technology meanwhile the design of the predriver stage, which was measured and characterized, was realized in a double poly three metal layers $0.5\mu m$ CMOS technology from MOSIS foundry.

Transistors	**Width (W)** $[\mu m]$	**Length (L)** $[\mu m]$
M_{PA}	972	0.18
M_N	324	0.18
M_P	828	0.18
M_r	720	0.36
M_m	10.08	0.36

Table 8.1: *Dimensions of the transistors of the 6 phases highly linear/highly efficient PA.*

8.2 Simulation Results

Following all the considerations described in the previous chapter, the designed of a six phases PA for mobile WiMAX with an UMC 0.18 Mixed Mode and RF CMOS technology was realized. Table 8.1 shows the dimensions obtained for the transistors of the six phases PA with high linearity and good efficiency of Figure 7.4. For simulation purposes, we employed the maximum voltage supply of 1.8V available for this technology for biasing the predriver stage and a voltage of 0.9V for biasing the power amplification stage. The choke inductors, L_{CH}, occupied in the simulation were considered to exhibit an inductance of 2nH with a series resistor whose resistance is 0.1Ω and a parallel capacitor with a capacitance of 120nF. Those elements with their respective values were taken from the model of a 2mm bond wire used in this particular technology. The value of C_{db} is compound by the contribution of the output capacitances of transistors M_{PA} and the pad capacitance. In order to have a tank circuit that resonates at 2.59GHz, which is the central frequency within the band of mobile WiMAX in America [1],[6], the size of the pad must be chosen such that the total value of C_{db} is 1.89pF.

The simulator used was $CadenceVirtuoso^{®}v5.0.0$. Table 8.2. summarizes the most important characteristics of the system. The RF band for which the circuit was tuned to operate was between 2.496GHz and 2.69GHz with an LO signal running from 2.486GHz to 2.68GHz and a BB signal of 10MHz. The power supply for the predriver stage was of 1.8V and 0.9V for the amplification stage. The total power consumption of the circuit was of approximately 26dBm. The peak output power obtained was 23dBm with a η_D of 83% and a PAE of 61%

RF band	2.496GHz - 2.69GHz
Power supply, V_{dd} (predriver stage)	1.8V
Power supply, $V_{dd}/2$ (power amplification stage)	0.9V
Power consumption	25.8dBm
Maximum output power	23dBm
η_D **@ maximum output power**	83%
η_D **@ 12dB output power back-off**	33%
PAE @ maximum output power	61%
PAE @ 12dB output power back-off	31%
Maximum IM suppression within the channel bandwidth	-60dBc
Minimum IM suppression within the channel bandwidth	-55dBc

Table 8.2: *Simulation results for 6 phases highly linear highly efficient PA.*

meanwhile for 12dB of output power back-off the η_D was 33% and the PAE of 31%. The harmonic suppression around the carrier in a range of $\omega_{LO} \pm 10\omega_{BB}$ presents a minimum value of -55dBc.

Figure 8.1 shows the output spectrum of a single phase PA obtained in the simulation. As can be seen, the output spectrum contains the harmonics and IM products predicted in the analysis when transistor M_{PA} is in saturation (in black) as well as some IM products (in red) that were not predicted in such analysis. It is important to recall the fact that in the analysis of the distortion components produced by the amplifier when the active device is in saturation, the quadratic model of the drain current, I_D, was used. Even though the quadratic model describes the typical current-voltage characteristics of a MOSFET when it is saturation mode, it is not an accurate model specially in submicrometric technologies where physical effects such as the velocity of saturation or the mobility degradation, among others, are avoided [39]. This is the reason of the unpredicted IM products obtained in the simulation. Also in Figure 8.1 a zoom to the neighborhood of

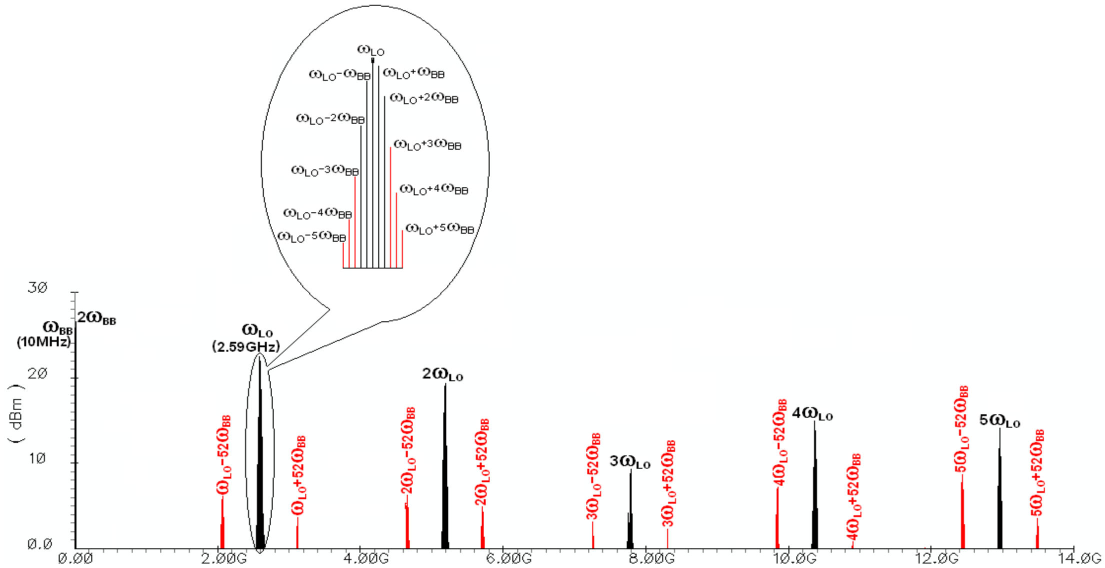

Figure 8.1: *Output spectrum of a single phase PA. Harmonics and IM products predicted are shown in black meanwhile unpredicted IM products are remarked in red.*

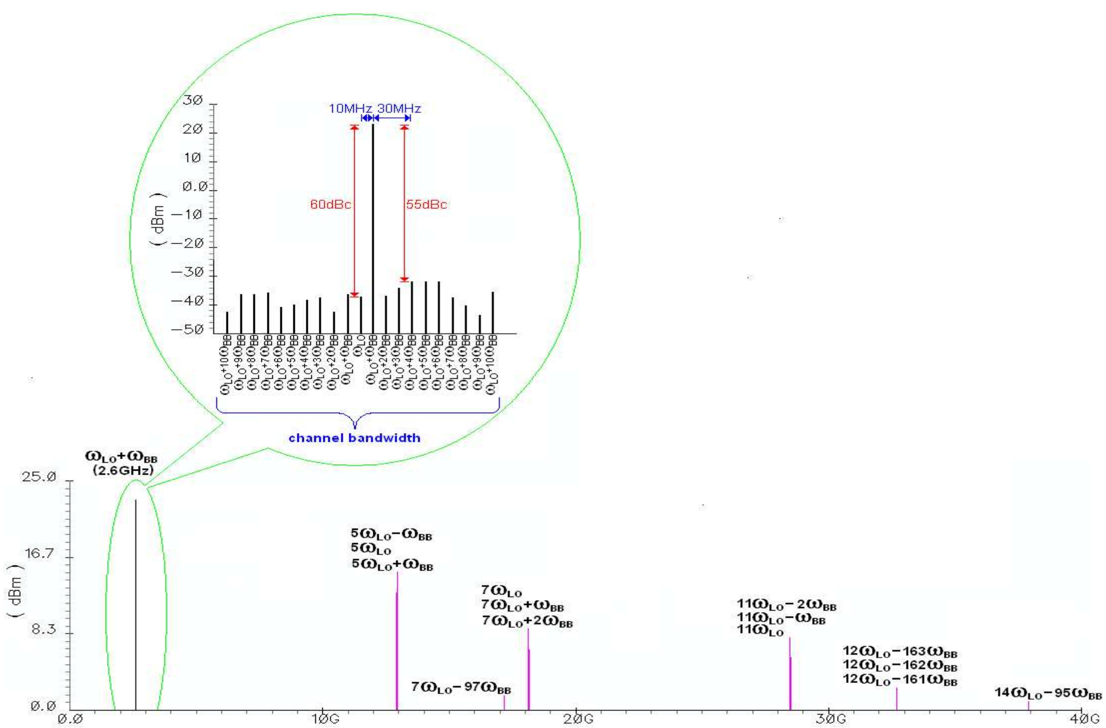

Figure 8.2: *Output spectrum of a 6 phases PA. In purple: harmonics and IM products with poor suppression.*

the fundamental component, ω_{LO}, is depicted. It can be noticed that also the IM products predicted appear (in black) and some other unpredicted IM products are present (in red).

Figure 8.2 shows the output spectrum obtained in simulation of a six phases PA. As can be seen, some uncancelled harmonics and IM products appear (in purple) with certain suppression at a relatively long distant from the frequency of interest, $\omega_{LO} + \omega_{BB}$. According to the analysis of the linearity of the overall system performed in chapter 6, those frequency components must not be there. Again, this is due to the use of the quadratic model of the transistor M_{PA} when it is in saturation. However, the harmonic suppression achieved is good enough for mobile WiMAX. Moreover, the zoom to the neighborhood of the frequency of transmission, $\omega_{LO} + \omega_{BB}$, also in Figure 8.2, shows that the circuit exhibits the adequate in-band linearity demanded for mobile WiMAX, which is 44dB of ACPR for 10MHz channel bandwidth [1], since it achieves an IM suppression around the carrier in a range of $\omega_{LO} \pm 10\omega_{BB}$ with a minimum value of 55dBc. No simulations which include the mismatch effects were performed. Nevertheless, it has been experimentally proved that expression (4.6) establishes a maximum phase error of 2% in order to cancel effectively the closest unwanted IM products around the frequency of interest.

On the other hand, Figure 8.3 shows both, the η_D and the PAE obtained in simulation at full output power range of the circuit. As predicted, the PAE preserves almost the same value of the η_D when a large output power back-off is present. It can be seen that η_D exhibits its larger value at peak output power and conforming the output power back-off becomes larger it decreases. This is due to the fact that the power amplification stage is designed to hand over the higher power demanded by the load and thus its DC consumption is high even when the output power requirements are low. However, because of the ability of the predriver stage of modifying its conduction angle and the power it delivers to the power amplification stage, the efficiency of the amplifier and its power gain are both increased allowing a less drastic drop in the PAE compared to the case of a typical mixer which only performs the up conversion of the BB signal to RF by mixing the BB signal with the LO signal.

These results obtained in the simulation are very important because they

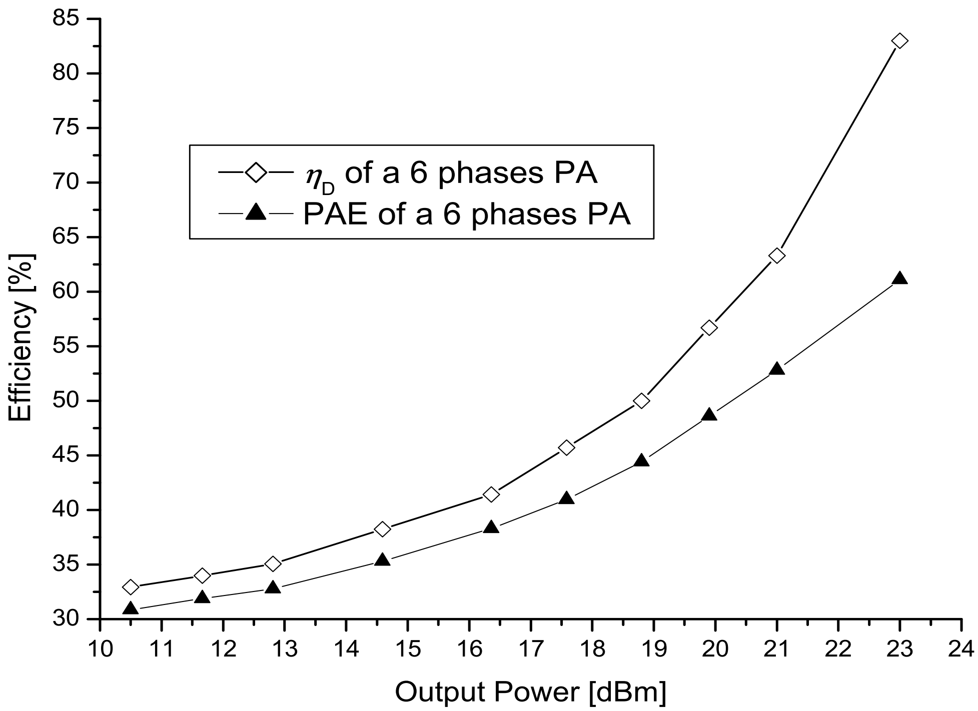

Figure 8.3: *PAE and η_D of a 6 phases PA obtained in simulation at full output power range.*

show that the proposed multipath polyphase PA exhibits both, a high linearity achieving until -60dBc of IM suppression with respect to the frequency of interest $(\omega_{LO} + \omega_{BB})$ within the mobile WiMAX bandwidth, and a high power-added efficiency of 61% at peak output power and 31% with 12dB of output power back-off. It is important to remark that in the simulations performed, the losses introduced by external circuitry such as the balun or the step-down network showed in Figure 7.4 were not considered, and thus, the efficiency attained with a real circuit is expected to be lower. However, it still is a good efficiency considering that the complete system also exhibits a high linearity and, by definition, the higher the linearity is in the PA the lower the efficiency becomes [15].

Since the key building block of the system is the predriver stage, some experimental results which describe its performance are reported in the following section.

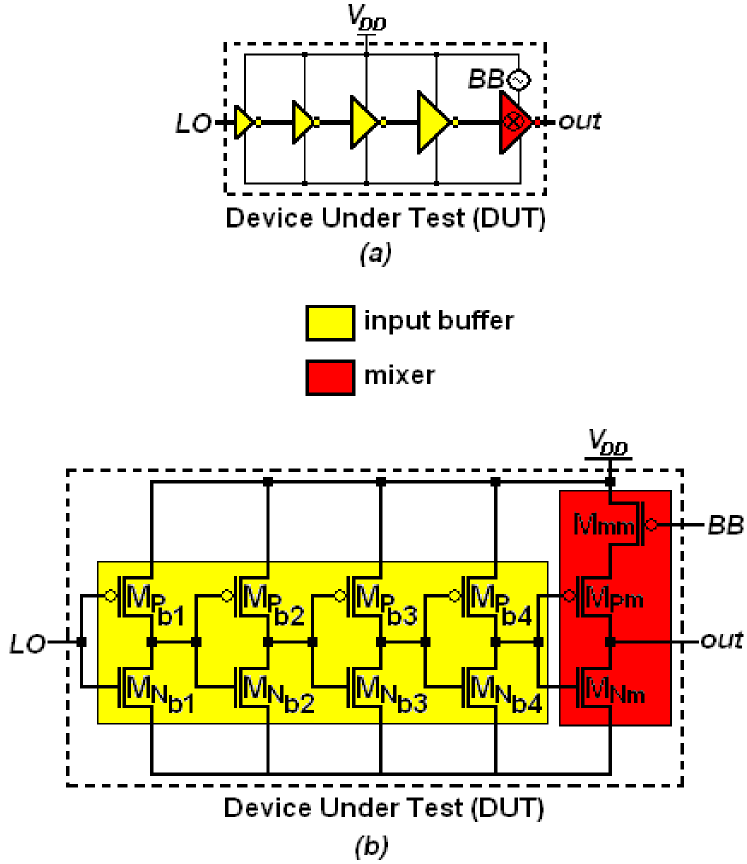

Figure 8.4: *Schematics of the fabricated circuit: (a)Block diagram and (b)Circuit diagram.*

8.3 Experimental Results

A prototype of the predriver stage was design and fabricated in a double poly three metal layers 0.5μm CMOS technology from MOSIS foundry. Figure 8.4 (a) shows the block diagram of the fabricated circuit. As can be seen, it consists of an input buffer which turns the input sinusoidal signal from the LO into a square wave signal with 50% duty cycle followed by the mixer. The circuit diagram with MOS transistors of the fabricated prototype is shown in Figure 8.4 (b). A total of 11 transistors are used. From those, only three belong to the mixer. The sizes of the transistors are presented in table 8.3.

The prototype area is 0.472μm $\times$ 0.148μm including the output pad. The prototype die photo is depicted in Figure 8.5. As can be appreciated, the bias

Transistor	**Width (W)** $[\mu m]$	**Length (L)** $[\mu m]$
M_{Pb1}	19.8	0.6
M_{Nb1}	15.0	0.6
M_{Pb2}	66.0	0.6
M_{Nb2}	30.0	0.6
M_{Pb3}	115.5	0.6
M_{Nb3}	45.0	0.6
M_{Pb4}	264.0	0.6
M_{Nb4}	120.0	0.6
M_{Pm}	180.0	0.6
M_{Nm}	540.0	0.6
M_{mm}	480.0	1.2

Table 8.3: *Dimensions of the transistors of the fabricated prototype.*

input, V_{DD}, the BB input, the LO input and the ground are fed to the bond pads of the chip meanwhile the output node is placed on an inner-pad labelled as 'out'. The die of the prototype device was packaged in a 40-pin Dual in-line package (DIP), which in turn was mounted in a 40-pin Socket soldered to the evaluation test board. Figure 8.6 shows the test board used for evaluating the prototype. The printed board circuit (PCB) was designed and fabricated quite straightforward with an standard FR4 material. Two SMA connectors are used to feed the LO and the BB signals and two groups of poles are used to bias (on the right hand side) and to ground (on the left hand side) the circuit.

The test-setup for evaluating the predriver stage is shown in Figure 8.7. It consists of an Agilent E3640A Power Supply which handed 3.3V for biasing the circuit, a Hewlett Packard 33120A Function Generator who provided the LO signal to the circuit, an Agilent 33250A Function Generator that delivered the BB signal to the prototype, an Agilent Infiniium 54833ADSO Oscilloscope which allowed us to realize the time domain characterization of the system, and a Rohde & Schwarz SMBV100A Spectrum Analyzer for the frequency domain characterization. Since the maximum frequency available at the Hewlett Packard 33120A Function Generator was 80MHz, this was the LO frequency at which the

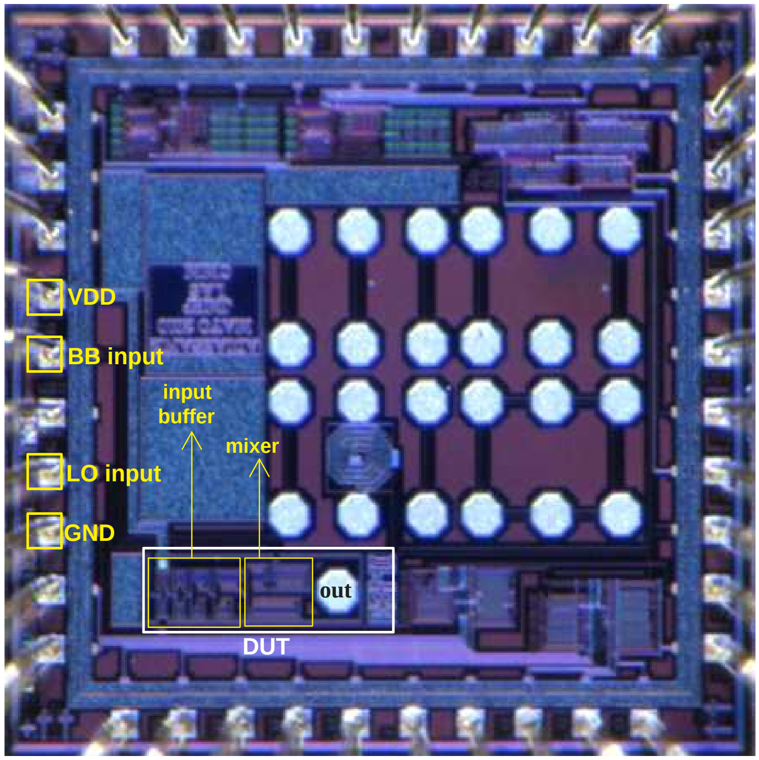

Figure 8.5: *Prototype die photo.*

circuit was tested. The LO signal had a voltage swing of $1.65V_P$ with an offset of $1.65V_{DC}$. The BB signal from the Agilent 33250A Function Generator was set at 1.6MHz (50 times smaller than the LO signal) with an amplitude of $300mV_P$ and a DC offset ranging from 1.0V to 1.4V. The DC offset variation from the BB signal was the control voltage which allowed to change the duty cycle of the output signal and also the power at the output. With the aid of the Agilent Infiniium 54833ADSO Oscilloscope we determined the duty cycle of the output waveform as well as the maximum and minimum voltages achieved at the output. Furthermore, with the Rohde & Schwarz SMBV100A Spectrum Analyzer we were able to determined the spectral content at the output of the circuit. Even though the test-setup was established at a low frequency compared to the RF band of mobile WiMAX, the aim of the characterization was to determine if the behavior of the predriver stage followed the course anticipated in the synthesis.

It is important to mention that since the output of the prototype was taken from an inner-pad on the die, the use of a microprobe of 10 micron shaft diameter

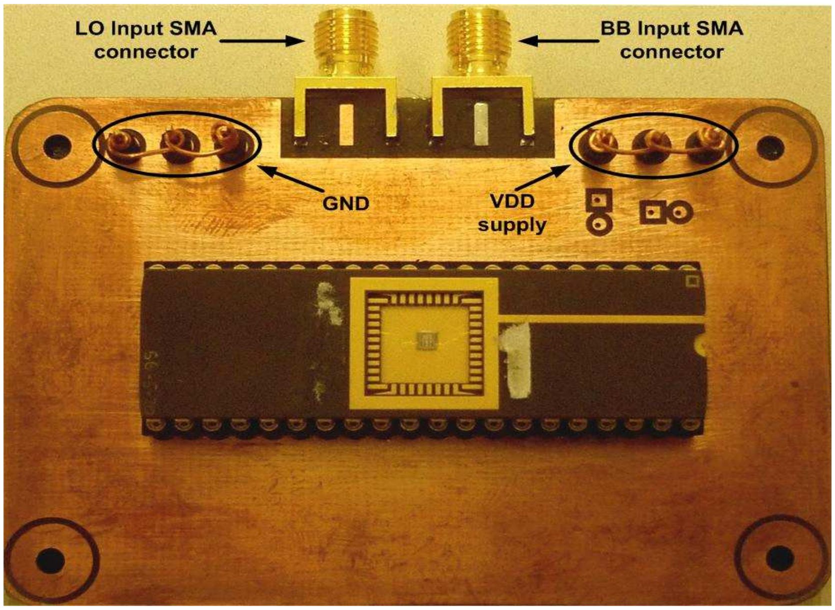

Figure 8.6: *Evaluation test board.*

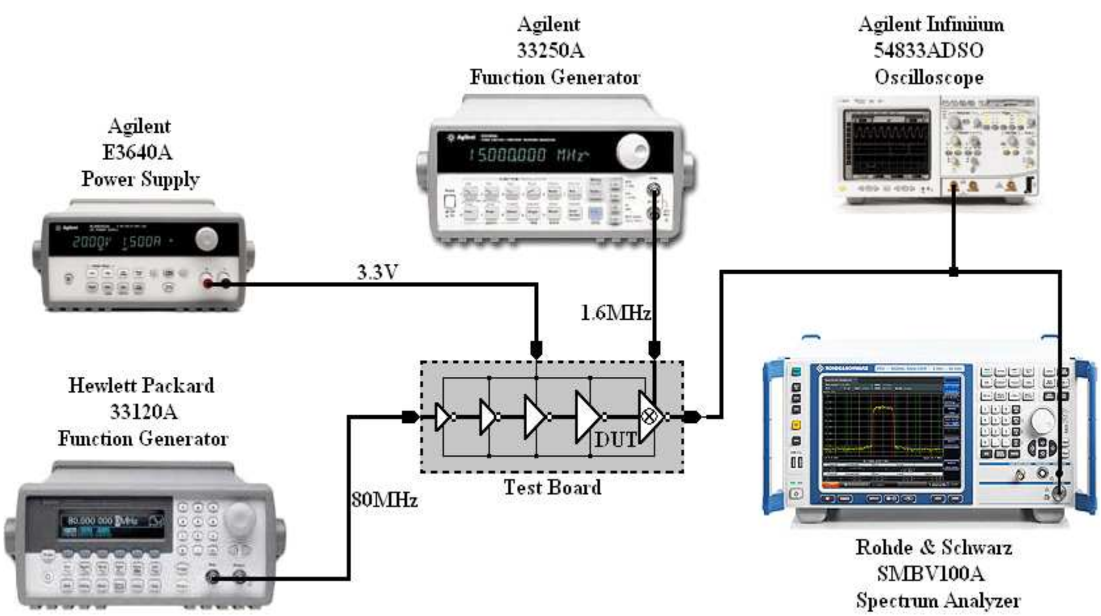

Figure 8.7: *Test-setup.*

model 35 of the brand Picoprobe® was necessary. The microprobe was mounted on a FPD-100 Fine Pitch Dual Positioner. In turn, the use of the microprobe demanded the use of a vibration isolation table. For that reason, we employ the table Newport model HL-3648W-OPT.

LO frequency	80MHz
BB frequency	1.6MHz
Power supply, V_{dd}	3.3V
Tuning control	1.0V-1.4V
Maximum power consumption	14.5dBm
Minimum power consumption	12.6dBm
Maximum output power	6.5dBm
Minimum output power	0.3dBm
Maximum duty cycle	49.4%
Minimum duty cycle	40.1%
Maximum pulse amplitude	1V
Minimum pulse amplitude	0.95V-0.2V

Table 8.4: *Experimental results of the predriver stage.*

Table 8.4. summarizes the most important characteristics of the prototype. As mentioned earlier, The LO frequency was 80MHz meanwhile the BB frequency was 1.6MHz. The power supply for the circuit was of 3.3V. The tuning control was of 400mV ranging from 1.0V to 1.4V. The maximum power consumption was 14.5dBm and the minimum power consumption was 12.6dBm. The maximum output power was 6.5dBm meanwhile the minimum output power was 0.3dBm. The duty cycle of the prototype was modifiable in a range of 9.3% from 49.4% to 40.1%. Finally, the maximum pulse amplitude of the output signal was 1V and the minimum pulse amplitude covers from 950mV to 200mV.

Figure 8.8 shows the waveforms obtained at the output of the prototype for some voltage values of the tuning control. As can be appreciated, conforming the tuning control goes from less to more, the pulse train at the output varies periodically its amplitude and also its duty cycle and consequently it changes the power delivered to the load. The variation of both, duty cycle and output power are desired in the circuit and were anticipated in the synthesis of the predriver such that it would drive more efficiently the power amplification stage. Figure 8.9 depicts the behavior of the duty cycle for the whole tuning control range. It can be seen that as the tuning voltage increases the duty cycle decreases. On the other

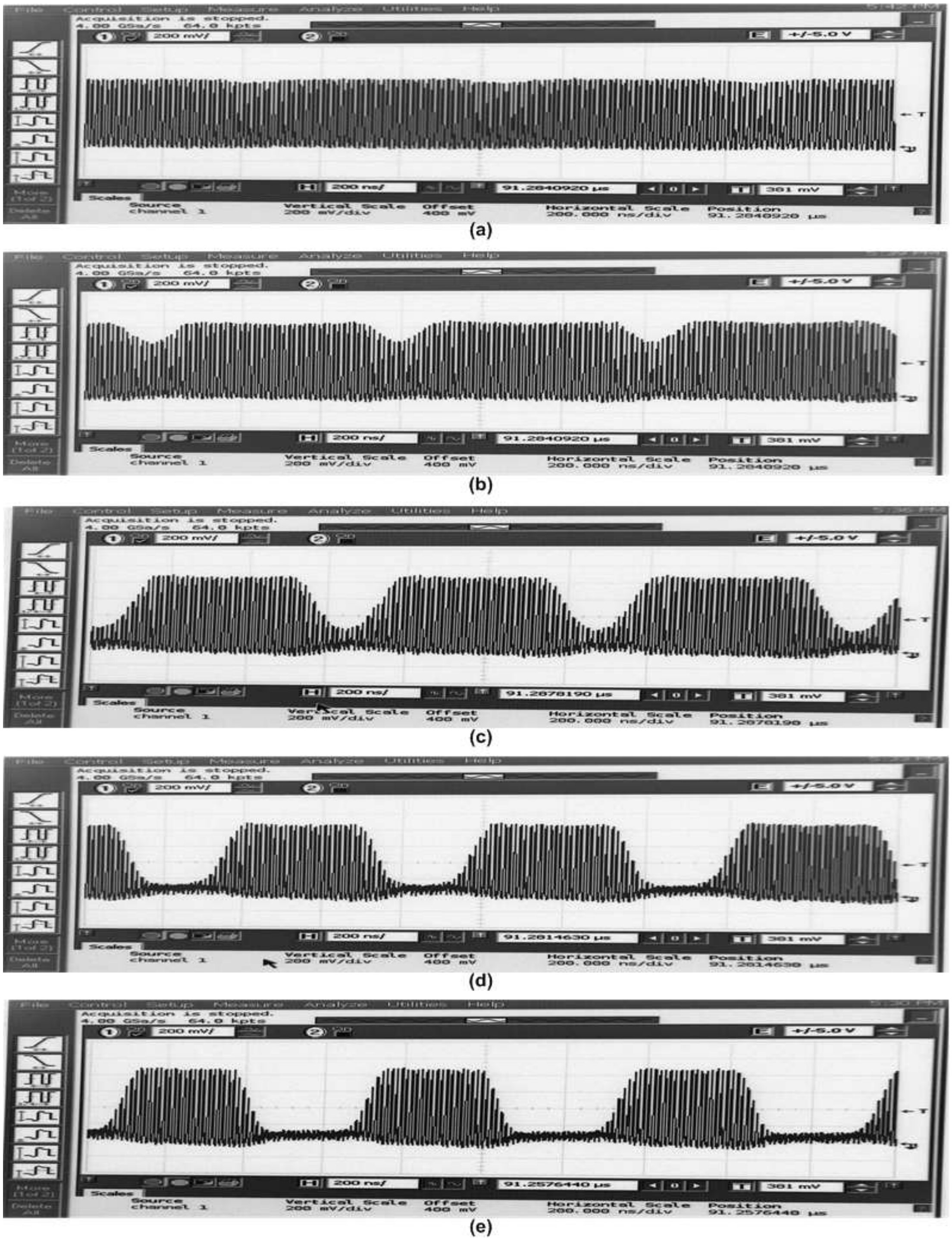

Figure 8.8: *Output waveforms of the prototype @: (a)1.0V of tuning control, (b)1.1V of tuning control, (c)1.2V of tuning control, (d)1.3V of tuning control, (e)1.4V of tuning control.*

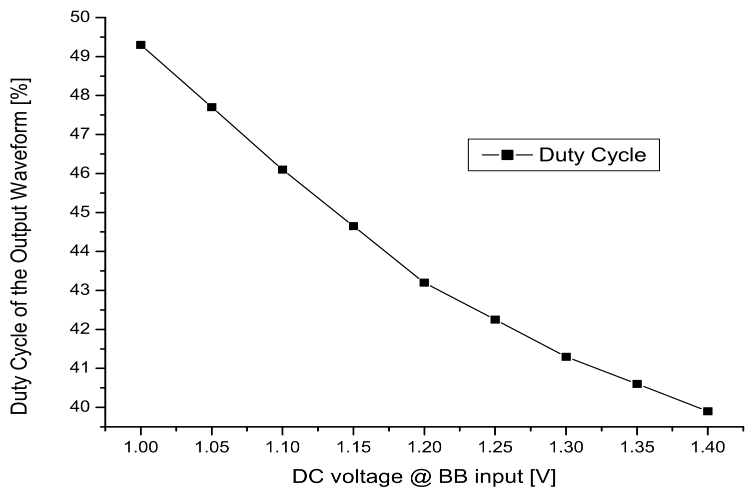

Figure 8.9: *Duty cycle of the prototype for the whole tuning control range.*

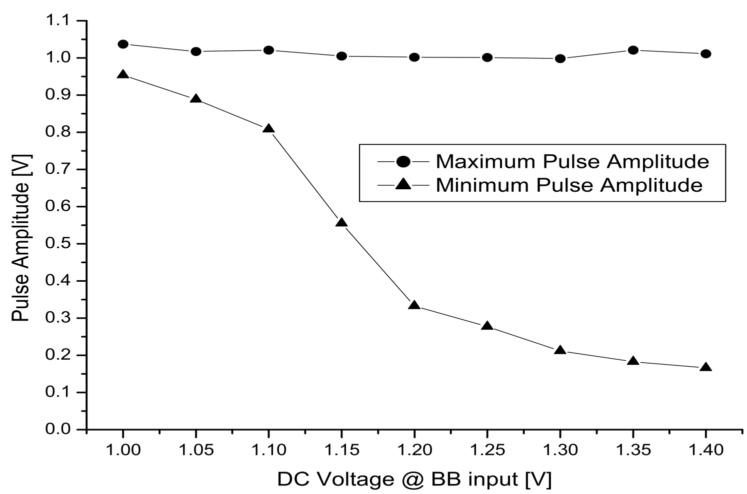

Figure 8.10: *Pulse amplitude of the prototype for the whole tuning control range.*

hand, Figure 8.10 shows the variation of the pulse amplitude at the output of the circuit in function of the tuning control voltage. We can see that the maximum pulse amplitude is kept almost constant over the entire tuning control range. Nevertheless, the minimum pulse amplitude decreases as the control voltage goes high.

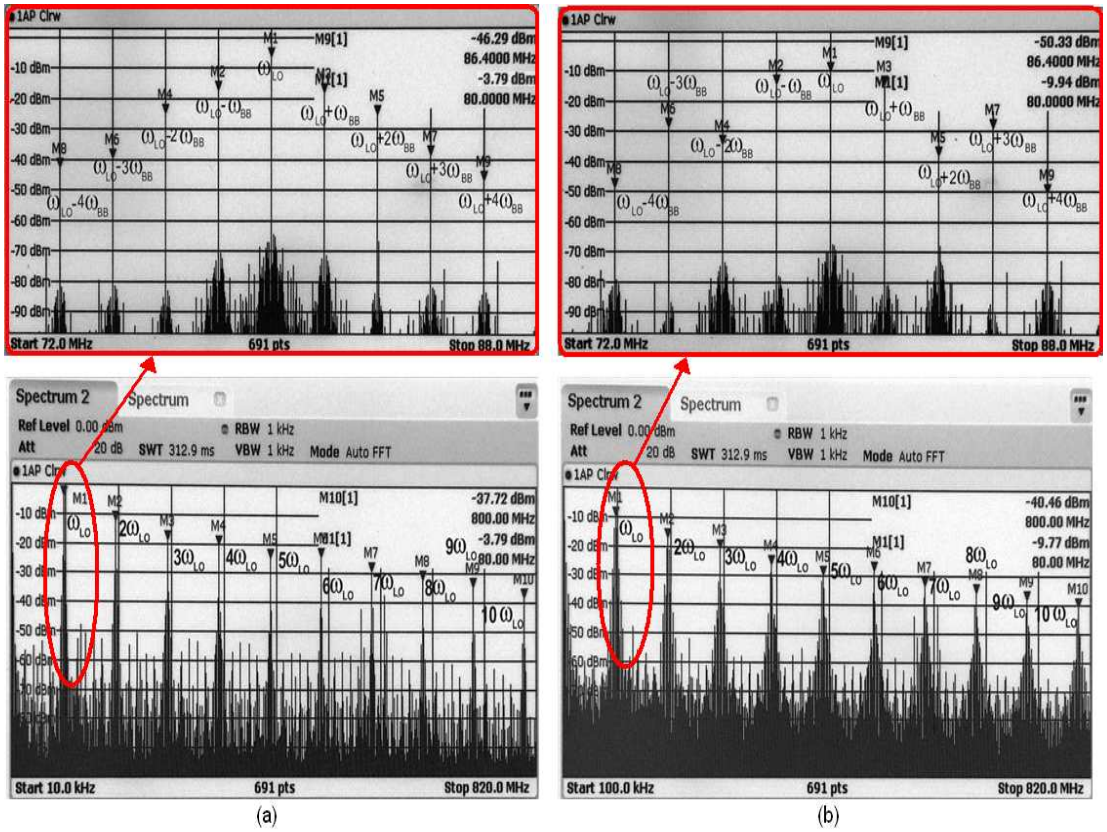

Figure 8.11: *Spectrum at the output of the prototype for: (a) the maximum output power handed to the load, and (b) the minimum output power handed to the load.*

It is also of major interest to examine the spectral content of the output signal in order to determine the harmonics and IM prodcust produced by the predriver stage. Figure 8.11 shows the spectrum at the output of the prototype for both, the maximum and minimum output power handed to the load. As predicted in the synthesis of the mixer, at least the ten higher order harmonics and IM products appear on the spectrum. A zoom to the neighborhood of the fundamental component shows that the frequency components $\omega_{LO}-4\omega_{BB}$, $\omega_{LO}-3\omega_{BB}$, $\omega_{LO}-2\omega_{BB}$, ω_{LO}, $\omega_{LO}+\omega_{BB}$, $\omega_{LO}+2\omega_{BB}$, $\omega_{LO}+3\omega_{BB}$, and $\omega_{LO}+4\omega_{BB}$ are present with enough power to be taken into account. From those IM products, only the terms $\omega_{LO}\pm\omega_{BB}$ were anticipated in the analysis. This can be explained by the fact that in the analysis performed a two third duty cycle square wave was considered to drive the mixer meanwhile in the experiment a 50% duty cycle signal obtained from a chain of inverters is driven the mixer. Thus, the changes

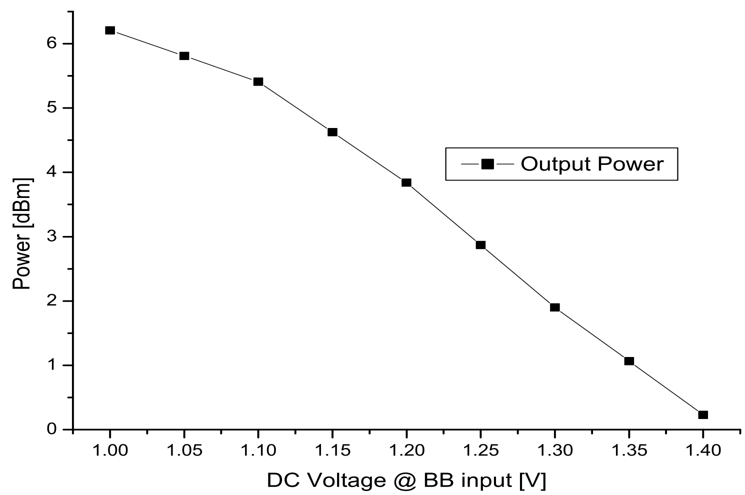

Figure 8.12: *Output power of the prototype for the whole tuning control range.*

in the shape of the driving signal modify the spectral content expected, specially the IM products.

Figure 8.12 shows the output power of the frequency of interest, $\omega_{LO}+\omega_{BB}$, as a function of the tuning control voltage. An output power back-off of almost 6dB is attained for the 400mV of tuning range. Again, for the lowest value of the tuning control the maximum output power is present and for the highest value of the control, the minimum output power is available in the circuit.

Finally, Figure 8.13 depicts the power consumption of the predriver stage in function of the control voltage. The behavior of the consumption is also inversely proportional to the tuning range. Thus, when the the maximum output power is demanded by the load, the duty cycle of the output wave form is increased as well as the voltage swing of the pulse train at the output. On the other hand, at maximum output power back-off, the duty cycle is reduced approximately a 10% and the pulse train at the output exhibits a periodic alternation between the maximum voltage swing and the minimum voltage swing ($\approx$ 20% of the maximum voltage swing). This in turn allows to the power amplification stage placed before the mixer to modify its conduction angle and its power gain and therefore, to improve its efficiency in function of the power demanded by the antenna.

According to the results obtained in the characterization of the prototype,

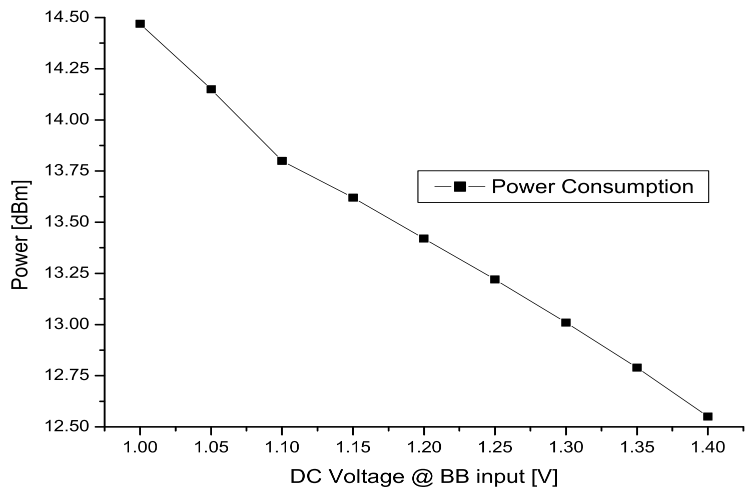

Figure 8.13: *Power consumption of the prototype for the whole tuning control range.*

we conclude that the behavior of the predriver stage follows the curse anticipated in the synthesis of the mixer performed in chapter 6.

8.4 Conclusions

The simulation in $CadenceVirtuoso^{®}v$5.0.0. of the complete power amplification stage for mobile WiMAX with the UMC 0.18μm MIxed Mode and RF CMOS technology was carried out. The RF band for which the circuit was tuned to operate was between 2.496GHz and 2.69GHz with an LO signal running from 2.486GHz to 2.68GHz and a BB signal of 10MHz. The power supply for the predriver stage was of 1.8V and 0.9V for the amplification stage. The total power consumption of the circuit was of approximately 26dBm. The peak output power obtained was 23dBm with a η_D of 83% and a PAE of 61% meanwhile for 12dB of output power back-off the η_D was 33% and the PAE of 31%. The harmonic suppression around the carrier in a range of $\omega_{LO} \pm 10\omega_{BB}$ presents a minimum value of -55dBc. These results indicate that the the proposed multipath polyphase PA exhibits both, a high linearity achieving until -60dBc of IM suppression with respect to the frequency of interest ($\omega_{LO}+\omega_{BB}$) within the mobile WiMAX bandwidth, and a high power-added efficiency at peak output power and at 12dB of output power back-off. However, in the simulations performed the losses introduced by external circuitry such as the balun or the step-down network showed in Figure 7.4 were not considered and thus the efficiency attained with a real circuit is expected to be lower. However, it still is a good efficiency considering that the complete system also exhibits a high linearity and, by definition, the higher the linearity is in the PA the lower the efficiency becomes [15].

In addition, the design and fabrication of the predriver stage was also realized but in a double poly three metal layers $0.5\mu m$ CMOS technology from MOSIS foundry. The fabricated prototype area was $0.472\mu m \times 0.148\mu m$. The printed board circuit (PCB) used for measurements was designed and fabricated with an standard FR4 material. The prototype was characterized with an LO frequency of 80MHz and a BB frequency of 1.6MHz. The power supply was of 3.3V. The tuning control was of 400mV ranging from 1.0V to 1.4V. The maximum power consumption was 14.5dBm and the minimum power consumption was 12.6dBm. The maximum output power was 6.5dBm meanwhile the minimum output power was 0.3dBm. The duty cycle of the prototype was modifiable in a range of 9.3% from 49.4% to 40.1%. Finally, the maximum pulse amplitude of the output signal was 1V and the minimum pulse amplitude covers from 950mV to 200mV. As predicted in the synthesis of the mixer, at least the ten higher order harmonics and IM products appear on the spectrum. A zoom to the neighborhood of the fundamental component shows that the frequency components $\omega_{LO} - 4\omega_{BB}$, $\omega_{LO} - 3\omega_{BB}$, $\omega_{LO} - 2\omega_{BB}$, ω_{LO}, $\omega_{LO} + \omega_{BB}$, $\omega_{LO} + 2\omega_{BB}$, $\omega_{LO} + 3\omega_{BB}$, and $\omega_{LO} + 4\omega_{BB}$ are present with enough power to be taken into account. From those IM products, only the terms $\omega_{LO} \pm \omega_{BB}$ were anticipated in the analysis. This can be explained by the fact that in the analysis performed a two third duty cycle square wave was considered to drive the mixer meanwhile in the experiment a 50% duty cycle signal obtained from a chain of inverters is driven the mixer. Thus, the changes in the shape of the driving signal modify the spectral content expected, specially the IM products. According to the results obtained in the characterization of the prototype, we conclude that the behavior of the predriver stage follows the curse anticipated in the synthesis of the mixer performed in chapter 6.

Chapter 9

Summary and Conclusions

In this chapter, the thesis is summarized, the main conclusions are listed and finally the suggestions for future research are given.

9.1 Summary of the Thesis

Chapter 1

The salient features of mobile WiMAX are highlighted as follows [1], [6]:

- The support of cost-effective broadband access services over large geographic areas with mobile transmission scenarios.
- High data rates.
- Improved multipath performance in non-line-of-sight ($NLOS$) environments.
- The capability to operate in scalable channel bandwidths to comply with various spectrum allocations worldwide.
- Quality of service (QoS).

In order to provide the necessary channel robustness for the support of a high spectral efficiency, mobile WiMAX employs *S-OFDMA*. Unfortunately, the use of *S-OFDMA* results in a high PAPR, which imposes stringent requirements on the transmitter, specially on the linearity of the PA, which has to include the high peak power value in its amplification range. Moreover, the ACPR established for mobile WiMAX tolerates an spectral regrowth of, maximum, -44dBc. On the other hand, since mobile WiMAX has been planned for being used in portable terminals, it is preferable to make use of an efficient PA to extend the duration of the battery which provides the power supply to the terminal. Therefore, a linear and efficient PA is demanded.

Chapter 2

A high linearity and a good efficiency are difficult, if not impossible, to get with conventional PAs. On one hand, the linearity of transconductance PAs decreases as the conduction angle of the input signal is reduced, but at the same time, the efficiency rises. On the other hand, switched PAs are essentially non-linear amplifiers, yet, their efficiency is better when compared to that attained with their transconductance counterparts.

The election of a particular class of operation depends on the needs of the system where the amplifier is going to be placed. If both, linearity and efficiency are wanted, then, a transconductance PA with a good trade-off between those figures of merit can be preferred. For instance, a class B or class C amplifer. However, if the linearity demands are stringent, then, the non-linearity introduced by such amplifiers may be inadmissible. Even though classes of operation such as AB and A are, in theory, more linear, in practice, however, the active devices employed in PAs have non-linearities that produce detrimental effects into the system. Therefore, there is the need to improve the linearity of conventional PAs. Specially when the demands of the system where they are used are strict, e.g. the mobile WiMAX technology.

Chapter 3

A comparison of many different linearization techniques used in RF systems was realized. We saw that the linearization performance of the cartesian feedback is good. Besides, it presents moderated efficiency and complexity. Nonetheless, its narrow bandwidth and low capacity for multicarrier make it impractical for mobile WiMAX. On the other hand, the low capability for cancelling distortion components with analog predistortion and bias adaptation, make them also inappropriate for systems where the linearity claims are demanding. However, those approaches offer a high efficiency. A moderate linearization effect, medium bandwidth and middling efficiency are appealing characteristics of the digital predistortion, EER and LINC linearizers. Notwithstanding, their high complexity is a drawback which may be difficult to overcome, specially in a system such as mobile WiMAX, with very stringent performance requirements. Finally, the multipath-polyphase PA posses very attractive features: a high linearization performance with a wide bandwidth and a moderate complexity. Unfortunately, the efficiency attained with the PA proposed in [27] is quite low. Anyhow, the system was not intended to exhibit a high efficiency, therefore, there is the possibility to conceive a new design with a better power conversion ability.

Chapter 4

The principle of operation for linearizing non-linear systems by means of the multipath-polyphase technique was described. It consists of dividing the non-linear block into smaller identical non-linear blocks with phase shifts before and after them. Depending on the number of paths and phases employed the non-linearities can be cancelled to some extent. This characteristic provides a high flexibility to the technique, and hence, it suits to different wireless technologies with diverse linearity requirements.

When the input signal is compound by more than a single tone, harmonics and IM distortion are produced. Moreover, since the last phase shifts in the system are performed with a mixer and one of the inputs to the mixer is a square wave signal, then XM modulation is also present. From those distortion components, the third order products are not cancelled regardless the number of paths and phases occupied. A solution for cancelling this troublesome non-linearities is to modify the duty cycle of the square wave signal to 1/3. However, by doing this, new even harmonics are produced. Fortunately, a differential architecture can be used to cancel this new unwanted products.

In a real multipath-polyphase linearizer mismatch plays a significant role. Perfect cancellation of distortion components is only possible if all the paths and blocks are identical. Unfortunately, this is not possible due to the fact that the materials employed to implement transistors and interconnection lines exhibit properties that vary randomly. As a result, distortion is not completely cancelled but suppressed to some extent. In general terms, the phase mismatch in the system is more crucial than the mismatch from the power gain among the non-linear blocks. The larger the number of paths and phases is, the more effective the harmonic suppression is accomplished.

Chapter 5

The efficiency analysis of the linearized multipath polyphase power upconverter circuit was introduced. The results obtained indicate that the circuit is inefficient at output power back-off. The cause of this drawback is the failure of the circuit to provide some power gain, which originates a deficient PAE. The proposed architecture of the power upconverter is such that the larger portion of the input power is proportional to the aspect ratio of the big transistor that performs as a hard switch driven by the fast LO. Consequently, the energy investment to mix the BB and LO by means of that topology is excessive.

Linear PAs for wireless communication systems which are considered to operate in portable terminals are preferable to exhibit a high efficiency in order to extend the battery duration. Since mobile WiMAX belongs to this class of transmission systems, a linear and efficient PA is preferred. Therefore, the design and implementation of a linearized multipath PA with improved efficiency is an assignment that must be addressed.

Chapter 6

The synthesis of a new multipath polyphase power amplifier with improved efficiency was introduced. Since the key factors for power saving in the PA lie on its power gain and the conduction angle at which the amplifier is driven, then the allocation of the upconverter at the amplification stage, as it was proposed originally, has been changed. Instead, the up-converter is now allocated behind the PA as a predriver stage whose functions are: to modify the conduction angle at which the PA is driven and, at the same time, to regulate the power it delivers to the amplifier. The use of a CMOS inverter gate with the inclusion of a current mirror was proved to be useful as a time variant mixer at high frequency capable of regulating its output power and the duty cycle of its output signal, i.e. the conduction angle of the signal which drives the PA. By doing this, the amplification stage becomes now a mixed mode class C PA whose PAE is high at both, peak output power and average output power even in the presence of a large power back-off. The suppression of many distortion components in function of the number of paths used still is preserved in the new multipath polyphase architecture. However, the carrier, ω_{LO}, as well as the lower side band, $\omega_{LO} - \omega_{bb}$, are not cancelled and therefore the inclusion of a bandpass filter at the output of the system to suppress to some extent such components may be necessary depending on the linearity requirements of the wireless technology where the technique is going to be applied. If the use of a bandpass filter is necessary, then the separation between ω_{LO} and ω_{bb} must be chosen taking into account this fact in order to relax the demands of the filter. The price paid by employing a filter is the reduction in the efficiency due to the loss mechanisms present on the filter. Thus, a trade-off between linearity and efficiency must be done if the new multipath polyphase PA is adopted.

Chapter 7

The design of a complete pseudo-differential power amplification system for mobile WiMAX in CMOS technology was presented. The new PA is intended to exhibit a high linearity which considers the cancellation of both: out-of-channel interferers established by the IEEE802.16e-2005 standard and high order harmonics and IM products which appear along the UHF and EHF bands. In addition, the proposed topology is also intended to present a high efficiency since the inclusion of a mixer with the ability of modifying its output power and conduction angle as the predriver stage of the amplifier have been employed. The inclusion of a step-down network to modify the impedance seen by the PA and thus deliver the adequate power to the antenna have been also addressed.

Finally, equations for sizing the transistors involved in the system and important considerations in the design procedure were also introduced.

Chapter 8

The simulation in $CadenceVirtuoso^{\circledR}v5.0.0.$ of the complete power amplification stage for mobile WiMAX with the UMC 0.18μm Mixed Mode and RF CMOS technology was carried out. The RF band for which the circuit was tuned to operate was between 2.496GHz and 2.69GHz with an LO signal running from 2.486GHz to 2.68GHz and a BB signal of 10MHz. The power supply for the predriver stage was of 1.8V and 0.9V for the amplification stage. The total power consumption of the circuit was of approximately 26dBm. The peak output power obtained was 23dBm with an η_D of 83% and a PAE of 61% meanwhile for 12dB of output power back-off the η_D was 33% and the PAE of 31%. The harmonic suppression around the carrier in a range of $\omega_{LO} \pm 10\omega_{BB}$ presents a minimum value of -55dBc.

These results indicate that the the proposed multipath polyphase PA exhibits both, a high linearity achieving until -60dBc of IM suppression with respect to the frequency of interest, $\omega_{LO}+\omega_{BB}$, within the mobile WiMAX bandwidth, and a high power-added efficiency at peak output power and at 12dB of output power back-off. However, in the simulations performed the losses introduced by external circuitry were not considered and thus the efficiency attained with a real circuit is expected to be lower.

In addition, the design and fabrication of the predriver stage was also realized but in a double poly three metal layers $0.5\mu m$ CMOS technology from MOSIS foundry. The fabricated prototype area was $0.472\mu m \times 0.148\mu m$. The prototype was characterized with an LO frequency of 80MHz and a BB frequency of 1.6MHz. The power supply was of 3.3V. The tuning control was of 400mV ranging from 1.0V to 1.4V. The maximum power consumption was 14.5dBm and the minimum power consumption was 12.6dBm. The maximum output power was 6.5dBm meanwhile the minimum output power was 0.3dBm both with a load of approximately 1pF. The duty cycle of the prototype was modifiable in a range of 9.3% from 49.4% to 40.1%. Finally, the maximum pulse amplitude of the output signal was 1V and the minimum pulse amplitude covers from 950mV to 200mV. As predicted in the synthesis of the mixer, at least the ten higher order harmonics and IM products appear on the spectrum. The frequency components $\omega_{LO}-4\omega_{BB}$, $\omega_{LO}-3\omega_{BB}$, $\omega_{LO}-2\omega_{BB}$, ω_{LO}, $\omega_{LO}+\omega_{BB}$, $\omega_{LO}+2\omega_{BB}$, $\omega_{LO}+3\omega_{BB}$, and $\omega_{LO}+4\omega_{BB}$ are present with enough power to be taken into account. From those IM products, only the terms $\omega_{LO}\pm\omega_{BB}$ were anticipated in the analysis.

This can be explained by the fact that in the analysis performed a two third duty cycle square wave was considered to drive the mixer meanwhile in the experiment a 50% duty cycle signal obtained from a chain of inverters is driving the mixer. Thus, the changes in the shape of the driving signal modify the spectral content expected, specially the IM products. According to the results obtained in the characterization of the prototype, we conclude that the behavior of the predriver stage follows the curse anticipated in the synthesis of the mixer performed in chapter 6.

9.2 Original Contributions

- The study and analysis of several linearization procedures used in RF PAs which culminated in the settlement that the multipath-polyphase technique employed in PAs is the most convenient approach from those for mobile WiMAX since it exhibits a high linearization performance with a wide bandwidth and a moderate complexity. (Chapter 3)

- The introduction of the efficiency analysis of the linearized multipath polyphase power upconverter proposed in [27]. By means of that analysis, the establishment of the causes because of such system is inefficient at output power back-off was found. The results obtained indicate that the cause of the drop in the efficiency of the circuit is its failure to provide power gain. (Chapter 5)

- The introduction of a new time variant mixer architecture useful at RF frequencies which has the ability of regulating its output power and the duty cycle of its output signal. (Chapter 6)

- The synthesis of a new multipath polyphase mixed mode class C Power Amplifier with improved efficiency at both, peak output power and average output power with a large power back-off, by means of the use of a subharmonic mixer allocated behind the PA as a predriver stage with the capability of modifying the conduction angle at which the PA is driven and, at the same time, regulating the power it delivers to the amplifier.(Chapter 6)

- The design of a complete pseudo-differential power amplification system for mobile WiMAX in CMOS technology with a high linearity intended to cancel both, out-of-channel interferers established by the IEEE802.16e-2005 standard and high order harmonics and IM products which appear along the UHF and EHF bands, and, at the same time, a high efficiency which make the system suitable to be used in portable terminals. (Chapter 7)

- The design, fabrication and characterization of the new time variant mixer realized in a double poly three metal layers $0.5\mu m$ CMOS technology from MOSIS foundry. The results obtained in the characterization of the prototype indicate that the behavior of the mixer follows the curse anticipated in the synthesis. (Chapter 8)

9.3 Recommendations for Future Work

- When using the multipath polyphase technique to linearize a circuit, the fact that mismatch plays a significant role must be taken into account. Consider that the perfect cancellation of the distortion components is only possible if all the paths and blocks used are identical. Unfortunately, this is not possible in reality and, as a consequence, the distortion is not completely cancelled but suppressed to some extent. In general terms, the phase mismatch in the system is more crucial than the mismatch from the non-linear blocks. Moreover, the larger the number of paths and phases is, the more effective the harmonics suppression is accomplished, but with a major complexity in the system.

- The analysis of the new mixer architecture introduced must be done if it is considered to be employed for down conversion purposes. In this work, the analysis of the system was performed assuming the LO signal was larger than the BB signal. Thus, the results attained may be different in the opposite case.

- In order to check the performance of the predriver stage at RF frequency, the characterization of this block must be realized at frequencies higher than that employed in this work. Here, the aim of the characterization was simply to determine if the behavior of the predriver followed the curse anticipated in the synthesis. Nevertheless, if the circuit is intended to be used at a high frequency, it is important to evaluate its functionality when the LO signal runs at a higher speed.

- The use of the mixed mode class C Power Amplifier introduced in this work can be extended to systems where efficient power amplification is required without the employment of the multiple paths/phases. If linearity is not an issue or the requirements are not so stringent, then the power amplification system proposed can be applied in a differential or even a stand alone way with or without the use of a filter at the output.

- An important task that must be carried out as part of the future work of this project is to test experimentally the complete power amplification system. The simulations provide a useful insight of the circuit. However, it is important to corroborate the functionality and performance of it with experimental data.

- Nowadays there are many sophisticated communication wireless technologies which make use of OFDMA with scalable bandwidths and diverse modulation techniques. Invariably, this results in a high PAPR present in the transmission path which, in turn, establishes constraints in the linearity of Power Amplifier since it has to include the high peak power value in its amplification range. Moreover, since most of those technologies are intended for portable terminals, then efficiency is also a major concern. Therefore, although the solution proposed in the present work was made specifically for mobile WiMAX, it can also be extended to other wireless systems were linearity and efficiency are required. Furthermore and without any loss of generality, the approach presented in this work can be used in any system where linearity and efficiency are important parameters that must be improved.

Bibliography

[1] IEEE Std 802.16eTM-2005 and IEEE Std 802.16TM-2004/Cor 1-2005, *IEEE Standard for Local and Metropolitan Area Networks Part 16: Air Interface for Fixed Broadband Wireless Access Systems, Amendment 2: Physical and Medium Access Control Layers for Combines Fixed and Mobile Operation in Licensed Bands*, IEEE-SA Standards Board.

[2] A. Syed and I. Mohammad, *WiMAX Technologies, Performance Analysis, and QoS*, CRC Press, USA, 2008.

[3] P. Deepak, *The Business of WiMAX*, John Wiley & Sons, England, 2006.

[4] http://www.wimaxforum.org

[5] *Understanding the Radio Technologies of Mobile WiMAX and their Effect on Network Deployment Optimization*, Alvarion, white paper, 2006.

[6] D. Gray, *Mobile WiMAX: A Performance and Comparative Summary, WiMAX forum white paper*, September 2006.

[7] Mobile WiMAX - Part I: A technical Overview and Performance Evaluation, WiMAX forum white paper, August 2006.

[8] S. Llyod, *Challenges of mobile WiMAX RF transceivers*, in Proc. IEEE International Conference on Solid-State integrated Circuits Technology (IC-SICT), pp. 1821-1824, 2006.

[9] European Standard Telecommunication Series, *Fixed Radio Systems; Point-to-Multipoint Equipment; TimeDivision Multiple Access (TDMA); Point-to-Multipoint Digital Radio Systems in Frequency Bands in the range 3 GHZ to 11 GHz*, ETSI EN 301 021 v1.6.1 (2003-07).

[10] ITU Radiocommunication Study Group, *Document 8F/1344-E, Unwanted Emission Characteristics of IMT-2000 OFDMA TDD WMAN Mobile Stations, Annex 6 of Recommendation ITU-RM 1581*, August 2007.

[11] G. Li and G. Stüber, *Orthogonal Frequency Division Multiplexing for Wireless Communication*, Springer, Dordrecht, 2006.

[12] F. Xiong, *Digital Modulation Techniques*, Artech House, Boston, 2006.

[13] K.C. Tsai, *CMOS Power Amplifiers for Wireless Communications*, PhD theses, Faculty of Electrical Engineering and Computer Sciences of the University of California at Berkeley, 2007.

[14] G. Liu, *Fully Integrated CMOS Power Amplifiers*, PhD theses, Faculty of Electrical Engineering and Computer Sciences of the University of California at Berkeley, 2006.

[15] T.H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, Cambridge, 2004.

[16] J. Vuolevi and T. Rahkonen, *Distortion in RF Power Amplifiers*, Artech House, Boston, 2003.

[17] S.A. Maas, *Nonlinear Microwave and RF Circuits*, Artech House, Boston, 2003.

[18] S.C. Cripps, *RF Power Amplifiers for Wireless Communications*, Artech House, Boston, 2006.

[19] J. Legarda, *Feedforward Amplifiers for Wideband Communication Systems*, Springer, Dordrecht, 2006.

[20] N. Pothecary, *Feedforward Linear Power Amplifiers*, Artech House, Boston, 1999.

[21] P.B. Kenington, *High-Linearity RF Amplifier Design*, Artech House, Boston, 2000.

[22] X. Zhang et al, *Design of Linear RF Outphasing Power Amplifiers*, Artech House, Boston, 2003.

[23] A. Shirvani and B. A. Wooley, *Design and control of RF Power Amplifiers*, Kluwer Academic Publishers, Dordrecht, 2003.

[24] J. Vankka, *Digital Synthesizers and Transmitters for Software Radio*, Springer, Dordrecht, 2005.

[25] N. Wongkomet, *Eficiency Enhancement Techniques for CMOS RF Power Amplifiers*, PhD theses, Faculty of Electrical Engineering and Computer Sciences of the University of California at Berkeley, 2006.

[26] E. Mensink et al, *Distortion Cancellation by Polyphase Multipath Circuits*, IEEE Transaction on circuits and systems-I:Regular papers, vol. 52, no. 9, September 2005.

[27] R. Shrestha et al, *A Polyphase Multipath Technique for Software Defined Radio Transmitters*, IEEE Journal of Solid State Circuits, Vol. 41, No. 12, pp. 2681-2692, Dec. 2006.

[28] E.A.M. Klumperink et al, *Cognitive radios for dynamic spectrum access Polyphase Multipath Radio Circuits for Dynamic Spectrum Access*, IEEE Communications Magazine, Vol. 45, Issue 5, pp. 104-112, May 2007.

[29] A. Levitin, *Introduction to the Design and Analysis of Algorithms*, Pearson Addison-Wesley, New Jersey, 2007.

[30] F. Behbahani et al, *CMOS mixers and polyphase filters for large image rejection*, IEEE Journal of Solid State Circuits, Vol. 36, No. 6, pp. 873-887, Jun. 2001.

[31] E.A.M. Klumperink et al, *A CMOS switched Transconductor Mixer*, IEEE Journal of Solid State Circuits, Vol. 39, No. 8, pp. 1231-1240, Aug. 2004.

[32] W. Sansen, *Distortion elementary transistor circuits*, IEEE Transaction on circuits and systems-II:Analog Digital Signal Processing, vol. 46, no. 3, pp. 315-325, Mar 1999.

[33] B. Razavi, *Design of Analog CMOS Integrated Circuits*, Mc Graw Hill, New Jersey, 2001.

[34] R. Gregorian, and G. C. Temes, *Analog MOS Integrated Circuits for Signal Processing*, John Wyley & Sons, USA, 1986.

[35] E. Mensink, *Cancelling nonlinearity with multiple paths*, MSc theses, Faculty of Electrical Engineering, Mathematics and Computer Science of the University of Twente, 2002.

[36] J.M. Rabaey, A. Chandrakasan, and B. Kikolic, *Digital Integrated Circuits: A Design Perspective*, Prentice Hall, New Jersey, 2003.

[37] B. Razavi, *RF Microelectronics*, Prentice Hall, New Jersey, 1998.

[38] Pui-In Mak, Seng-Pan U and Rui P. Martins, *Tranceiver Architecture Selection: Review, State-of-the Art Survey and Case Study*, IEEE Circuits and Systems Magazine, Second Quarter 2007.

[39] H. Veendrick, *Deep-Submicron CMOS ICs, From Basics To ASICs*, Kluwer Academic Publishers, Dordrecht, 2000.

[40] D. Johns and K. Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, New Jersey, 1997.

[41] H. Darabi and A. Abidi, *Noise in RF-CMOS mixers: A simple physical model*, IEEE Journal of Solid State Circuits, vol. 35, No. 1, pp. 15-25, Jan. 2000.

[42] R.S. Narayanaswami, *RF CMOS Class C Power Amplifiers for Wireless Communications*, PhD theses, Faculty of Electri-

cal Engineering and Computer Sciences of the University of California at Berkeley, 2001.

[43] U.S. Deparment of Commerce, *National Telecommunications and Information Administration, Office of Spectrum Management*, October 2003.

[44] R. Shrestha, *A Wideband and Flexible Power Upconverter Using Multiple Paths*, MSc theses, Faculty of Electrical Engineering, University of Twente, The Netherlands, 2004.

Resumen

El presente trabajo trata acerca del diseño de un sistema de amplificación de potencia en tecnología CMOS submicrométrica que satisface los requerimientos establecidos por el estándar IEEE802.16e-2005 para terminales inalámbricas de tipo WiMAX móvil. Las características de este tipo de tecnología de acceso inalámbrico que dificultan la realización del amplificador de potencia son las siguientes:

- La frecuencia de operación a la cual el amplificador de potencia debe funcionar en el continente americano se ubica entre los 2.496GHz y los 2.69GHz. Por lo tanto, el ancho de banda efectivo es de 196MHz a una velocidad de operación alta. Esto implica dificultades en el diseño del amplificador ya que las dimensiones del mismo son grandes debido a los requerimientos de potencia pico (23dBm) y por tanto, los elementos parásitos presentes en el circuito son considerables. Esto impacta directamente en la velocidad de operación que puede alcanzarce, añadiendo dificultad en el diseño.

- Las especificaciones del enmascaramiento espectral de WiMAX móvil demandan un rechazo de potencia en canales adyacentes (ACPR) de al menos -44dBc para canales de 10 MHz de ancho de banda y un mínimo de -33dBc para canales con un ancho de banda de 5 MHz. Esto exige una gran linealidad por parte del amplificador de potencia ya que la energía generada para transmisión debe ser mucho mayor que la energía generada por efecto de las no linealidades en las bandas de frecuencia adyacentes.

- La razón de potencia pico a potencia promedio (PAPR) de salida presenta un rango muy grande (12dB), por lo que el valor máximo de potencia debe ser considerado en el diseño del amplificador de potencia. Esto trae como consecuencia que la eficiencia de dicho amplificador se vea afectada ya que el transmisor opera la mayor parte del tiempo a potencia promedio y sólo de manera esporádica debe operarar a máxima potencia. A su vez, una pobre eficiencia se va a reflejar en una duración menor de la batería con la que se está alimentando al circuito. Dado que las terminales móviles son típicamente portátiles y en consecuencia polarizadas con baterías, entonces un tiempo de duración de la batería extendido es deseable.

- El mercado para terminales móviles inalámbricas ha experimentado un crecimiento exponencial en los últimos años. La proyección del mercado para WiMAX móvil estima ventas de alrededor de 18 billones de terminales en el 2012 alrededor del mundo. Esto motiva a una reducción en los costos de manufactura para dichos equipos. Actualmente, es la tecnología CMOS la que es preferible para la realización de sistemas electrónicos debido a sus bajos costos de fabricación, entre otras ventajas. Por tanto, uno de los retos para los diseñadores de circuitos integrados es la realización de amplificadores de potencia de alto desempeño y confiabilidad en tecnología CMOS submicrométrica. Hoy en día son sólo algunas tecnologías de acceso inalámbrico que hacen uso de etapas de amplificación de potencia en tecnología CMOS. El uso de este tipo de sistemas realizados en dicha tecnología para WiMAX móvil es aún un problema abierto que debe ser atendido.

En principio, un amplificador de potencia que es lineal exhibe una eficiencia baja y viceversa, si la eficiencia del amplificador es alta entonces éste es un amplificador no lineal. Sin embargo, WiMAX móvil demanda linealidad y eficiencia. Existen algunas propuestas mediante las cuales es posible mejorar alguna de estas características. Dentro de la investigación llevada a cabo, se revisaron estas soluciones con el objetivo de determinar si alguna de ellas podía aplicarse de manera efectiva en WIMAX móvil. El estudio reveló que la técnica de múltiples trayectorías y múltiples fases ofrece una solución flexible con las características adecuadas para ser empleadas en WiMAX móvil. Hasta el momento existe reportado un amplificador de potencia en tecnología CMOS de $0.13\mu m$ de longitud de canal empleando esta técnica con una linealidad bastante alta, de -40dBc, y que opera a 2.4GHz. Sin embargo, la potencia de salida alcanzada es de tan sólo 9dBm con una eficiencia del 11%. Por tanto, la tesis fue enfocada hacia el diseño de un amplificador de potencia polifásico multitrayectoría en tecnología CMOS de $0.18\mu m$ de longitud de canal que satisface las demandas de WiMAX móvil.

Dentro de las aportaciones del trabajo se encuentra la síntesis de una etapa manejadora novedosa que es capaz de regular su potencia de salida y el ángulo de conducción de su señal de salida. A su vez, se diseño un sistema de amplificación de potencia multitrayectoría polifásico que hace uso de dicha etapa y con ello alcanza una mejor eficiencia tanto a potencia máxima como a potencia promedio de salida manteniendo la buena linealidad propia de un sistema multitrayectoria. Resultados experimentales obtenidos muestran que la etapa manejadora realiza satisfactoriamente la función para la cual fue diseñada. Con un area de $0.472\mu m \times 0.148\mu m$ en una tecnología CMOS de $0.5\mu m$ de la empresa MOSIS con doble polisilicio y tres capaz de metal, el prototipo realizado fue caracterizado con una frecuencia de la señal del oscilador local (LO) de 80MHz y una frecuencia de la señal de banda base (BB) de 1.6MHz. El voltaje de polarización empleado fué 3.3V. El voltaje de control fué de 400mV desde 1.0V hasta 1.4V. El máximo consumo de potencia fué de 14.5dBm y el mínimo de 12.6dBm. La máxima potencia de salida fué de 6.5dBm mientras que la mínima de 0.3dBm. El ciclo de trabajo de la señal a la salida fué modificable en un rango del 9.3% variando desde un 49.4% hasta un 40.1%. Finalmente, la amplitud máxima del pulso de la señal de salida fue de 1V y la mínima variaba desde 950mV a 200mV. Tal y como se predijo en la síntesis, al menos los primeros 10 armónicos de alto orden y productos de intermodulación aparecen en el espectro de la señal de salida. Los componentes de frecuencias $\omega_{LO} - 4\omega_{BB}$, $\omega_{LO} - 3\omega_{BB}$, $\omega_{LO} - 2\omega_{BB}$, ω_{LO}, $\omega_{LO} + \omega_{BB}$, $\omega_{LO} + 2\omega_{BB}$, $\omega_{LO} + 3\omega_{BB}$, and $\omega_{LO} + 4\omega_{BB}$ están presentes con suficiente potencia para ser tomados en cuenta. De estos productos de intermodulación, únicamente los términos $\omega_{LO} \pm \omega_{BB}$ fueron anticipados en el análisis. Esto se debe al hecho de que en el análisis realizado una señal cuadrada con un ciclo de trabajo del 66.66% fue considerada como la señal a la entrada del mezclador mientras que en la carcaterización experimental, la señal cuadrada que manejaba al mezclador provenía de una cadena de inversores lógicos con un ciclo de trabajo del 50%. De este modo, los cambios en la forma de onda de la señal cuadrada modifican el contenido espectral esperado, especialmente los productos de intermodulación. De acuerdo con estos resultados, verificamos que efectivamente es posible manejar de manera más eficiente a un amplificador.

Por otro lado, la simulación en $CadenceVirtuoso^{\circledR}v$5.0.0. del sistema de amplificación de potencia completo para WiMAX móvil en una tecnología CMOS de modo mixto/RF UMC de 0.18μm se llevó a cabo. La banda de RF para la cual el circuito fue sintonizado para operar fué entre los 2.496GHz y los 2.69GHz con una señal LO corriendo desde los 2.486GHz hasta los 2.68GHz y una señal BB de 10MHz. El voltaje de alimentación del circuito manejador fue de 1.8V y de 0.9V para la etapa de amplificación. El consumo de potencia total fue de 26dBm. La potencia máxima de salida fue de 23dBm con una eficiencia de drenador, η_D, del 83% y una eficiencia de potencia añadida, PAE, del 61% mientras que para 12dB de retroceso de potencia de salida la η_D fué de 33% y la PAE de 31%. La supresión de armónicos alrededor de la portadora en un rango de $\omega_{LO} \pm 10\omega_{BB}$ presentó un valor mínimo de 55dBc. Estos resultados indican que el amplificador de potencia multitrayectoría polifásico propuesto exhibe una alta linealidad alcanzando hasta 60dBc de supresión de productos de intermodulación con respecto a la frecuencia de interés, $(\omega_{LO} + \omega_{BB})$, dentro del ancho de banda de WiMAX móvil, así como una alta eficiencia de potencia añadida tanto a potencia de salida pico como con un un gran retroceso de potencia de salida de 12dB. Sin embargo, en las simulaciones realizadas las pérdidas introducidas por la circuitería externa que pudiera llegarse a emplear no fueron consideradas y de este modo la eficiencia alcanzada con un circuito real se espera que sea menor. Con estos resultados verificamos que efectivamente el sistema propuesto es lineal y eficiente.