Development of a hybrid simulation methodology for circuits composed by MOS and SET transistors

by

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Thank You!

Once upon a time...

Resumen

A corto plazo, se espera que la tecnología MOS (Metal-óxido-semiconductor) comparta espacio en el desarrollo de circuitos integrados con las tecnologías emergentes. Una de éstas es la electrónica de un solo electrón, lo que implica la generación de circuitos empleando transistores MOS y transistores de un solo electrón (o SET por su acrónimo en inglés). La integración de ambas tecnologías (SET y MOS) resulta en un circuito híbrido y los beneficios de combinarlos son múltiples. Por ejemplo, los circuitos híbridos proveen dimensiones nanométricas, ultra-bajo consumo de potencia y la presencia del fenómeno fsico conocido como Bloque Coulómbico, los cuales son característicos de la tecnología de un solo electrón. Por otro lado, alta ganancia, alta velocidad y una tecnología de fabricación madura son ventajas de la tecnología MOS. Aunque los beneficios de combinar dispositivos MOS y SET en el mismo circuitos son atractivos, hay retos en cada paso del flujo de diseño.

En particular, ésta tesis se enfoca en la etapa de simulación, donde el principal problema es la naturaleza del flujo de la carga, siendo continua para dispositivos MOS, mientras que para dispositivos de un solo electrón es discreta. Por lo que los métodos para resolver las ecuaciones de ambos mecanismos son de diferente naturaleza.

El principal problema discutido en éste trabajo es atacar los retos de incluir la tecnología emergente en el flujo de diseño de circuitos integrados. Y en específico, incorporar al SET empleando los estándares de modelado del transistor MOS.

El principal objetivo de ésta investigación es desarrollar una metodologa de modelado capaz de simular circuitos híbridos que contengan transistores MOS y de un solo electrón. Además, como objetivos particulares es la de generar modelos con diferentes niveles de complejidad. Los modelos desarrollados con ésta metodología han sido verificados usando diferentes circuitos mostrando excelentes resultados.

Finalmente, aunque éste trabajo se enfoca en el modelado del dispositivo SET, la metodología propuesta puede ser extendida a otros dispositivos o sistemas siempre que la datos de observación/medición sean conocidos.

Abstract

In a near future, MOS technology is expected to share space in electronic design with emerging technologies. One of these is single-electronics, which implies the generation of circuits employing MOS and single-electron transistors (SET).

Integrating components of both technologies SET and MOSFET results in a hybrid circuit. The benefits of combining them are multiples. For instance, the hybrid circuits provide nanoscale dimensions, ultra-low power consumption and the Coulomb Blockade Oscillation phenomenon, all of which are characteristics of the SET. By contrast, high gain and current drive, high speed and very mature fabrication technology are all advantages of the MOSFET technology.

Although the benefits of combining MOSFET and SET devices in the same circuit are attractive, there are challenges at every step in the design path. In particular, this thesis focuses on the simulation stage where the main problem is the nature of the flow of the charge, being continuous for CMOS-devices while for SET-devices the flow is discrete. Thus, the methods to solve the equations from both mechanisms are of different natures.

The main problem discussed in this thesis is that of tackling the challenge of including electronic nanodevices in the integrated circuit design flow. More specifically, incorporating the SET while employing the electrical modeling standards of the MOS transistor is the central difficulty to be considered.

The main objective of this research is to develop the modeling methodology of hybrid circuit simulation MOS-SET. Besides, we will pursue particular objectives such as the development of models for the single-electron transistor at functional level, and the proposed methodology for hybrid simulation. The models that have been developed are fully compatible with standard IC circuit simulation frameworks such as HSPICE.

The models have been tested in a series of bench-mark circuits showing excellent results. The straightforward incorporation of the models into the IC verification flow results in a reduction on the simulation time with respect to a model suggested in the literature.

Finally, although this work focuses on the modeling of the single-electron transistor device, the methodology proposed can be extended to other devices or systems where the observed/measured data is known.

1 Introduction

In recent years, the electronic science has been growing exponentially. It is due to the constant development of new technologies, new ideas and principles. For example, the state-of-the-art MOSFET technology currently provides the capacity to build transistors with a channel length of 22 nanometers. Fifty years ago similar structures had a size of tens of micrometers. In other words, early integrated circuit (IC) only contained a few dozens of MOSFET transistors. And today, it is possible to have billions of MOSFET transistor built in a single IC.

More transistors, in the same space, improve the functionality of many aspects of ICs (cost, speed, power consumption, etc.) [1–4]. Shrinking the structures of MOSFET transistor would continue to enhance the cost, speed, and power consumption in ICs [1]. However, there are problems with further miniaturization. One way to classify these problems is to conceptualize their limits which are listed as follows; the fundamentals [5, 6], relate to materials [7–9], relate to device-level [10–12], related to circuitry and system [13–15]. In addition to these already mentioned limits, one must also keep in mind manufacturing cost and market demands – perhaps the most important factor determining the future of any technology.

Many of the above-referenced limitations can be resolved. However, one limit remains insurmountable – the physical limit. This relates to thermodynamics and to information theory, which define the minimum switching energy and hence the minimum channel length. For example, for an oxide thickness of 1.5 nanometers, the minimum channel length round at 14 nanometers a temperature of 300K [16].

While shrinking the transistor size is one option for improving the performance of ICs, it is not the only option. For instance, it is possible to incorporate non-classical Field Effect transistors such as fin-fet, multi-gate transistors, and others [17]. Another possibility would be to use unconventional materials such as dielectric with High-k, metals such as Cooper, etcetera [18, 19]. New emerging technologies such as the Single-Electron Transistor (SET), the memristor and, nanotubes, among others

may offer a way around the limits facing MOSFET technology. Coupling an emerging technology with the MOSFET technology is known as heterogeneous integration. And this is done with the aim to maximize the advantages of each technology. These options are found in the literature as More Moore, Beyond CMOS and More than Moore [20–22].

Integrating components of both technologies –SET and MOSFET – results in a hybrid circuit. The benefits of combining them are multiples. For instance, the hybrid circuits provide nanoscale dimensions, ultra-low power consumption, and Coulomb Blockade Oscillation phenomenon, all of which are characteristics of the SET transistor. By contrast, high gain and current drive, high speed and very mature fabrication technology are all advantages of the MOSFET technology.

Although the benefits of combining MOSFET and SET devices in the same circuit are attractive, there are challenges at every step in the design path. In particular, this dissertation focuses on the simulation stage where the main problem is the nature of the charge flow nature, being continuous for CMOS-devices while for SET-devices the flow is discrete. Thus, the methods to solve the equations from both mechanisms are of a different nature.

The main problem discussed in this dissertation is that of tackling the challenge of including electronic nanodevices in the integrated circuit design flow. More specifically, incorporating the SET transistor while employing the electrical modeling standards of the MOS transistor is the central difficulty to be considered.

The main objective of this research is to develop the modeling methodology of hybrid circuit simulation MOS-SET. From this, we will pursue particular objectives such as the development of models for the single-electron transistor for different abstraction levels, and the proposed methodology for hybrid simulation. The models developed are considered behavioral models and their constructions comply with the suggested of [23].

Finally, although this work focuses on the modeling of the single-electron transistor device, the methodology proposed can be extended to other devices or systems where the observed data is known. The methodology involved can easily be translated to other branches of engineering or science.

1.1 Manuscript Structure

The structure of this manuscript is given hereafter.

In Chapter 2, two main topics are presented; (1) the criteria formulation for device modeling and (2) the background of single-electron based electronics. The first deals with the abstraction of a system in order to be represented in a useful form. Also, the different kinds of model representation are depicted. The second topic is developed to give a brief history of single-electron based electronics in order to introduce the SET. In addition, some basic structures built with this technology are shown with the aim of introducing their main features.

In Chapter 3, the three main approaches to simulate the Single-electron transistors are depicted. Likewise, the advantages and disadvantages of each approach are shown. This chapter presents a proposed methodology for hybrid simulation. Finally, this chapter depicts the SET model development.

In Chapter 4, the applications of the modeling methodology developed in this dissertation are shown. This was achieved by using the proposed models in several hybrid and non-hybrid structures. The chapter starts with a section of a hybrid and a non-hybrid logic gates. It continues with an analogical section in which negative differential resistance (NDR) is shown. In order to verify the model, in some cases, the structures are compared with a device-level simulator.

In Chapter 5, some important conclusions are drawn while proposing key items for future improvements of this research.

2 State of the Art

This chapter is divided into two parts. The first part focusses on the classification of the device modeling, namely according to the stage of the modeling process where the information on the device is acquired, either an *a priori* or an *a posteriori* knowledge. In the second part, we examine the state-of-the-art of single-electron devices, with emphasis on the single-electron transistor operation and its voltage-current characteristics.

2.1 Device Modeling

Describing a system from the real world is not an easy task. In fact, an absolutely complete understanding of the device can never be attained. Humbly, we decide that the task is accomplished when there is an agreeable approximation between reality and model. The resulting model is thus valid under a series of constraints and assumptions.

Device modeling is a formulation developed from knowledge of a device in order to represent it in a useful form, more often based on a mathematical abstraction level. A conceptual item of interest is when the knowledge of the device under test is obtained. There are two fundamental stages when this information can be obtained:

A priori knowledge Herein this knowledge is strongly related to the structure of the device that can be glossed in terms of mechanical, chemical or physical descriptions. In electronics, devices modeled with this information resort to the internal structure of the device, and their models are studied by resorting to Semiconductor Physics. The resulting model is a structural one.

A posteriori knowledge When this type of knowledge is used to obtain the model of a device, the user makes direct observation of the device electrical behavior under various kinds of circumstances. In electronics, the models of devices obtained with this type of knowledge are generated from measurements under diverse types of stimuli signals. The result is a behavioral model.

Both categories need to be expressed in a useful form, for that purpose, a mathematical representation may be used. In the next section, we explain the importance of the mathematical modeling.

2.2 Mathematical Modeling

As mentioned above, the most frequently used representation of the model occur at mathematical abstraction level since Mathematics is the natural language for expressing abstractions. In this way, the resulting mathematical model is linked to the relevant information about the device.

Modeling methodology is generally accepted as an empirical science [24]. Implying that the model should be formulated starting from a hypothesis that is valid under certain constraints and assumptions. In practice, the model is validated through experiments; that is to say the real device is observed under various measurement conditions. In the end, the methodology should provide a reasonable correlation between the real object and model. This asseveration reveals the following modeling criterion:

When the observed behavior of the device and the behavior predicted are identical, then the correspondence between device and model is considered valid. [23]

Obviously the previous criterion assumes ideal conditions. In the real world, the prediction is done through the concept of accuracy that implies that the quality required by the model depends on the purpose of modeling. In [23] four stages to develop a device model are suggested as follows:

1. Define the model interface,
2. Determine a suitable model structure,
3. Determine the values of the model parameters, and
4. Determine the domain of validity of the model.

In the first stage, the form of interaction between the physics of the device and the model is determined. This is accomplished through a set of variables related to the behavior of the device that are cataloged as either dependent or independent. The variable classification is done according to the suitability of the model.

The target of the stage two is to obtain an appropriate mathematical formulation that relates the behavior of the device with the set of the variables proposed in stage one.

During stage three an appropriate method must be used in order to solve the mathematical formulation from the previous stage in terms of the device parameters. As a direct result, the quantitative

behavior of the device is obtained.

Obviously, it is impossible to represent the overall behavior of a device with a mathematical formulation. For that reason, in stage four the range of validity of the model domain is defined. Here, the operating ranges of the model are determined to have a functioning model.

2.3 Model Representations

As stated above, the least that one expects from a useful model is that it should reproduce the behavior of the device with sufficient accuracy for a region of operation. This is achieved in accordance with the stage when the information on the device is obtained.

2.3.1 A priori knowledge - based models

Generally speaking, models that are generated from an "a priori" knowledge are denoted as structural models because they resort to the internal physical structure of the device. As a consequence, the set up of equations that govern the functioning of the device are obtained [25]. In electronics, these models correspond to the study of solid state physics. The approach of these models occurs at many levels of abstraction depending on the detail that takes place within the internal structure of the device.

Physical models

These kinds of models are based on the fabrication process that has been used to built the device. This means that physical models resort to the information that is acquired during every fabrication step. At this level of abstraction, a logical consequence is that the construction of the model is steadily detailed [26]. In Semiconductor Physics, the information data that are used to describe the model are doping profiles, geometry structure and external contacts of the device.

The equations that governs the functioning of this description consists of a set of partial differential equations (i.e., Poisson's equation, or the current-continuity equation) that are valid for a variety of devices. There are in the market some examples of device simulators that uses this type of description, such as PISCES [27], ATLAS [28], among others.

The final goal of the modeling methodology is to determine the parameters of the device, which are obtained by solving the set of partial equations. The main deficiency lies in the resolution of the numerical integration methods used to solve them. Appropriate meshing techniques and step-size

control of the integration method are commonly used forms of speeding up the simulation procedure. However, a trade-off between execution times and resolution is usually applied in order to provide a good accuracy and insight of the internal perspective of the structure of the device.

Analytical models

Physical models have a reduced set of applications, in fact when a device is used within a circuit the previous level of abstraction is not suitable for determining the behavior of the whole circuit [1].

While device modeling is focused on electric field, electric charge as main variables, circuit modeling has voltage and current as interface variables, therefore another level of abstraction is needed in order to incorporate a device model to circuit-oriented applications. Hence, it is possible to define a higher level abstraction, which encompasses the development of the device structure in order to limit the total number of parameters of the device model. As a result, upon solving the basic equations of the physical model a reduced expression representing the device electrical behavior is obtained [29].

The structure of an analytic model consists of functional relationships between the device parameters and the interface variables at circuit-level. These relationships depend on the structural parameters, which are derived from the primary device parameters. The validity of the these depends on the assumptions made for its derivation at device-level. When, using a specific device within a circuit, the parameters of the device should be particularized according to the structure of the primary device.

2.3.2 A posteriori knowledge - based models

Models that are generated from an "a posteriori" knowledge are known as behavioral models because they focus on the observed behavior of the device under a specific set of stimuli [30,31]. The methodology for determining the properties of the device rest most of the times on a measurement procedure. This procedure consists in registering the observations of the device in a suitable storage form. It has a discrete nature due to there exists a single observation for a given measurement. As a result, a massive data must be stored for a sweep of observations. Furthermore, a mathematical treatment of this data must be carried out in order to determine the parameters of the device. This modeling technique conceives the device as a "black box" so the device structure becomes uncertain. However, its behavior is defined by extracting data information from observations. In the following, two mathe-

[1] The basic laws that are used to describe a circuit are Kirchhoff's laws. The resulting representation is not compatible with the level of abstraction of a physical device model.

matical techniques to obtain the model are explained.

Data-interpolation models

These kinds of models are described by tables containing the values of the interface variables of the device during a series of observations. The set of tables is a multidimensional representation of the electrical variables involved in the model [32,33]. The basic idea of this description is to use the tables to predict the device behavior between a pair of observations by resorting to interpolation methods such as polynomial interpolation, B-spline approximation, among others [34]. In Figure 2.1, an illustration of a data-interpolation model is shown. This model has two electric variable ($EV1$ and $EV2$) that represent another electric variable ($EV3$). The $EV1$ has 8 $j-$samples and their range of values is from 0 to 2.1 in steps of 0.3. Besides, the $EV2$ has 7 $i-$samples and their range of values is from 0 to 3 in steps of 0.5. In order to find a value of $EV3$ is necessary to provide values for each electric variable EV1 and EV2. For instance, given $EV1 = 1.3$ and $EV2 = 1.7$ the nearest table entries are selected. These values correspond to the measure samples of $i = [3,4]$ and $j = [4,5]$ see (shaded cells). With this selection, an interpolation method is used to define a function of EV3(EV1,EV2).

	i	0	1	2	3	4	5	6
j	EV1 \ EV2	0.0	0.5	1.0	1.5	2.0	2.5	3.0
0	0.0	###	###	###	###	###	###	###
1	0.3	###	###	###	###	###	###	###
2	0.6	###	###	###	###	###	###	###
3	0.9	###	###	###	###	###	###	###
4	1.2	###	###	###	###	###	###	###
5	1.5	###	###	###	###	###	###	###
6	1.8	###	###	###	###	###	###	###
7	2.1	###	###	###	###	###	###	###

Figure 2.1: An example of a two dimensional look-up table.

The simplicity of the methodology to develop models based on data-interpolation results in an easy implementation, less time-consuming parameter extraction and fewer errors. Furthermore, the accuracy of the model is established by the density of data and the interpolation method.

Storing the data of the model implies large size files, which results in a large amount of used memory. The quality of the predicted values lies in the interpolation technique according to the shape of the observed samples in a space of interface variables.

For circuit simulation applications, data-interpolation models are extremely time-consuming be-

cause the whole communication process between the simulator and the table arrays occurs for every iteration in the simulation task (see Figure 2.2).

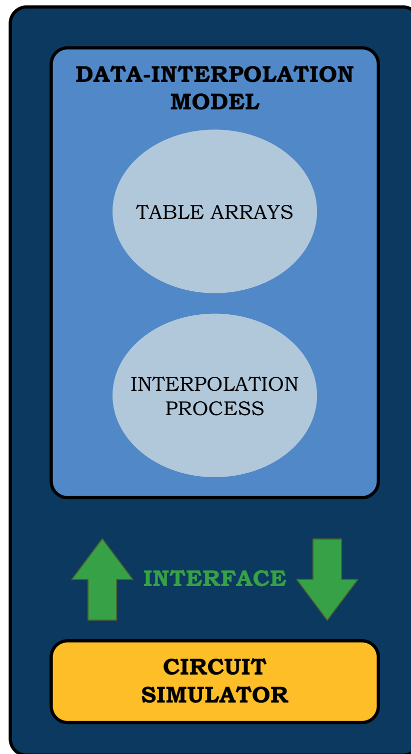


Figure 2.2: Communication process between the data-interpolation model and the circuit simulator.

Data-fitting models

In a repetitive way, the starting point for these kinds of models is the conformation of the tables. These contain values from observation series of the device interface variables. In contrast to the previous modeling technique, here we are interested in determining the mathematical function that fit all data of the observed samples in a space of interface variables.

Usually, curve-fitting models are expressed by an analytic function. However, because the device is treated as a "black box" where no information about the internal structure of the device is given.Then, it is advisable to use universal functions to define the model such as polynomial; piecewise linear; splines functions among others [35].

The accuracy of the model parameters is determined by the difference between the observed data and the evaluated function that models the behavior of the device, i.e. the numerical error of the fitting procedure. Since often the error is nonzero, a tolerance criterion must be defined by the user, but also it has to be associated with the model purpose. As a result, this criterion should be part of the model's hypothesis.

2.4 Single-electron based electronics

In traditional semiconductor devices, the electric current is considered a continuous flow because the large amount of electrons that these structures are capable of driving. Therefore, the discrete nature of the charge flow have been disregarded. However, as mentioned before, the trend has been oriented to shrink the device dimensions. In fact, nowadays it is possible to build structures around 10nm in research laboratories [36], which leads to the need of considering the charge flow in its discrete nature. Consequently, phenomena such as quantum tunneling, Coulomb Blockade, among others should be taking into account. A group of devices that are governed by the discrete nature of the electric charge flow is formed by the single-electronics devices.

The single-electron transistor is part of the family of single-electron based electronics. Therefore, in this section a brief historical review of the single-electronics is given, as well as, a description of the main phenomena involved.

2.4.1 History Review

In 1951, C. J. Gorter was researching granular thin-film metallic structures at low-temperature. He observed the abatement of the DC conductivity at low voltages [37]. He explains that phenomenon due to charging of grains with single electrons. He was the first person in observing the *Coulomb Blockade* phenomenon that is one of the essential pillars of single-electron based electronics.

After two decades without significant advances in single-electron based electronics, in 1969, Lambe and Jacklevic studied the charge quantization in tunnel capacitors [38]. During the same time, Zeller and Giaever developed the theory of Coulomb Blockade in tunnel junctions [39].

In the 80s, Averin and Likharev introduced the theory of the oscillation transfer [40–42] and the single-electron transistor operation [43, 44]. These contributions foretold the use of the single-electron transistor as a basic cell for developing logic cells and memories.

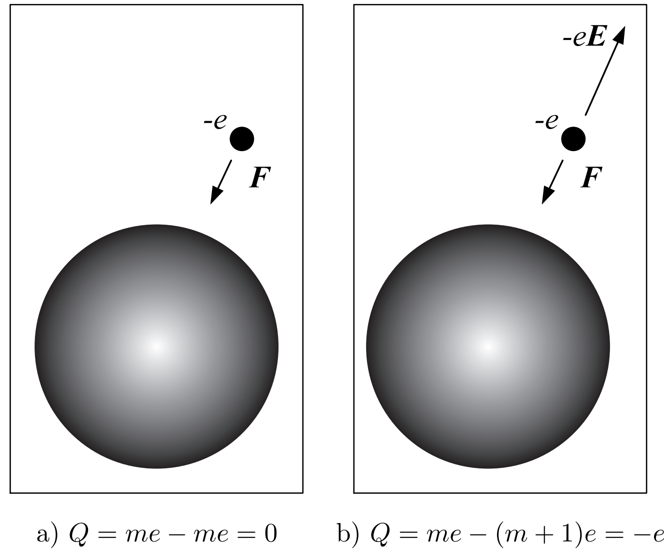
Nowadays, with the significant advances in lithography it is possible to build structures at a nanometric scale [45–47], which are appropriate to work with the devices that exhibit the aforementioned phenomena.

2.4.2 Physical Phenomena in Single-electron based Electronics

The basic operation of single-electronics is described by the quantum tunneling and the Coulomb Blockade phenomena. The first one refers to the possibility that has one particle to cross a potential barrier although this is greater than itself particle energy. The second one refers to the backscattering produced by an electric field over carriers trying to enter in a non-electroneutral system of small dimensions.

Coulomb Blockade

In order to explain the Coulomb Blockade phenomenon, a metallic sphere is considered as a simple structure to represent an electroneutral system. In other words, the system has the same number m of electrons and protons ($\Sigma Q = 0$). As a result, the electric field produced by them on the borders of the system is considered negligible. If an electric field is applied to the system, then it can catch one single electron from the exterior, leaving the system with a charge of $-e$. As a consequence, an electric field is formed in the system, and it rejects other electrons trying to enter into the system (see Figure 2.3).



a) $Q = me - me = 0$ b) $Q = me - (m+1)e = -e$

Figure 2.3: Metallic sphere; a) before and b) after to add one single electron in it. When having extra electrons in the sphere, then an electric field produced by them may reject other electrons trying to enter in this.

Single-electron tunneling

In order to explain the phenomenon of a single electron tunneling, we start with the idea of a metal conductor. This conductor has free electrons, which can be displaced by the influence of an electric field. Hence, the electron flow is considered continuous, and practically can take any value, usually as a multiple of the electron charge. This large number of electrons can be regarded as a cloud of

electrons moving through the metal in the same direction of the electric field.

If two conductors are placed together but separated by a tiny distance as shown in Figure 2.4, then a barrier to the cloud movement stops in front of the dielectric in the separation of the conductor edge. As long as more electrons are accumulated, the potential difference increases, until one electron crosses the barrier by the quantum tunneling process. Barriers exhibiting this phenomenon are known as tunnel junctions, and they are represented by a combination of capacitance and resistance (C_T and R_T, respectively) to express their leaky behavior.

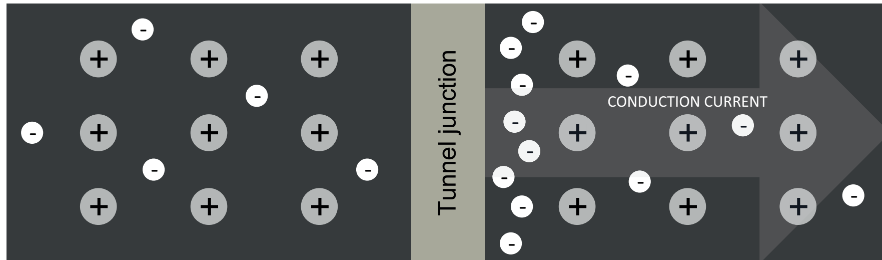


Figure 2.4: Accumulation of electrons in a metal adjacent to a tunnel junction.

It means that the flow of charge in the system has a continuous and discrete compound characteristic at the same time. The vacancy left by the absence of one electron relaxes the saturation of the other electrons in the cloud until a new electron has the possibility of crossing the barrier again, causing a repetitive process. K. Likharev [48] named this process as a "dripping tap" by analogy with a tap with small leak.

If the structure above is connected in series to a constant current source I. Then the frequency of the Coulomb Oscillation is $f = I/e$, where e is the electron charge (see Figure. 2.5).

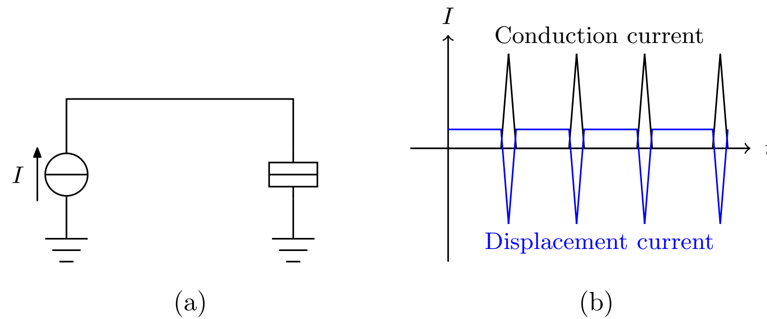


Figure 2.5: (a) Tunnel junction biased with a current source. (b) Coulomb Oscillations representation.

2.4.3 The Electron-Box

The electron-box is a structure that exhibits both phenomena, the quantum tunneling, and the Coulomb Blockade. This structure can be described in plain words as a tunnel junction placed near to a capacitor, as shown in Figure 2.6-a. The electrode in the middle is called the island.

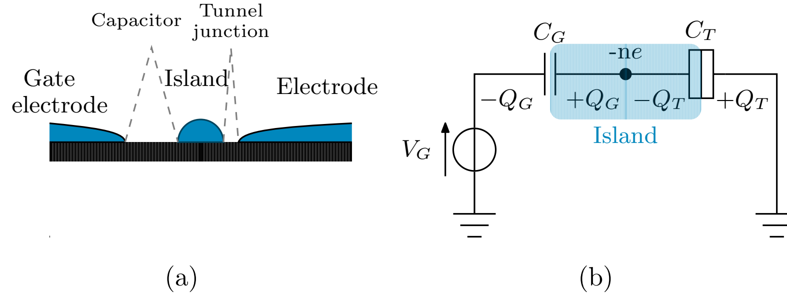


Figure 2.6: (a) Schematic of the electron-box. (b) Equivalent circuit of the electron-box structure.

In order to explain how an electron-box works, this structure is connected to a DC supply voltage V_G as shown in Figure 2.6-b. Assuming that the energy in the electron-box is provided only by the voltage source (neglecting other energies such as the thermal energy). Then the energy required to introduce one single electron into the island is $E_C = e^2/(2C)$ —this relation is known as the *Coulomb energy* or the *charging energy* [49]. In other words, from the energy expression given by $E = VQ$ –V is the potential difference, and Q is the charge, then a minimum voltage is required to allow an electron to tunnel namely the threshold voltage ($V_{th} = e/(2C)$). As the gate voltage increases, for each multiple of V_{th} a single charge enters into the island. Figure 2.7 shows the average charge $<n>$ versus the normalized gate voltage V_{G_n} with the shape of a staircase-like characteristic.

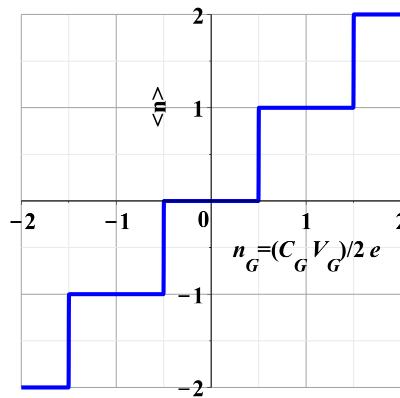


Figure 2.7: Ideal average charge $<n>$ versus normalized gate voltage.

This phenomenon is represented by the following Equation [50]:

$$< n > = \frac{\displaystyle\sum_{n=-\infty}^{n=+\infty} n \exp\left(\frac{-E_n}{k_B T}\right)}{\displaystyle\sum_{n=-\infty}^{n=+\infty} \exp\left(\frac{-E_n}{k_B T}\right)} \tag{2.1}$$

where T and k_B are the absolute temperature and Boltzmann's constant, respectively. Besides, E_n is the electrostatic energy of the whole electron-box circuit, which is expressed as:

$$E_n = \frac{\left[n(-e) + \tilde{Q}\right]^2}{2(C_G + C_T)} - \frac{\tilde{Q}^2}{2C_G} \tag{2.2}$$

where $\tilde{Q} = C_G U$ and where $-e$ denotes the electron charge [51].

In order to determine the non-ideal behavior of the electron-box, Equation 2.1 is evaluated for three values of the parameter $\theta = k_B T (C_G + C_T)/e^2 = 0.01$, 0.1 and 10, and the resulting Q_n–V_{G_n} plots are given in Figure 2.8 by the solid line, the dashed line and the dotted line, respectively.

For small θ, higher abruptness of the steps is obtained which is closer to the ideal behavior as $\theta \to 0$. Otherwise, a quasi-linear behavior is obtained, which is closer to the response of an RC-circuit when $\theta \to \infty$.

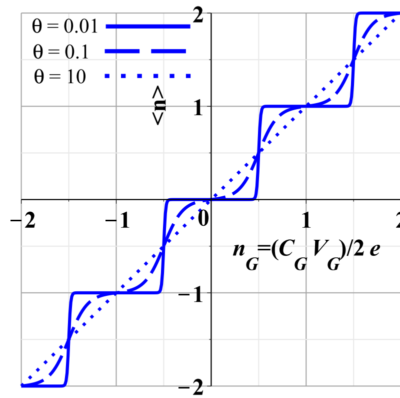


Figure 2.8: Average charge versus normalized gate voltage for several values of θ parameter.

2.4.4 Requirement for Coulomb Blockade

Two requirements are needed to have an appropriate control of the Coulomb Blockade:

REQUIREMENT ON TEMPERATURE

This requirement is related with the Coulomb energy E_C. And establishes that this must be greater than the thermal energy, which is expressed for $E_{thermal} = k_B T$, where k_B and T is the Boltzmann constant and absolute temperature, respectively.

$$E_C = \frac{e^2}{2C} \gg k_B T \tag{2.3}$$

Otherwise, thermal fluctuations will provide enough energy to the electron to pass the barrier and masking the quantization of the charge.

REQUIREMENT ON RESISTANCE

This requirement arises from the Heisenberg's uncertainty principle of the energy-time relationship [52, 53], which is expressed as

$$\Delta E \Delta t \geq \hbar \tag{2.4}$$

where ΔE is the uncertainty of the energy of an observed system, Δt is a certain time interval, and $\hbar$ is the reduced Planck constant.

In Figure 2.9 a system containing three electrodes coupled by tunnel junctions is shown. In the figure, the island electrode stores the electric charge. The typical time to allow the charge/discharge process of the island is given by [54]:

$$\Delta t = R_T C \tag{2.5}$$

where R_T is the tunnel resistance given by the tunnel junctions and C is the capacitance of the island.

Figure 2.9: A system with three electrodes coupled by tunnel junctions.

When a potential difference is applied to the island through a capacitor, then the energy levels of the island electrode are uniformly spaced with a separation of ΔE. As a result, this generates a self-capacitance C of the island [55], which is defined as

$$C = \frac{e^2}{\Delta E} \tag{2.6}$$

$$\therefore \Delta E = \frac{e^2}{C} \tag{2.7}$$

By substituting expressions 2.7 and 2.5 into the expression 2.4, one gets

$$\Delta E \Delta t \geq \hbar \quad = \quad \frac{e^2}{C} R_T C \geq \hbar$$

$$\therefore$$

$$R_T \geq \frac{\hbar}{e^2} = R_Q \cong 25k\Omega \tag{2.8}$$

The amount given by R_Q is known as the *quantum resistance*. This should not be understood as an exact limit, but rather as an attempt to define the order of magnitude. In an individual tunnel junction, if the tunneling resistance is less than the quantum resistance, then the charge is not quantized causing a vanishing of the Coulomb Blockade. Therefore, for practical Coulomb Blockade applications, $R_T \gg R_Q$.

2.4.5 Size-temperature compromise

In order to achieve the first aforementioned requirement for the single-electron transport, two options are available. On one hand, it is keeping the device at very low temperatures. On the other hand, it is to build single-electron structures on a nanometric scale. The last option also provides the theoretical possibility to work at room temperature, which is highly desired in common circuits.

In Figure 2.10 an illustration of a system composed of a metal sphere and one electron is shown. The figure shows that the necessary energy to charge the metal sphere with a single electron is given by $E_C = e^2/(2C)$. Based on this relation, in Table 2.1 a quantitative representation of the variables of the system is given. The capacitance is computed for a sphere by using $C = 4\pi\varepsilon_0 R$, where ε_0 is the vacuum permittivity, and R is the radius. According to the table, only having a sphere with a ratio of 10nm is possible to reach an energy charging sufficient to work at environment temperature. Otherwise, it is required a cooling system in order to reach an appropriate charging energy.

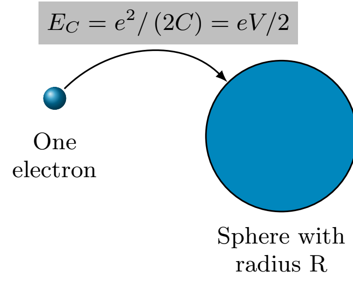


Figure 2.10: Charging energy required to add one electron into a metal sphere.

Radius	Capacitance	Temperature (E/k_B)	E
10μm	1.1×10^{-15}F	0.84K (^{3}He)	70μeV
1μm	1.1×10^{-16}F	8.4K (LHe)	0.7meV
0.1μm	1.1×10^{-17}F	84K (LN_2)	7meV
0.01μm	1.1×10^{-18}F	840K (>RT)	70meV

Table 2.1: Size-temperature quantitative relationships for the system shows in Figure 2.10.

2.5 The Single-Electron Transistor

The schematic of a single-electron transistor is depicted in Figure 2.11. This structure is composed of two tunnel junctions in series; the union between them is called the island. The island is connected to the gate node by a capacitor (C_G). As mentioned before, each tunnel junction is represented by a combination of capacitance and resistance (C_T *and* R_T) in order to express a leaky capacitor.

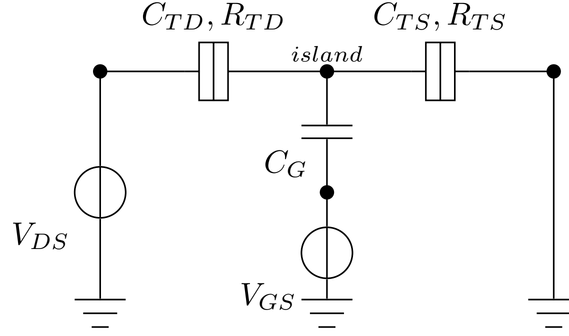


Figure 2.11: Schematic of a SET transistor with its main parameters.

By means of the energy exchange, the carrier transport in a SET can be explained. The initial energy (before a tunnel event) is expressed by:

$$E_B = \frac{Q^2}{2C_\Sigma} \tag{2.9}$$

When after a tunnel event takes place (by adding one electron into the island), then the energy in the circuit changes as follows:

$$E_A = \frac{(Q-e)^2}{2C_\Sigma} \tag{2.10}$$

It is considered that one single electron crosses a tunnel barrier only if the total energy of the system decreases, hence

$$\begin{aligned} E_B - E_A &= \frac{e(Q-e/2)}{2C_\Sigma} > 0 \\ &\therefore \quad Q > e/2 \end{aligned} \tag{2.11}$$

Keeping in mind that $Q = C_\Sigma |V|$, where $|V|$ is the voltage drop across the tunnel junction, then we can infer that one single electron is able to cross it only when

$$|V| > \frac{e}{2C_\Sigma} \tag{2.12}$$

which is another way to look at the Coulomb Blockade phenomenon.

In order to simplify the carrier transport in a SET, the circuit configuration shown in Figure 2.11 is used. Then, the voltage in the island is expressed as

$$V_{island} = \frac{C_G}{C_\Sigma} V_G + \frac{C_{TD}}{C_\Sigma} V_D \tag{2.13}$$

where

$$C_\Sigma = C_{TS} + C_{TD} + C_G \tag{2.14}$$

From Equation 2.12 we know that one electron can tunnel only if $|V_{island}| > e/\left(2C_\Sigma\right)$ (through the source tunnel barrier) or if $|V_D - V_{island}| > e/2C_\Sigma$ (through the drain tunnel barrier). Considering that the system keeps the $V_D = e/\left(2C_\Sigma\right)$ and varying V_{GS} from zero to higher positive value, then V_{island} increase from $eC_{TD}/\left(2C_\Sigma^2\right)$ to higher positive values linearly with V_{GS}. It is important to mention that $C_\Sigma = 2C_{TD}$ to hold the voltage symmetry. Under these considerations, the carrier transport in a single-electron transistor is described as follows:

A) When $V_{island} < e/\left(2C_\Sigma\right)$, the voltage difference between the terminals of each junctions is smaller than $e/2C_\Sigma$. Therefore the SET is in Coulomb Blockade state. (see Figure 2.12-A).

B) If we start increasing the value of V_{GS} until the $V_{island} \approx e/\left(2C_\Sigma\right)$, one single electron can tunnel through the source junction (see Figure 2.12-B-1). As a consequence, the potential at the island drops in amount of e/C_Σ. Hence, the voltage difference in the drain junction becomes higher than $e/\left(2C_\Sigma\right)$ and then one single electron can tunnel through it (see Figure 2.12-B-2). After that, the potential in the island is restored and the process is repeated. As a result, a continuous flow of charge from the source to drain terminals is established.

C) Increasing the gate-to-source voltage until $V_{island} > e/(2C_\Sigma)$, then the SET enters again in Coulomb Blockade state. This is because the voltage in the source junction establishes that one electron can tunnel (see Figure 2.12-C-1). Therefore, the voltage in the other junction is reduced, avoiding the conduction in this part. (see Figure 2.12-C-2).

D) The conduction in the SET starts again for $V_{island} \geq 3e/\left(2C_\Sigma\right)$. From the tunnel voltage condition, two electrons can tunnel through the source junction (see Figure 2.12-D-1). After that, the voltage in the drain junction becomes higher than $e/\left(2C_\Sigma\right)$, then one single electron can tunnel through it (see Figure 2.12-D-2). After that, the V_{island} decreases by an amount of e/C_Σ causing the tunnel condition in the source junction. Therefore, one electron can tunnel through it. As a result, a continuous current path from source to the drain is established. It is noteworthy that the normal state of the island (for this case) is to contain one extra electron.

As a result of above discussion, if we have a constant drain voltage then the Coulomb Blockade state in the SET has a periodic behavior respect to the gate voltage (e/C_G). Also, we can infer for $|V_{DS}| > e/C_G$ the Coulomb Blockade state disappears for any value of V_{GS}. In this transport mechanism, we assume that the temperature must accomplish the next condition: $T << E^2/(k_B C_\Sigma)$. Otherwise, the electrons can tunnel via environment thermal energy, inclusive if the voltage drop across of the junction is lower than $e/\left(2C_\Sigma\right)$.

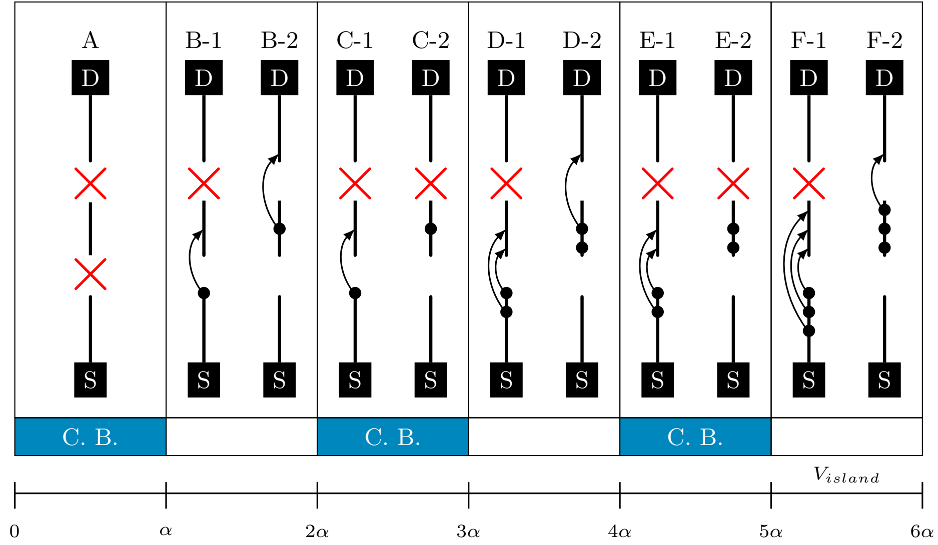


Figure 2.12: Illustration of carrier transport in a SET.

In Table 2.2 a numerical representation of the phases between conduction and Coulomb Blockade states in a SET is shown. In the table, the relation $\alpha = e/\left(2C_\Sigma\right)$ is introduced to simplify the writing. The column V_{DI} represent the drain-to-island voltage while the column V_{IS} represent the island-to-source voltage. Also, the colored rows refer to a Coulomb Blockade state.

		V_{DI}	V_{IS}
A)	C.B.	$< \alpha$	$< \alpha$
B-1)	1 T.S.	$< \alpha$	$\sim 1.5\alpha \Rightarrow 1.5\alpha - 2\alpha = -0.5\alpha$
B-2)	1 T.D.	$\alpha - (-0.5\alpha) = 1.5\alpha$	
C-1)	1 T.S.	$< \alpha$	$\sim 2.5\alpha \Rightarrow 2.5\alpha - 2\alpha = 0.5\alpha$
C-2)	C.B.	$\alpha - (0.5\alpha) = 0.5\alpha$	
D-1)	2 T.S.	$< \alpha$	$\sim 3.5\alpha \Rightarrow 3.5\alpha - 2\alpha = 1.5\alpha$ $\Rightarrow 1.5\alpha - 2\alpha = -0.5\alpha$
D-2)	1 T.D.	$\alpha - (-0.5\alpha) = 1.5\alpha$	
E-1)	2 T.S.	$< \alpha$	$\sim 4.5\alpha \Rightarrow 4.5\alpha - 2\alpha = 2.5\alpha$ $\Rightarrow 2.5\alpha - 2\alpha = 0.5\alpha$
E-2)	C.B.	$\alpha - (0.5\alpha) = 0.5\alpha$	
F-1)	3 T.S.	$< \alpha$	$\sim 5.5\alpha \Rightarrow 5.5\alpha - 2\alpha = 3.5\alpha$ $\Rightarrow 3.5\alpha - 2\alpha = 1.5\alpha$ $\Rightarrow 1.5\alpha - 2\alpha = -0.5\alpha$
F-2)	1 T.D.	$\alpha - (-0.5\alpha) = 1.5\alpha$	

Table 2.2: Numerical representation between conduction and Coulomb Blockade states in a SET. Colored row represent a Coulomb Blockade state.

2.5.1 Stability diagram for the SET

The representation of the free energy (or Gibbs free energy [56]) in a system at constant temperature and pressure can be mathematically formulated by:

$$G = E + PU - TS \tag{2.15}$$

where E, P, U, T and S are energy, pressure, volume, temperature, and entropy of the system respectively. Since the free energy changes when one electron tunnels, then it is possible to reformulate the last equation for single-electron devices as follows:

$$G = E - Q_G V_G \qquad \text{(for a single-box)} \tag{2.16}$$

$$G = E - QV_{DS} \qquad \text{(for a tunnel junction)} \tag{2.17}$$

$$G = E - Q_D V_{DS} - Q_G V_{GS} \qquad \text{(for a SET with a single gate)} \tag{2.18}$$

In the last equations, E represents the charging energy, whereas Q_G and Q_D represent the charge of the gate capacitance and the drain junction capacitance, respectively. When any change occurs in the Gibbs free energy, then it can be expressed as follows:

$$\Delta G = G_f - G_i \tag{2.19}$$

where G_f and G_i are the Gibbs free energy after and before a tunnel event takes place, respectively. It occurs when ΔG is negative at absolute zero of temperature.

If we consider the setup configuration of the SET shown in Figure 2.11, where the source is connected to the ground. While the drain and the gate terminals are connected to two voltage sources (V_{DS} and V_{GS}, respectively), then, before any electron tunnels, the next expressions can be formulated:

$$V_{DS} = \frac{Q_S}{C_{TS}} + \frac{Q_D}{C_{TD}} \tag{2.20}$$

$$V_{GS} = \frac{Q_S}{C_{TS}} + \frac{Q_G}{C_{TD}} \tag{2.21}$$

$$Q_0 = Q_S - Q_D - Q_G \tag{2.22}$$

where Q_S, Q_D and Q_G represent the charge in the source, the drain, and the gate terminals, respectively. On the other hand, Q_0 represents the charge in the island. By solving equations 2.20 to 2.22 we get

$$Q_D = \frac{C_{TD}\left(-Q_0 + C_{TS}V_{DS} + C_G\left(V_{DS} - V_{GS}\right)\right)}{C_\Sigma} \tag{2.23}$$

$$Q_S = \frac{C_{TS}\left(Q_0 + C_{TD}V_{DS} + C_G V_{GS}\right)}{C_\Sigma} \tag{2.24}$$

$$Q_G = \frac{C_G\left(-Q_0 + C_{TS}V_{GS} + C_{TD}\left(V_{GS} - V_{DS}\right)\right)}{C_\Sigma} \tag{2.25}$$

Finally, the whole electrostatic energy can be calculated as

$$E = \frac{Q_D^2}{2C_{TD}} + \frac{Q_S^2}{2C_{TS}} + \frac{Q_G^2}{2C_G} \tag{2.26}$$

When a tunnel event takes place in the SET, then the Q_0 also changes. In consequence E, Q_D, Q_G and G also change. The tunnel event in a SET is possible in two ways. On one hand, the tunnel event can happen from the source terminal to the island or vice-versa (see first column of Table 2.3). On the other hand, the tunnel event can occur from island to the drain terminal or vice-versa (see second column of table 2.3).

Change of Q_0 from $-ne$ to $-(n+1)\,e$	Change of Q_0 from $-ne$ to $-(n-1)\,e$
$\Delta E = \frac{(n+1)^2 e^2 - n^2 e^2}{2C_\Sigma} = \frac{(2n+1)\,e^2}{2C_\Sigma}$ (2.27)	$\Delta E = \frac{(n-1)^2 e^2 - n^2 e^2}{2C_\Sigma} = \frac{(2n-1)\,e^2}{2C_\Sigma}$ (2.28)
$\Delta Q_D = \frac{C_{TD}\,((n+1)\,e - ne)}{C_\Sigma} = \frac{eC_{TD}}{C_\Sigma}$ (2.29)	$\Delta Q_D = \frac{C_{TD}\,((n-1)\,e - ne)}{C_\Sigma} + e = \frac{e\,(C_{TS}+C_G)}{C_\Sigma}$ (2.30)
$\Delta Q_G = \frac{C_G\,((n+1)\,e - ne)}{C_\Sigma} = \frac{eC_G}{C_\Sigma}$ (2.31)	$\Delta Q_G = \frac{C_G\,((n+1)\,e - ne)}{C_\Sigma} = \frac{eC_G}{C_\Sigma}$ (2.32)
$\Delta G = \Delta E - \Delta Q_D V_{DS} - \Delta Q_G V_{GS}$ (2.33)	
$\Delta G\|_{S\to I} = \frac{(2n+1)\,e^2}{2C_\Sigma} - \frac{eC_{TD}}{C_\Sigma}V_{DS} - \frac{eC_G}{C_\Sigma}V_{GS} < 0$ (2.34) $= \frac{C_{TD}}{C_\Sigma}V_{DS} + \frac{C_G}{C_\Sigma}V_{GS} - \frac{(2n+1)\,e}{2C_\Sigma} > 0$ (2.35)	$\Delta G\|_{I\to D} = -\frac{(2n-1)\,e^2}{2C_\Sigma} - \frac{e\,(C_{TS}+C_G)}{C_\Sigma}V_{DS} + \frac{eC_G}{C_\Sigma}V_{GS} < 0$ (2.36) $= \frac{(C_{TS}+C_G)}{C_\Sigma}V_{DS} - \frac{C_G}{C_\Sigma}V_{GS} + \frac{(2n-1)\,e}{2C_\Sigma} > 0$ (2.37)
$\Delta G\|_{I\to S} = -\frac{(2n-1)\,e^2}{2C_\Sigma} + \frac{eC_{TD}}{C_\Sigma}V_{DS} + \frac{eC_G}{C_\Sigma}V_{GS} < 0$ (2.38) $= -\frac{C_{TD}}{C_\Sigma}V_{DS} - \frac{C_G}{C_\Sigma}V_{GS} + \frac{(2n-1)\,e}{2C_\Sigma} > 0$ (2.39)	$\Delta G\|_{D\to I} = \frac{(2n+1)\,e^2}{2C_\Sigma} + \frac{e\,(C_{TS}+C_G)}{C_\Sigma}V_{DS} - \frac{eC_G}{C_\Sigma}V_{GS} < 0$ (2.40) $= -\frac{(C_{TS}+C_G)}{C_\Sigma}V_{DS} + \frac{C_G}{C_\Sigma}V_{GS} - \frac{(2n+1)\,e}{2C_\Sigma} > 0$ (2.41)

Table 2.3: Gibbs free energy calculation when one electron tunnels from source terminal to the island and viceversa –see left column, and also when one electron tunnels from the island to the drain terminal and viceversa –see right column.

In Table 2.3 the conditions for different electron tunneling in a SET is given. Using the table, a graphical illustration of Equation 2.40, 2.41, 2.40, and 2.41 are plotted in Figure 2.13 for $n = 0$. This kind of plot is known as stability diagram, and it is useful to observe the regions where the operation is stable (shaded regions).

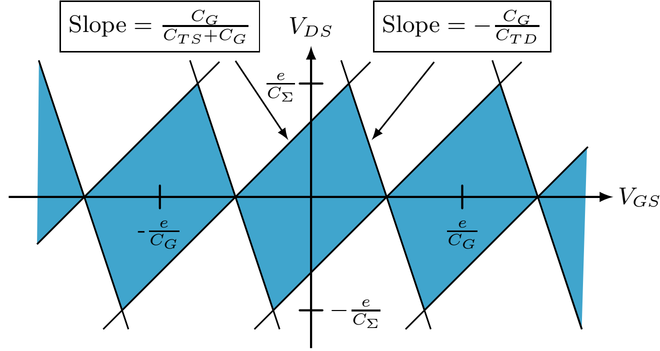


Figure 2.13: Stability diagram of the SET.

2.5.2 Characteristic curves of the SET

At zero temperature, the $I_D - V_{DS}$ characteristic curve is shown in the left of Figure 2.14 for a symmetric device where $C_{TD} = C_{TS}$ and $R_{TD} = R_{TS}$ at $V_{GS} = 0$. In the left of the figure, it is possible to observe that having values of $|V_{DS}| < e/C_\Sigma$ the current is suppressed. This fact is due to the *Coulomb Blockade* and it is present in low voltage. This behavior is due to the charging energy that has opened a gap in the available chemical potentials. The only way to have a current flow is to overcome the threshold voltage established by the charging energy. Beyond that value, the junction acts like a resistor. If one electron that enters to the island using the source junction, then one electron leaves the island via drain junction. This phenomenon is known as *correlated tunneling of electrons.*

On the other hand, for an asymmetric device where $R_{TD} << R_{TS}$, the $I_D - V_{DS}$ characteristic curve is shown in the right of Figure 2.14. Some electrons entering the island via source junction will be retained by the high resistance until one single electron tunnels via the drain current. As a result, most of the time there will be an electron overpopulation in the island. Hence, the $I - V_{DS}$ curve denotes a staircase-like characteristics, usually named as *Coulomb staircase*. Otherwise, when the asymmetry is reversed (that means that $R_{TD} >> R_{TS}$) the island gets more depleted.

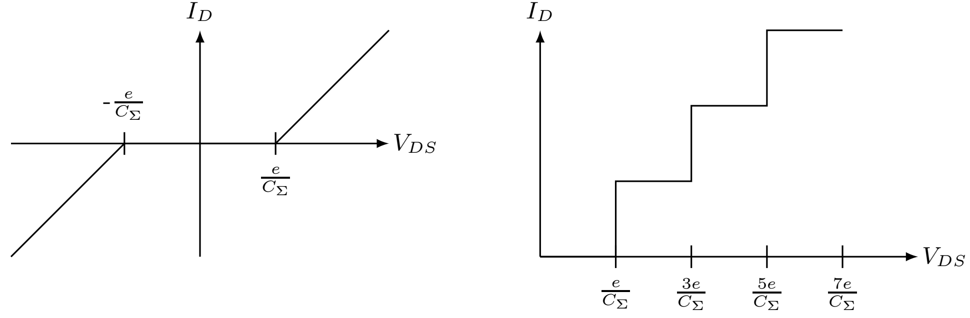


Figure 2.14: $I_D - V_{DS}$ characteristic curves of the Single-electron transistor. Left: Symmetric device. Right: Asymmetric device.

The $I_D - V_{GS}$ characteristic curve of the SET at low voltage and low temperature is shown in Figure 2.15. The curve looks like a set of deltas whose width depends on temperature and the size of the island. Also, the current exhibits a periodic behavior with a frequency of e/C_G. This plot is equivalent to a cut along the x-axis through the stability plot shown in Figure 2.13. In stable regions, where the correlated tunneling occurs, the current peaks take a value of $V_{DS}/\left(\sqrt{R_{TS}} + \sqrt{R_{TD}}\right)^2$. When increasing the drain-to-source voltage at finite temperature, the some electrons can overcome the charging energy for intermediate values of V_{GS} between the peaks. As a result, a conductance is presented into Blockade regions. Besides, the Coulomb Blockade phenomenon begins to disappear when the temperature is increased. When $k_B T \sim e^2/C_\Sigma$ this phenomenon is vanished.

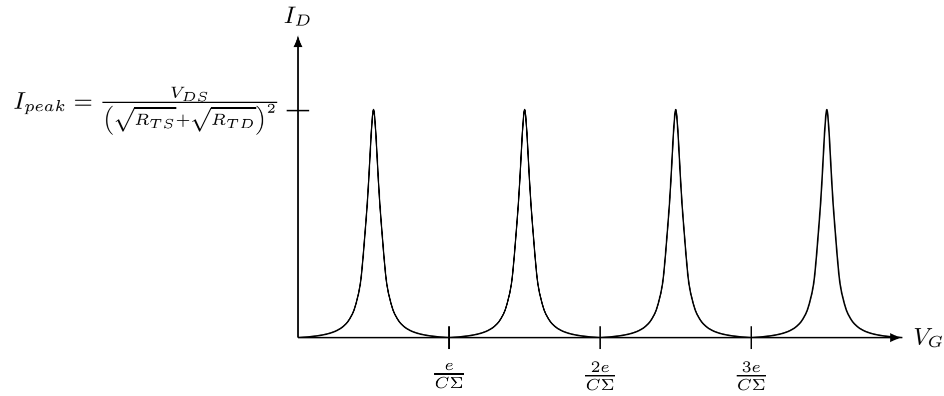


Figure 2.15: $I_D - V_{GS}$ characteristic curve of the SET. When $|V_{DS}| < e/C_\Sigma$, the I_{peak} is defined by the junction resistance and the drain-to-source voltage.

3 Modeling the Single-Electron Transistor

In this chapter, the proposed methodology for modeling the single-electron transistor is presented. Hold together with the modeling methodology, a complete simulation scheme is also introduced. As a result, behavioral models of the single-electron transistor that can be used for circuit simulation are generated.

Two models are developed: a first-order model that contains a reduced number of parameters and is easy to evaluate, and a second-order model that has a larger set of parameters and yields a more complex mathematical expression.

This chapter is organized as follows: in Section 1 a glimpse on the main existing simulation approaches for the single-electron transistor are presented, Section 2 the modeling methodology is explained, Section 3 introduces both models.

3.1 Common approaches for SET Simulation

The simulation of the single-electron transistor has been tackled by using several approaches, the most commonly used are:

1. Monte Carlo (MC)
2. Master equation (ME)
3. Circuit Macromodeling (CM)

Monte Carlo Analysis

Monte Carlo techniques are focused on analyzing processes where probabilistic play an important role. In the transport mechanism of the single-electron transistor, the analysis of the probability of tunneling events is best suited for this technique. Its operation is based on considering all possible

tunnel events, to which a certain probability of occurrence is assigned, and then randomly choose one of these. This choice is made on multiple occasions in order to describe the transport of electrons. Therefore, the core part of Monte Carlo based simulators is a random number generator. As a result, this approach yields high accuracy for describing system based on tunnel junctions. In fact, this approach is applicable for all single-electronics structures.

However, this approach shows several shortcomings. First, it constitutes a slow process for arrays containing a large number of single-electronics structures. Secondly, it does not allow the simulation of hybrid circuits that contain single-electron devices and traditional MOS devices.

Some simulators that use this approach are: SIMON [57], MOSES [58], KOSEC [59] and SENECA [60].

Master Equation approach

The Master Equation is a mathematical expression obtained from describing the Markov process [61] for the tunneling of an electron moving from one island to another one. The array of single-electronics structures can be regarded in fact as an electric circuit that can be defined by a set of states. The circuit is excited by external voltage sources that represent the states. With the purpose of solving the Master Equation, a finite number of states must be defined. There are two ways to do this; the first one is to solve the equation for the probability density function. The second way implies to simulate the stochastic process taking into account that one or more particles jump from a state to another state in accordance with the transition probabilities. By using an adequate set of samples, an analytical representation can be obtained.

The accuracy of this approach depends on the number of states described within the Markov process. The number of required states also grows with the number of single-electronics structures, which represent a serious drawback when attempting to simulate large arrays.

This approach allows simulation of hybrid circuits because the single-electron devices are represented by a mathematical equation that can be incorporated via a functional model.

A simulator developed with this technique is SETTRANS [62].

Circuit Macromodeling

The essence of this approach is to represent the electrical characteristics of the single-electron transistor using an equivalent circuit. Therefore, the inclusion of a macromodel developed under this concept would be done directly in a conventional integrated circuit simulator, saving the construction of the work platform –the simulation software used for IC. Hence, the cosimulation with MOSFET devices and other structures would be allowed.

However, the main disadvantage of developing this kind of macromodel is the empirical nature of its creation, which results in serious problems of adaptability to changes in the values of the SET parameters.

One of the most popular macromodels of the SET was proposed by Yu, and it is shown in Figure 3.1.

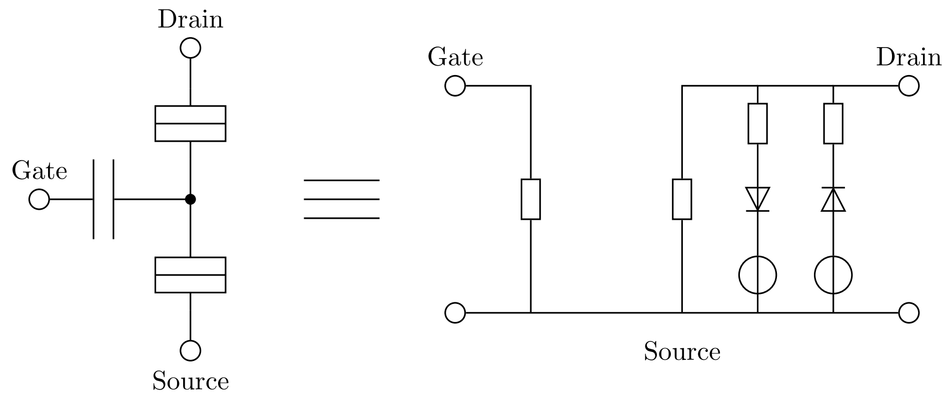


Figure 3.1: Macromodel proposed by Yu.

In summary, although the Monte Carlo method is the best approach to describe the behavior of the SET, it has two major disadvantages. The first one is that it does not allow the simulations with MOSFET devices, and the second one is that for large-scale circuit is impractical. On the other hand, the ME approach results in an equation that can be included in a conventional integrated circuit simulator by a behavioral description. It is noteworthy that the complexity of the master equation increases with the number of states considered, which means that a better approximation of the transistor behavior is achieved considering a more complex equation. An equivalent circuit of SET using typical elements in a simulator looks like a good method. However, its empirical basis results in problems of scalability and accuracy.

The simulation methodology proposed in this dissertation comes from a different perspective. It takes the advantage of the great accuracy obtained by a device-level simulator (MC approach) in

order to generate the electric characteristics of the SET. Then, these are expressed by a mathematical equation that best fits the initial simulation data. Subsequently, the resulting math equation is coded in a behavioral model with the aim to be used in an SPICE-like simulator.

3.2 Proposed Methodology for Hybrid Simulation

The approach used in this thesis can be summarized in the flowchart shown in Figure 3.2. In the figure, there are three stages. In the first one, the model of the SET is developed. The next one uses the resulting SET functional model from the previous stage in order to be implemented as a user-defined model in an SPICE-like simulator. Finally, this behavioral model can be used as a sub-circuit module into the circuit description. We will now examine each one of these three stages in more detail.

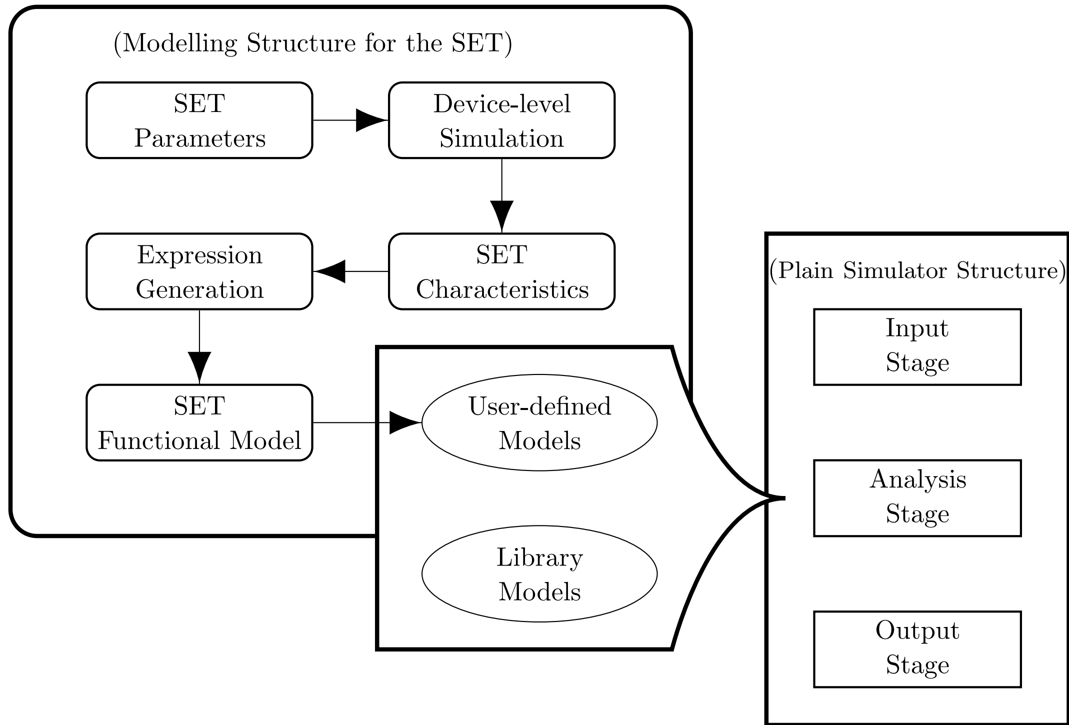


Figure 3.2: Modeling methodology for the simulation of hybrid circuits.

3.3 Modeling methodology for the SET

The idea in this part of the thesis is to show the development of the SET model. It begins by defining the type and range of variables involving the transistor. After that, several device-level simulations of the SET are done in order to get the electrical behavior. Specifically, the characteristics of the drain current as a function of the selected variables are obtained. From the data collected, and the shape shown, a mathematical expression is chosen. This expression has as its core a sinusoidal function due to the periodic behavior of the SET. The simulation data are treated with a curve fitting technique

in order to find the parameters of the mathematical expression. Consequently, a functional model of a transistor suitable for incorporation into the next stage is achieved. A brief description of each step of this process is given as follows.

3.3.1 SET variables

At this stage of the methodology, the variables must be defined and selected. For the case of the single-electron transistor, usually it is described by four sets of variables that are electric, design, process, and temperature (see Figure 3.3).

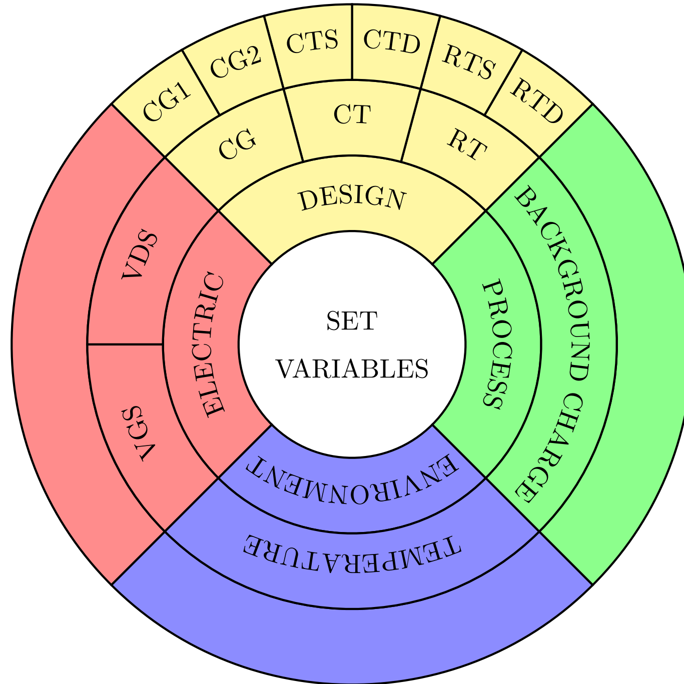


Figure 3.3: SET variables.

The electric variables group is subdivided into drain-source and gate-source voltages (V_{DS} and V_{GS} respectively) which correspond to the voltage biasing of the SET.

In the case of the group of design variables, it can be divided into gate capacitance (C_G), source tunnel junction capacitance and resistance (C_{TS} and R_{TS}) and drain tunnel junction capacitance and resistance (C_{TD} and R_{TD}). The simplest SET structure has one gate capacitance, but also many gates could be coupled to the island (C_{G1}, C_{G2}, ..., C_{GN}).

The process variable considered in this thesis is the random background charge. This variable represents some unwanted charge that is located nearby to the SET.

Finally, the only environment variable is the temperature, which is directly related to the Coulomb phenomenon.

In this part of the methodology, the validity of the model is defined. In other words, the model should be defined according to the variables selected as well as the range of operation.

3.3.2 Device-level simulation

Using SIMON software, which is a device-level simulator, the schematic of the SET transistor (see Figure 2.11) is simulated. As previously mentioned, SIMON uses a Monte Carlo approach, therefore it provides greater accuracy in simulation results.

In this stage, the SET transistor is simulated by using the set of variables with their respective range of operation from the last stage. In Figure 3.4 a screenshot of the graphical user interface of SIMON software is shown.

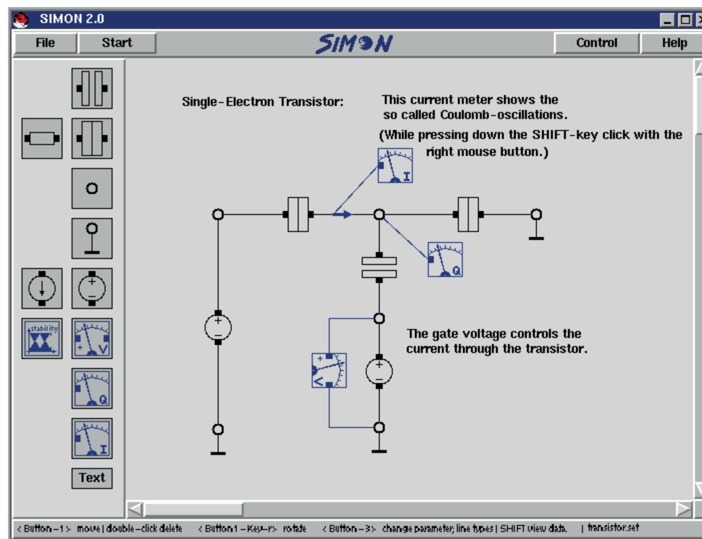


Figure 3.4: Screenshot of SIMON simulator.

Although SIMON software offers simulations with high accuracy for circuits that contain tunnel junctions, it has three main disadvantages. First, it works with a reduced closed-set of elements. Secondly, it has a symbolic nature. And finally, as previously discussed, the use of a Monte Carlo technique makes it a slow process. For these reasons, SIMON software is not suitable for simulating hybrid and large circuits.

Given that a large number of simulations must be carried out on the same structure. And knowing

the symbolic limitation of SIMON, a front-end tool has been developed as a part of this dissertation by using a computer lab: MAPLE [63] (see Figure 3.5). This tool can create a netlist that can be used in linear or logarithmic sweeps over some variables available in the SIMON software.

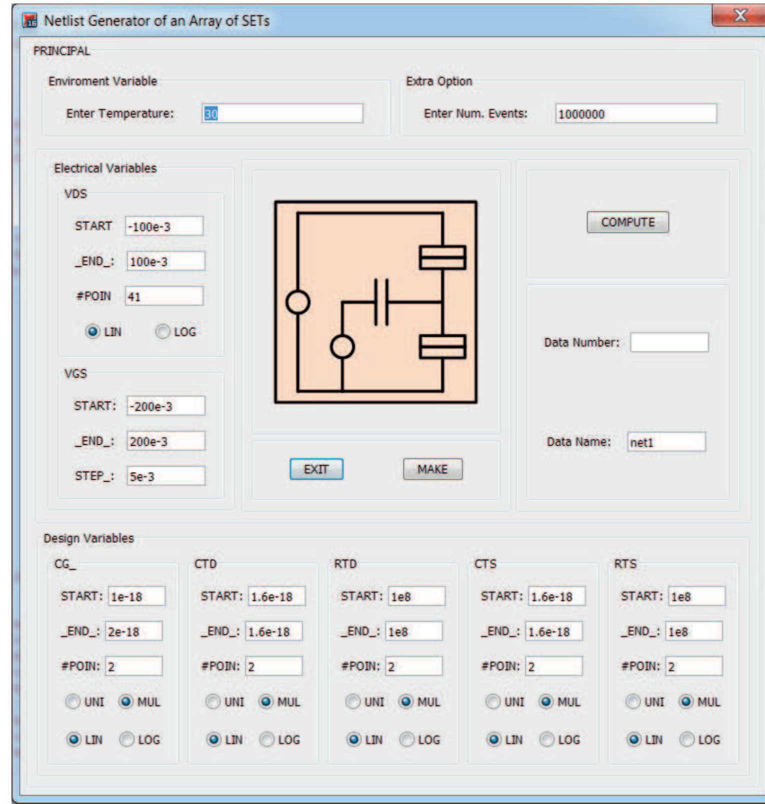
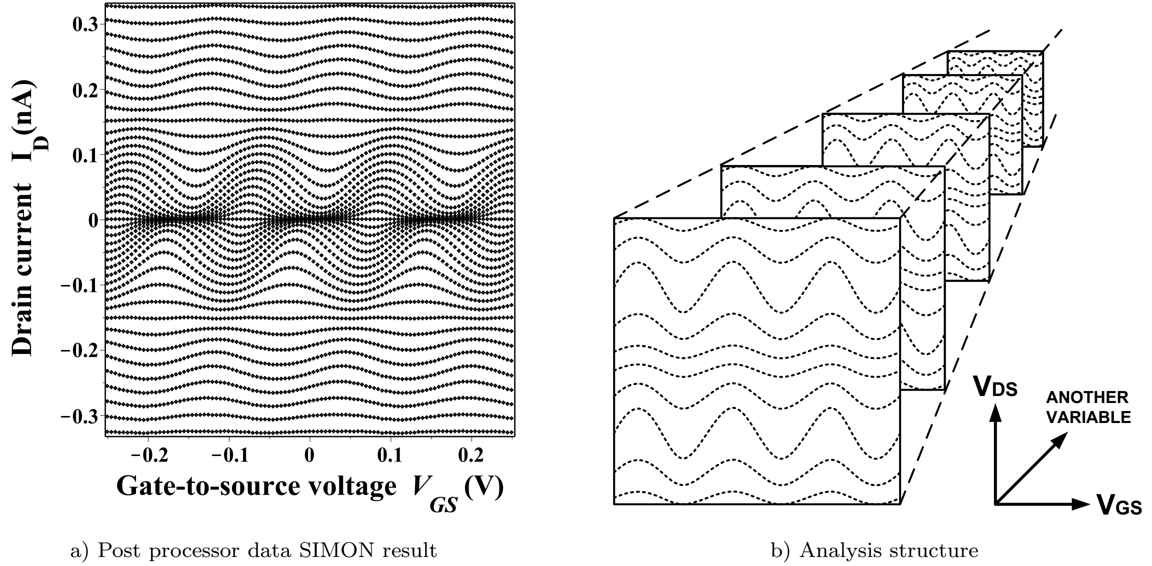


Figure 3.5: Tool to sweep variables of the SET.

3.3.3 SET characteristics

From the previous stage, several $I - V$ curves for the SET were obtained. These curves represent the electric behavior of the SET as shown in Figure 3.6 (a). In the figure, it is possible to see a family of curves of $I_{DS} - V_{GS}$ for several values of V_{DS}. An illustration that indicates how to embed another variable into the model is shown in Figure 3.6 (b) (for instance, the gate capacitance — C_G).



a) Post processor data SIMON result

b) Analysis structure

Figure 3.6: (a) Drain current as a function of gate voltage for several drain voltages. (b) An extended analysis illustrates adding another variable.

3.3.4 Expression generator

In this stage of the modeling methodology, a suitable mathematical expression must be generated in order to represent the electric behavior from the previous stage. It is done according to the obtained I-V plot shapes.

As the drain current is the main electric variable to represent the electric behavior of any transistor, the mathematical formulation must express the drain current as a function of the biasing voltage. For the case of a SET, there are two options to generate a mathematical expression. The first option is taking the relation of drain current as a function of the drain-to-source voltage,$I_D - V_{DS}$, as shown in Figure 3.7-a. The second option is taking the relation of drain current as a function of the gate-to-source voltage, $I_D - V_{GS}$, as shown in Figure 3.7-b.

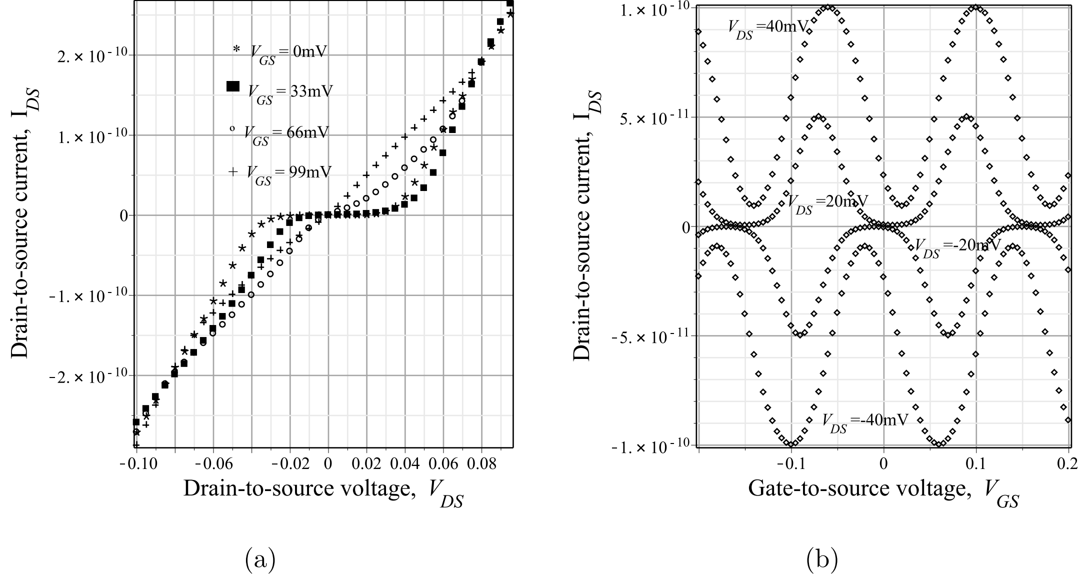


Figure 3.7: I-V relationship. (a) $I_D - V_{DS}$ and (b) $I_D - V_{GS}$ characteristic of a single-gate SET at a temperature $T = 30$K. The device parameters used for simulations are $C_G = 1\times10^{-18}$F, $C_{TD} = C_{TS} = 1\times10^{-18}$F and $R_{TD} = R_{TS} = 1\times10^{8}\Omega$.

This dissertation works formulating a mathematical expression based on the $I_D - V_{GS}$ relationship because it has several advantages over the $I_D - V_{DS}$. For instance, the $I_D - V_{GS}$ there is no overlap between adjacent curves. Besides, the same family of curves exhibits a periodic behavior, which may be treated by using a periodic function. Both characteristics are shown in Figure 3.7-b.

The final result in this stage is to develop a behavioral model that expresses the drain current, I_D, in the following way:

$$I_D = f(\text{SET variables}) \tag{3.1}$$

where *SET variables* refer to the variables involved in the model.

3.3.5 SET Functional Model

In order to allow the cosimulation with the MOSFET, a behavioral language (Verilog-A) is used. The Verilog-A hardware description language (HDL) is a behavioral language widely used to incorporate user-defined models into the conventional design flow. In this thesis, the equation resulting from the previous stage is coded in this language as a module as shown in Figure 3.8-(a). As a result, this module can be used in an SPICE-like netlist as exemplified in Figure 3.8-(b) for a hybrid inverter circuit. The SET module is invoked as a subcircuit of the standard netlist, where the value of the parameters of the SET (R_T and C_T in the figure) can be established.

```
//  SET module; setequ.va

'include "std.va"
'include "const.va"

module set(D, G, S);
  inout D, G, S;
  electrical D, G, S;

//Parameter default values
  parameter RT = 100e6;
  parameter CG = 1e-18;

  analog
    begin
      I(D,S) <+ ...
                ...
                ...;
    end
  end module
```

(a) Verilog-A SET module

```
*** HYBRID INVERTER ***

.HDL seteq.va //Adds SET module

M1 out d g s b CMOSP L=1u W=2u
Cl out 0  '32*1e-18'
::::::::::::::::::::::::::::::
vdd  d  0  dc  0.1
vgg  g  0  dc  -0.25
vin  in  0  dc  0 AC 0
::::::::::::::::::::::::::::::
x1 out in 0 set RT=1e6 CG=1e-18
* Instantiate SET
::::::::::::::::::::::::::::::
.dc vin 0 30m 1m
.print dc v(out)
::::::::::::::::::::::::::::::
.MODEL CMOSP PMOS (  ...  )
.end
```

(b) Illustrative SPICE netlist

Figure 3.8: (a) Verilog-A SET module; (b) SPICE-like netlist using the SET module.

3.4 Developed models

As mentioned early, in order to represent the behavior of a SET, the $I - V_{GS}$ relationship was selected. The simulation results of this kind of relation were previously shown in Figure 3.6 and Figure 3.7-b. Both figures exhibit curves with a sinusoidal shape, in fact, any $I - V_{GS}$ curve presents this kind of shape that can be expressed as:

$$y \quad = \quad A \cdot f_{NL}\left(cos\left(f \cdot x + \beta\right)\right) + O$$

where A, f_{NL}, f, β and O are the parameters of the amplitude, warping, frequency, phase and offset respectively. It is worth stressing that the f_{NL} is a non-linear function that represents a warping in a sinusoidal function. The y axis represents the drain current and the x axis is the gate-to-source voltage.

All models developed in this thesis are characterized by the latter formulation. That means that the sinusoidal parameters are associated with a set of SET variables.

This section presents and discusses two models developed with the modeling methodology proposed in this thesis. On the one hand, a model called “First-order model” considers a reduced set of SET variables. On the other hand, a model called “Second-order model” takes into account a large number of SET variables.

3.4.1 First-order model

In order to provide a basic understanding of the usefulness of the modeling methodology, the first-order model is developed. It represents the drain current of the SET (I_D) as a function of the gate voltage (V_{GS}) and the tunnel resistance (R_T) variables. Therefore, the resulting mathematical expression is defined as follows:

$$I_D = f(V_{GS}, R_T) \tag{3.2}$$

SET variables and device-level simulation

The variables and their respective values involved in the model are shown in Table 3.1. The swept variables are the gate-to-source voltage, V_{GS}, from -100mV to 100mV in steps of 5mV and the tunnel resistance, R_T, from 100MΩ to 1GΩ in steps of 100MΩ. The values of the other variables are $V_{DS} = -30mV$, $C_G = 1aF$, $C_{TD} = C_{TS} = 1aF$ at a temperature (T) of 30K. Figure 3.9 depicts the corresponding graphic representation after device-level simulation of the SET.

VARIABLE	RANGE OF VALUES
V_{GS}	$[-100mV, 100mV : 5mV]$
R_T	$[100M\Omega, 1G\Omega : 100M\Omega]$
V_{DS}	$[-30mV]$
C_G	$[1aF]$
C_T	$[1aF]$
T	$[30K]$

Table 3.1: Variables and values used for the first-order model.

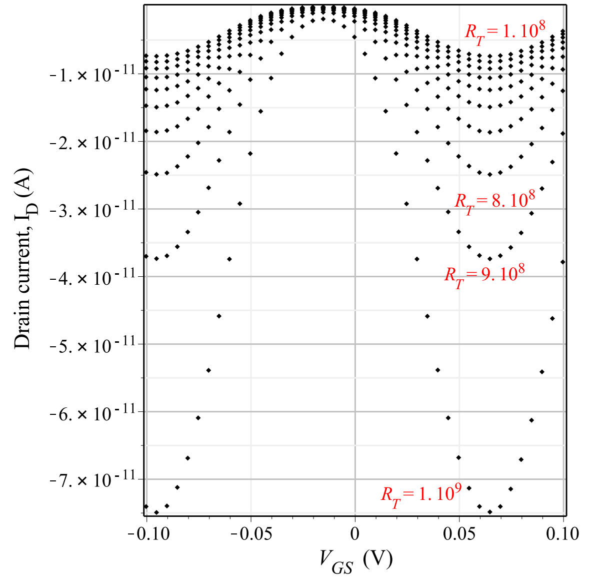


Figure 3.9: Graphic representation for the first-order model.

Expression generator

Based on simulation results and the instructions of the modeling methodology, the formulation of the mathematical expression is derived by using Equation 3.2. Therefore, each parameter of the sinusoidal expression must be found. For this purpose, the corresponding analysis is shown below:

a) *Analysis of the amplitude:* The amplitude is computed using the difference between an y-maximum and an y-minimum values for each single $I_D - V_{GS}$ curve (see Figure 3.10).

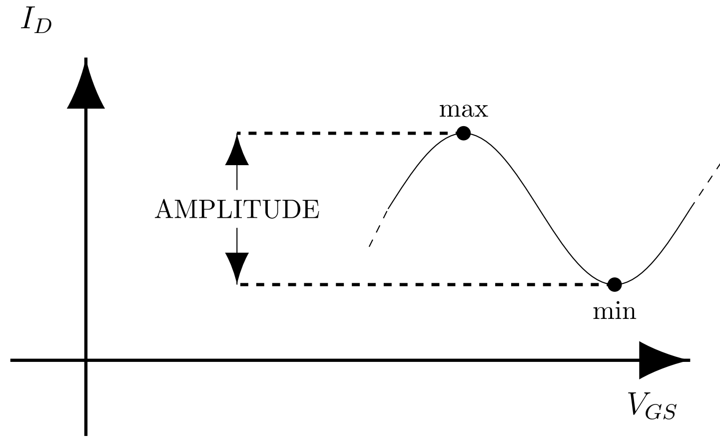


Figure 3.10: Illustration indicates how the amplitude parameter is computed.

b) *Analysis of the frequency:* The frequency is computed using the difference between two adjacent x-maxima (or x-minima) values for each single $I_D - V_{GS}$ curve (see Figure 3.11).

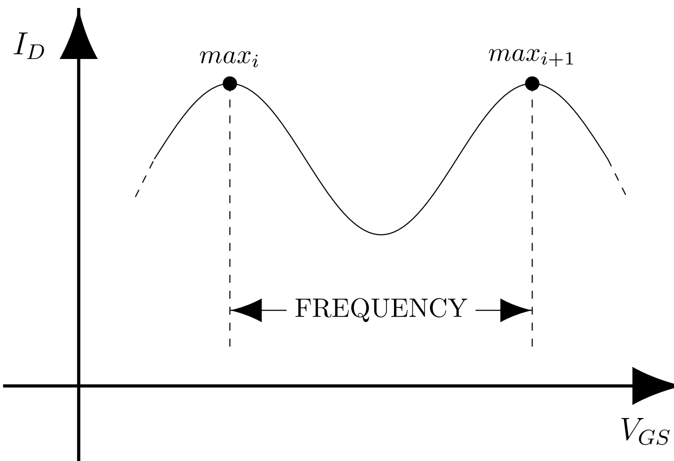


Figure 3.11: Illustration indicates how the frequency parameter is computed.

c) *Analysis of the phase:* The phase is computed from x-zero to the first x-maximum for each single $I_D - V_{GS}$ curve (see Figure 3.12).

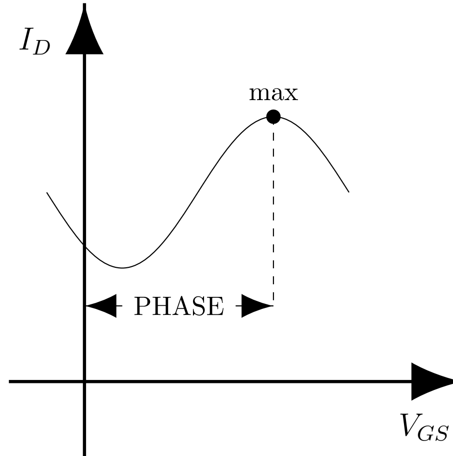


Figure 3.12: Illustration indicates how the phase parameter is computed.

d) *Analysis of the offset:* The offset parameter is computed by using the average of the sum between the y-maximum and the y-minimum values for each single $I - V_{GS}$ curve (see Figure 3.13).

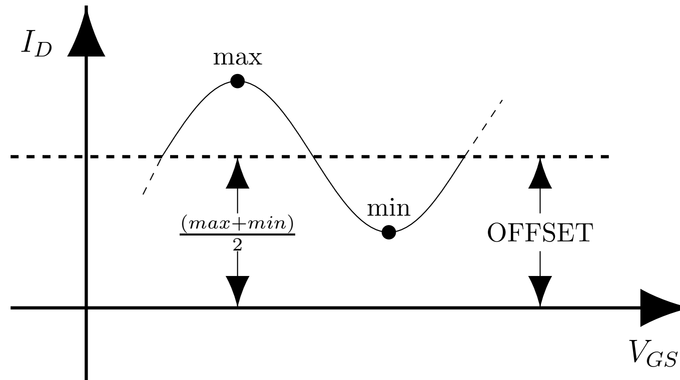


Figure 3.13: Illustration indicates how the offset parameter is computed.

e) *Analysis of the warping:* The warping is computed by using a non-linear function applied on a sinusoidal function and comparing it to a pure sinusoidal function for each $I_D - V_{GS}$ curve (see Figure 3.14).

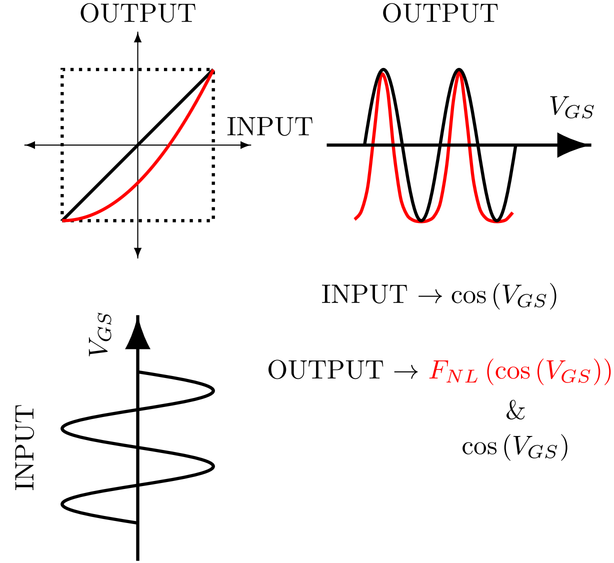


Figure 3.14: Illustration representing the application of a non-linear function over a sinusoidal wave.

Returning to Figure 3.9, it is possible to observe the evident variation of the amplitude and the offset in each curve. However, with regards to the warping distortion, although this parameter retains a constant value, it is difficult to detect with the naked eye but this will be discussed below. Keeping in mind the last observations, a mathematical expression for the first-order model could be:

$$I_D = k_0\left(R_T\right) \cdot \left(\frac{1}{2} \cdot cos(f\left(V_{GS}\right) + \beta) + \frac{1}{2}\right)^W + k_1\left(R_T\right) \tag{3.3}$$

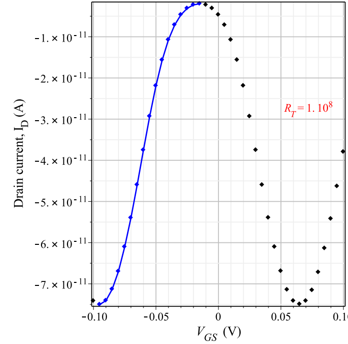
where k_0 and k_1 represent the coefficients of the amplitude and the offset respectively, which depend on the R_T. On the other hand, the remaining coefficients (f, β and W which are the frequency, the phase and the warping parameters) are independent of the R_T variable, which means that they are computed only ones.

In the case of the frequency parameter, it can be described using the relationship offer in Figure 2.15. In the figure, the periodicity of the Coulomb Oscillations is given by $2\pi C_G/e$ –where C_G is the gate capacitance parameter and e is the value of the elementary charge. On the other hand, the analysis of the phase parameter gives a value of ≈ 3.729. Finally, the warping parameter is found following the next steps:

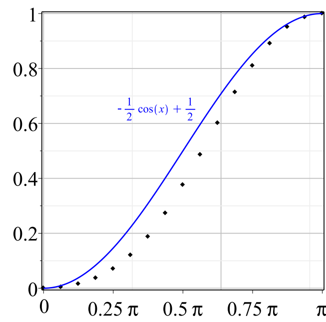
1. Select only the data from a minimum to the next maximum adjacent as shown in Figure 3.15-a (blue line),
2. Apply an horizontal and a vertical displacement over all data selected in order to position it in the origin of the plane,
3. Apply a vertical normalization in order to enclose the data from 0 to 1,

4. And finally, apply an horizontal normalization in order to enclose the data from 0 to Pi.

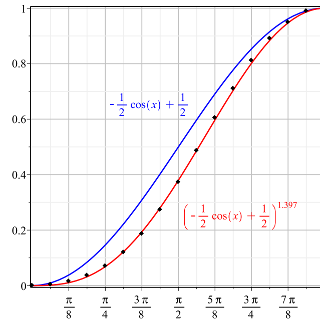
As mentioned above, it is difficult to determine with the naked eye a variation over the warping. However, after applying the above process to each single $I-V$ curve, they display the same warping as shown in Figure 3.15-b. In the figure, all data of each $I-V$ curve are overlaid on the plot. After to apply a curve fitting process, the value of the warping parameter is ≈ 1.4 as shown in Figure 3.15-c.



a) A simple curve.



b) Reorganized data (dots) and sinusoidal function (blue line).



c) Quasi-pure sinusoidal (blue line) and non-linear sinusoidal (red line).

Figure 3.15: Warping analysis.

As the amplitude and the offset parameters are changing for each curve, it is necessary to find one single value for each curve. In Figure 3.16-a and -b the corresponding values of these parameters are shown to be the amplitude and the offset respectively. The resulting datasets are adjusted by using the command *fit* of MAPLE software –which uses a least-squares method. This is done to find the k_0 and the k_1 coefficients of Equation 3.3. In the same figure, the corresponding value for each parameter is shown.

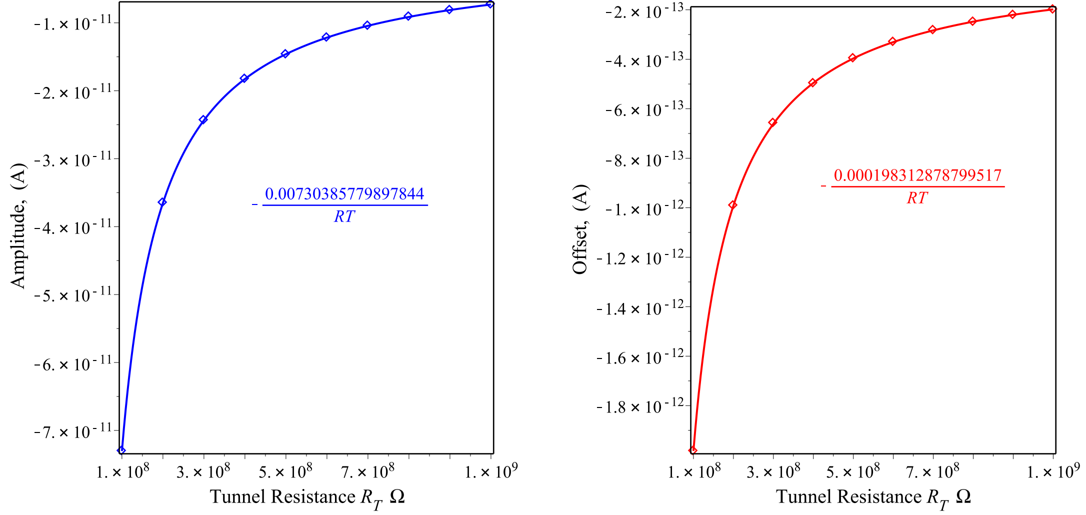


Figure 3.16: Calculation of the amplitude and the offset parameters by using a fitting technique.

A summary of the sinusoidal parameters previously computed is shown in the next table:

SINUSOIDAL PARAMETER	COMPUTED VALUE
Frequency (f)	$\frac{2\pi C_G}{e}$
Phase (β)	≈ 3.729
Warping (W)	≈ 1.4
Amplitude (k_0)	$\approx \frac{-0.00730}{R_T}$
Offset (k_1)	$\approx \frac{-0.000198}{R_T}$

Table 3.2: Summary of the sinusoidal computed parameters.

The Equation 3.3, when coupled with the above equations found (the frequency, the phase, the warping, the amplitude and the offset), produces a closed function. Hence, the drain current is expressed as a function of gate bias and the tunnel resistance ($I_D\,(V_{GS}, R_T)$), as shown below:

$$I_D = \frac{-0.0073038577\,(0.5\,\cos(39.21655982\,V_{GS} + 3.729841) + 0.5)^{1.4} - 0.00019831287}{R_T} \tag{3.4}$$

In Figure 3.17, the proposed function is evaluated and represented with lines. In the same figure, the dots are the data simulations from SIMON. As seen in the figure, there is an excellent correlation for all cases.

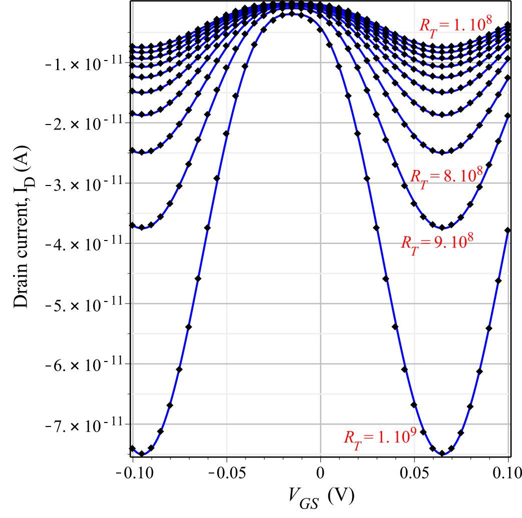


Figure 3.17: Comparison of simulation data vs proposed function.

In order to improve the accuracy of Equation 3.4, the Copycat tool is used to optimize the results (see Appendix A). This tool has been developed for the purpose of determining the values of the parameters in a function to produce the lowest error. After using it, the improved mathematical expression is amended as:

$$I_D = \frac{-0.00733008\,(0.5\cos(39.21655982\,VG + 3.729841) + 0.5)^{1.406257482} - 0.000211708}{RT} \tag{3.5}$$

Once again, a visual comparison between data simulation and the above expression is shown in Figure 3.18. Apparently the correlations exhibited in Figure 3.17 and Figure 3.18 are quite similar. In fact, by using a histogram in both cases, the difference is hardly noticeable (see Figure 3.19). Nonetheless, there has been a slight improvement in Equation 3.5.

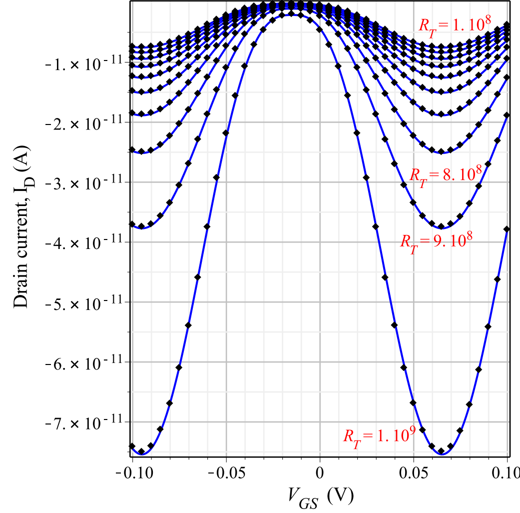
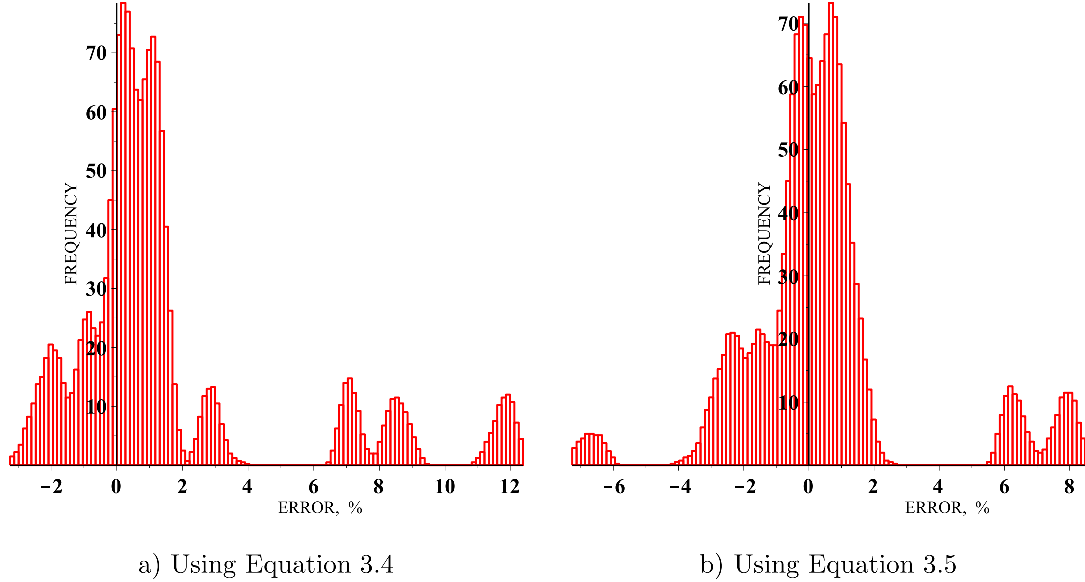


Figure 3.18: Comparison of simulation data vs proposed function after using Copycat tool.



a) Using Equation 3.4

b) Using Equation 3.5

Figure 3.19: Histogram of first-order model. Before Copycat (a), and after the Copycat (b).

As a conclusion, the first-order model has been developed using the modeling methodology proposed. The resulting model has been formulated in Equations 3.4 and 3.5, which have demonstrated their ability to reproduce the behavior of the SET with excellent correlation.

3.4.2 Second-order model

Before proceeding to describe the second-order model of the SET, a short review of the articles generated during the time frame of the writing of this Ph.D. thesis is mentioned. It is done to emphasize some relevant observations. For instance, in [64] it was discovered that tunneling resistance takes a symbolic form for symmetric single-electron transistors (for the case when both tunnel junctions have

the same value). This observation is represented in blue in the following equation:

$$I(V_{GS}, R_T) = (A_0 \sin(fV_{GS} + \beta) + A_{off}) \cdot \frac{1 \times 10^8}{R_T} \tag{3.6}$$

On the other hand, symbolic relationships involving the drain voltage (V_{DS}), the gate and tunnel capacitance (C_G, C_{TS}, C_{TD}) and the background charge (BC) have been reported in [65]. These are related to the parameters of the frequency and the phase from Equation 3.2 as follows:

$$f = \frac{2\pi C_G V_{GS}}{e} \tag{3.7}$$

$$\beta = \pi - BC - \frac{\pi V_{DS}\left(C_G + C_{TS} - C_{TD}\right)}{e} \tag{3.8}$$

In fact, the relation obtained in 3.7 has the same pattern as in [66]. As a result, the modeling methodology proposed in this thesis has the possibility of obtaining pseudo-analytic expressions.

While finding a symbolic expression for some parameters will prove difficult. And while most researchers will not want to devote excessive time to such a task, there exists, nonetheless, the possibility of arriving at an approximate parameter using fitting techniques. As a result, the models developed with this methodology may be part symbolic, part approximate. The second-order model developed in this section works under this assumption.

SET variables

In Figure 3.20 a representation of the variables of the single-electron transistor and the parameters of the proposed function is shown. The figure describes how the second-order model relates the SET variables to the sinusoidal parameters. Intersection between a variable and a parameter indicates if the relation is symbolic, curve-fitting, not applicable or not process. For instance, the phase parameter is only affected by the V_{DS}, the C_G, the C_{TD}, C_{TS}, and the BC. Also, it has a symbolic representation as shown in Equation 3.8.

SET-TRANSISTOR VARIABLES

FUNCTION PROPOSED PARAMETERS	ELECTRICAL		DESIGN					PROCESS	ENVIROMENTAL
	VDS	VGS	CG	CT		RT		BACKGROUND CHARGE	TEMPERATURE
				CTD	CTS	RTD	RTS		
AMP	CF	NA	CF (CZ)			A		NA	NF
FRE	NA	A	A	NA	NA	NA		NA	NF
PHA	A	NA	A	A	A	NA		A	NF
OFF	CF	NA	CF (CZ)			A		NA	NF
WAR	A	NA	A			NF / A	NF / A	NA	NF

A = ANALYTICAL; CF = CURVE-FITTING; NA = NOT APPLICABLE; NF = NOT FOUND

Figure 3.20: Second-order model configuration.

In the above figure, the yellow areas indicate the use of a curve-fitting technique. As a consequence, the accuracy as well as the range of operation are compromised. Such is the case with the drain voltage (V_{DS}) and the gate and tunnel capacitance that resort to a curve fitting technique in order to add the amplitude and offset parameters. The red areas show relations between variables and parameters that are not included in the model.

In accordance with the above, the second-order model has been developed with the following characteristics:

1. It works for any gate-to-source voltage (V_{GS}),
2. It works for any drain-to-source voltage (V_{DS}),
3. It works for any background charge (BC) value,
4. It works for any tunnel resistance (R_T) value for an quasi-asymmetric device (which means $R_{TD} = R_{TS}$),
5. It works when the sum of all capacitance involved in the SET is from 3aF to 4.5aF (in other words, $C_\Sigma = C_G + C_{TS} + C_{TD}$),
6. Temperature at 30K.

Device-level simulation and SET characteristics

Following the modeling methodology, the simulation data from SIMON that are used to develop this model are shown in a graphical way in Figure 3.21. The range of values for the variables used are as follows: the V_{GS} is from $-200mV$ to $200mV$ in steps of $5mV$. The V_{DS} is from $5mV$ to $195mV$ in

steps of $5mV$. Whilst temperature at $30K$. The total capacitance C_Σ presented in the device is shown in the figure for the next cases: $3aF$ in (a), $3.5aF$ in (b), $4aF$ in (c) and $4.5aF$ in (d).

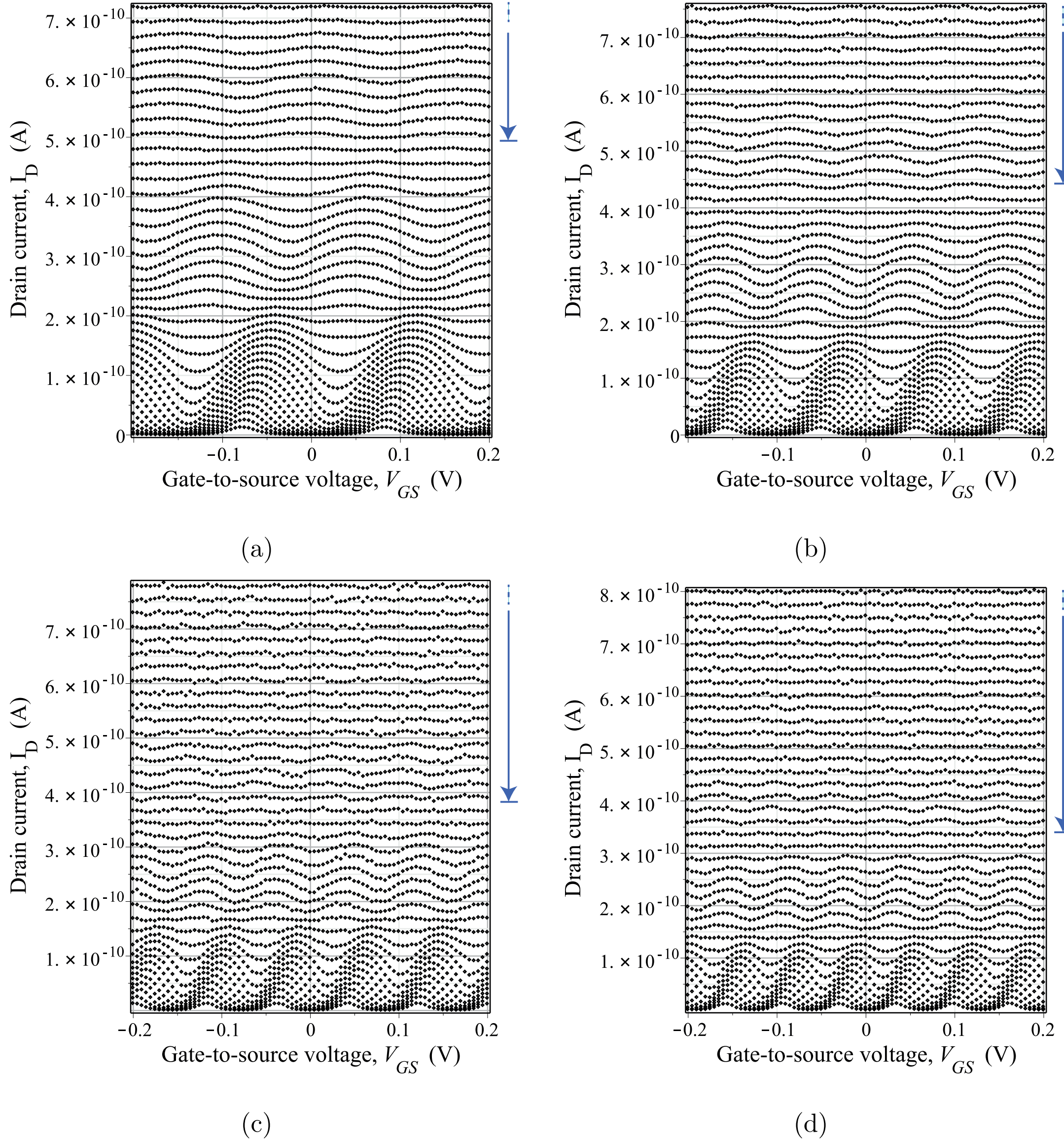


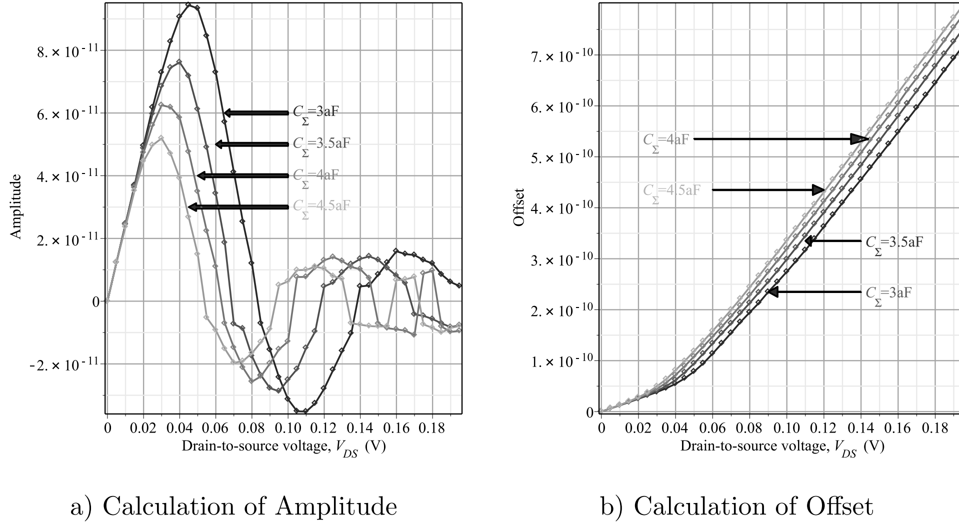
Figure 3.21: Device-level simulations used to develop the second-order model. In (a) $C_\Sigma = 3.0aF$. In (b) $C_\Sigma = 3.5aF$. In (c) $C_\Sigma = 4aF$. In (d) $C_\Sigma = 4.5aF$.

Using [67, 68] and the earlier graphs, some observations serve as guidelines for the development of the model. On the one hand, some parts in the development of the model are based upon the next relation: $V_{DS} \propto \lambda e/C_\Sigma$ where λ is a real number. On the other hand, it also noteworthy that the single-electron transistor eventually starts to display a quasi-linear behavior like a two-terminal resistance. It happens when the drain voltage exceeds a value of $3e/C_\Sigma$, as shown in Figure 3.21 with a quasi-constant current (see blue arrows in each plot).

Expression generator

In this stage, the amplitude and the offset parameters are first computed directly from data simulations for all curves. Then, it is explained how to embed them into the sinusoidal function. After that, the warping parameter is embedded. Finally, the resulting equation for each parameter is substituted in the proposed function.

From data simulations, the amplitude and the offset are computed for each curve, and it is represented in Figure 3.22. In other words, each dot in the figure implies the corresponding calculation of the amplitude (a) or the offset (b) for each V_{DS} curve. In the figure, there are lines overlap the dots in order to distinguish each C_{Σ} value.



a) Calculation of Amplitude b) Calculation of Offset

Figure 3.22: Calculation of the amplitude and the offset parameters as a function of V_{DS} for several C_{Σ} values.

Amplitude of the second-order model The following discussion describes how the amplitude is incorporated into the model. For this purpose, only one curve of C_{Σ} is explained because the procedure is repeated for the other curves.

The selected curve is for the case of $C_{\Sigma} = 3aF$ and it is shown in Figure 3.23. The figure shows that the curve is divided into two regions (R1 and R2). Region one represents all V_{DS} values for $0 < V_{DS} < 1.5e/C_{\Sigma}$, while region two includes all values of $V_{DS} > 1.5e/C_{\Sigma}$. The dots in region one are described by using a polynomial function. Besides, the dots in the second region are described by using a sinusoidal function.

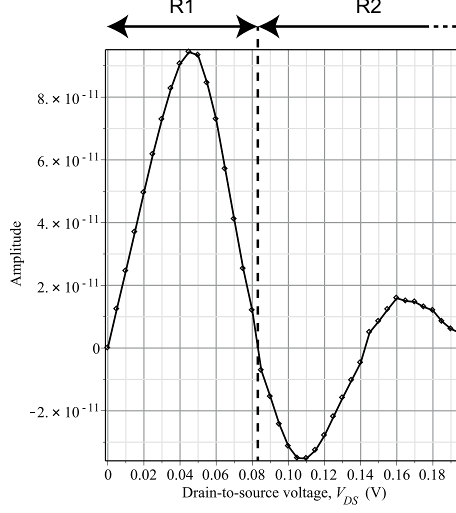


Figure 3.23: One single amplitude curve, where $C_{\Sigma} = 3aF$.

The resulting expressions for each region are defined as follows:

$$R1 = G{V_{DS}}^7 + F{V_{DS}}^6 + E{V_{DS}}^5 + D{V_{DS}}^4 + C{V_{DS}}^3 + B{V_{DS}}^2 + AV_{DS} \tag{3.9}$$

$$R2 = a\left(\frac{\sin(bV_{DS} - 1)}{bV_{DS} - 1} - \frac{\sin(bV_{DS} + 1)}{bV_{DS} + 1}\right) \tag{3.10}$$

where A, B, C, D, E, F, G, a and b are the set of coefficients for each region. After applying a curve-fitting technique, the values of the coefficients are:

$$\begin{aligned}
A &= 2.14720049069445 \times 10^{-9} \\
B &= 8.50058655463879 \times 10^{-8} \\
C &= -0.00000793627130770438 \\
D &= 0.000348965918492733 \\
E &= -0.00765942254302220 \\
F &= 0.0767255035231360 \\
G &= -0.283663045303538 \\
a &= 1.27201274287920 \times 10^{-10} \\
b &= 54.7305802047579
\end{aligned} \tag{3.11}$$

The above results are substituted into Equations 3.9 and 3.10. After performing this process, the following equations are obtained:

$$\begin{aligned} R1 &= 2.1472 \times 10^{-9}\, V_{DS} + 8.5005 \times 10^{-8}\, {V_{DS}}^2 - 7.936 \times 10^{-6}\, {V_{DS}}^3 + 3.490 \times 10^{-6}\, {V_{DS}}^4 \\ &\quad -0.007659\, {V_{DS}}^5 + 0.07673\, {V_{DS}}^6 - 0.2837\, {V_{DS}}^7 \qquad (3.12) \\ R2 &= 1.27201 \times 10^{-10} \left(\frac{\sin(54.7305\, V_{DS} - 1.0)}{54.7305\, V_{DS} - 1.0} - \frac{\sin(54.7305\, V_{DS} + 1.0)}{54.7305\, V_{DS} + 1.0} \right) \qquad (3.13) \end{aligned}$$

Figure 3.24 indicates the evaluation of each function separately within its range of validity (blue line for $R1$ and red line for $R2$).

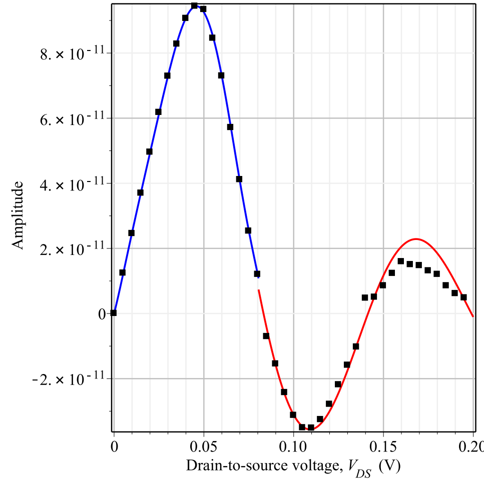


Figure 3.24: Curve fitting to the amplitude for each region ($R1$ in blue and $R2$ in red).

Using the piece-wise exponential technique (PWET) provided in Appendix B, it is possible to merge the Equations 3.12 and 3.13 into a single expression. As a consequence, the resulting equation that expresses the amplitude parameter when $C_{\Sigma} = 3aF$ is given as:

$$A|_{C_{\Sigma}=3aF} = \frac{(\text{Equation-3.12})}{1 + e^{300\, V_{DS} - 24.135}} + \frac{e^{300\, V_{DS} - 24.135} \cdot (\text{Equation-3.13})}{1 + e^{300\, V_{DS} - 24.135}} \qquad (3.14)$$

The evaluation of Equation 3.14 is shown in Figure 3.30. In the figure, we can see a continuous curve that is useful in order to avoid convergence problems.

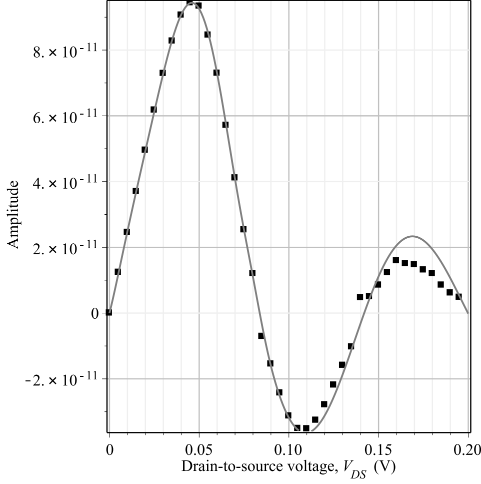


Figure 3.25: Evaluation of Equation 3.14.

Equation 3.9 was chosen because a high degree of certainty is required at low voltage. It is noteworthy that at low voltages of V_{DS}, the Coulomb Blockade is more noticeable and important. For this reason, a good convergence is a priority in this zone. But there is always the possibility of proposing some other function in order to describe this zone. Besides, the selection of Equation 3.10 was made because the amplitude behavior presents a shape very similar to a decreasing sinusoidal.

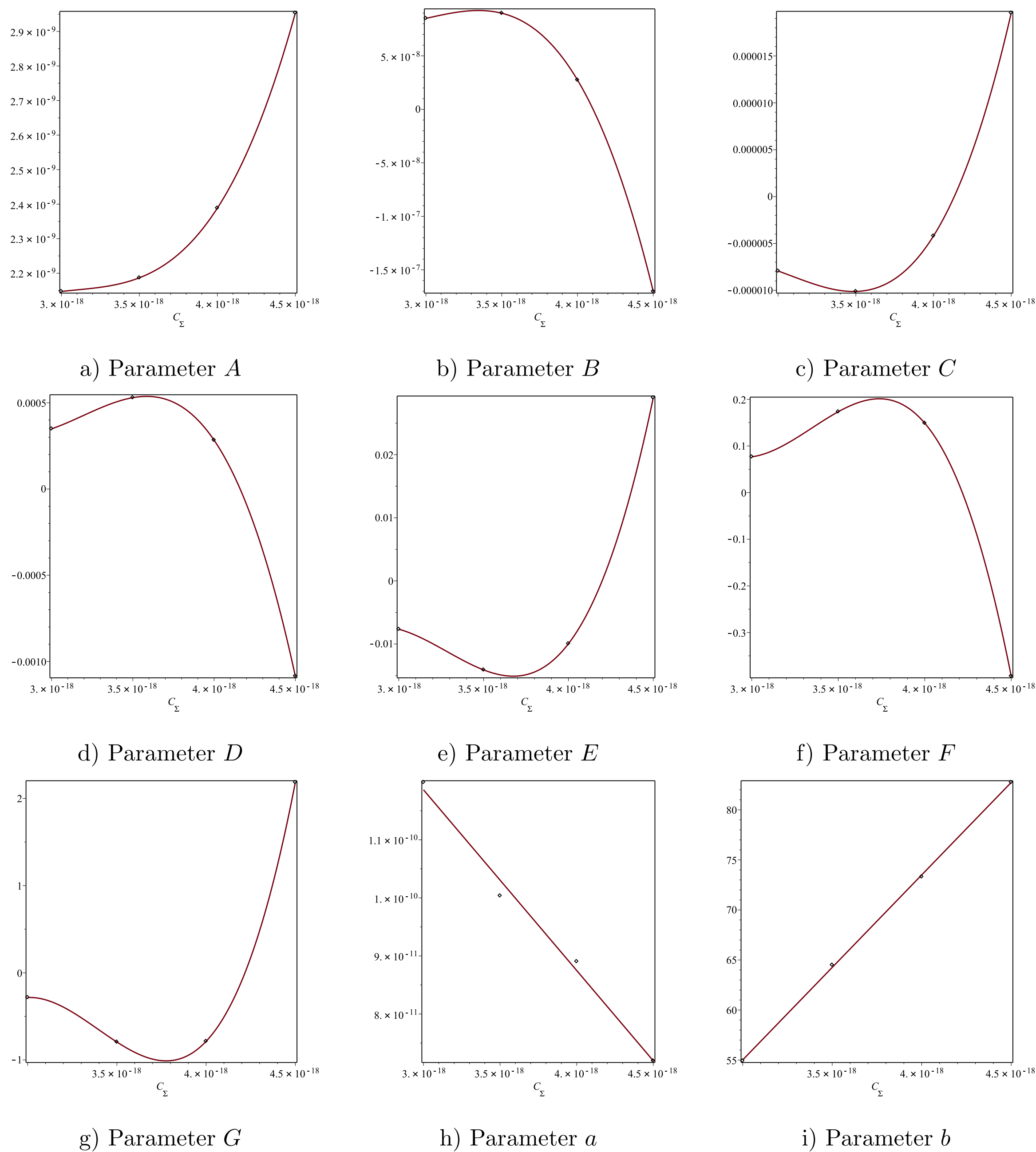
The previous analysis must be done for each curve of C_Σ. As a result of this process the values obtained are shown in Table 3.3.

	C_Σ			
	$3aF$	$3.5aF$	$4aF$	$4.5aF$
A	2.1472×10^{-9}	2.1868×10^{-9}	2.3885×10^{-9}	2.9534×10^{-9}
B	8.5005×10^{-8}	8.9843×10^{-8}	2.74×10^{-8}	-1.7023×10^{-7}
C	-7.9362×10^{-6}	-1.0115×10^{-5}	-4.196×10^{-6}	1.9581×10^{-5}
D	3.4896×10^{-4}	5.2974×10^{-4}	2.8343×10^{-4}	-1.0852×10^{-3}
E	-7.6594×10^{-3}	-1.4102×10^{-2}	-9.9589×10^{-3}	2.903×10^{-2}
F	7.6725×10^{-2}	0.1733	0.1489	−0.3936
G	−0.2836	−0.7942	−0.7863	2.1843
a	1.2720×10^{-10}	1.0217×10^{-10}	8.9936×10^{-11}	7.0796×10^{-11}
b	54.7305	64.57	73.384	82.6623

Table 3.3: Computed values for each parameter of Equations 3.9 and 3.10.

In order to introduce the capacitance variable into the second-order model, the values of the above table are adjusted (see 3.26). For the case of coefficients from A to G, they are adjusted using a

polynomial function because they do not exhibit an obvious tendency. However, the parameters a and b are adjusted using a linear function.



a) Parameter A b) Parameter B c) Parameter C

d) Parameter D e) Parameter E f) Parameter F

g) Parameter G h) Parameter a i) Parameter b

Figure 3.26: Curve adjustments for the parameter in Table 3.3.

The corresponding equation for each parameter depicted in Figure 3.26 is shown as follows:

$$A(C_\Sigma) = -5.9584\times10^{-9} + 7.7674\times10^{9}\,C_\Sigma - 2.4935\times10^{27}\,{C_\Sigma}^2 + 2.6834\times10^{44}\,{C_\Sigma}^3 \quad (3.15)$$

$$B(C_\Sigma) = 2.44544\times10^{-6} - 2.42014\times10^{12}\,C_\Sigma + 8.16050\times10^{29}\,{C_\Sigma}^2 - 9.05355\times10^{46}\,{C_\Sigma}^3 \quad (3.16)$$

$$C(C_\Sigma) = -3.712610^{-4} + 3.65269\times10^{14}\,C_\Sigma - 1.20421\times10^{32}\,{C_\Sigma}^2 + 1.30113\times10^{49}\,{C_\Sigma}^3 \quad (3.17)$$

$$D(C_\Sigma) = 2.92234\times10^{-2} - 2.79169\times10^{16}\,C_\Sigma + 8.87806\times10^{33}\,{C_\Sigma}^2 - 9.26892\times10^{50}\,{C_\Sigma}^3 \quad (3.18)$$

$$E(C_\Sigma) = -1.10492 + 1.02987\times10^{18}\,C_\Sigma - 3.18394\times10^{35}\,{C_\Sigma}^2 + 3.23402\times10^{52}\,{C_\Sigma}^3 \quad (3.19)$$

$$F(C_\Sigma) = 19.18074 - 1.75489\times10^{19}\,C_\Sigma + 5.31467\times10^{36}\,{C_\Sigma}^2 - 5.29232\times10^{53}\,{C_\Sigma}^3 \quad (3.20)$$

$$G(C_\Sigma) = -123.19062 + 1.11176\times10^{20}\,C_\Sigma - 3.31784\times10^{37}\,{C_\Sigma}^2 + 3.25865\times10^{54}\,{C_\Sigma}^3 \quad (3.21)$$

$$a(C_\Sigma) = 2.11961\times10^{-10} - 3.11173\times10^{7}\,C_\Sigma \quad (3.22)$$

$$b(C_\Sigma) = -0.42196 + 1.84729\times10^{19}\,C_\Sigma \quad (3.23)$$

The above expressions depend on the C_Σ variable. These are substituted in Equations 3.9 and 3.10 giving:

$$R1(C_\Sigma) = G(C_\Sigma){V_{DS}}^7 + F(C_\Sigma){V_{DS}}^6 + E(C_\Sigma){V_{DS}}^5 + D(C_\Sigma){V_{DS}}^4 + C(C_\Sigma){V_{DS}}^3 + B(C_\Sigma){V_{DS}}^2 + A(C_\Sigma)V_{DS} \quad (3.24)$$

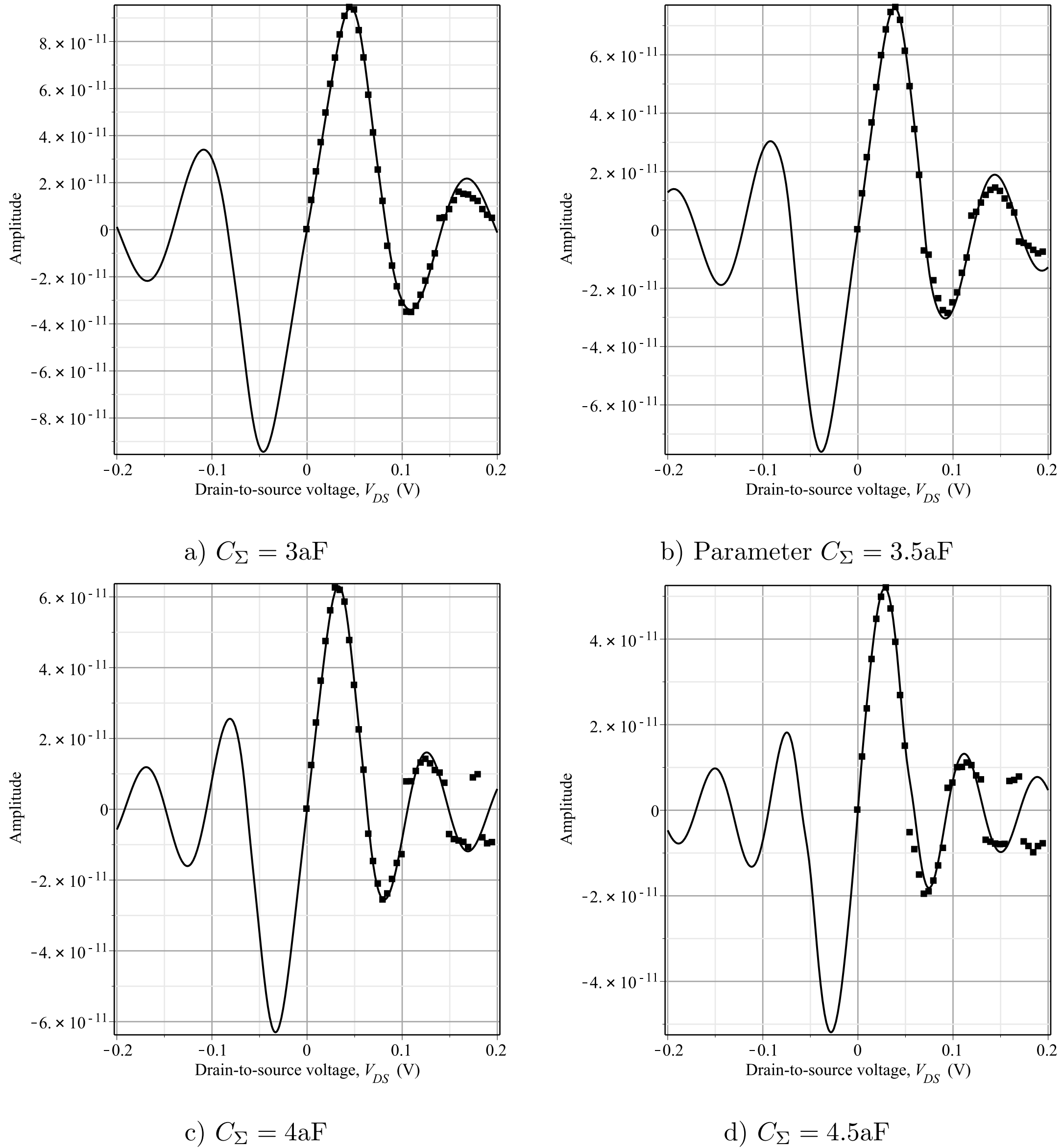
$$R2(C_\Sigma) = a(C_\Sigma)\left(\frac{\sin\left(b(C_\Sigma)V_{DS}-1\right)}{b(C_\Sigma)V_{DS}-1} - \frac{\sin\left(b(C_\Sigma)V_{DS}+1\right)}{b(C_\Sigma)V_{DS}+1}\right) \quad (3.25)$$

Merging Equations 3.24 and 3.25 by using the PWET, the amplitude parameter is expressed as

$$A_{C_\Sigma} = \frac{(\text{Equation-3.24})}{1+\mathrm{e}^{300\,V_{DS}-24.135}} + \frac{\mathrm{e}^{300\,V_{DS}-24.135}\cdot(\text{Equation-3.25})}{1+\mathrm{e}^{300\,V_{DS}-24.135}} \quad (3.26)$$

In addition, due to the symmetry in the charge transport in a SET, it is possible to cover negative values of V_{DS}. This is accomplished using the property of a odd function to Equation 3.26, which means that $-f(x) = f(-x)$.

In Figure 3.27, a comparison of original amplitude data and the evaluated amplitude equation is shown for each C_Σ value.



a) $C_\Sigma = 3$aF

b) Parameter $C_\Sigma = 3.5$aF

c) $C_\Sigma = 4$aF

d) $C_\Sigma = 4.5$aF

Figure 3.27: Amplitude. Dots: Computed. Line: Evaluation of Equation 3.26.

Offset of the second-order model In this part, a discussion of how to introduce the offset into the second-order model is done. Since the procedure is very similar to the amplitude, a brief analysis of the offset is offer.

The selected curve has the value of $C_\Sigma = 3aF$ and it is shown in Figure 3.28. In this case, the figure shows that the curve is divided into three regions (R1, R2 and R3). Region one and two are adjusted using a polynomial function whereas the third region has a symbolic form.

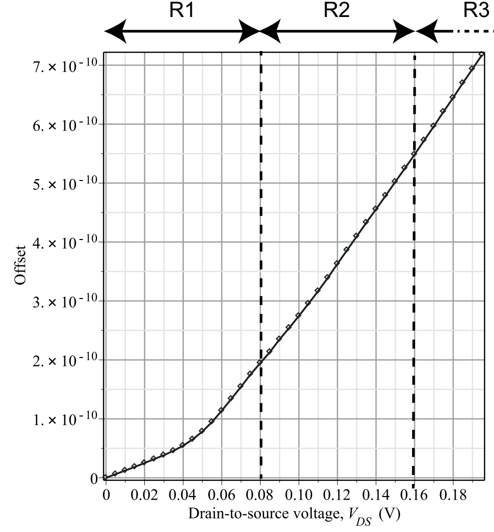


Figure 3.28: Representation of offset for $C_{\Sigma} = 3aF$.

The expressions for each region are defined as follows:

$$R1 \;:=\; E\,{V_{DS}}^5 + (D)\,{V_{DS}}^4 + C\,{V_{DS}}^3 + B\,{V_{DS}}^2 + A\,V_{DS} \tag{3.27}$$

$$R2 \;:=\; c\,{V_{DS}}^2 + b\,V_{DS} + a \tag{3.28}$$

$$R3 \;:=\; \frac{\left(V_{DS} - \frac{e}{C_{\Sigma}}\right)}{R_{TS} + R_{TD}} \tag{3.29}$$

where A, B, C, D, E, a, b, and c are the coefficient for each region. Region one covers the values of $0 \leq V_{DS} < 1.5e/C_{\Sigma}$, while region two covers the values of $1.5e/C_{\Sigma} < V_{DS} < 3e/C_{\Sigma}$. Finally, the region three has a symbolic form. After applying a fitting process, the previous coefficients are defined as follows:

$$\begin{aligned}
A &= 1.08857888849387 \times 10^{-9} \\
B &= 2.88671279831877 \times 10^{-8} \\
C &= -0.00000166164412174138 \\
D &= 0.0000368273485011814 \\
E &= -0.000224315290437542 \\
a &= -9.31038699690412 \times 10^{-11} \\
b &= 3.13617131062953 \times 10^{-9} \\
c &= 5.53147574819397 \times 10^{-9}
\end{aligned} \tag{3.30}$$

Substituting the above results into Equations 3.27 and 3.28 we get:

$$\begin{aligned} R1 &:= -2.24315\times10^{-4}\,{V_{DS}}^{5}+3.68273\times10^{-5}\,{V_{DS}}^{4}-1.66164\times10^{-6}\,{V_{DS}}^{3} \\ &\quad +2.88671\times10^{-8}\,{V_{DS}}^{2}+1.088578\times10^{-9}\,V_{DS} \end{aligned} \tag{3.31}$$

$$R2 := 5.53147\times10^{-9}\,{V_{DS}}^{2}+3.13617\times10^{-9}\,V_{DS}-9.310387\times10^{-11} \tag{3.32}$$

The evaluation of these equations together with Equation 3.29 in their corresponding regions are shown in Figure 3.29.

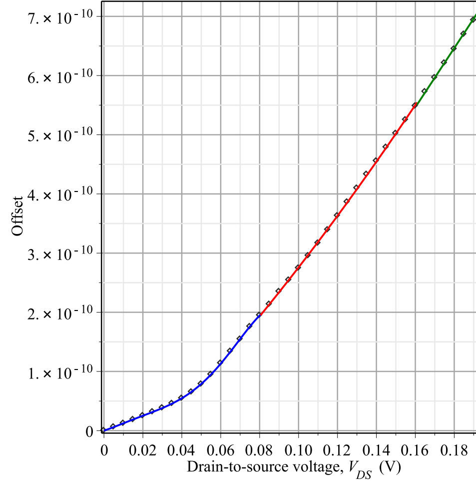


Figure 3.29: Curve adjusting to the offset for each region ($R1$ in blue, $R2$ in red and $R3$ in green).

The PWET is applied to merge the Equations 3.31 and 3.32 into a single expression. The resulting equation of the offset parameter when $C_\Sigma = 3\text{aF}$ is given as:

$$\begin{aligned} O|_{C_\Sigma=3aF} &= \frac{(\text{Equation-3.31})}{1+e^{300\,V_{DS}-24.135}}+\frac{(\text{Equation-3.32})\left(-e^{300\,V_{DS}-48.27}+e^{300\,V_{DS}-24.135}\right)}{\left(1+e^{300\,V_{DS}-24.135}\right)\left(1+e^{300\,V_{DS}-48.27}\right)} \\ &\quad +\frac{e^{300\,V_{DS}-48.27}\left(V_{DS}-\frac{e}{C_\Sigma}\right)}{(R_{TS}+R_{TD})\left(1+e^{300\,V_{DS}-48.27}\right)} \end{aligned} \tag{3.33}$$

In Figure 3.30 the evaluation of Equation 3.33 is shown. The curve in the figure exhibits a continuous behavior that is a desired characteristic to avoid convergence problems.

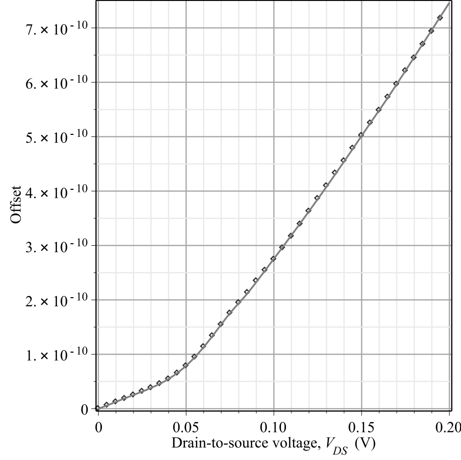


Figure 3.30: Evaluation of Equation 3.33.

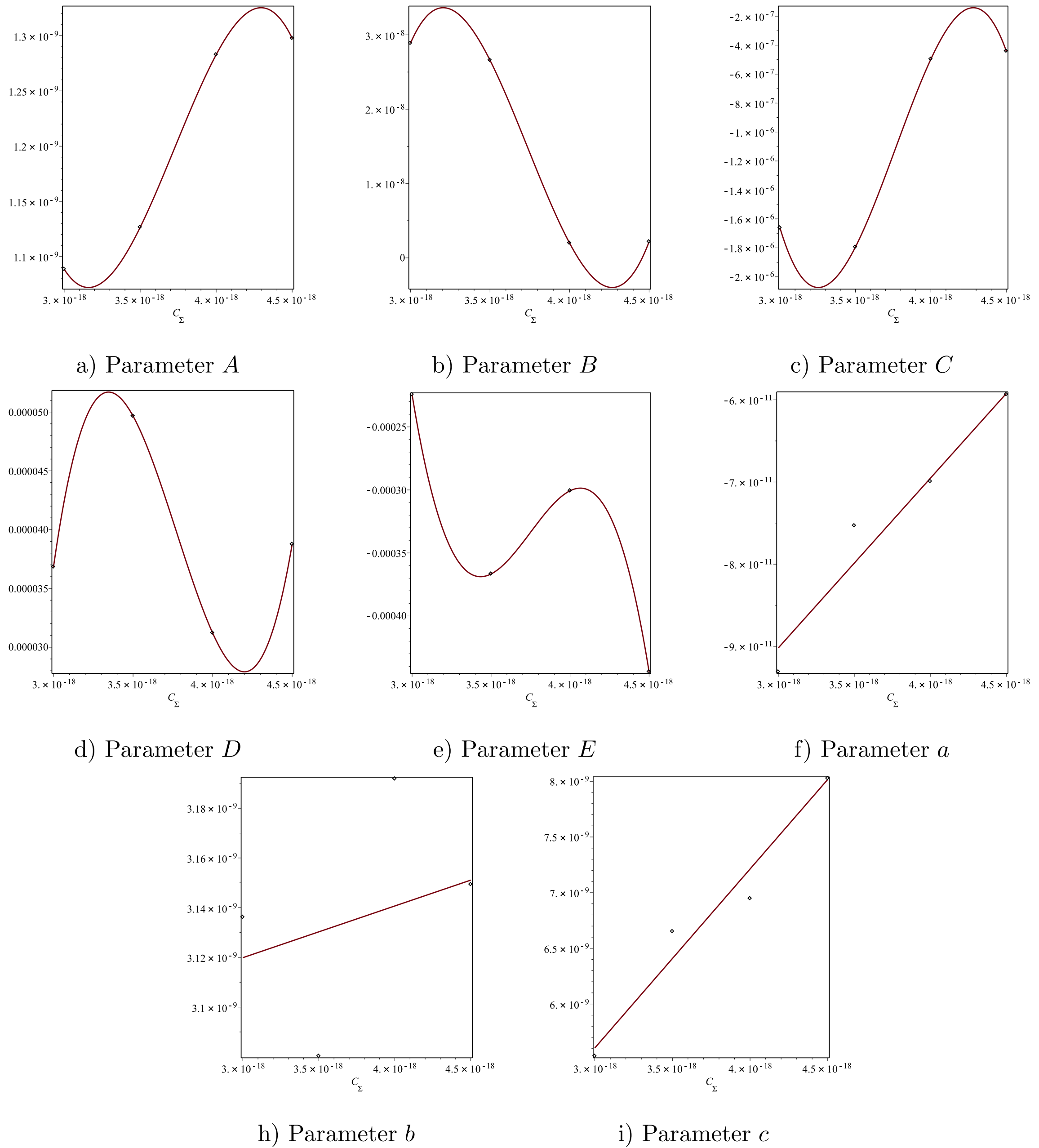
The selection of equations 3.27 and 3.28 was based upon the high correlation between the calculated offset data and the functions proposed for each zone. As stated earlier, it is extremely important to make a good description of the SET behavior for low voltages of V_{DS} since the Coulomb Blockade phenomenon is more pronounce.

Once again, the previous analysis is carried out for each curve of C_Σ. After this process, the resulting values are shown in Table 3.4.

	C_Σ			
	$3aF$	$3.5aF$	$4aF$	$4.5aF$
A	1.08857×10^{-9}	1.126513×10^{-9}	1.28279×10^{-9}	1.29767×10^{-9}
B	2.88671×10^{-8}	2.6591×10^{-8}	1.99608×10^{-9}	2.1704×10^{-9}
C	-1.66164×10^{-6}	-1.79461×10^{-6}	-4.96991×10^{-7}	4.40850×10^{-7}
D	3.68273×10^{-5}	4.96589×10^{-5}	3.12127×10^{-5}	3.875620×10^{-5}
E	-2.24315×10^{-4}	-3.66666×10^{-4}	-3.0066×10^{-4}	4.44317×10^{-4}
a	-9.31038×10^{-11}	-7.53078×10^{-11}	-6.9927×10^{-11}	-5.9349×10^{-11}
b	3.1361×10^{-9}	3.08056×10^{-9}	3.19182×10^{-9}	3.14934×10^{-9}
c	5.53147×10^{-9}	6.65132×10^{-9}	6.94695×10^{-9}	8.02577×10^{-9}

Table 3.4: Computed values for parameter of Equations 3.27 and 3.28.

In order to introduce the offset parameter, the values in Table 3.4 are adjusted, and this process is shown in Figure 3.31. Coefficients from A to E are treated using a polynomial function because the values do not exhibit an obvious tendency. However, the coefficients a, b and c are adjusted using a plain linear function because in this zone the Coulomb Blockade phenomenon begins to vanish, and less accuracy is required.



a) Parameter A b) Parameter B c) Parameter C

d) Parameter D e) Parameter E f) Parameter a

h) Parameter b i) Parameter c

Figure 3.31: Curve fitting for the coefficient in Table 3.4.

The corresponding equation for each coefficient from Figure 3.31 is shown as follows:

$$A(C_\Sigma) = 1.7889 \times 10^{-8} - 1.4101 \times 10^{10}\, C_\Sigma + 3.8726 \times 10^{27}\, {C_\Sigma}^2 - 3.4628 \times 10^{44}\, {C_\Sigma}^3 \quad (3.34)$$

$$B(C_\Sigma) = 3.0625 \times 10^{-6} + 2.576 \times 10^{12}\, C_\Sigma - 7.0375 \times 10^{29}\, {C_\Sigma}^2 - 6.2773 \times 10^{46}\, {C_\Sigma}^3 \quad (3.35)$$

$$C(C_\Sigma) = 1.787810^{-4} - 1.4887 \times 10^{14}\, C_\Sigma + 4.0263 \times 10^{31}\, {C_\Sigma}^2 - 3.5621 \times 10^{48}\, {C_\Sigma}^3 \quad (3.36)$$

$$D(C_\Sigma) = -3.9033 \times 10^{-3} + 3.2187 \times 10^{15}\, C_\Sigma - 8.6415 \times 10^{32}\, {C_\Sigma}^2 + 7.6343 \times 10^{49}\, {C_\Sigma}^3 \quad (3.37)$$

$$E(C_\Sigma) = 2.8409 \times 10^{-2} - 2.3333 \times 10^{16}\, C_\Sigma + 6.2679 \times 10^{33}\, {C_\Sigma}^2 - 5.5726 \times 10^{50}\, {C_\Sigma}^3 \quad (3.38)$$

$$a(C_\Sigma) = -1.5212 \times 10^{-10} + 2.0645 \times 10^{7}\, C_\Sigma \quad (3.39)$$

$$b(C_\Sigma) = 3.0574 \times 10^{-9} + 2.081 \times 10^{7}\, C_\Sigma \quad (3.40)$$

$$c(C_\Sigma) = 7.8210 \times 10^{-10} + 1.6075 \times 10^{9}\, C_\Sigma \quad (3.41)$$

The above expressions are substituted in Equations 3.27, and 3.28 in order to introduce the offset parameter into the model. The resulting equations are given as follows:

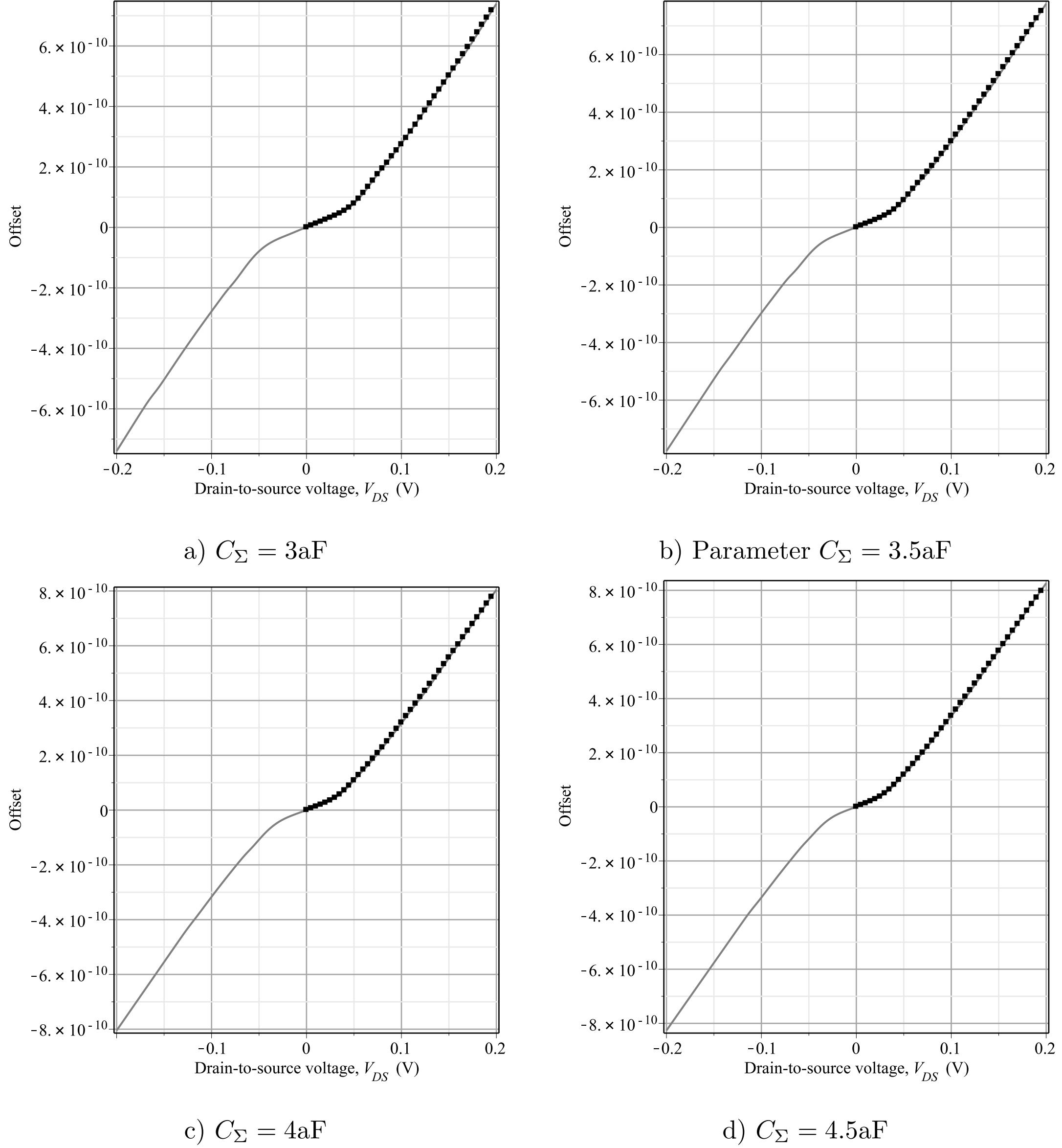
$$R1(C_\Sigma) := E(C_\Sigma)\, {V_{DS}}^5 + D(C_\Sigma)\, {V_{DS}}^4 + C(C_\Sigma)\, {V_{DS}}^3 + B(C_\Sigma)\, {V_{DS}}^2 + A(C_\Sigma)\, V_{DS} \quad (3.42)$$

$$R2(C_\Sigma) := c(C_\Sigma)\, {V_{DS}}^2 + b(C_\Sigma)\, V_{DS} + a(C_\Sigma) \quad (3.43)$$

Merging Equations 3.42, 3.43 and 3.29 by using the PWET, the offset parameter is expressed as:

$$O_{C_\Sigma} = \frac{(\text{Equation-3.42})}{1 + \mathrm{e}^{300\, V_{DS} - 24.135}} + \frac{(\text{Equation-3.43})\left(-\mathrm{e}^{300\, V_{DS} - 48.27} + \mathrm{e}^{300\, V_{DS} - 24.135}\right)}{\left(1 + \mathrm{e}^{300\, V_{DS} - 24.135}\right)\left(1 + \mathrm{e}^{300\, V_{DS} - 48.27}\right)} + \frac{\mathrm{e}^{300\, V_{DS} - 48.27}\left(V_{DS} - \frac{e}{C_\Sigma}\right)}{(R_{TS} + R_{TD})\left(1 + \mathrm{e}^{300\, V_{DS} - 48.27}\right)} \quad (3.44)$$

Similar to the amplitude case, it is possible to cover negative values of V_{DS} by using the property of the odd function. After this process, a comparison of offset-data computed and the offset equation is shown in Figure 3.32.



a) $C_{\Sigma} = 3\text{aF}$

b) Parameter $C_{\Sigma} = 3.5\text{aF}$

c) $C_{\Sigma} = 4\text{aF}$

d) $C_{\Sigma} = 4.5\text{aF}$

Figure 3.32: Offset. Dots: Computed. Line: Evaluation of Equation 3.44.

Warping of the second-order model The warping function used in this model is expressed as follows:

$$\frac{e^{b(1/2\ \cos(x)+1/2)} - 1}{e^{b} - 1} - 1/2 \tag{3.45}$$

where x represents the frequency and the phase variables, which are mentioned in Equation 3.7 and 3.8 respectively. Besides, Equation 3.45 has a single fitting coefficient (b), which provides an easier curve fitting process.

In Figure 3.33, the behavior of Equation 3.45 for several evaluations of the b coefficient is presented. In the figure, four plots are depicted. A pure sinusoidal function ($cos(x)$). A curve when $b = 1$ that exhibits a similar shape of a pure sinusoidal function but reduced in amplitude and lightly warping. A curve when $b = 10$ that exhibits a strong warping. And finally, a curve when $b = -10$ that presents a flipped behavior from the previous case.

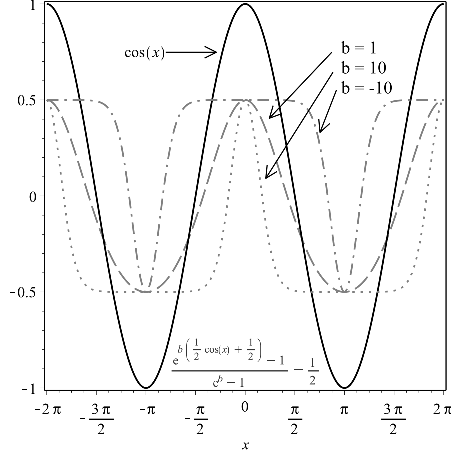


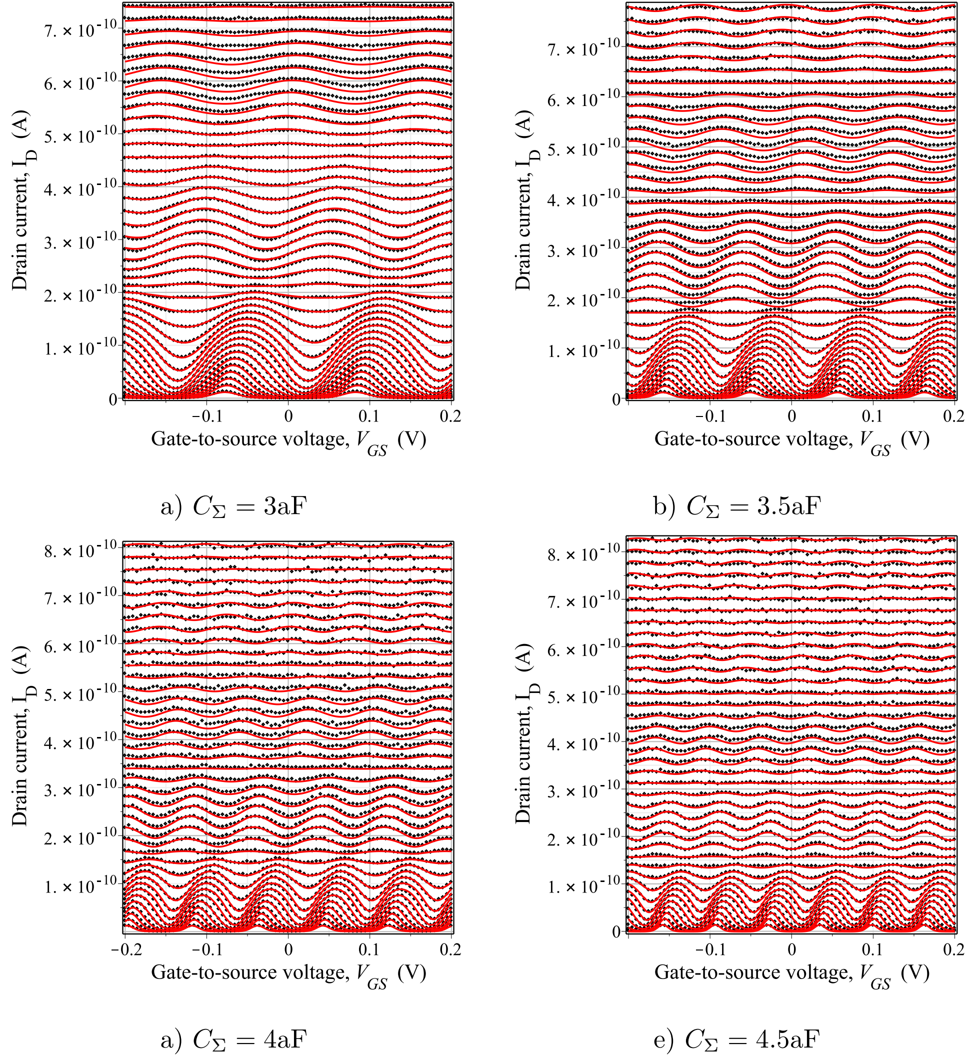
Figure 3.33: Non-linear function (exponential case) over the natural sinusoidal function.

After to compute the warping parameter for each case, the b coefficient is expressed as follows:

$$b = \frac{1.2\, e \sin\left(1.5\, \frac{\pi\, C_\Sigma\, V_{DS}}{e}\right)}{C_\Sigma\, V_{DS}} \tag{3.46}$$

where e is the elementary charge.

Evaluation of the second-order model In Figure 3.34, the resulting mathematical expression of the second-order model for the SET has been evaluated to observe the convergence with data simulation. The figure shows the four C_G cases, where data simulations are represented by dots while the evaluation of the second-order model is shown with red lines. In Figure 3.34, the resulting mathematical expression of the second-order model for the SET has been evaluated to observe the convergence with data simulation. The figure shows the four C_G cases, where data simulations are represented by dots while the evaluation of the second-order model is shown with red lines. In all cases, the correlation between function and data is achieved.



a) $C_{\Sigma} = 3\text{aF}$

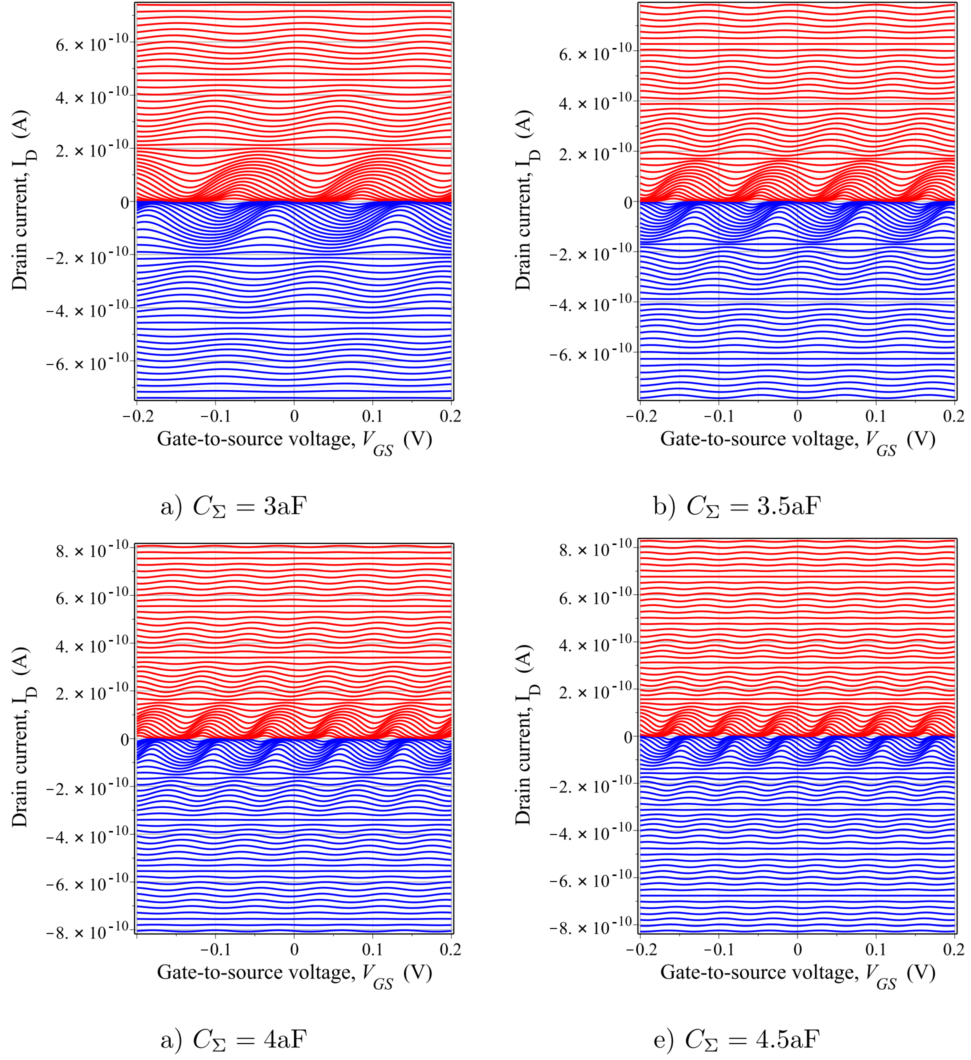
b) $C_{\Sigma} = 3.5\text{aF}$

a) $C_{\Sigma} = 4\text{aF}$

e) $C_{\Sigma} = 4.5\text{aF}$

Figure 3.34: Data simulation vs evaluated mathematical expression of second-order model.

In Figure 3.35, an evaluation of the second-order model equation to positive and negative values of V_{DS} is shown.



a) $C_\Sigma = 3$aF

b) $C_\Sigma = 3.5$aF

a) $C_\Sigma = 4$aF

e) $C_\Sigma = 4.5$aF

Figure 3.35: Evaluation of the mathematical expression of the second-order model for positive and negative values of V_{DS}.

4 Examples

In this chapter, a set of only-SET structures and hybrid circuits is presented with the aim of verify and to use the second-order model. First, two only-SET circuits are presented. One of them is an invert. The other is a NOR/NAND-gate. These circuits are simulated both on SIMON and on SPICE simulations in order to be compared. Secondly, three hybrid circuits are depicted: an inverter, an NAND-gate, and an NDR cell. Lastly, with the aim of demonstrating the effectiveness of the second-order model, a chain of only-SET inverters is simulated in runtime.

4.1 Only-SET Structures

Currently, the most promising circuits using SET transistors are related to memory applications [69]. It is because integrated circuits composed of only SET transistor are capable of obtaining high-density integration. Such ICs round at 10^{11}bits/cm^2 and work with extremely low power consumption that round in 10^{-10}W/gate. These attractive advantages have motivated the development of other useful structures such as logic circuits, a pair of which are described below.

4.1.1 Single-electron inverter

Tucker [70] proposed the first only-SET inverter. Later, it was improved by Likharev [71, 72]. The inverter is composed of two identical SET transistors in series. The gate terminal of both is connected to the input stage. The union between them is the output stage. Upper SET transistor is the active load. Meanwhile, the lower transistor is the driver (see Figure 4.1).

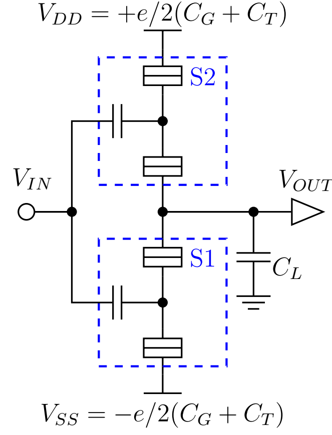
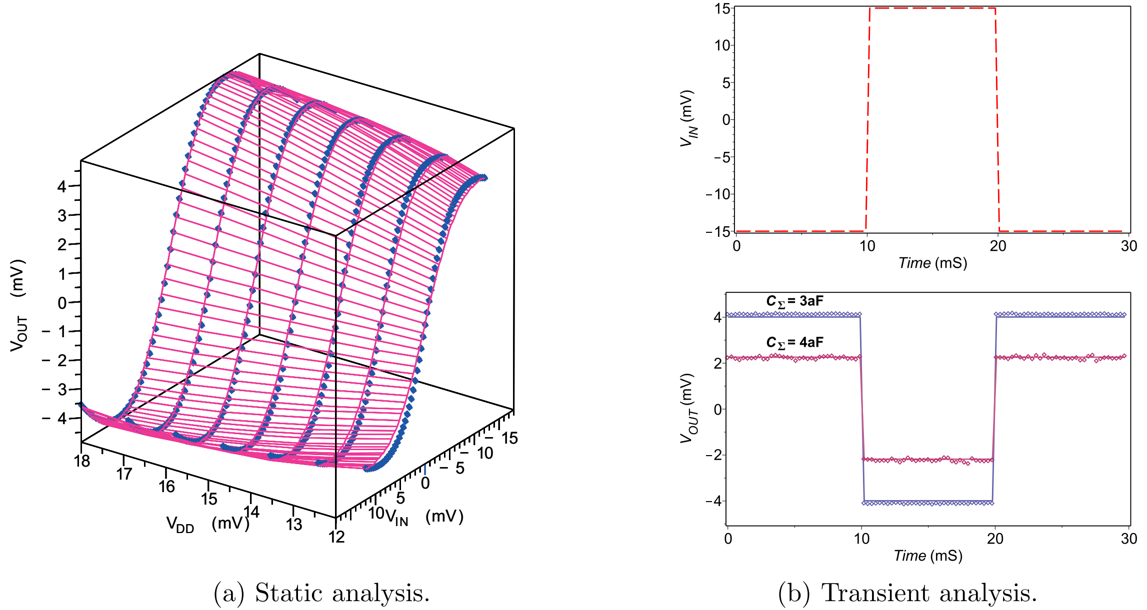


Figure 4.1: Schematic of SET inverter.

Tucker proposed that Logic Levels (LL, which represents the voltage difference between the signals, as well as the biasing,) are defined by $e/2(C_G + C_T)$. Then, assuming a gate capacitance of 3aF and a tunnel capacitance has a value of 1aF, the LL values should be around 17mV. However, in Figure 4.2-a, where the DC characteristics are shown, this amount produces a lower gain. In the same figure, the dots represent SIMON simulations while the lines represent our second-order model.



(a) Static analysis.

(b) Transient analysis.

Figure 4.2: DC and transient responses for the only-SET inverter. (a) Comparison of SIMON (blue dots) versus second-order model (red curve) for several LLs. (b) Transient simulation for two values of the C_G parameter.

A transient simulation of the only-SET inverter is shown in Figure 4.2-b. The top and lower plot are the input and output voltage, respectively. At that point, the dots represent SIMON simulations while the solid lines are our proposed model (second-order). Both outputs exhibit an excellent correlation.

4.1.2 Single-electron NOR/NAND gate

Another logic circuit composed of only-SET transistors is the single-electron NOR/NAND gate depicted in Figure 4.3. This dual logic gate is made up of eight single-electron transistors (S_1 to S_8). Depending upon the polarization, can be an NOR-gate if the biasing is from positive to negative ($V_{DD} - V_{SS}$) or an NAND-gate when the polarization is reversed ($V_{SS} - V_{DD}$).

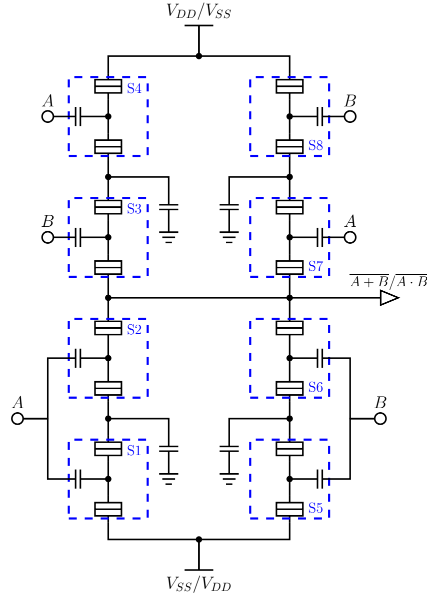


Figure 4.3: Schematic of only-SET NOR/NAND gate.

Figures 4.4 and 4.5 show the DC characteristics for only-SET NOR/NAND gate when it is working as an NOR-configuration or as an NAND-configuration, respectively. Both plots in each figure show the same results but from different angles. Also, in both figures, the sA curve represents the sweeping of the A-input keeping the B-input low while the sB curve denotes the sweeping of the A-input keeping the B-input high. In all plots, there is a set of dots that represents the biasing where the maximum transfer voltage is presented.

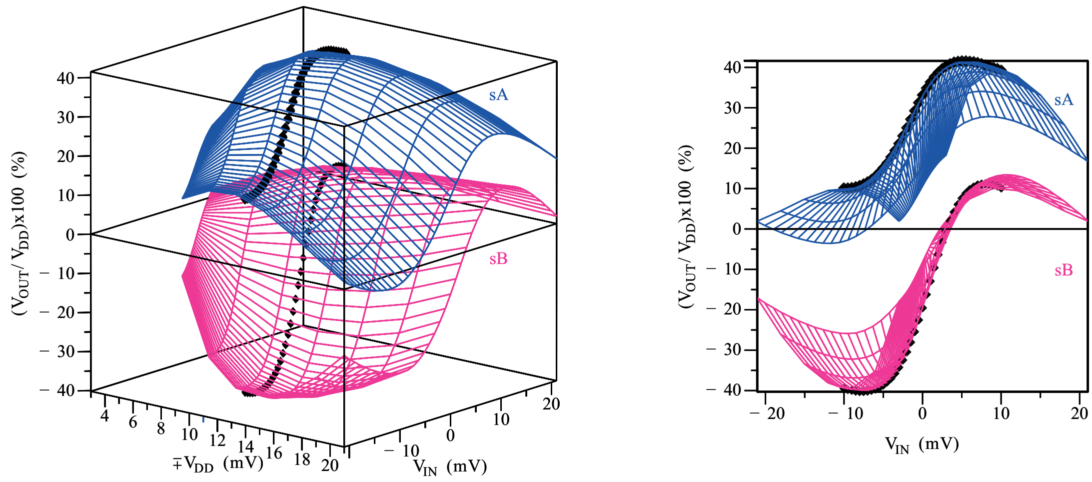


Figure 4.4: DC characteristics in NOR-gate configuration.

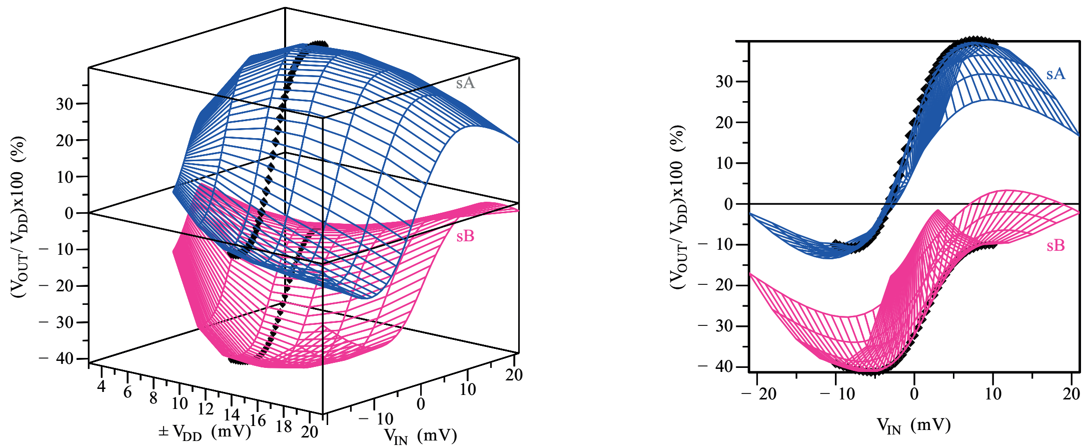
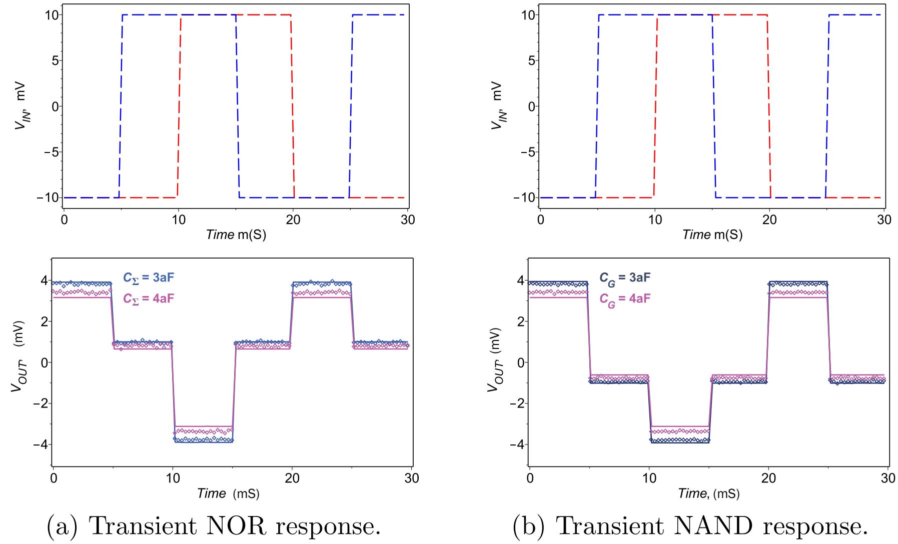


Figure 4.5: DC characteristics in NAND-gate configuration.

The transient characteristics are exhibited in Figure 4.6-a and -b for the NOR-configuration and the NAND-configuration, respectively. In both cases, two values of C_Σ (3aF and 4aF) are shown. The plots shown in the upper graphs represent the input while those displayed in the lower graph show the output voltage.



(a) Transient NOR response. (b) Transient NAND response.

Figure 4.6: Transient results for only-SET NOR/NAND gate.

4.2 Hybrid CMOS/SET Architecture

The advantage of combining SET and MOSFET devices in the same circuit is that the combination appropriates the best characteristics of each technology. In this section, two logic gates and an NDR circuit are studied.

4.2.1 Hybrid inverter

The hybrid inverter was proposed by Uchida [73, 74]. It is built with a PMOS transistor as load and a SET transistor as driver (see Figure 4.7).

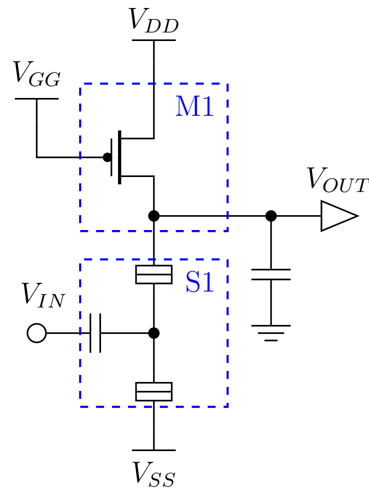


Figure 4.7: Schematic of a hybrid inverter composed by a PMOS and a SET transistors.

In the hybrid inverter, the PMOS transistor acts as a load resistor (R_{pmos}). Hence, the PMOS must work in the linear region where the channel resistance is given by:

$$r_{ds} = \left[\kappa_n' \frac{W}{L} (v_{GS} - V_t)\right]^{-1} \tag{4.1}$$

In Figure 4.8-a different curves corresponding to the output transfer voltage for several values of r_{ds} are shown. The points refer to the SIMON simulation using a simple resistor whose value is $6M\Omega$ equivalent to the resistance of the PMOS transistor in a linear region calculated with the equation 4.1. An optimization curve is done in order to find the maximum output transfer, as illustrated in Figure 4.8-b.

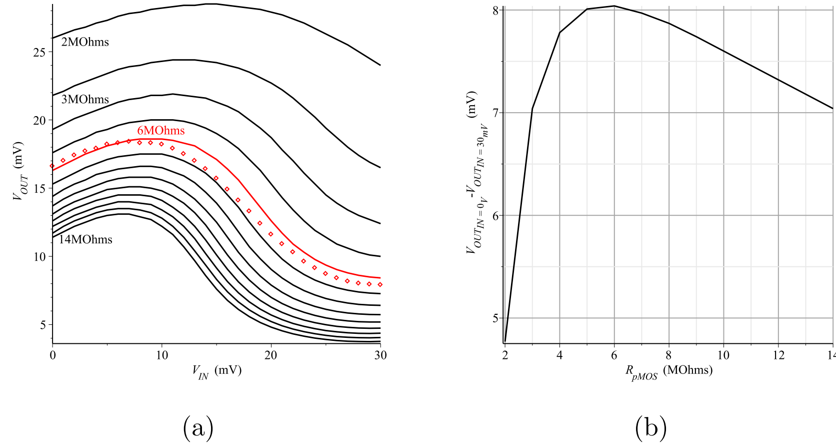


Figure 4.8: (a) Output transfer curves of the hybrid inverter. (b) Optimization curve to obtain the maximum output transfer.

Figure 4.9 shows the transient response of the hybrid inverter. The top plot indicates the input voltage, as well as the output voltage for two values of the total capacitance (C_Σ) as shown in the bottom plot. In this figure, we can see that the output transfer decreases when C_Σ increases, according to Lientsching [75].

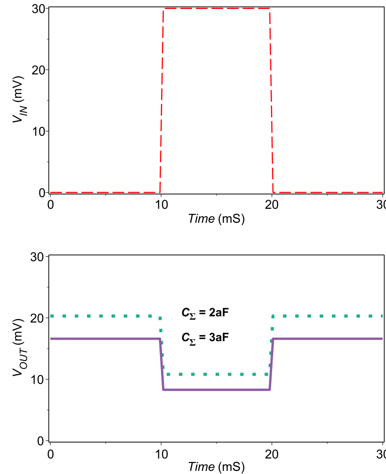


Figure 4.9: Transient characteristics for the hybrid inverter.

The hybrid NOR-gate [76] is composed of a pair of PMOS transistors in series (called *pull-up*) and two SET transistors in parallel (called *pull-down*) –see Figure 4.10. The PMOS transistors act as switches. If either of the input values are high, one or two PMOS transistors are in the *cutoff region* (acting as an open circuit). For this reason, the output voltage is closer to the low state. If both inputs are low, the PMOS transistors will conduct. Table 4.1 indicates the operation region for the PMOS transistors.

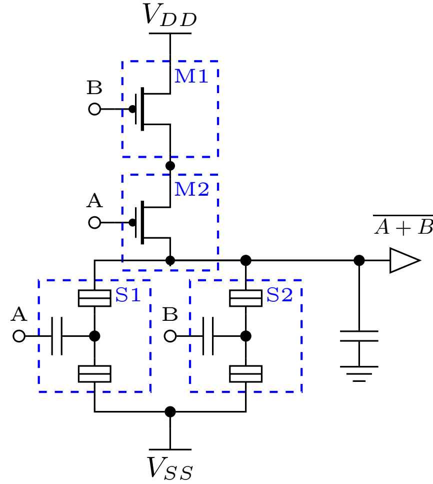


Figure 4.10: Schematic of a hybrid NOR-gate.

Input		Region	
A	B	M1	M2
0	0	Linear	Saturation
0	1	Cutoff	Cutoff
1	0	Linear	Cutoff
1	1	Cutoff	Cutoff

Table 4.1: Operation region in each MOSFET transistor of the hybrid NOR-gate.

In Figure 4.11-a, the response of several values of LL is shown. In the figure, it is possible to observe different V_{OUT}/V_{IN} ratio. Also in the figure, several values of the aspect ratios $(W/L)_p$ for the PMOS transistor are shown. These sweeps are useful to obtain the higher V_{OUT}/V_{IN} ratio. For instance, using the minimum size transistor ($W/L = 0.16um/0.12um$), a gain of 36.9% is obtained at 560mV. Increasing the value of the channel width to 1.16um and keeping the minimum channel length, the maximum gain possible is of 43.6% at 630mV. When increasing the value of the channel length to 1.12um with the minimum values of the channel width, a gain of 47% is obtained. Finally, increasing both values (channel width and channel length) produces a gain of 64.6% at 140mV, which is the optimum case. As a result, it is possible to achieve the highest V_{OUT}/V_{IN} ratio with a lower voltage.

From the previous analysis, the Figure 4.11-b shows the voltage-transfer curves taking the best values of the aspect ratio of the PMOS transistor. The dotted line indicates an input voltage in A node equal to V_{DD} while the input voltage in B node is switched from 0V to V_{DD}. The dashed line depicts an input voltage in B node equal to V_{DD} while the input voltage in A node is switched from 0V to V_{DD}. The solid line is the unity gain line.

A final static analysis is shown in Figure 4.11-c for two values of the C_Σ. Two important points are revealed. First, we see that the gain decreases when the value of C_Σ increases. Second, the V_{OUT}/V_{IN} ratio appears an oscillation, due to the Coulomb Blockade Oscillations. These are better defined for low values of LL.

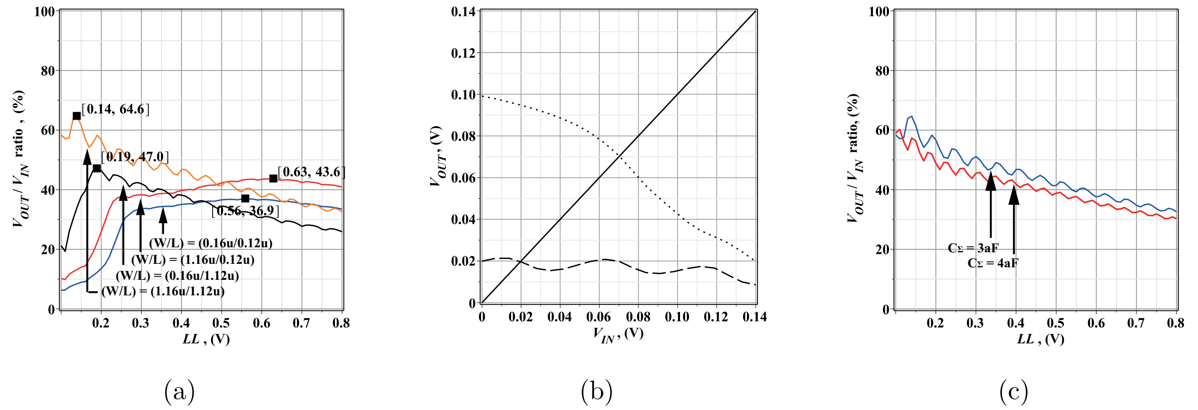


Figure 4.11: Static characteristics of the hybrid NOR-gate: In (a) for several ratios of W/L. In (b) the voltage transfer is shown for $C_\Sigma = 3aF$. And (c) depicts the V_{OUT}/V_{IN} ratio for two values of the C_Σ.

Figure 4.12 shows the transient response for the hybrid NOR-gate for several values of the gate capacitance. The values of LL were obtained from Figure 4.11-c with the aim of select the maximum output voltage that is approximately of 600mV of LL.

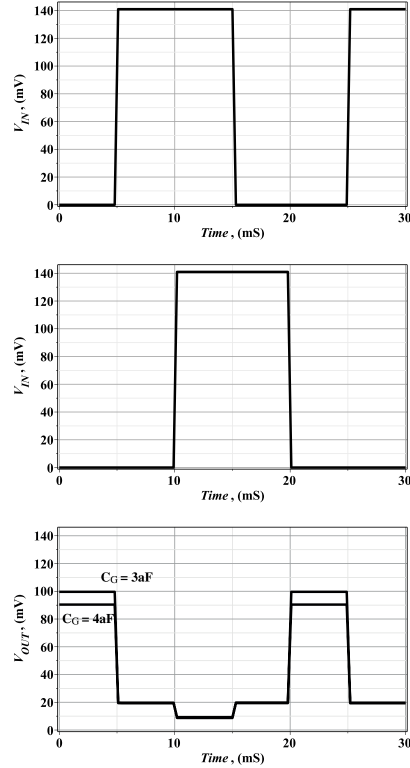


Figure 4.12: Transient characteristics for the hybrid-NOR gate.

The previous analysis gives the logical characteristics for the hybrid NOR-gate. Although the output voltage drops below the value of the rails, this deficiency could be compensated with an amplification stage provided by a simple CMOS buffer. In sum, this hybrid gate is a good candidate to be considered as part of future hybrid circuits.

Figure 4.13 depicts the hybrid NAND-gate. For this gate, the *pull-up* is built with two PMOS transistors in parallel. The *pull-down* is composed of two SET transistors in series. Table 4.2 gives the operation region in each PMOS transistor for the hybrid NAND-gate.

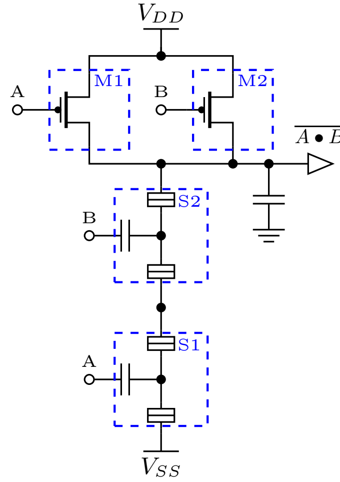


Figure 4.13: Schematic of a hybrid NAND-gate.

Input		Region	
A	B	M1	M2
0	0	Linear	Linear
0	1	Linear	Cutoff
1	0	Curoff	Saturation
1	1	Cutoff	Cutoff

Table 4.2: Operation region in each MOSFET transistor of the hybrid NAND-gate.

The static response for the hybrid NAND-gate is drawn in Figure 4.14. We can see in Figure 4.14–a that the maximum voltage gain is obtained when the ratio W/L is $1.16u/0.12u$. In Figure 4.14–b the voltage transfer (V_{OUT}/V_{IN}) is shown for $C_\Sigma = 3aF$. In Figure 4.14–c the V_{OUT}/V_{IN} ratio for two values of the C_Σ.

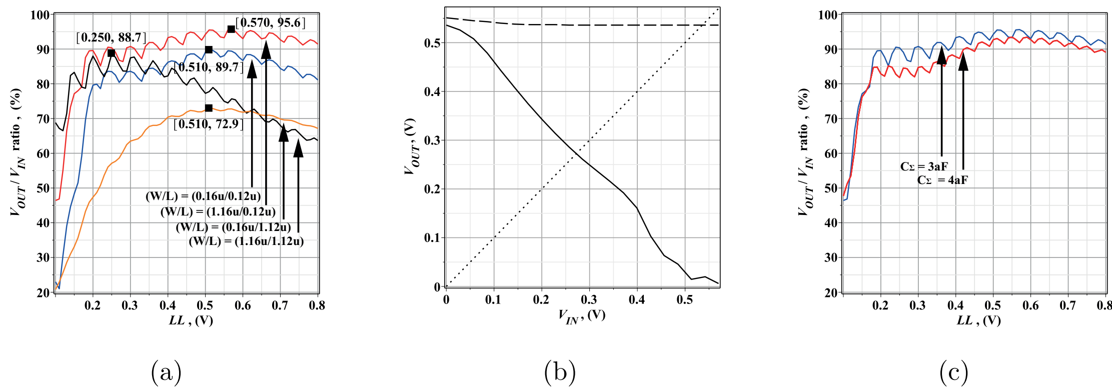


Figure 4.14: Static characteristics of the hybrid NAND-gate. (a) The V_{OUT}/V_{IN} ratio for several aspect ratios. (b) Voltage transfer of $C_\Sigma = 3aF$. (c) The V_{OUT}/V_{IN} ratio for two values of C_Σ.

The transient response for several values of the gate capacitance is illustrated in Figure 4.15. Here, the values of LL were obtained from Figure 4.14-b in order to obtain the maximum ratio of voltage for each value of the C_Σ parameter.

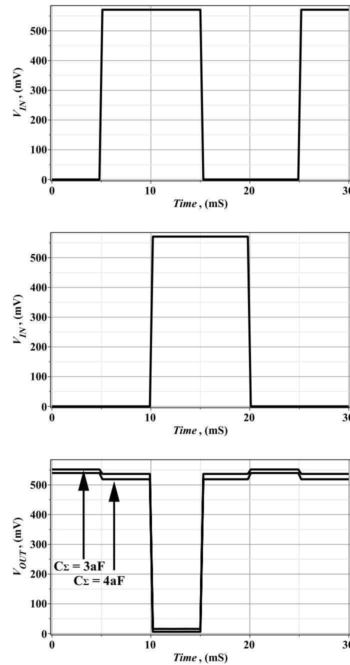


Figure 4.15: Transient characteristics for the hybrid NAND-gate.

From the previous analysis, this hybrid structure expresses the characteristics expected of an NAND-gate. Under certain conditions, it is possible to obtain an output voltage very close to the rails. It is unnecessary to use an amplifier stage.

4.2.2 NDR circuit

An important basic cell for the design of a wide number of applications, such as oscillator, is the negative differential resistance cell (NDR). In this example, the hybrid NDR from Figure 4.16 is simulated. The hybrid NDR cell [77] is composed by an n-MOSFET and a SET in series. V_{GG} constitute a constant bias voltage and V_{DD} is swept from 0 to 2V.

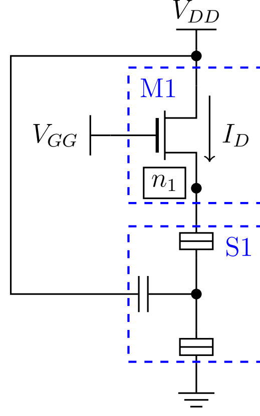


Figure 4.16: Schematic of a hybrid-NDR cell.

The MOSFET acts as a buffer, then, the DC voltage at the drain terminal of the SET remains almost constant and less than e/C_Σ while V_{DD} is increasing. Therefore, the MOSFET must be working in deep subthreshold region (i.e. $V_{GG} < V_{TH}+e/C_\Sigma$). Since V_{DD} is also connected to the gate terminal of the SET, then when V_{DD} increases, the SET current oscillates, yielding a periodic NDR behavior. The values used to simulate the NDR are C_Σ = 3aF, $R_{TD} = R_{TS} = 100\text{K}\Omega$, $V_{TH} = 0.5139946\text{V}$, $W = 20\mu\text{m}$, $L = 1\mu\text{m}$ and $V_{GG} = 0.5\text{V}$ at $T = 30\text{K}$.

Electrical simulation of the NDR cell was achieved by combining a traditional model for the MOS transistor with the functional model for the single-electron transistor.

Figure 4.17–a shows that voltage n_1 reaches an almost constant value when V_{DD} is larger than the stipulated condition.

The NDR static characteristic (I_D versus V_{DD}) is plotted in Figure 4.17–b. It exhibits several regions of negative slopes which implies locally negative differential resistance. The $i - v$ characteristic of Figure 4.17–b has been contrasted with the results reported in [78, 79], where a steady-state master equation model for the SET was used to simulate a similar NDR cell.

In Figures 4.17–a and –b, the solid line represents the use of our model (second-order) while the dots represent the use of an analytic model [80].

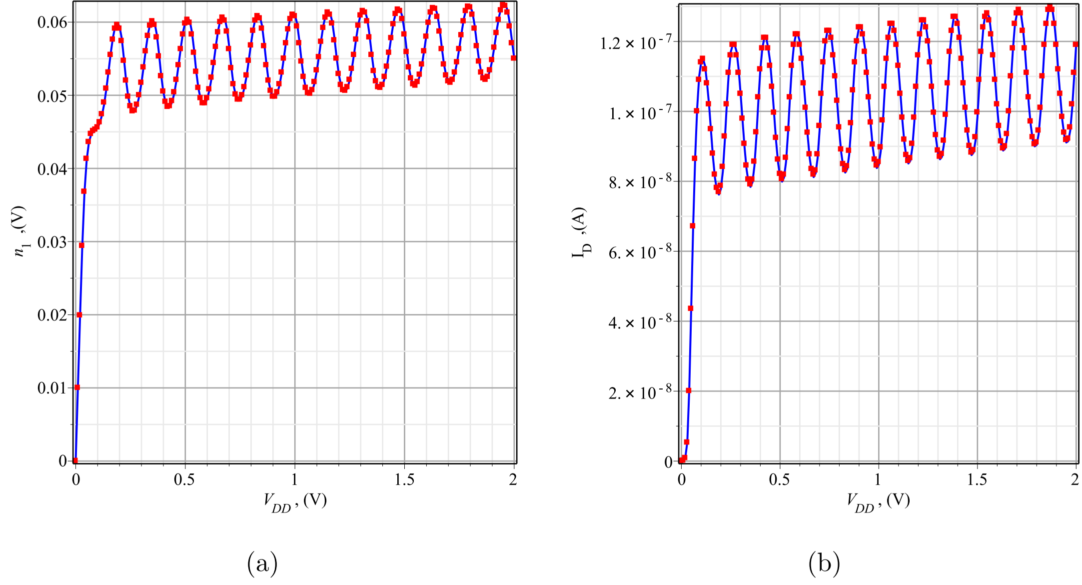


Figure 4.17: Periodic NDR characteristic. (a) n_1 versus V_{DD}. (b) I_D versus V_{DD}.

4.3 Extra

4.3.1 Scalability of runtime

In order to demonstrate the effectiveness of the model developed with the proposed methodology, we performed a runtime scalability using a large size circuit composed of only SET transistors and simulated in a SPICE simulator. The circuit was built using a chain of SET-inverters with a biasing of 30mV to 30mV with a step of 1mV. In Figure 4.18, the biggest test circuit contained 100K SET transistors in a runtime of about half an hour using a model developed with the proposed modeling methodology in this thesis [81] (red line). In order to compare this result, an analysis of the runtime using the MIB model [80] (blue line) takes more than two hours for a chain of only 50K SET transistors.

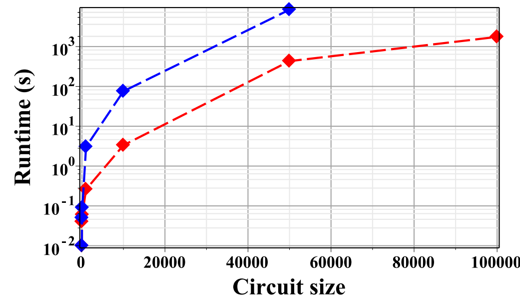


Figure 4.18: Scalability of runtime.

5 Conclusions and future work

5.1 Conclusions

This thesis has tackled an important issue in the context of the problems imposed by simulations techniques by the advent of single-electronics and its coexistence with traditional MOS technology. In a near future, mature MOS circuity must share space with emerging technologies, such as single-electronics.

On one the hand, current circuits simulators are based on the paradigm established by the legendary Kirchhoff's Laws that assume a continuum nature for the electric current. On the other hand, single-electronics is based on the effect of tunneling a single electron that implies a discrete nature of the electric flow. It clearly results that the coexistence of these paradoxical natures in a circuit composed of MOS and single-electron devices must be smartly handled by an appropriate modeling methodology.

This research work introduces a modeling methodology to generate functional models for the single-electron transistor that can be used in an industrial circuit simulation framework in order to simulate hybrid circuits. Functional models resort to mathematical descriptions of the system under analysis that can be easily evaluated and consulted during the iterative process of simulation. Specifically, the functional models introduces in this work are based on the constitutive branch-relationships of SET because they are excellent tools for the complete and detailed description of the device for circuit simulation purposes.

In this thesis, two functional models of the single-electron transistor are presented. The models are aimed for co-simulation of hybrid systems and can be easily coded in a high-level description language.

The most important points of the proposed modeling methodology can be highlighted as:

- The methodology rests on the concept of "a posteriori knowledge" of the device, which is obtained by a starting device-level series of simulations of the SET. This knowledge is translated into a branch-relationship that has a mathematical representation including voltages and currents.

- An appropriate classification of the device parameters that are included in the modeling methodology has been achieved with the aim of deciding if a given parameter contributes with a purely symbolic function or it is treated by a curve-fitting technique.

- The resulting model comes in two flavors, namely a first-order and a second-order model. The first-order model includes a reduced set of variables, and its final expression can be easily evaluated. This model represents a trade-off between accuracy and complexity. In contraposition, the second-order model spans over a larger number of parameters and it has a larger operating range. As a result, the final expression is more complex.

- The models generated in this research work can be coded in a hardware description language. We have chosen VERILOG-A because it is fully compatible with SPICE simulator.

- The thesis reports several single-electronics circuits as well as hybrid circuits. The feasibility of employing the models obtained with this methodology has been verified.

An important point of the proposed modeling methodology is that it can be straightforwardly extended to model other devices, such as single-electronics working at room temperature, NEMS, memristors and devices with dynamic memory. Last but not less, a programming framework was developed for the SET, which can be tailored for modeling these devices.

5.2 Future Work

Further analysis of the SET must include effects of the temperature and asymmetric structure of the device. One line of research is to be able of including the temperature as a variable in the resulting branch-relationships which will be useful not only for the SET, but also for other devices. With respect to asymmetric SETs, a complete symbolic analysis must be carried out by considering different tunnel resistances, altogether with sensitivity, common-mode, and differential-mode analyzes.

Further work can be also focused on avoiding the use of curve-fitting techniques for some SET variables in order to obtain a complete symbolic model. A brute force way of achieving this is empirically,

realizing several simulations, analyzing their tendencies and trying to associate symbolically the device variables with the parameters of the mathematical expression.

Appendices

Automatic Curve Fitting Software - COPYCAT

A.1 Description

As previously mentioned, the behavior of a physical system can be obtained in several ways. A very appeal, it is using the data obtained from direct observation (i.e. experimentally). These data can be expressed by a mathematical equation. The correlation between data and the mathematical equation depends on two ways. First, it is about the election of the kind of the mathematical expression (for instance, polynomial, exponential, among others). Second, it is the selection of the values of the coefficients of the mathematical expression. The COPYCAT tool tries to obtain the coefficients of a mathematical expression that produce the minimum error. The tool gives the mean error over all operation range. The tool use:

- A least squares method in order to adjust the mathematical function to the optimum curve.
- A numerical method of approximation selective in order to work with non-linear functions and to allow quick assessment.
- An homotopy method to ensure finding all minima in order to choose the best (in other words, the minimum of the minima).

A.2 General system operation

A.2.1 Least squares method

This method tries to reduce the mean square error (MSE) between a curve based on numerical data and a mathematical function that model the phenomenon. In order to achieve this, it is finding the parameters (p) that produce the minimum error. The MSE expression is given as:

$$MSE(p) = \sum_{\forall x}^{N} \left(\frac{(M_x - F_x(p))^2}{N} \right) \tag{A.1}$$

where M_x is the value of the numerical data that represent the x conditions, and $F_x(p)$ is the value of the mathematical model when is evaluated in x for the p parameters conditions (see Figure A.1).

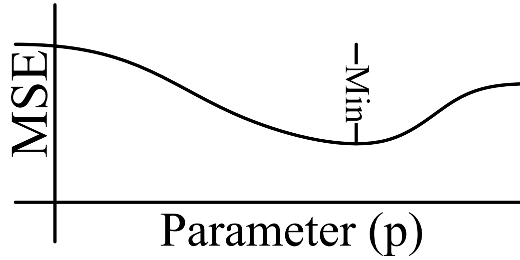


Figure A.1: Illustration of a MSE minimum.

A.2.2 Numerical method of approximation

In order to find a local minimum, a numerical method is used. This method works varying the parameters (p). The values of the p are varying progressively until to find the closest minimum.

The preferred method for determining zeros in nonlinear systems is the Newton-Raphson (NR) method. However, because we are finding the minimum values of an expression of $f(p)^2$ then we use a tangential approximation method (see Figure A.2).

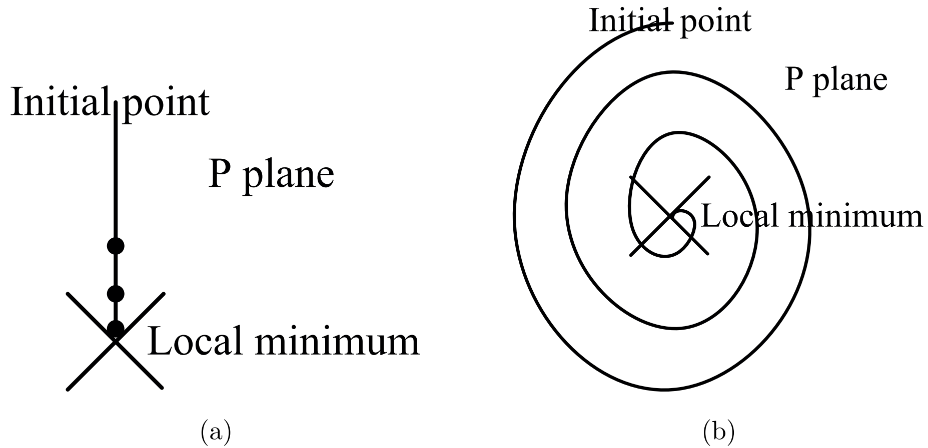


Figure A.2: Illustration of two approximation methods. (a) NR method. (b) Tangential method.

In Table A.1 a comparison of Newton-Raphson vs a tangential approximation is given.

	Newton-Raphson	Tangential approximation
Stability	Almost steady	Steady
Convergence	Quadratic	Linear
Complexity per iteration	Cubic	Linear
Method to find a minimum	Deriving $\frac{dF(x)}{dx}$	Direct evaluation. The method always moves towards a lowest point.
Uniqueness	The method may jump solutions.	The method obtain all solutions.

Table A.1: Comparison of NR and tangential methods.

The tangential method does not resolve all the unknown variables simultaneously rather solves a single variable at a time and creates a new approach. With this new point start, anther unknown variable is solved, tangentially approaching the minimum. The stability of this method does not guarantee the same method, but rather the type of function which must be differentiable at any point. Therefore:

$$\frac{dF(p)^2}{dp} = 2 \cdot F(p) \cdot dF(p) \tag{A.2}$$

ECM is differentiable whenever $F(p)$ is differentiable at any point.

A.2.3 Method for multiple solutions

The method should ensure finding all minimum points and choose the lowest of these. Algorithm is summarized: Under any initial point, it is generated multiples directions of search towards each of the unknown variables. In a R^n plane is generated n search paths. Every time a minimum is found, it is stored and generates n new search paths. If this minimum had been previously recorded, it does not generate more paths.

B

Piece-wise exponential technique

The system modeling tries to describe the behavior that exhibit a physical phenomenon. When a system is highly non-linear is a common practice to split the global behavior in regions where certain effects are dominant. Every region is easily modeled even analytically ignoring the other effects non-dominant. But a problem with using this approach is when the system is working around the edges of the regions where is not well-defined what effect is the dominant. It is possible to think that near of the edges of the regions, the model has a poor accuracy and discontinuities problem in the values and their derivatives.

Although the poor accuracy problem is important, the most relevance is in the treatment of discontinuities because it may produce that the numerical methods of the simulation tools do not converge. As a consequence, it is impossible the use of the models when clearly is unknown the operation region of the system. In order to solve these problems, it is customary to make a deeper modeling to match values and derivatives at the interfaces. This is a task of high complexity and timing consumption.

In this Appendix is presented a new technique to achieve a smooth behavior between the region transitions, which avoid the discontinuities of the values and their derivatives even in regions with strong changes. The technique is based on modulating the models in regions smoothly near to the interface by using the logistic function shown in equation B.1. This function and its complementary function allow to realize a gradual switching between two regions.

$$f(x) = \frac{1}{1 + \exp(-x)} \tag{B.1}$$

This Appendix is organized as follows: in the next section is depicted the proprieties of *the logistic function*, also is defined and analyzed the switching of the models by using the logistic function. In Section III is deduced the general formula to join smoothly many regions by using modulators with a shape of a pulse. In section IV, a case study for the simplest model of the MOS transistor is presented.

B.1 Piece-Wise Exponential Technique

The mathematical technique developed in this appendix is named as Piece-Wise Exponential Technique. This is based on *the logistic function* which was defined in Equation B.1. A double evaluation of this function for values of x in the range of real numbers is shown in Figure B.1.

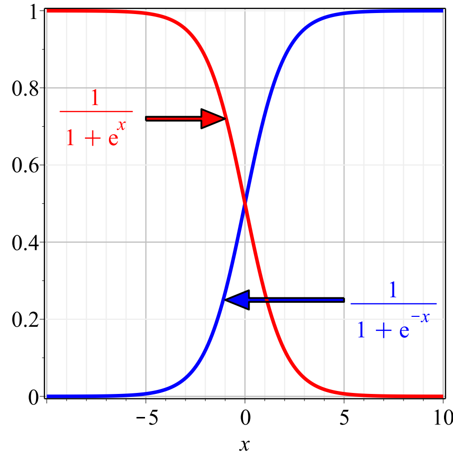


Figure B.1: Evaluation of *the logistic function*.

The range of this function is defined by $0 \leqslant y \leqslant 1$. It is also noteworthy that the curve rises from 0 to 1 (or vice-versa) on a single occasion. The evaluation of this function gives two possible values: zero or one. When this function is zero, the multiplier function is canceled. When the function is one, the multiplier function is preserved.

The abruptness over the commutation can be modified varying *the logistic function* as:

$$f(x) = \frac{1}{1 + \exp(-Sx)} \tag{B.2}$$

where S is a real number. The Figure B.2 shows this change in the base function.

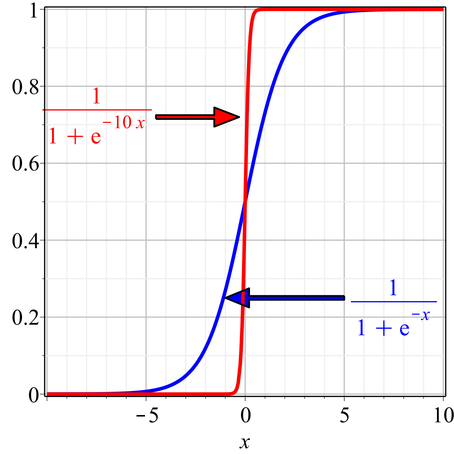


Figure B.2: The *logistic function* varying the abruptness.

Also the position where the transition occurs (breakpoint or BP) can be controlled by the following modification:

$$f(x) = \frac{1}{1 + \exp\left(S\left(-x + BP\right)\right)} \tag{B.3}$$

An example modifying the BP and the abruptness is shown in Figure B.3.

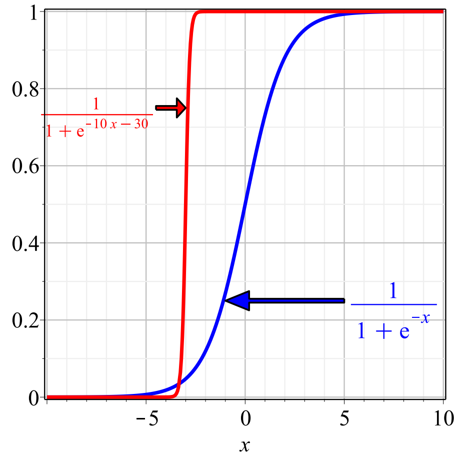


Figure B.3: The *logistic function* varying the abruptness and the breakpoint.

With logistic functions is possible to join a set of functions that are working in different regions. For instance, in the case of joining two functions, it is possible to formulate the equation:

$$f(x) = \frac{F_0}{1 + \exp\left(S\left(x - BP\right)\right)} + \frac{F_1}{1 + \frac{1}{\exp(S(x-BP))}} \tag{B.4}$$

where F_0 and F_1 could be two different functions. It is worth noting that the exponential parts in above equation are always located in a denominator in order to disappear this part when the evaluation of

the exponential causes an overflow. It is very useful when the mathematical expressions are translated into a programming language.

A plain example using Equation B.4 is shown in Figure B.4. In the example, a cubic function is joined by a linear function in a breakpoint of $x = 1$ and abruptness of $S = 100$. Therefore, the example is expressed as:

$$f(x) = \begin{cases} x^3, & x < 1 \\ 3x - 2, & \text{otherwise} \end{cases}$$

After substituting the cubic and the linear function in Equation B.4, the resulting equation is given as:

$$f(x) = \frac{x^3}{1 + \exp\left(100\,(x-1)\right)} + \frac{3x-2}{1 + \frac{1}{\exp(100(x-1))}} \tag{B.5}$$

The evaluation of the above equation is shown in Figure B.4 with a solid line. In the same figure, the dots represent the evaluation of each single function (cubic in red and linear in blue). It is possible to note the smooth transition that has the evaluation of Equation B.4 in the breakpoint ($x = 1$).

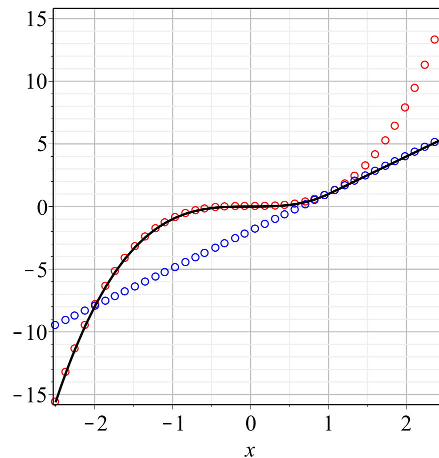


Figure B.4: Cubic and linear functions joined with PWET.

Not only a smooth transition is presented in the original function but also in their respective derivatives as is shown in Figure B.5. In the figure is depicted the first derivative of the Equation B.5, which can be expressed as:

$$f(x) = \frac{3x^2}{1+\exp\left(100\left(x-1\right)\right)} - \frac{100x^3}{2+\exp\left(100\left(x-1\right)\right)+\frac{1}{\exp(100(x-1))}} + \frac{3}{1+\frac{1}{\exp(100(x-1))}} + \frac{100\left(3x-2\right)}{\exp\left(100\left(x-1\right)\right)+\left(1+\frac{1}{\exp(100(x-1))}\right)^2} \tag{B.6}$$

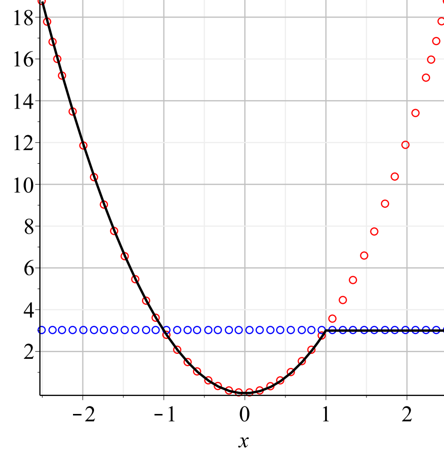


Figure B.5: First derivative of Equation B.5.

B.2 Modulator General Formula

Another way to use the piece-wise exponential technique is to define a unitary pulse function enclosed in a region and multiply this part by the required function. The previous case may be defined as:

$$f\left(x\right) = F_0 \left(\frac{1}{1+\exp\left(S\left(x-BP_1\right)\right)} - \frac{1}{1+\exp\left(S\left(x-BP_0\right)\right)}\right) \tag{B.7}$$

where BP_0 and BP_1 are the edges of the region.

An example of this procedure is shown in Figure B.6, where the PWET is given as:

$$f(x) = \begin{cases} \sin\left(x\right), & -1 < x < 1 \\ 0, & \text{otherwise} \end{cases}$$

Taking an S of 100 for the abruptness and substituting the last conditions in Equation B.7 yields:

$$f\left(x\right) = \sin(2\pi)\left(\frac{1}{1+\exp\left(100\left(x-1\right)\right)} - \frac{1}{1+\exp\left(100\left(x+1\right)\right)}\right) \tag{B.8}$$

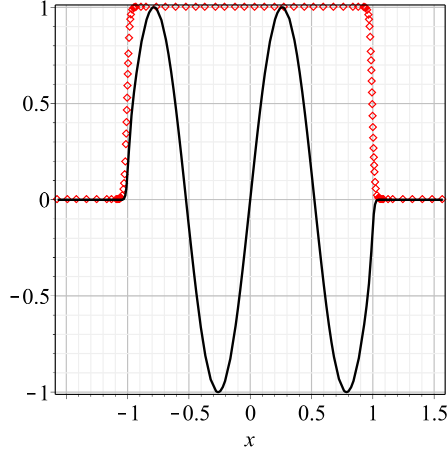


Figure B.6: Sinusoidal function enclosed in a region by using PWET.

An extension of this technique would be using several unitary pulses in order to satisfy each region for the required functions. Mathematically, it can be expressed as:

$$
\begin{aligned}
f(x) = & \frac{F_0}{1+\exp\left(S\left(x-BP_0\right)\right)} \\
& + \sum_{i=1}^{n-1} F_i \left[\frac{1}{1+\exp\left(S\left(x-BP_i\right)\right)} - \frac{1}{1+\exp\left(S\left(x-BP_{i-1}\right)\right)}\right] \\
& + \frac{F_n}{1+\exp\left(-S\left(x-BP_n\right)\right)}
\end{aligned}
\tag{B.9}
$$

In Figure B.7 an example using the last expression is shown under the conditions:

$$
f(x) = \begin{cases}
\sin(x), & x < -10 \\
\frac{x}{10}+1, & -10 < x < -5 \\
\frac{x^2}{20}-1, & -5 < x < 0 \\
-\frac{x}{5}-1, & 0 < x < 5 \\
-2, & 5 < x < 10 \\
\csc(x), & x > 10
\end{cases}
$$

The corresponding equation for this example is given as:

$$
\begin{aligned}
f(x) = & \frac{\sin(x)}{1+\exp(100(x+10))} \\
& + \left(\frac{x}{10}+1\right)\left(\frac{1}{1+\exp(100(x+5))} - \frac{1}{1+\exp(100(x+10))}\right) \\
& + \left(\frac{x^2}{20}-1\right)\left(\frac{1}{1+\exp(100(x))} - \frac{1}{1+\exp(100(x+5))}\right) \\
& + \left(-\frac{x}{5}-1\right)\left(\frac{1}{1+\exp(100(x-5))} - \frac{1}{1+\exp(100(x))}\right) \\
& + (-2)\left(\frac{1}{1+\exp(100(x-10))} - \frac{1}{1+\exp(100(x-5))}\right) \\
& + \frac{\csc(x)}{1+\exp(-100(x-10))}
\end{aligned}
\tag{B.10}
$$

where the abruptness coefficient is $S = 20$.

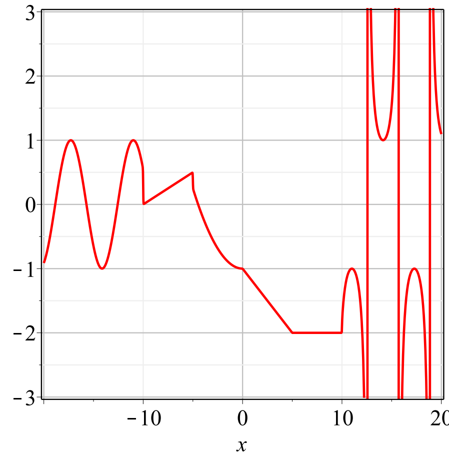


Figure B.7: Multiples functions joined with PWET.

B.3 Case of studies

B.3.1 SPICE model DC diode

The diode is a semiconductor device widely used in electrical circuits. This device works allowing current to move through it in one direction with far greater ease than in the other. If it is necessary to use a diode in an electrical simulator is very common describe it by a model, in fact, the most popular are the SPICE models. One of them (in DC analysis) assume three regions which are defined as:

$$I_D = \begin{cases} I_S\left(\exp\left(\frac{v_D}{nV_T}\right)-1\right)+v_D G_{min}, & -5V_T < v_D \\ -I_S + v_D G_{min}, & -BV < v_D < -5V_T \\ -I_S\left(\exp\left(-\frac{BV+v_D}{nV_T}\right)-1+\frac{BV}{V_T}\right), & v_D \leq BV \end{cases}$$

where V_T is the thermal voltage ($\approx 26m$V at 300K), I_S is the saturation current, n the emission coefficient, G_{min} is the minimum conductance, and BV is the breakdown voltage.

Taking into account these regions and using the PWET the resulting equation is given as:

$$\begin{aligned} f(x) = & \frac{I_S\left(\exp\left(\frac{v_D}{nV_T}\right)-1\right)+v_D G_{min}}{1+\exp\left(S\left(v_D - BV\right)\right)} \\ & + \left(-I_S + v_D G_{min}\right)\left[\frac{1}{1+\exp\left(S\left(v_D-5V_T\right)\right)} \right. \\ & \left. - \frac{1}{1+\exp\left(S\left(v_D-BV\right)\right)}\right] \\ & + \frac{-I_S\left(\exp\left(-\frac{BV+v_D}{nV_T}\right)-1+\frac{BV}{V_T}\right)}{1+\exp\left(-S\left(v_D-5V_T\right)\right)} \end{aligned} \tag{B.11}$$

For this case of study we select the next values: $I_S = 10^{14}$, $n = 1$, $V_T = 26mV$, $G_{min} \approx 3.836127 \times 10^{-13}$ and a $BV = 50$ in order to evaluate the above equation. The evaluation is then shown in Figure B.8. In the left, a close-up is done over the left junction of the functions.. Besides, on the right, another close-up is done to observe the remain junction of the functions. The abruptness for this case is $S = 100$.

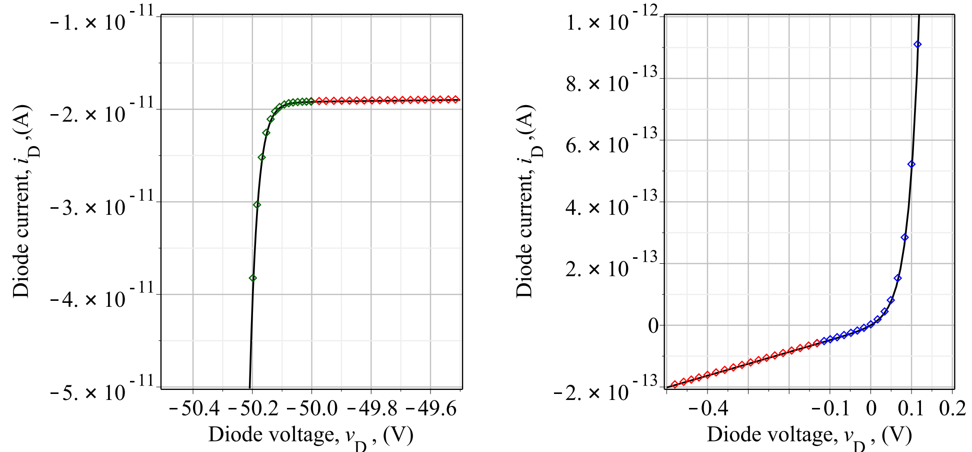


Figure B.8: Left: negative exponential function (green dots) joined with a linear function (red dots). Right: a linear function (red dots) joined with a positive exponential function (blue dots). Continuous line depicts the use of the PWET.

B.3.2 MOSFET transistor

The MOSFET transistor is the most used semiconductor device in integrated circuits due to high-density integration. It has three terminals and its operation depend on the biasing applied in them. The simplest model used to define the behavior of the drain current (I_D) of this device has three operation regions that are: cutoff, triode, and saturation.

In the first region, the transistor is turned off. Therefore, there is no conduction between drain and source, which means that the drain current is ideally zero. In the second region, the transistor is turned on, and a channel of charge carrier has been created between the drain and the source terminals, which allows current flow for it. In this region, the behavior of the transistor is like a resistor controlled by the gate voltage relative to both the source and drain voltages. Finally, in the third region, the channel has reached a saturation of charge carriers and, therefore, a constant current is established.

The mathematical formulation of the above-mentioned regions for an enhancement NMOS transistor is:

CONDITION TO CONDUCTION	OPERATION REGION
No channel $v_{GS} < V_{tn}$	Cutoff region $i_D = 0$
Channel induced $v_{GS} = V_{tn} + v_{OV}$	Triode region ($v_{GD} > V_{tn}$) $i_D = \kappa_n^{'} \left(\frac{W}{L}\right) \left[(v_{GS} - V_{tn}) v_{DS} - \frac{1}{2} v_{DS}^2\right]$
	Saturation region ($v_{GD} \leq V_{tn}$) $i_D = \frac{1}{2} \kappa_n{'} \left(\frac{W}{L}\right) (v_{GS} - V_{tn})^2$

Table B.1: Basic operation regions of the enhancement NMOS transistor.

where v_{GS} is the gate-to-source voltage, v_{DS} is the drain-to-source-voltage, V_{tn} is the threshold voltage of the NMOS transistor, $\kappa_n^{'}$ is defined as the process transconductance parameter ($\kappa_n^{'} = \mu_n C_{ox}$, where μ_n is the mobility of the electrons in the induced n channel and C_{ox} is the oxide capacitance), W and L are the width and the length of the channel region and v_{OV} is the overdrive voltage (denoted by $V_{GS} - V_t$).

In order to use the technique developed here, we consider the next parameters of a NMOS transistor: $L = 0.18 \mu m$, $W = 0.2 \mu m$, $C_{ox} = 8.6 fF/\mu m^2$, $\mu_n = 450 cm^2/V{\cdot}s$ and a $V_{tn} = 0.5V$. The corresponding PWET taking a abruptness of $S = 100$ expression is:

$$
\begin{aligned}
f(x) \quad = \quad & \frac{i_D = \kappa_n^{'}\left(\frac{W}{L}\right)\left[\left(v_{GS}-V_{tn}\right)v_{DS}-\frac{1}{2}v_{DS}^2\right]}{1+\exp\left(100\left(v_{DS}-v_{OV}\right)\right)} \\
& + \frac{i_D = \frac{1}{2}\kappa_n{'}\left(\frac{W}{L}\right)\left(v_{GS}-V_{tn}\right)^2}{1+\frac{1}{\exp(100(v_{DS}-v_{OV}))}}
\end{aligned} \tag{B.12}
$$

In Figure B.9 the triode region (red circles) and the saturation region (blue circles) are shown in a separate way. Also in the figure, the evaluation of Equation B.12 is depicted. In this case, the triode and saturation regions are joined and show a smooth transition (black line).

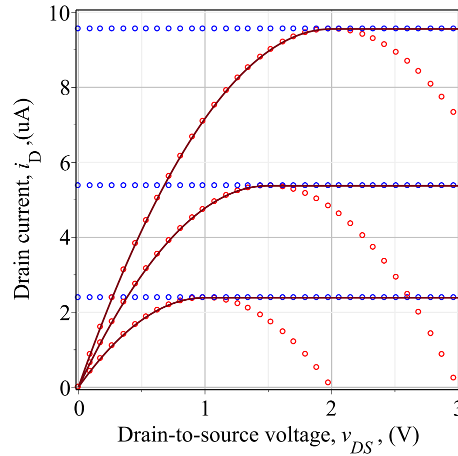


Figure B.9: Triode and linear regions of a MOSFET joined with PWET.

B.4 Conclusion

This Appendix has presented a technique for post-production for the global model of a physical system. This is useful in system where the behavior can be divided into regions with a single dominant effect. The technique joins and achieves a single model with smooth transitions in their interfaces.

EXTRAS

C.1 Tool to sweep the variables of the SET

This Section depicts the functioning of the tool that allow to sweep the variables of the SET. The tool has a graphical interface in order to be friendly to the user. Its parts are explained as follows:

- **Environment variable.** This variable cannot be swept because in each netlist of SIMON is only specified one time. The unit is the Kelvin.
- **Electrical variables.** In this part two variables can be swept; the drain-to-source voltage; V_{DS} and the grate-to-source voltage; V_{GS}. Both variables are specified with an initial and a final value. Besides, the number of samples are specified. Only the V_{DS} variable can be swept in a linearly or logarithmically way. The unit used is the Volt.
- **Design variables.** The set of design variables available to sweep are the gate capacitance; C_G, the source tunnel junction capacitance and resistance; C_{TS} and R_{TS}, and the drain tunnel junction capacitance and resistance; C_{TD} and R_{TD}. There are two options to define their values: if the "uni ratio" is selected they take only the start value. Otherwise, they will need a final value and consequently is possible to define the number of samples. The sweep can be expressed by a linear or logarithmic form. The units are Farads for the capacitance and Ohms for the resistance.
- **COMPUTE Button.** It computes the number of samples after the SIMON simulation, and it is shown in the "TextField Data Number".
- **MAKE Button.** It generates three files according to the name put into the "TextField Data Number":
  1. ***.INFO File** It contains information about the swept variables in a list form.
  2. ***.HEAD File** It contains an array of all possible combinations of the variables.

3. ***.SET File** It is the file used by the SIMON simulation.

- **EXIT Button.** It closes the program.

The **INFO** and the **HEAD** files may be used to built an input stage that could help to the analysis stage.

NOTE: Because the front-end was developed in a Windows Environment, then, the resulting **SET** file has the same codification. If the SIMON software works in a Linux environment, then the **SET** file must be changed to Linux format as follows:

```
unix2dos file.set file.set
```

C.2 Chain of inverters

The following netlist can be used to simulate a chain of inverter for the cases of 1, 5, 500, 1K, 5K, 10K, 20K, 40K, 80K inverters.

```
******************** Chain of inverters ********************
.HDL neq992.va
.op

vin in  0  dc 30m
vd  dd  0  dc 30m
vs  ss  0  dc -30m

* 1 Inverter
.subckt inv2 in2 out2 dd2 ss2
  x2a  dd2 in2 0 out2 set RT=100e6 CG1='1*1e-18'
  x2b out2 in2 0  ss2 set RT=100e6 CG1='1*1e-18'
.ends

* 5 Inverters
.subckt inv5 in5 out5e dd5 ss5
  x5a in5   out5a dd5 ss5 inv2 * 1 Inverters
  x5b out5a out5b dd5 ss5 inv2 * 2 Inverters
  x5c out5b out5c dd5 ss5 inv2 * 3 Inverters
  x5d out5c out5d dd5 ss5 inv2 * 4 Inverters
  x5e out5d out5e dd5 ss5 inv2 * 5 Inverters
.ends

* 50 Inverters
.subckt inv50 in50 out50j dd50 ss50
  x50a   in50 out50a dd50 ss50 inv5 *  5 Inverters
  x50b out50a out50b dd50 ss50 inv5 * 10 Inverters
  x50c out50b out50c dd50 ss50 inv5 * 15 Inverters
  x50d out50c out50d dd50 ss50 inv5 * 20 Inverters
  x50e out50d out50e dd50 ss50 inv5 * 25 Inverters
  x50f out50e out50f dd50 ss50 inv5 * 30 Inverters
```

```
  x50g out50f out50g dd50 ss50 inv5 * 35 Inverters
  x50h out50g out50h dd50 ss50 inv5 * 40 Inverters
  x50i out50h out50i dd50 ss50 inv5 * 45 Inverters
  x50j out50i out50j dd50 ss50 inv5 * 50 Inverters
.ends

* 500 Inverters
.subckt inv500 in500 out500j dd500 ss500
  x500a   in500 out500a dd500 ss500 inv50 *  50 Inverters
  x500b out500a out500b dd500 ss500 inv50 * 100 Inverters
  x500c out500b out500c dd500 ss500 inv50 * 150 Inverters
  x500d out500c out500d dd500 ss500 inv50 * 200 Inverters
  x500e out500d out500e dd500 ss500 inv50 * 250 Inverters
  x500f out500e out500f dd500 ss500 inv50 * 300 Inverters
  x500g out500f out500g dd500 ss500 inv50 * 350 Inverters
  x500h out500g out500h dd500 ss500 inv50 * 400 Inverters
  x500i out500h out500i dd500 ss500 inv50 * 450 Inverters
  x500j out500i out500j dd500 ss500 inv50 * 500 Inverters
.ends

* 1K Inverters
.subckt inv1K in1K out1Kb dd1K ss1K
  x1Ka   in1K out1Ka dd1K ss1K inv500 *  500 Inverters
  x1Kb out1Ka out1Kb dd1K ss1K inv500 *   1K Inverters
.ends

* 5K Inverters
.subckt inv5K in5K out5Ke dd5K ss5K
  x5Ka   in5K out5Ka dd5K ss5K inv1K * 1K Inverters
  x5Kb out5Ka out5Kb dd5K ss5K inv1K * 2K Inverters
  x5Kc out5Kb out5Kc dd5K ss5K inv1K * 3K Inverters
  x5Kd out5Kc out5Kd dd5K ss5K inv1K * 4K Inverters
  x5Ke out5Kd out5Ke dd5K ss5K inv1K * 5K Inverters
.ends

* 10K Inverters
.subckt inv10K in10K out10Kb dd10K ss10K
  x10Ka   in10K out10Ka dd10K ss10K inv5K *  5K Inverters
  x10Kb out10Ka out10Kb dd10K ss10K inv5K * 10K Inverters
.ends

* 20K Inverters
.subckt inv20K in20K out20Kb dd20K ss20K
  x20Ka   in20K out20Ka dd20K ss20K inv10K * 10K Inverters
  x20Kb out20Ka out20Kb dd20K ss20K inv10K * 20K Inverters
.ends

* 40K Inverters
.subckt inv40K in40K out40Kb dd40K ss40K
  x40Ka   in40K out40Ka dd40K ss40K inv20K * 20K Inverters
  x40Kb out40Ka out40Kb dd40K ss40K inv20K * 40K Inverters
.ends

* 80K Inverters
```

```
.subckt inv80K in80K out80Kb dd80K ss80K
  x80Ka   in80K out80Ka dd80K ss80K inv40K * 40K Inverters
  x80Kb out80Ka out80Kb dd80K ss80K inv40K * 80K Inverters
.ends

x1 in out dd ss inv2
.dc vin -30m 30m 1m

.alter
x5 in out dd ss inv5
.alter
x50 in out dd ss inv50
.alter
x500 in out dd ss inv500
.alter
x5K in out dd ss inv5K
.alter
x1K in out dd ss inv1K
.alter
x10K in out dd ss inv10K
.alter
x20K in out dd ss inv20K
.alter
x40K in out dd ss inv40K
.alter
x60K in out dd ss inv60K
.alter
x80K in out dd ss inv80K

.end
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