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Charge trapping and de-trapping in Si-nanoparticles embedded in silicon oxide films

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Electrical properties of silicon nanoparticles (Si-np's) embedded in a silicon oxide matrix were studied using MOS-like structures. Si-np's were created after silicon rich oxide (SRO) films were thermally annealed at 1100 ºC. Capacitance–voltage (C–V) characteristics showed downward and upward peaks in the accumulation region. Current–voltage (I–V) measurements exhibited current valleys and downward and upward peaks. Current versus time (I–t) measurements were also done at a negative constant gate voltage. A switching behaviour between two current states (ON and OFF) was observed. These effects have been related to the charge trapping and de-trapping of the Si-np's embedded in the SRO films.

1 Introduction The study of silicon at nanometric scale in the form of silicon nanoparticles (Si-np's) has increased during last decade. Light emitting devices (LED) [1], single electron memories, [2] and UV photodetectors [3] are some of their interesting demonstrated devices. These potential applications have recently been of great interest for many researchers. Single electron charging effects in Si-np's have been also studied; however, these effects are usually observed at very low temperature [4]. Such effects could be obtained at room temperature if Si-np's were small enough (<10 nm), in such a way that the charging energy for adding one electron to a Si-np becomes larger than the thermal energy (>26 meV) [5], and single electron memories could be done. These quantum effects has been observed in the form of current peaks and discrete steps and associated with charge trapping into and de-trapping from nanoparticles [5].

Several different techniques are used in order to fabricate materials with embedded Si-np's including chemical vapor deposition (CVD), silicon implantation into thermal silicon dioxide, SiO_2/SiO multilayers, etc. [1-3, 5-7]. However, compatible techniques with complementary metal oxide semiconductor (CMOS) are preferred. In this work, the charge trapping and de-trapping properties of Si-np's embedded in silicon rich oxide (SRO) films deposited by LPCVD and using MOS-like structures are presented. The electrical characterization done at room temperature revealed important results such as downward and upward peaks in the accumulation capacitance. Current wells and downward and upward peaks were also observed. These effects are explained by Coulomb blockade effects between charges trapped in Si-np's.

2 Experimental

Metal–oxide–semiconductor (MOS) structures were fabricated in order to study the charge trapping properties of silicon nanoparticles embedded in SRO films. 25 nm thick SRO films were deposited on p type silicon wafers ((100)-oriented, resistivity 0.1–1.4 Ω-cm) by low pressure chemical vapor deposition (LPCVD). The silicon excess is easily controlled by $R_0 = P(N_2O)/P(SiH_4)$, the ratio of partial pressure of the reactant gases (N_2O and SiH_4). $R_0 = 30$ was used for this experiment. After deposition, a thermal annealing at 1100 ºC in N_2 atmosphere was carried out for 180 minutes in order to induce the silicon excess agglomeration. A 100 nm thick SRO film was also deposited and

thermally annealed in the same type of substrates in order to observe the silicon agglomeration by measuring the photoluminescence (PL) response. The estimated silicon excess of the SRO films is ~4 at.% [6]. All devices feature 1μm thick Al/Cu backside contacts and a 350 nm thick n+ polysilicon gate with an area of 9.604×10^{-3} cm^2.

Room temperature PL was carried out with a Perkin Elmer luminescence spectrometer model LS50B controlled by computer. The sample was excited using a 250 nm radiation and the emission signal was collected between 400 and 900 nm with a resolution of 2.5 nm. A cut-off filter to pass only wavelengths above 430 nm was used to block the light scattered from the source.

High frequency capacitance–voltage (C–V) measurements were performed at 100 kHz using a computer-controlled Keithley 590 C–V analyser. Current–voltage (I–V) measurements were performed using a computer-controlled Keithley 2400 source meter. Electrical stress was applied between the gate electrode and the back contact. All the electric measurements were carried out at room temperature in dark.

3 Results and discussion The SRO film shows a PL peak centered at about 716 nm after thermal annealing, as shown in Fig. 1. It is widely accepted that visible red emission observed in silicon rich oxide films after annealed in high temperature is related to the presence of embedded silicon nanoparticles (Si-np's) [6, 7]. Therefore, the PL peak observed in Fig. 1 indicates that Si-np's were created after the annealing process in the present studied SRO films.

The charge trapping and de-trapping effects in SRO films were analyzed by capacitance versus voltage (C-V) measurements. Figure 2 shows the C–V curves of the MOS-like structures measured with voltage scanned from inversion to accumulation at different sweep rates. When the sweep was done at a rate of 0.1 V/s, a downward valley was observed in the capacitance between -4.5 and -6.5 V. As the gate voltage becomes more negative, the capacitance tends to increase to a maximum value. However, after voltage is even more negative, the capacitance decreases in an abrupt way until 500 pF.

For a sweep rate of 0.05 V/s, the maximum capacitance value is not reached, but a downward valley is observed at a lower capacitance value and at a lower voltage. Afterwards, the capacitance tends to rise as the negative gate voltage becomes larger, but finally decreases.

When the sweep rate is reduced to 0.01 V/s, the accumulated capacitance jumps to a lower value at a small voltage of about -0.5 V. The silicon agglomeration in the form of Si-np's inside of this SRO film could be creating conduction paths between the substrate and polysilicon gate. Therefore, these effects would be associated with the charge trapping and de-trapping in the Si-np's during the voltage sweep. A possible explanation will be discussed later.

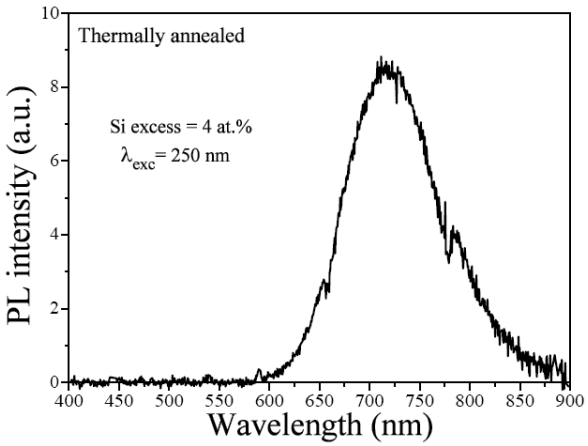

Figure 1 PL spectra measured from thermally annealed 100 nm thick SRO film.

Figure 3 shows the I-V curves from the MOS-like devices at different sweep rates. Different anomalies such as current jumps, downward and upward current peaks were observed.

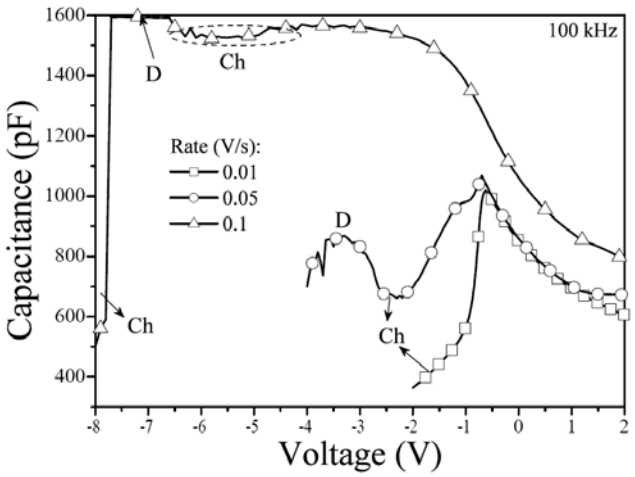

Figure 2 C–V curves of MOS-like devices at different sweep rates.

For a fast sweep (0.1 V/s), the current shows a strong dependence on voltage until it drops almost by 4 orders of magnitude at -5.8 V. The dropping in current would correlate with that abrupt reduction of capacitance observed in Fig. 2. The strong increasing of current could be related to flow of charge through uncharged Si-np's embedded in the SRO film.

For a sweep rate of 0.05 V/s, the current reduces appearing some downward and upward peaks between -2 and -4 V until a current jump is observed at -4.2 V. For a slow sweep rate (0.01 V/s), the current decreases even more and some current valleys (Coulomb blockade) with different widths appeared. For this sweep rate, a current jump is observed at -4 V, as well. A clear relation between the charge trapping and the sweep rate is observed.

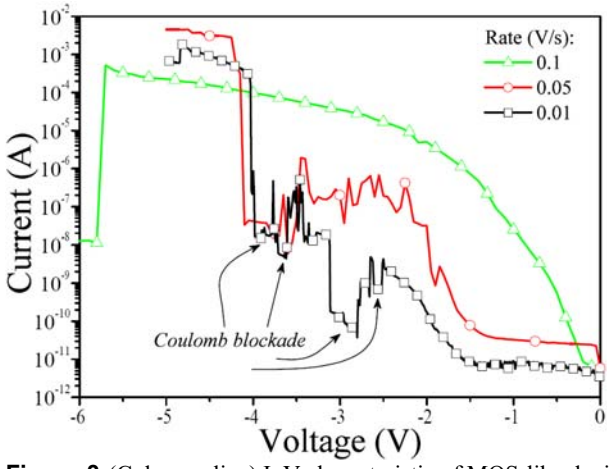

Figure 3 (Colour online) I–V characteristic of MOS-like devices at different sweep rates.

The total capacitance (C_T) of the MOS-like structure is given by the combination of the capacitance of the SRO film (C_{SRO}) in series with the capacitance of silicon substrate surface (C_S) as Eq. (1):

$$C_T = \frac{C_{SRO} \cdot C_S}{C_{SRO} + C_S} \quad (1)$$

In negative gate voltages (V_G<0), an accumulation of holes at the substrate surface is obtained. Then C_S is much higher than C_{SRO}. From Eq. (1), the total capacitance is now related to the SRO capacitance as $C_T = C_{SRO}$. Therefore, the anomalies observed in the C-V curve in Fig. 2 would be related to changes in C_{SRO}.

It is well known that a phase separation between silicon and silicon dioxide is created after a thermal annealing is applied to silicon rich oxide films [6, 7]. Moreover, a visible red emission in the 100 nm thick SRO film was observed. Therefore, silicon nanoparticles inside of the SRO films have been formed for this experiment.

As mentioned before, the embedded Si-np's in the SRO films could explain the observed effects since they could form conductive paths between the gate and the silicon substrate, as shown by rows in Fig. 4(a).

During the voltage sweep, when V_G is negative, holes accumulate at the substrate surface meanwhile electrons do in the polysilicon gate. These charges, whether electrons or holes tunnel into the SRO film through such conduction paths. Charges close to Si-np's can get trapped in the Si-np's and if charge-trapping occurs, some conduction paths will be blocked, as shown in Fig. 4(b) (marked by black dots). In this case, the current will decrease as a result of the Coulomb blockade effect.

At a fast sweep rate (0.1V/s), most of the carriers can transport through the entire SRO layer because they do not have enough time to get trapped in Si-np's. However, at a slow sweep rate (0.01 V/s) and when the bias is larger than a threshold value, charge-trapping will occur and in this case, most of the conduction paths will be blocked, making the capacitance has a lower value.

In order to clarify the charge trapping in the SRO films; we have also measured the current as a function of time for a constant gate voltage of V_G = -4 V, as shown in Fig. 5. A clear charge trapping and de-trapping effect is observed in form of a current switching between ON and OFF states. The current is about 6.8×10^{-5} and 1.4×10^{-3} A for OFF and ON switching states, respectively.

A similar switching behaviour was observed when the gate voltage was V_G = -4.5 V, as shown in the inset of Fig. 5. For this voltage, the OFF and ON switching states were about 1 and 3 mA, respectively. Then, the charge trapping or de-trapping in some Si-np's, leads to the blocking or formation of some conduction paths and then the increasing or reduction of current, respectively.

4 Conclusion The C-V and I-V characteristics of SRO films with Si-np's embedded were studied. Charge trapping and de-trapping effects were observed in the capacitance and current. I-t measurements demonstrated a switching behaviour of conductive paths between ON and OFF states. These effects were related to Coulomb blockade effect produced by charge trapping and de-trapping in the Si-np's which form conductive paths between the Si-substrate and the polysilicon gate.

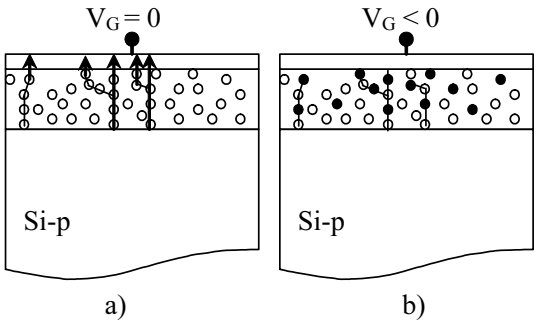

Figure 4 Schematic of the MOS-like structures with Si-np's embedded forming conductive paths (a). In (b), white and black dots correspond to uncharged and charged Si-np's, respectively.

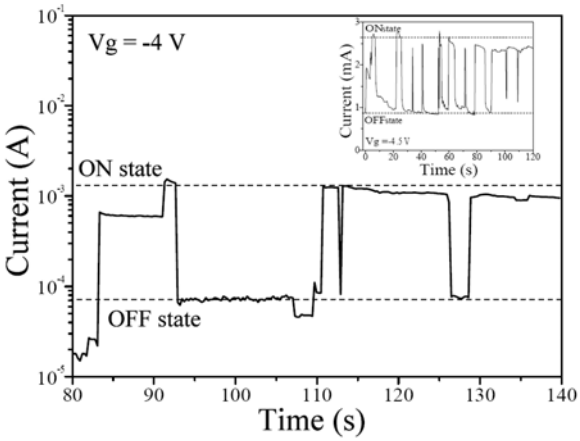

Figure 5 Current through the SRO films as a function of time for a gate voltage of V_G = -4 V. Inset shows the I-t curve measured at V_G = -4.5 V.

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