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# A Test Generation Methodology for Interconnection Opens Considering Signals at the Coupled Lines

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**Abstract** Interconnection opens have become important defects in nanometer technologies. The behavior of these defects depends on the structure of the affected devices, the trapped gate charge and the surrounding circuitry. This work proposes an enhanced test generation methodology to improve the detectability of interconnection opens. This test methodology is called OPVEG. OPVEG uses layout information and a commercial stuck-at ATPG. Those signal values at the coupled lines which favor the detection of the opens, under a boolean based test, are attempted to be generated. The methodology is applied to four ISCAS85 benchmark circuits. The results show that a significant number of considered coupled signals are set to proper logic values. Hence, the likelihood of detection of interconnection opens is increased. The results are also given in terms of the amount of coupling capacitance having logic conditions favoring the defect detection. This shows the OPVEG benefits. Furthermore, those lines difficult to test can be identified. This information can be used by the designer to take design for test measures.

**Keywords** Interconnection opens · Coupling capacitances · Boolean testing · Favorable logic conditions · Test generation methodology

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## 1 Introduction

Opens in interconnection paths disconnect the driven gate(s) from the driving gate. Due to the break the Pmos and Nmos transistors connected gates of the driven gate (s) float. From experiments made on ISCAS'85 benchmark circuits, it has been found that interconnection opens have the highest probability of occurrence among the different types of opens [37]. Vias are also a likely place for an open to occur [7, 28] and the number of vias has become greater than the number of transistors in some large IC's such as microprocessors [36]. Random particle induced-contact defects is the main test target in production testing [2]. Break defects have been found to be an important contributor of test escapes [25]. In damascene-copper process vias and metal are patterned and etched prior to the additive metalization. Because of this micro-masking during the next lithography step can occur [33]. The open density in copper shows a higher value than those found in aluminum [33].

The behavior of interconnection open defects has received significant attention in the past years [4, 12, 14, 16–19, 21, 22, 26, 27]. Some circuits with these defects may work logically correctly at low frequencies, but fail at higher frequencies [12, 26]. Other researchers have observed a stuck-at behavior and negligible quiescent current values for an inverter with a given interconnection open defect [22]. Makki et al. [21] have made measurements on intentionally-designed defective circuits. They have found defect coverages of 90.9% and 90.6% for $I_{DDQ}$ and transition fault logic testing, respectively. Konuk [16, 17] have analyzed the testability of interconnection opens under a voltage (stuck-at) and current based tests. Using Spice pre-simulations and

analytical expressions the detectability of interconnection opens is investigated. Interconnection opens may also present oscillations and sequential behavior under certain conditions [19]. Diagnosis of opens using physical information has been addressed in [29, 31, 40]. Spinner et al. [32] have developed a simulation approach for open-via defects. They use a segmentation fault model [29, 31, 32, 40]. Rodriguez et al. [30] shows that gate tunneling impacts the behavior of CMOS circuits with full open defects.

Let us focus more specifically in prior work dealing with the influence of coupling signals on the behavior of interconnect opens which is the subject of this paper. Konuk [16, 17] models the effect of coupling signals on interconnect opens. The interaction between opens and coupling signals is analyzed by Moore et al. [23]. They give conditions to test opens in the context of delay fault testing. Logic conditions at the coupling for favoring the detection of interconnect opens by logic testing have been analyzed by Zenteno et al. [4, 39]. Ghosh et al. [8] proposed a method that uses the probability of detecting interconnect opens applying randomly selected $n$ stuck-at 0 and $n$ stuck-at 1 tests for each fault location. They uses a statistical model that uses the length distribution of the surrounding wires instead of their logic values. Gomez et al. [10] proposed to obtain an enhanced test vector set for interconnect opens applying favorable logic conditions at the coupling lines using a stuck-at test generator. A recent paper [35] proposed a method for generating test for open faults by using a stuck-at fault test with do not cares. Adjacent lines are considered. Arumi et al. [1] doing measurements in a fabricated chip show the influence of coupling capacitances with adjacent lines on the electrical behavior of the defective line.

In this work an enhanced test generation methodology, using a boolean based test [11], to improve the detectability of interconnection opens is proposed. The testability of interconnection open defects is enhanced by applying proper logic levels at the coupled lines to the defective one [10]. In this way, proper signal values at the coupled lines which favor the detection of the opens are attempted to be generated. The tool uses layout information and a commercial ATPG (automatic test pattern generator). Those lines difficult to test can be identified. Using this information the designer can take some DFT (design for testability ) measures.

The rest of the paper is organized as follows: in Section 2 a fault model for the interconnection opens is presented. In Section 3, the influence of coupling signals over floating lines is analyzed. In Section 4, the proposed test vector generation methodology is presented. In Section 5, the results of applying the proposed methodology to four ISCAS85 benchmark circuits are presented. In Section 6, a case showing the detectability of an interconnection open using a conventional ATPG and the proposed strategy in this work is analyzed. In Section 7, critical cases for which is not possible to generate favorable test vectors are identified. Finally, in Section 8 the conclusions of the work are given.

## 2 Modeling of Interconnection Opens

In this work large breaks are considered so there is non-significative influence from the input signal on the floating line (e.g. tunneling effect [12, 20]). The behavior of the defective gate(s) is determined by the induced voltage on the floating line ($V_{if}$). This voltage depends on technology and topology parameters [12, 14, 16, 18, 19, 22, 26, 27, 39].

In Fig. 1 the main factors influencing the behavior of the interconnect open are shown. $C_r^0$ ($C_r^1$) is the part of the routing capacitance with one terminal connected to $V_{\mathrm{GND}}$ ($V_{\mathrm{DD}}$). The loading gates influence the floating line with the parasitic overlap capacitances ($C_{\mathrm{gdon}}$, $C_{\mathrm{gson}}$, $C_{\mathrm{gdop}}$, $C_{\mathrm{gsop}}$), intrinsic gate charge ($Q_{\mathrm{GT}}$) [17] of the transistors connected to the floating line and

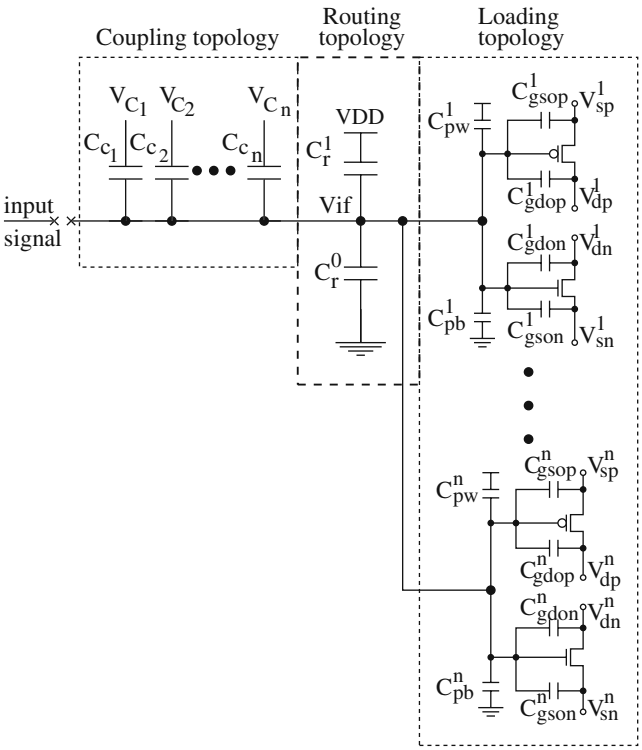


**Fig. 1** Electrical model of an interconnect open considering several loading gates

poly-bulk/well capacitances ($C_{pb}$, $C_{pw}$) of each transistor connected to the floating line. The voltages at the drain/source terminals of the transistors ($V_{sn}$, $V_{dn}$, $V_{sp}$, $V_{dp}$) connected to the floating line need to be determined. These voltages depends on the actual test pattern and the gate topology. Furthermore they may depend on the history of the gate [17]. $C_{C_1}$ to $C_{C_n}$ are the capacitances coupled to the floating line. Their terminal voltages $V_{C_1}$ to $V_{C_n}$ depend on the actual test pattern. This will be further discussed in the next section. The behavior of a gate with an interconnect open also depends on the trapped gate charge deposited during fabrication ($Q_{tr}$) whose value is difficult to predict. The trapped gate charge builds up a voltage at the floating gate called "trapped gate voltage" [14, 17].

## 3 Coupling Signal Influence on Interconnection Opens

The floating line can be influenced by signals running at adjacent coupling lines and/or by lines located above/below the floating line (see Fig. 2). The capacitance of adjacent lines can significantly influence the voltage at the floating node in modern technologies. This coupling capacitance can exceed 70% of the total capacitance [13]. As the technology scales, to avoid degrading interconnect resistance, the vertical dimension of wires is being scaled more slowly compared to the horizontal dimension. Hence, for the same metal level the ratio of coupling capacitance between lines to the total capacitance tends to increase [6]. Furthermore, in higher levels of interconnections the capacitance of adjacent lines is more pronounced due to increased wire thickness and the reduction of the substrate capacitance [38].

The signals at the coupled lines may have a high logic value ($V_{DD}$) or a low logic value ($V_{GND}$). The logic state at the coupled signals influences significantly the behavior of interconnection open defects. In Fig. 3, a floating line influenced by three signals through the coupling capacitances is shown. The first coupling capacitance has a value of 0.35 fF, the second one has a higher value (1.5 fF) and the third one has a value even higher (2.35 fF). Let us assume that an input vector for a stuck-at zero fault at the open is applied. Different possible exciting conditions at the coupling signals have been considered (see Fig. 4). For $V_{C1}V_{C2}V_{C3}$ = 000 the voltage at the floating node is low, and the output is at a high logic level (see Fig. 4). Hence the interconnection open defect is detected for these exciting conditions. The voltage at the floating node increases when a high logic level is applied at the coupling signal(s). As a consequence the value of the output voltage is lowered. Furthermore, for $V_{C1}V_{C2}V_{C3}$ = 111 the voltage at the floating node increases significantly, and the output goes low. Hence the interconnect open is non-detected. These results show the importance of applying proper logic conditions at the coupling signals to be able to detect an interconnection open defect.

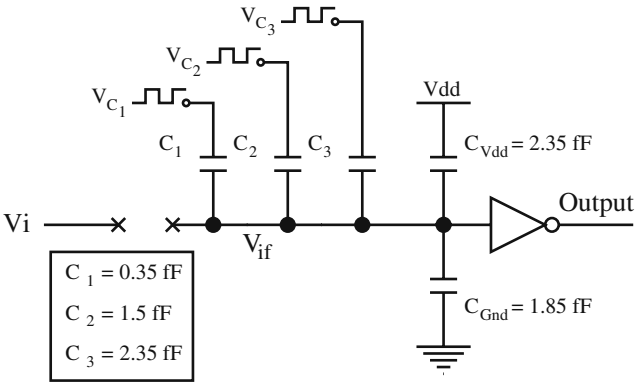


**Fig. 3** Interconnection open with three coupled lines

Let us summarize the detection conditions for interconnection opens. The circuit shown in Fig. 5 is considered. For testing a SA-0 at the interconnection open 0's at the coupling signals favor detection of the open defect. This is because the coupled signal(s) pulls to a lower level the voltage at the floating line. Hence, the voltage at the floating line is more likely to be interpreted as a low logic level which is the wrong logic value for the applied input vector. This most favorable exciting condition corresponds to the case of $V_{C1}V_{C2}V_{C3}$ = 000 shown in Fig. 4. In the other hand 1's at the coupling signals make the open more difficult to detect. This is because the coupled signal(s) pulls to a higher level the voltage at the floating node. Hence, the voltage at the floating line may be interpreted as a high logic level which is the correct logic value. The worst case exciting condition corresponds to the case $V_{C1}V_{C2}V_{C3}$ = 111 shown in Fig. 4. The same is true for testing the interconnection open assuming an SA-1 fault but the logic values are opposite. The most favorable exciting conditions at the coupling signals and assured detection voltage ranges at the floating line are

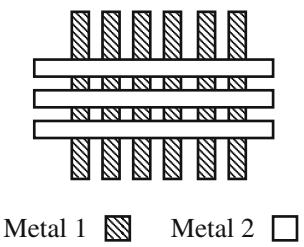


**Fig. 2** Adjacent and vertical coupling lines

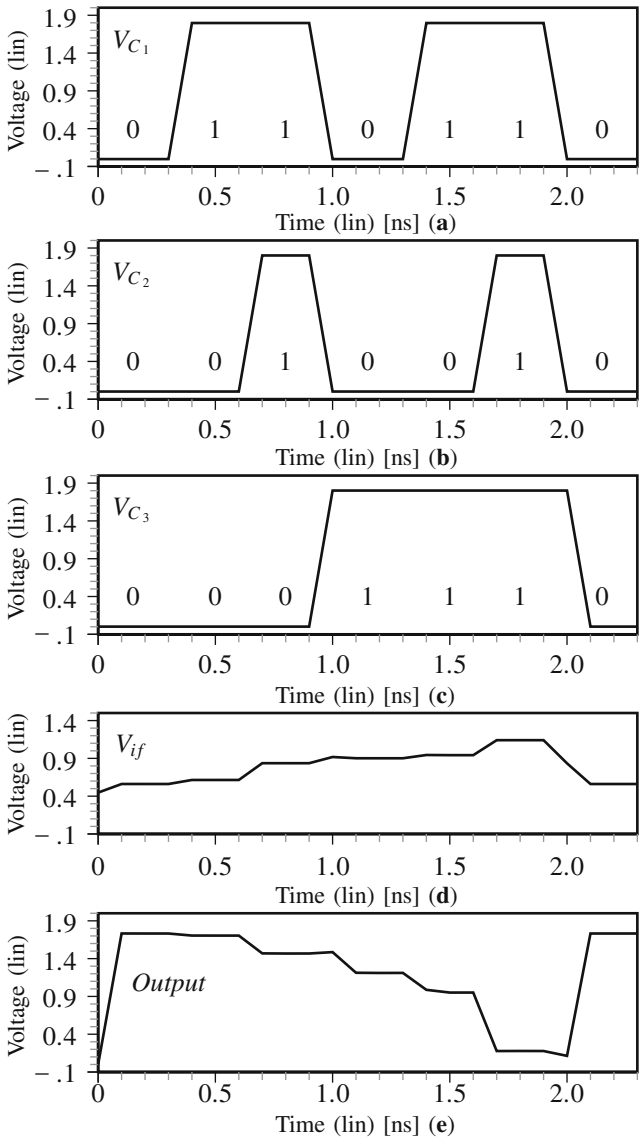


**Fig. 4** Waveforms for the circuit shown in Fig. 3 under different exciting conditions

given in Table 1. Controllable coupling signals from $V_{C1}$ to $V_{CN}$ are assumed.

## 4 Test Vector Generation Methodology for Interconnection Opens

The test vector generation methodology attempts to obtain favorable logic conditions at the coupled signals. This methodology has been implemented in a test framework tool called OPVEG (Opens Vector Generator). OPVEG also allows to identify those critical cases which have non-favorable conditions. Using this information, DFT techniques can be applied for improving detectability of interconnection open defects.

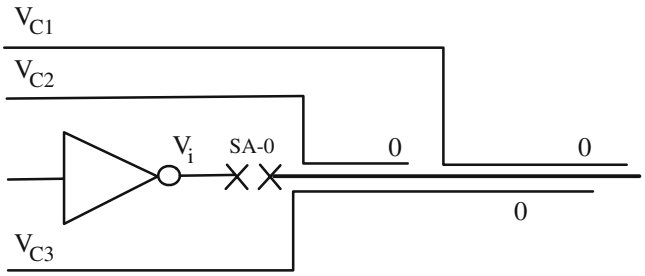


**Fig. 5** Favorable signals coupling influence for detection of an interconnection open under an SA-0 vector

The simplified flowchart of OPVEG is shown in Fig. 6. OPVEG uses information obtained from a circuit layout and a commercial ATPG tool [34]. The input files are the Verilog description of the circuit, coupling extracted capacitances and node equivalence names of the Verilog file and the file of extracted capacitances. The coupling capacitances have been obtained from the circuit layout using Cadence design tools [3]. In the first step (see Fig. 6) the coupling capacitances to each node are identified. Also, the capacitances of each node to VDD and GND are obtained. In the second step, the critical lines (*candidate lines*) affected by significative values of coupling capacitances are selected. This will be further explained in the next paragraph. The lines influencing to the candidate lines are also identified. In the third step, Tetramax ATPG tool [34] is run for the *candidate lines* imposing logic constraint values in the lines coupled to the candidate lines. The constraint values correspond to the most favorable conditions to detect the interconnection opens. In this way a test vector set for testing interconnection opens under favorable conditions is obtained. This is a supplemental vector set to the set obtained using conventional ATPG.

**Candidate lines and Selection Factor** The layout information of all the interconnect lines can be obtained from the physical design. The strengths of the drivers handling a line under analysis and the coupled lines are not important when large breaks are considered. Most VLSI chips contains a huge number of pairs of lines with non-zero coupling capacitance values [24]. In the ISCAS'89 benchmark circuit s38584 the total number

**Table 1** Most favorable test conditions and assured detection ranges

| $V_i$ | $V_{C1}$ ... $V_{CN}$ | Detectable range $V_{if}$ | Fault |
|---|---|---|---|
| 0 | 1 ... 1 | $[V_{DD} - \|V_{TP}\|, V_{DD}]$ | SA-1 |
| 1 | 0 ... 0 | $[0, V_{TN}]$ | SA-0 |

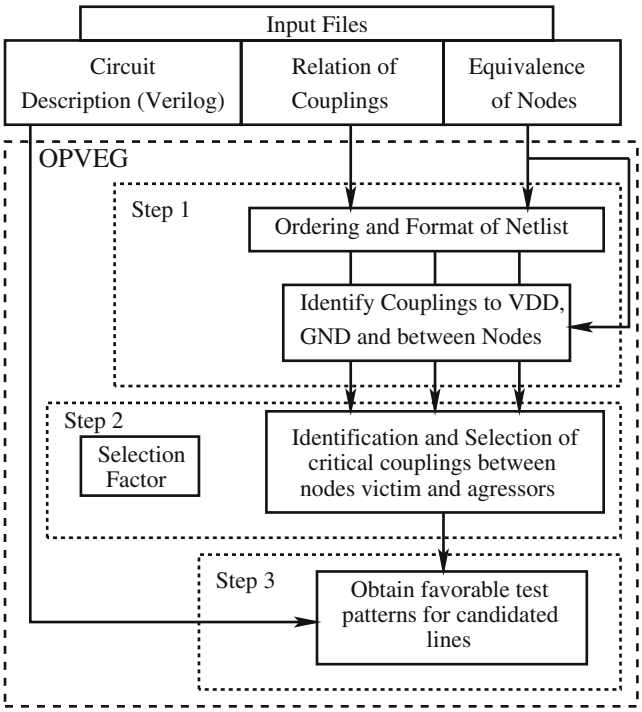


**Fig. 6** Simplified flowchart of OPVEG

of aggressor and victim lines pairs is over 400 million [15]. Test generation for lines under crosstalk effects is a computationally intensive process [5]. Because of this only those lines susceptible (*candidate lines*) to be significantly influenced by their coupled signals are considered for test process generation using OPVEG.

The total capacitance ($C_T^{if}$) of a line ($if$) is composed by its capacitance to ground $C_{\text{GND}}^{if}$ and to the power supply $C_{VDD}^{if}$. A line is considered as candidate when the following condition is satisfied for at least one coupled line:

$$C_c^{if} \geq f\left(C_{\text{GND}}^{if} + C_{VDD}^{if}\right) \tag{1}$$

where $C_c^{if}$ is a coupling capacitance to the line under analysis and $f$ is the *selection factor*.

In other words a line is considered as candidate when it has at least one coupling capacitance equal or greater than $C_T^{if}$ multiplied by the Selection Factor. The previous equation gives a quick measure on how the voltage at the floating line is impacted by the voltage at the coupled signal. The Selection Factor determines the set of candidate lines, and also determine those couplings that are considered for each candidate line. In this way the signals with coupling capacitance values equal or higher than $fC_T^{if}$ are considered for test process generation. The ATPG tool attempts to obtain an input vector forcing favorable logic values (*constraints*) at the considered coupled signals of the selected candidate lines. Constraints are only imposed on the selected coupled lines. A simple algorithm is used for running ATPG for the different constraints of a candidate line. The algorithm gives priority to the signals with higher coupling capacitance values [9].

The Selection Factor can take values between 0 and 1 (0 and 100%). The number of candidate lines and selected coupled signals for ATPG process increases (decreases) as the Selection Factor decreases (increases). Because of this there is a trade-off between the computational time and the improvement on the defect coverage of interconnection opens. We are actually working in a Fault Simulator for interconnect opens to determine the value of the Selection Factor according to the desired defect coverage.

## 5 Application and Results

OPVEG has been used to obtain favorable vectors for interconnection opens in four ISCAS 85 benchmark circuits. These circuits have been designed using standard design layout techniques [9]. *Chip assembly router* from Cadence [3] has been used for automatic place and route. First, a conventional ATPG has been run for the four ISCAS85, the fault coverage is up of 99% for all the circuits except C499 which it has a coverage of 97%. Then, ATPG is run for the selected candidate lines imposing favorable conditions at the considered coupled signals. Different selection factors have been considered. In TetraMAX [34], it has been used the default number for maximum number of allowed iterations.

The results of applying OPVEG to the ISCAS benchmark circuits are given in terms of: (a) measuring the number of favorable logic conditions at the coupling signals (logic effectiveness), and (b) measuring the amount of coupling capacitance under the favorable logic condition (coupling capacitance effectiveness).

### 5.1 Logic Effectiveness

The benefits of OPVEG in terms of the obtained favorable logic conditions at the coupled lines is analyzed. To account this the metric *logic effectiveness* has been defined. This metric gives a measure about how successful is the test process generation for obtaining favorable logic constraints at the considered coupled lines. This

process is carried-out for the selected lines. This metric is calculated as follows:

$$\text{Logic}_{\text{eff}} = \frac{\sum_{n=0}^{t} \frac{G_n}{P_n}}{t} x100 \quad (2)$$

where,

$G_n$: is the number of considered couplings of a candidate line having favorable conditions for the generated test vector.
$P_n$: is the number of considered couplings of a candidate line obtained by a selection factor.
$t$: is the total number of possible stuck-at faults of the candidate lines. Note that two vectors are generated for each candidate line, one for the stuck-at 0 and the other for the stuck-at 1 fault.

The results obtained for the four ISCAS 85 benchmark circuits are given in Table 2. It can be observed that the number of considered critical faults, which is equal to twice the number of candidate lines, increases as the selection factor decreases. This is because it is more likely that for a lower selection factor appears at least one coupled capacitance equal or higher to the sum of its capacitances to $V_{DD}$ and GND multiplied by the selection factor. The number of considered coupled lines also increases for a lower selection factor. It has been found than a significant number of vectors (*generated vectors*) are generated with at least one favorable logic condition at the coupling signal. The column *compacted vectors* shows the set of vectors obtained deleting repeated vectors (from *generated vectors*) and also deleting those vectors contained in the conventional ATPG process. From the column of *compacted vectors*, it can be stated that most of the generated vectors do not appear in the conventional ATPG process. For the considered selection factors, the generated vectors obtained with all the most favorable test conditions (*Vectors 100% OK*) is high. This depends on the type of analyzed circuit. The *logic effectiveness* gives a more realistic metric of the number of test constraints that were successfully generated. This is high for the analyzed ISCAS 85 benchmark circuits. This means than a high number of values of the coupled signals are forced successfully to the favorable test vector condition.

The computer times for obtaining favorable test vector conditions are given in Table 3. The set of candidate lines can be minimized by selecting only those lines with significative coupling capacitance values. This reduces the computer time.

The *logic effectiveness* of interconnection opens under significant coupling capacitances for the conventional stuck-at ATPG is given in Table 4. Only the case of a selection factor of 100% is considered. It can be observed that the *logic effectiveness* of the conventional stuck-at ATPG is significantly lower than that using OPVEG.

### 5.2 Coupling Capacitance Effectiveness

The benefits of OPVEG in terms of the amount of coupling capacitance having a logic condition favoring the open detection by the stuck-at vectors are analyzed. Two metrics have been defined.

The first metric gives the amount of coupling capacitance under the favorable logic condition considering both stuck-1 and stuck-0 vectors for each candidate line. This metrics is called *coupling capacitance effectiveness* and it is calculated as follows:

$$C_{\text{eff}}^{sa} = \left( \sum_{n=0}^{tl} \frac{C_n^0}{C_T} + \sum_{n=0}^{tl} \frac{C_n^1}{C_T} \right) x100 \quad (3)$$

where,

$C_n^0$: is the amount of coupling capacitance (all the capacitance coupled to the floating line is accounted

**Table 2** Logic effectiveness for four ISCAS 85 benchmark circuits using OPVEG vectors

| Circuit | Selection factor | Critical faults | Generated vectors | Compacted vectors | Vectors 100% OK | $Logic_{eff}$ |
|---|---|---|---|---|---|---|
| C432 | 100% | 32 | 27 | 27 | 24 | 79.7% |
| | 60% | 88 | 73 | 71 | 67 | 79.9% |
| | 20% | 320 | 298 | 226 | 229 | 82.8% |
| C499 | 100% | 48 | 38 | 23 | 37 | 78.1% |
| | 60% | 158 | 137 | 72 | 129 | 83.2% |
| | 20% | 418 | 388 | 240 | 311 | 85.5% |
| C1908 | 100% | 20 | 17 | 17 | 17 | 85.0% |
| | 60% | 104 | 95 | 82 | 92 | 89.9% |
| | 20% | 428 | 421 | 326 | 386 | 92.5% |
| C2670 | 100% | 206 | 197 | 155 | 187 | 93.3% |
| | 60% | 408 | 373 | 310 | 355 | 89.6% |
| | 20% | 1454 | 1318 | 1067 | 1130 | 85.2% |

**Table 3** Computer time for the ISCAS 85 benchmark circuits

| Circuit | Selection factor | Time of selection of nodes (m:s) | CPU usage | Time of ATPG stuck-at-0(m:s) | CPU usage | Time of ATPG stuck-at-1(m:s) | CPU usage |
|---|---|---|---|---|---|---|---|
| C432 | 100% | 00:46 | 42% | 00:36 | 94% | 00:30 | 94% |
| | 60% | 00:45 | 45% | 01:43 | 94% | 01:41 | 94% |
| | 20% | 00:41 | 47% | 15:42 | 93% | 10:51 | 95% |
| C499 | 100% | 01:25 | 50% | 00:51 | 89% | 00:45 | 89% |
| | 60% | 01:26 | 49% | 03:08 | 94% | 02:59 | 92% |
| | 20% | 01:44 | 41% | 22:32 | 95% | 16:51 | 89% |
| C1908 | 100% | 03:00 | 43% | 00:19 | 86% | 00:20 | 91% |
| | 60% | 02:56 | 44% | 01:41 | 93% | 01:41 | 93% |
| | 20% | 03:12 | 41% | 11:28 | 93% | 11:14 | 94% |
| C2670 | 100% | 52:48 | 34% | 04:22 | 94% | 04:08 | 93% |
| | 60% | 50:53 | 41% | 11:15 | 86% | 09:53 | 89% |
| | 20% | 43:40 | 48% | 49:17 | 94% | 46:04 | 94% |

for) of a candidate line under the favorable logic condition for the stuck-at 0 vector.

$C_n^1$: is the amount of coupling capacitance of a candidate line under the favorable logic condition for the stuck-at 1 vector.

$C_T$: is the total amount of coupled capacitance of a candidate line *tl*: is the number of candidate lines.

The results obtained using this metric are given in the third column of Table 5 for different selection factors. It can be observed that the favorable coupling capacitance increases for a lower value of the selection factor. The coupling capacitance effectiveness is in the range between 70% and 80%.

The second metric is called *modified coupling capacitance effectiveness* ($C_{\text{eff}}^{sa*}$). In this metric, for each candidate line only the coupling capacitance for the vector contributing most to the coupling capacitance effectiveness is computed. This metric is calculated as follows:

$$C_{\text{eff}}^{sa*} = \sum_{n=0}^{tl} \frac{C_n^{0/1}}{C_T} x100 \tag{4}$$

where,

$C_n^{0/1}$ is amount of coupling capacitance of a candidate line under the favorable logic condition for the vector contributing most to the coupling capacitance effectiveness.

**Table 4** Logic effectiveness using a conventional stuck-at ATPG process

| Circuit | Critical faults | Generated vectors | Stuck-at ATPG effectiveness (%) |
|---|---|---|---|
| C432 | 32 | 30 | 46.8 |
| C499 | 48 | 62 | 48.8 |
| C1908 | 20 | 41 | 52.5 |
| C2670 | 206 | 44 | 54.4 |

Selection factor = 100%

The results obtained for the ISCAS85 benchmark circuits are given in the fourth column of Table 5 for different selection factors. Again, the favorable coupling capacitance increases as the value of the selection factor decreases. The *modified coupling capacitance effectiveness* decreases significantly with respect to the previous metric. Actually, this metric gives a more realistic measure of the detectability of interconnection opens.

The *modified coupling capacitance effectiveness* is also given for four ISCAS85 benchmark circuits using test vectors obtained with a conventional ATPG test process (see Table 6). A selection factor of 100% has been considered. It can be observed that the *modified coupling capacitance effectiveness* using OPVEG is higher than that using conventional test vectors.

**Table 5** Capacitance coupling effectiveness using OPVEG vectors

| Circuit | Selection factor (%) | $C_{\text{eff}}^{sa}$ (%) | $C_{\text{eff}}^{sa*}$ (%) |
|---|---|---|---|
| C432 | 100 | 89.01 | 65.40 |
| | 60 | 89.97 | 69.35 |
| | 20 | 93.52 | 74.68 |
| C499 | 100 | 89.18 | 73.18 |
| | 60 | 90.95 | 75.86 |
| | 20 | 94.07 | 79.13 |
| C1908 | 100 | 81.25 | 72.73 |
| | 60 | 86.06 | 75.74 |
| | 20 | 88.16 | 78.70 |
| C2670 | 100 | 75.01 | 65.55 |
| | 60 | 85.13 | 70.37 |
| | 20 | 89.42 | 73.81 |

**Table 6** Capacitance coupling effectiveness using a conventional stuck-at ATPG process

| Circuit | $C_{eff}^{sa}$ (%) | $C_{eff}^{sa*}$ (%) |
|---|---|---|
| C432 | 72.17 | 57.59 |
| C499 | 81.80 | 64.67 |
| C1908 | 73.69 | 65.86 |
| C2670 | 67.54 | 57.17 |

Selection factor of 100%

## 6 Simulation Electrical Results in ISCAS Circuit

In this section, electrical simulation (Hspice) results in ISCAS C499 using both vectors obtained by conventional ATPG and OPVEG are shown. The selected line for this analysis and its surrounding circuitry is shown in Fig. 7. The line has two coupled lines. The values of the capacitances of the coupled lines are indicated in Fig. 7. The total capacitance of the floating line is 1.7fF.

The vector generated for a stuck-at 1 fault at this line using conventional ATPG process is:

00000000000000000000000000000000010010011

And the vector obtained using OPVEG is:

00000000000001000000000000000000000111011

Logic simulation has been made to the circuit ISCAS C499 using the previous vectors. It has been found that the vector obtained by the conventional ATPG applies the two non-favorable test conditions to detect a stuck-at 1 fault at the selected line. In other words the logic values at the coupled lines M2/E28/Y and ID[13] (see Fig. 7) are 00. An electrical simulation of the circuit shown in Fig. 7 shows that the voltage at the floating node is pulled down by the effect of the coupled signals (see Fig. 8). Hence the, interconnection open is non-detected. However, the most favorable logic conditions at the coupled lines to put an evidence the defect are generated by OPVEG. The logic values of M2/E28/Y and ID[13] (see Fig. 7) are 11. In this case, the interconnection open is detected (see Fig. 8).

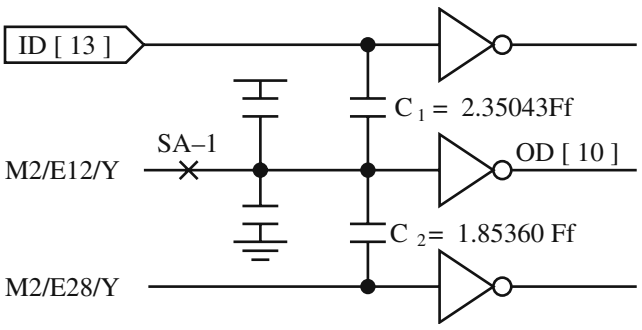


**Fig. 7** Analyzed section of ISCAS C499

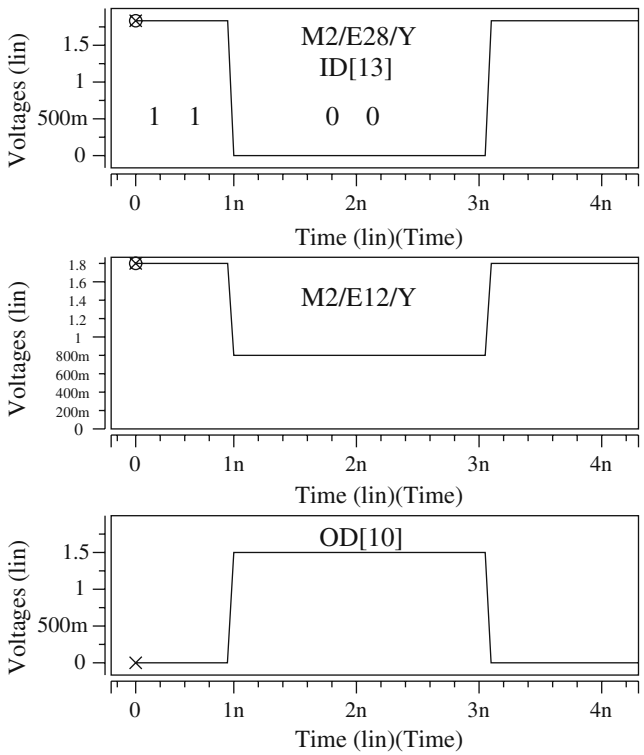


**Fig. 8** Electrical simulation of the circuit shown in the previous figure using the favorable and unfavorable test conditions. Zero Volts as initial condition at the floating line has been assumed

## 7 Identification of Critical Cases

OPVEG allows to identify those candidate lines for which favorable logic conditions can not be generated. Using this information DFT measures can be taken [9, 39]. Critical cases depend on the circuit topology surrounding the candidate line. Two cases may appear: a) Non-observable Case, and b) Non-controllable Case.

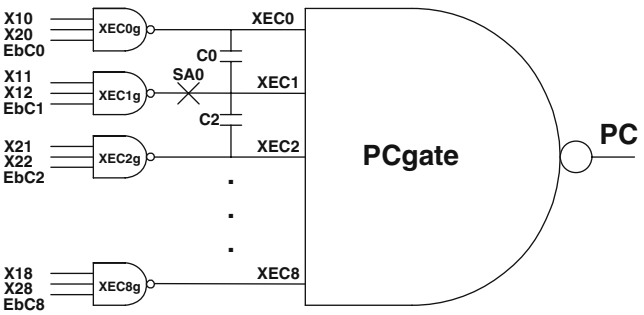


**Fig. 9** A non-observable case located in module M3 of the ISCAS C432

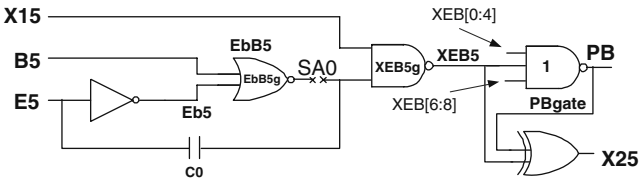


**Fig. 10** A non-controllable case located in module M2 of the ISCAS C432

### 7.1 Non-observable Case

A non-observable case appears when it is not possible to propagate the fault-effect from the candidate line under favorable logic conditions. An example of this case has been found for the gate named PCgate (see Fig. 9) of module M3 in the ISCAS C432. An open defect in line XEC1 (see Fig. 9) is considered. For generating a favorable vector for a SA-0 fault at line XEC1, the signals at XEC0 and XEC2 should be at 0 logic. However, these conditions do not propagate the fault effect to the output of PCgate. Hence, the conventional vector for a SA-0 fault would be used to test this open. Note that the vector for a SA-1 fault can still be used but it is not considered for this analysis.

### 7.2 Non-controllable Case

A non-controllable case appears when it is not possible simultaneously to sensitize the fault and to have favorable conditions at the coupled signals. An example of this case has been found for one input of the gate XEB5g (see Fig. 10) of module M2 in the ISCAS C432. An open defect in line EbB5 (see Fig. 10) is considered. For generating a favorable vector for a SA-0 fault at line EbB5, the signal at E5 should be at 0 logic. However, a 0 logic at E5 does not sensitize the fault.

## 8 Conclusion

A test vector generation methodology, called OPVEG, to improve the detectability of interconnection opens by applying proper logic levels at the coupled signals has been proposed. OPVEG uses layout information and a commercial stuck-at ATPG. The methodology has been applied to four ISCAS85 benchmark circuits. Most of the generated vectors using OPVEG do not appear in the set of vectors obtained with the conventional ATPG process. The logic effectiveness is high for the analyzed ISCAS 85 benchmark circuits. For the considered selecting factors, the percentage of generated vectors with all the most favorable test conditions is between 70% and 90% depending on the type of analyzed circuit. The second metric *coupling capacitance effectiveness* shows the benefits of OPVEG in terms of the amount of coupling capacitance under the favorable logic condition. The *coupling capacitance effectiveness* using OPVEG is significantly improved with respect to that obtained using conventional test vectors. The number of considered candidate lines can be minimized by selecting only those lines with significant coupling. Based on this our approach is non-exhaustive. However, the testability of interconnection opens is enhanced because those nodes with significant coupling capacitances are considered. Furthermore, those nodes difficult to test can be identified. This information can be used by the designer to take design for test measures.

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