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Pulse characteristics of silicon double barrier optical sensors with signal amplification

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Abstract

The pulse characteristics of optical sensors with double potential barriers formed on the opposite sides of a high-resistivity (ν) silicon substrate have been studied. The first barrier is formed by multiple micro-sized Ti–νSi contact barriers surrounded by Ti–SiO_2–νSi MOS structures. The second one is the ν–n^+ potential barrier formed at the bottom of the wafer. The structure presents signal amplification for both polarities of the applied voltage. Under negative bias applied to the semi-transparent Ti-electrode, the reason of the current gain is the change in the transport mechanism of carriers through the potential barrier of the Schottky barrier along its perimeter, which is due to the strong electric field originated by the photogenerated minority carriers forming an inversion layer at the silicon-oxide interface. Under positive bias, the current gain is due to the operation of the ν–n^+ potential barrier, which was studied earlier, and in this work it is used for comparison purposes.

Keywords: Optical sensors; Silicon; Signal amplification; Double barrier structures

1. Introduction

The conception of obtaining signal amplification in silicon optical sensors with multiple micro-sized Schottky diodes (SD) surrounded by metal-oxide-silicon (MOS) capacitors, or with the potential barrier formed by contacts of lightly (ν) and heavily doped (n^+) silicon, was reported recently [1,2]. In both cases significant photocurrent amplification takes place. For the multiple micro-sized SDs surrounded by MOS capacitors it was supposed that the photocurrent gain occurs due to the modulation of the barrier height along the periphery of the SDs by the positive charge of the photogenerated holes accumulated at the insulator/Si interface. This accumulated charge induces a sharp-edge electrostatic field along the perimeter of the SDs. This electric field gives rise to a significant reduction of the ITO–Si potential barriers, leading to an additional electron flow from the ITO film into the silicon, when the structure is irradiated. The photocurrent amplification in such structures was found to be lower than the amplification in structures with the ν–n^+ potential barrier. In this work we discuss the difference between these two devices when they operate under pulse irradiation.

2. Design of the sensors and experimental setup

Double barrier structures with SDs and ν–n^+ contacts were fabricated on the opposite sides of the same high-resistivity (ν) silicon substrate. The design of the optical sensor is shown in Fig. 1.

The sensors were fabricated on a high-resistivity (2–5 kΩ cm) ν-type 250 μm thick silicon substrate (1). Multiple 10 μm × 2000 μm strip lines of Ti–νSi SDs were formed by depositing a semi-transparent titanium film (3) on an etch-patterned SiO_2 layer (2) fabricated by thermal oxidation of the silicon wafer; the thickness of this SiO_2 layer is 60 nm. The transparency of the 9 nm thick titanium film deposited on a glass substrate presented a quite uniform value of about 55% from the visible to the near infrared range.

At edges of etched SiO_2 layer, the discontinuity of the Ti film was not observed because the silicon oxide was chemically etched (Fig. 11 in Section 4). In Fig. 1, one can see that the complete structure is formed by a parallel connection of multiple micro-sized SDs and the MOS capacitors surrounding these SDs. The second potential barrier (4), the ν–n^+ contact, is formed at

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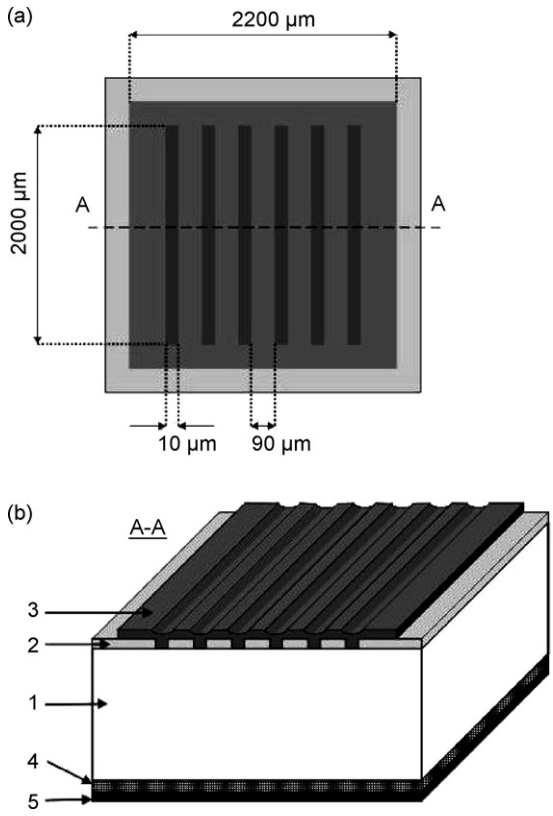

Fig. 1. Design of the double barrier silicon optical sensor: (a) top view and (b) cross-section A–A view.

the bottom of the silicon substrate by phosphorus diffusion and the deposition of an Al film (5).

For the measurements, the structure was connected in series with a constant voltage source and a load resistor (R_L). A two-channel digital oscilloscope with a preamplifier was used for recording the time-dependent current characteristics at different voltages under both, dark and irradiated conditions. A light emitting diode (LED), with a wavelength of 930 nm, was used for characterizing the structure under pulse irradiation.

3. Experimental part

The oscillogram in Fig. 2 shows the time dependence of the voltage (Ch1) applied to the structure, as well as the dependence of the output signal (Ch2) on the load resistor, $R_L = 100\ \Omega$, obtained under pulse irradiation from a near infra-red LED ($\lambda = 930$ nm). The output characteristics obtained for a linear voltage ramp from -2 V to $+2$ V is almost symmetric; this quasi-ohmic behavior was because the heights of both potential barriers (Ti–νSi and νSi–n^+Si) have approximately the same value (0.43–0.45 eV). This is usual for structures fabricated on high-resistive substrate having two contacts that inject majority carriers [3]. The response to the pulse irradiation became apparent as photocurrent pulses.

The value of the experimental photocurrent is higher than that from a usual one-photon optical sensor, in which not more than one electron–hole pair is created after the absorption of

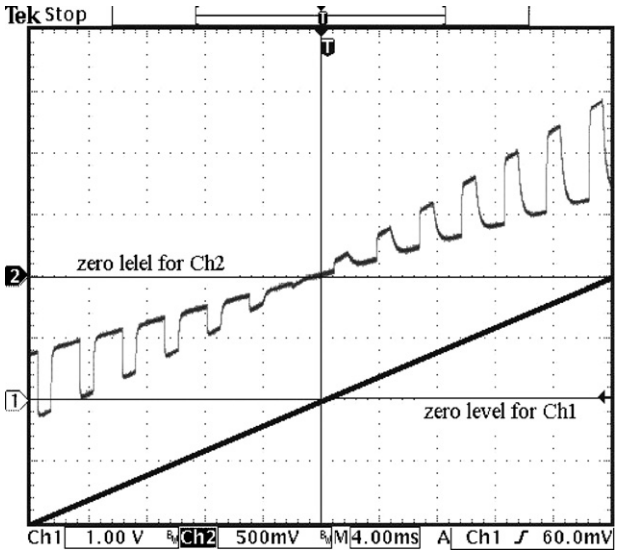

Fig. 2. Time dependence of the voltage ramp (Ch1) applied to the structure, and dependence of the output signal (Ch2) on the load resistor ($R_L = 1$ kΩ) obtained under pulse irradiation.

one photon. Thus, the photocurrent gain takes the place for both polarities of the voltage applied to the structure.

For the structure biased with a constant voltage source and irradiated with the LED, the photocurrent gain (M) was estimated as the ratio of the photocurrent of the biased structure to that obtained under short circuit conditions (the photocurrent I_{ph}^{SD} of SDs without amplification). The relevancy of such estimation for the photocurrent gain was verified with a specially fabricated Ti–νSi discrete 2 mm × 2 mm SD (not surrounded by a SiO_2 layer) operating under short circuit conditions, as well as under negative voltage bias. Fig. 3 shows the photocurrent gain obtained under both polarities of the applied voltage.

From Fig. 3, it is obvious that a significant photocurrent gain takes place under both polarities of the voltage applied to the structure.

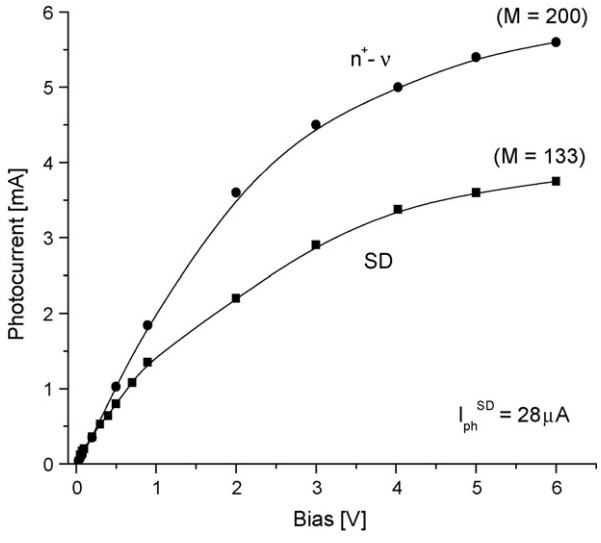

Fig. 3. Photocurrent gain (M) obtained for negatively biased SDs surrounded by the MOS capacitors, and for the n^+–ν barrier obtained under a positive bias applied to the Ti-electrode.

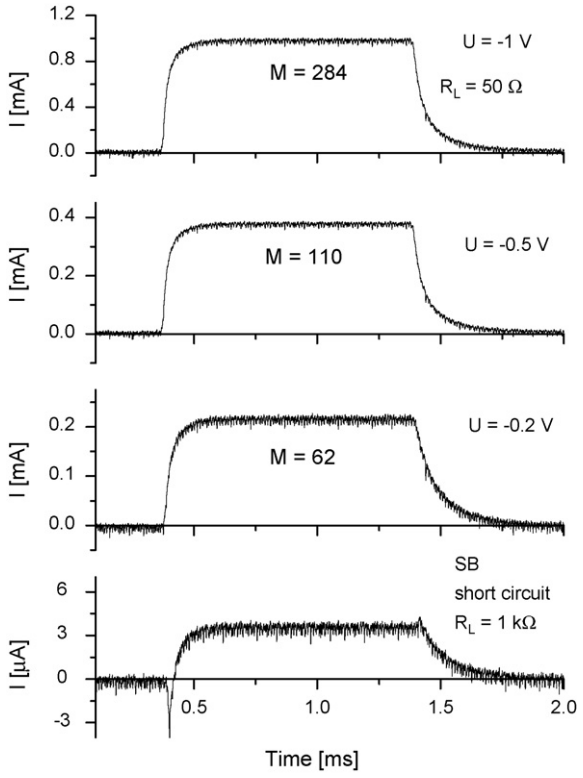

Fig. 4. Output signal obtained on a load resistor $R_L = 50\ \Omega$ under a negative bias applied to the Ti-electrode. The output signal for the short-circuited structure and $R_L = 1\ k\Omega$ is also shown.

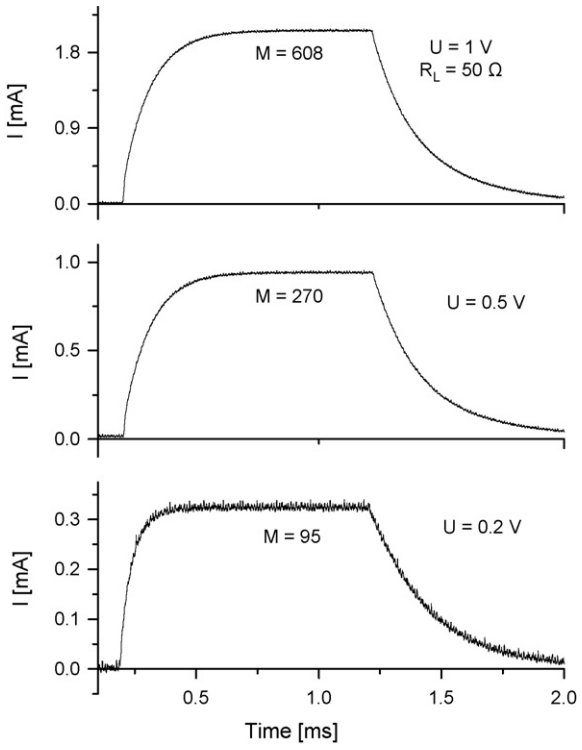

Fig. 5. Output signal obtained for a positive bias applied to the Ti-electrode. The conditions are the same as those used in Fig.4.

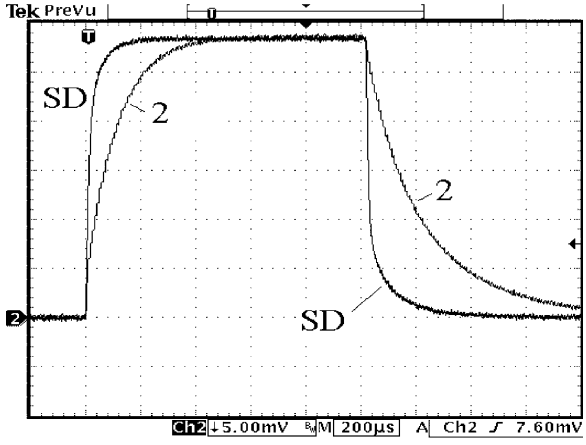

Fig. 6. Waveforms of the output signal for two operating modes: SD, the structure at −1 V bias; 2, the structure at +1 V bias.

Our interest in this work is not connected with the photocurrent gain obtained under a positive voltage applied on the Ti-electrode, when the Ti–νSi Schottky diodes (SD) are forward-biased and the Ti–SiO_2–νSi MOS capacitors are in the accumulation mode. The properties of this n^+–ν potential barrier, formed on the backside of the substrate, have been reported recently [2]. The role of this barrier for the confinement of minority photogenerated carriers (holes), which leads to a reduction of the potential barrier for electrons to be injected from the n^+-silicon region into the ν-silicon substrate, has been shown.

Our present interest is the origin of the photocurrent gain in these structures under a negative bias applied to the Ti-electrode. Thus, in this work, the photocurrent gain under a positive voltage is only used for comparison.

Figs. 4 and 5 show the waveforms of the output signal under pulse irradiation from a LED obtained for both polarities of the voltage applied to the Ti-electrode. The photoresponse of the sensor is faster when the structure is negatively biased (Fig. 4).

Fig. 6 shows the normalized output signal of the structure under both polarities of the applied voltage with the same absolute value of 1 V. The rise and fall times of the negatively biased structure are 80 µs and 100 µs, respectively.

On the other hand, the rise and fall times for the positively biased structure are 300 µs and 480 µs, respectively. In both cases, these times are determined by the physical processes occurring in the structures, and are not determined by the RC time constant of the circuit, which is a few orders of magnitude shorter than the observed times.

The gain obtained for the positively biased structure, which is determined by the n^+–ν potential barrier, is higher than that obtained for the negatively biased structure (Fig. 7).

The photocurrent gains shown in Fig. 7 are higher than those shown in Fig. 3. Actually, we found experimentally a decreasing photocurrent gain for an increasing optical power. This circumstance, for the n^+–ν potential barrier, has been explained in our previous work [2].

4. Discussion

Because the sensors are formed by the integrated combination of two semiconductor devices, namely the Schottky diodes and

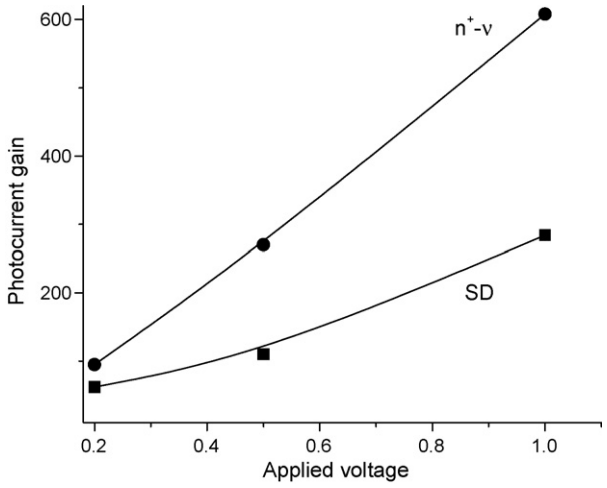

Fig. 7. Dependence of the photocurrent gain on the applied voltage obtained for the structure under pulse irradiation. The photocurrent is 3.5 μA for the short-circuited structure and $R_L = 1\,k\Omega$.

the MOS capacitors surrounding these diodes, we need to considerate separately the physical processes taking place in these devises under different polarities of the voltage bias.

The energy diagram of the double barrier structure for the Schottky diode case is shown in Fig. 8 under different conditions: equilibrium (a), negative bias (b), and positive bias (c) applied to the Ti-electrode. The last two diagrams are shown also for irradiated conditions.

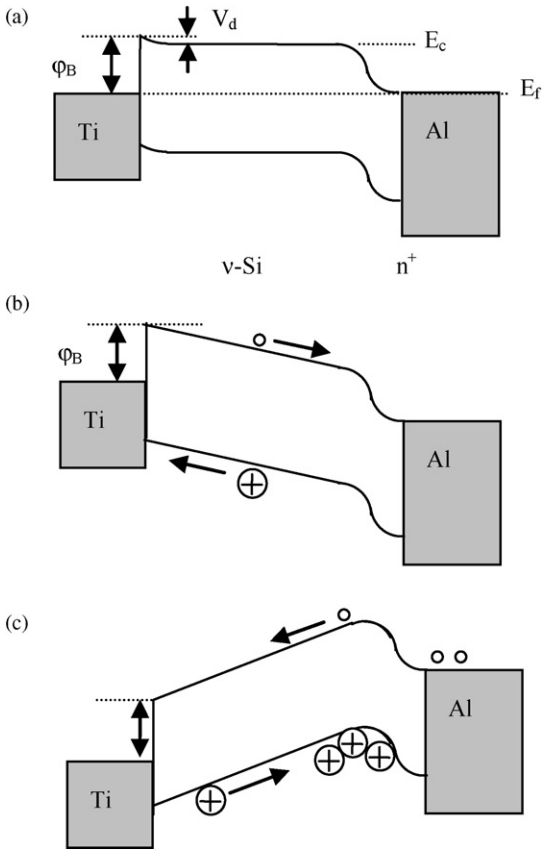

Fig. 8. Energy diagram of the double barrier structure for the Schottky diode under different conditions: equilibrium (a), negative bias (b), and positive bias (c) applied to the Ti-electrode.

The calculated value of the potential barrier (φ_B) for the Ti–Si contact is very similar to (E_c–E_f) for the used ν-silicon substrate, and is about 0.43 eV. E_c and E_f are the conduction and Fermi level, respectively. The diffusion potential (V_d) does not exceed 0.1 eV (Fig. 8a). Thus, the Ti–Si contact behaves as a quasi-ohmic contact instead of as a rectifying contact. However, in equilibrium and under a negative bias, a superficial space-charge region (SCR) exists at the Ti–Si interface.

The applied voltage is divided between the SCR and the high-resistivity silicon neutral region, and photogenerated carriers are separated by the internal electric field as shown in Fig. 8b. If a positive bias is applied to the Ti-electrode (Fig. 8c), photogenerated holes will accumulate in the potential well at the ν–n^+ interface leading to a modulation of the barrier for electrons injected from the n^+ contact. This is the origin of the gain for this polarity of the voltage bias [2].

The operating condition of the MOS capacitors surrounding the SDs is also important. According to measured *C*–*V* characteristics, the Ti–SiO_2–Si capacitors under equilibrium operate very close to the flat-band condition; this is due to the compensation of a positive fixed charge at the SiO_2–Si interface by a comparatively high value of the work function of titanium (∼4.3 eV). The threshold voltage is slightly positive (∼0.4 V), and this implies a depletion mode device for an n-type silicon high-resistivity substrate [4]. A low negative bias applied to the electrode will induce a large inversion layer charge due to the accumulation of thermo- or photogenerated electrons in the potential well at the SiO_2–Si interface. Every microscopic Schottky diode is surrounded by MOS capacitors. It is possible to expect an influence of the MOS capacitor on the properties of the Schottky diode along its perimeter. A rigorous two-dimensional theoretical consideration of this problem is a quite difficult task at the present moment. Recently, some solution for a similar but one-dimensional model, shown in Fig. 9, has been reported [1].

The rectangular geometry of the SDs leads to a large perimeter/area ratio ($2 \times 10^3\,cm^{-1}$). Thus, a strong fringe effect takes place in the SDs perimeter when a negative bias is applied to the Ti-electrode, due to the accumulation of minority carriers (holes) at the SiO_2–Si interface of the MOS capacitors. Under such conditions, the calculated value of the electric field along the perimeter of the SDs is shown in Fig. 10. Below, we discuss the nature of this field with more detail.

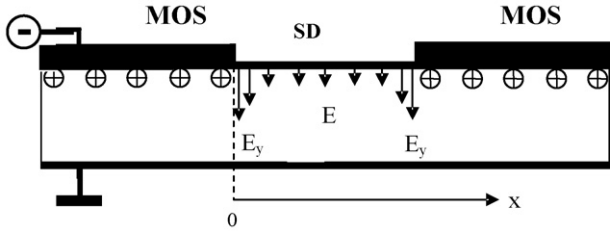

Fig. 9. Simplified model for the electric field along the perimeter of each SD surrounded by MOS capacitors; the cross-section A–A of Fig. 1 is shown.

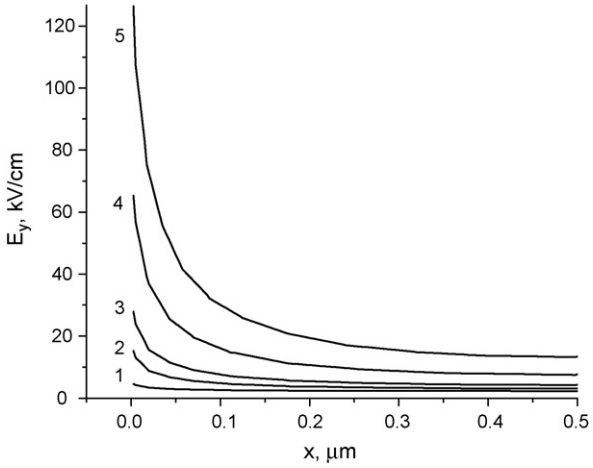

Fig. 10. Calculated transverse electric field at the MOS–SD boundary along the perimeter of the SD for different conditions of the SiO_2/Si interface [1]: curves 1 and 5 correspond to full depletion and strong inversion at the SiO_2/Si interface, respectively. Curves 2–4 show the intermediate cases.

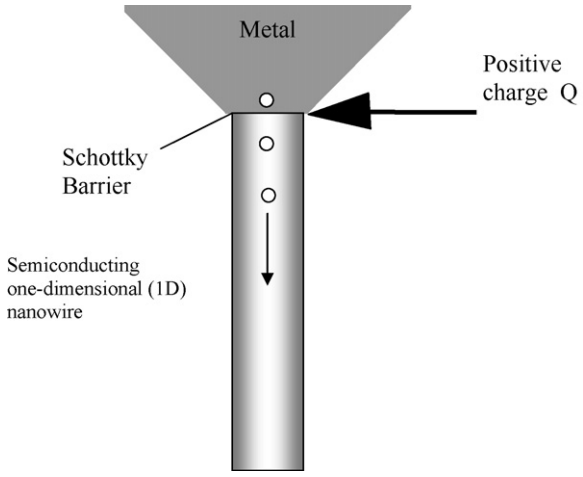

Fig. 12. Schematic representation of a one-dimensional model for studying the Coulombic interaction at the Schottky barrier interface (taken from Ref. [8]).

It was noted in Refs. [5,6] that the electric field along the Si–SiO_2 interface shows a peak near the edge of the gate electrode. The value of this electric field ($\sim 10^7$ to 10^8 V/cm) can be from one to two orders of magnitude higher in a few tens of angstroms from the electrode edge than the value ($\sim 10^6$ V/cm) it has in the electrode area for a given bias [6]. Such electric field, shown in Fig. 10, can reduce the potential barrier of the SDs along their perimeter. A barrier reduction depends on the inversion charge. Under that condition, the additional electron flow will take place through the Ti–νSi potential barrier into the silicon substrate from the metallic electrode. This additional flow of electrons increases the photocurrent caused by photogeneration of the carriers inside the silicon substrate, and it is the origin of the gain.

Of course, the abrupt edge of the MOS capacitor surrounding the SDs is a rough approximation. Fig. 11 shows a real side-view for one of the 10 μm-wide strips obtained by chemically etching the thermal oxide film grown on the silicon substrate.

The thickness of the SiO_2 film decreases almost linearly from 60 nm to 0 nm during ~2 μm in the direction of the Schottky diode. Thus, the MOS capacitors surrounding the SDs are not uniform near the perimeter of these diodes. Furthermore, one

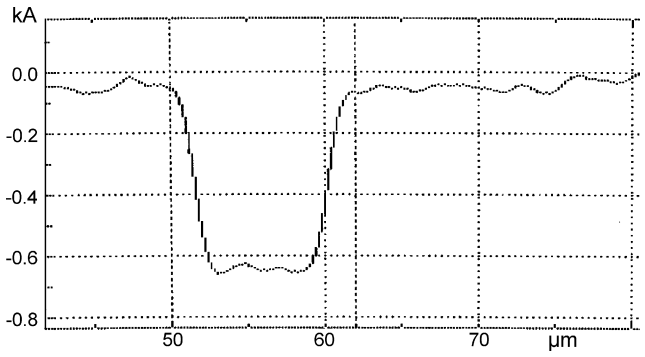

Fig. 11. Side-view for one of the 10 μm-wide strips obtained by chemically etching the thermal oxide film grown on the silicon substrate; one point in the vertical scale: 1000 Å.

can expect a difference in the surface potential at the Si–SiO_2 interface when the MOS capacitor is biased, as predicted by the theory of MOS capacitors [6,7]. However, for a high-resistivity silicon substrate this effect should not be so important for the given difference in oxide thickness. Nevertheless, very close to the perimeter of the SDs, the oxide is very thin and carriers can tunnel through it. From this point of view, for a negative bias the formation of an inversion layer at the silicon surface below the oxide is impossible under dark conditions. The rate of thermogeneration of holes can be nearly equal to their leakage through the thin oxide. A high electric field effect close to the perimeter of the SDs does not appear without an inversion layer. Hence, the sensor operates in a steady-state non-equilibrium mode. However, under irradiation, when a flow of photogenerated holes towards the insulator–silicon boundary is higher than its leakage, the inversion layer appears at the interface producing a two-dimensional layer with positive charge surrounding the SDs along their perimeter. This gives rise to a question: can this quasi-two-dimensional charge change the electron transport along the perimeter of the SDs?

This question has been studied in Ref. [8], where a Schottky barrier between a metallic contact and a semiconducting one-dimensional (1D) nanowire was considered (Fig. 12). Authors of this work examined how a local charge concentrated in the vicinity of a wire can modify the electrostatic potential profile at the junction, thus affecting the height and shape of the barrier, and leading to a significant change of the current flowing across the barrier.

It was found that the electric field generated by the charge Q possess a potential energy (PE) experienced by a carrier moving through the wire as

$$\mathrm{PE} = \frac{Qq}{4\pi\varepsilon r},$$

where r is the coordinate of the charge location. If charge Q is located in immediate proximity to the metal–wire boundary, the lowering of the potential barrier at the metal–wire interface was estimated in addition to the well-known barrier lowering due to image forces. The value of this additional barrier lower-

ing is 0.05 eV, if the charge is located at a distance of tens of nanometers from the boundary.

We suppose that this effect takes place in the perimeter of the SDs, when photogenerated holes accumulate near the insulator–silicon interface. This two-dimensional distribution of holes modulates the Ti–Si potential barrier along the perimeter of the SDs leading to an additional electron flow from the titanium to the silicon. This additional current is significantly high because of its exponential dependence on the barrier lowering. Thus, a low photocurrent due to photogeneration of electron–hole pairs causes a high current of electrons from the Ti-electrode into the silicon substrate over the potential barrier in the Ti–Si interface, and a transistor action takes place.

From experimental data one can see that the photocurrent amplification is higher when a positive voltage bias is applied to the Ti-electrode (Fig. 9c). This difference can be explained as due to a stronger modulation of the barrier height when the ν–n^+ barrier is operating at the bottom side of the silicon substrate. One can find details of this experimental fact in our earlier work [2].

Finally, the obtained photocurrent gain is difficult to explain based on the model of a vertical photoconductor, which requires an ohmic contact and the lack of accumulation of photogenerated minority carriers taking place in the described devices. Even, if we try to estimate the photocurrent gain as in an usual photoconductor with two ohmic contacts as the ratio of the majority carriers' transit time to the minority carriers' recombination time [9] (that not exceed the value of 10^{-5} s), the result for the gain is less than 25 at 1 V bias applied to the structure.

5. Conclusions

The optical sensors studied in this work, which are based on the integration in one single chip of micro-sized Schottky diodes surrounded by metal-oxide-semiconductor capacitors, present an internal photocurrent gain.

The origin of this current gain is the change in the transport mechanism of carriers through the potential barrier of the Schottky barrier along its perimeter; this is due to the strong electric field originated by the photogenerated minority carriers forming an inversion layer at the silicon-oxide interface.

These new optical sensors are simple to fabricate, and the gain is of about of 200 at 1 V bias. Thus, they are low voltage devices, and can be used for different applications in optoelectronic circuits, where signal amplification is required.

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Biographies

Oleksandr Malik received his M.Sc. degree in optics and Ph.D. in physics of semiconductors and dielectrics from the Chernovtsy University, Ukraine, in 1971 and 1980, respectively. He specialized in thin metal-oxide film technology and its applications used in optoelectronic devices during 36 years of scientific and industrial activity. From 1996 to 1999, he worked in Portugal as an invited scientist. Since 2000 he works as a titular researcher at National Institute for Astrophysics, Optics, and Electronics (INAOE), Electronics Department, Puebla, Mexico. His activity is connected with the development of new transparent conducting semiconductor films and novel optoelectronic devices with theirs applications. O. Malik is an author of about 200 scientific papers. He is a senior member of IEEE.

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Carlos Zuñiga Islas studied electrical engineering in the Instituto Politécnico Nacional (IPN), Mexico City, and obtained the Master and Ph.D. degrees in 1997 and 2005, respectively, from the National Institute for Astrophysics, Optics and Electronics (INAOE), Puebla, Mexico. Since 1982, he has worked at the Electronics Department of INAOE, giving technical support to the equipment and fabrication processes of devices and circuits, and has also participated in group, individual and independent projects. Currently, he is the head of the Microelectronics Laboratory and a full time researcher at INAOE. Among his fields of interest is the deposition of dielectric and semiconductor materials using low frequency plasma enhanced chemical vapor deposition (PECVD). He has produced several scientific and technical contributions that have been published in book chapters and journal papers, as well as many presentations in conferences.