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Degradation and Breakdown of W–La$_2$O$_3$ Stack after Annealing in N$_2$

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We report the effect of relatively high-voltage stressing (under substrate injection) on the stress-induced leakage current (SILC) and breakdown of W–La$_2$O$_3$ stacked structures. It is shown that the gate area of the metal–insulator–semiconductor (MIS) devices under evaluation influences their final degradation characteristics after stress. Once the samples reach breakdown, their post-breakdown current–voltage ($I–V$) characteristics suggest that leakage spots are highly localized and are caused by the accumulation of defects. [DOI: 10.1143/JJAP.47.7076]

KEYWORDS: La$_2$O$_3$, PMA, SILC, breakdown, reliability

1. Introduction

High dielectric constant materials for the gate of metal–oxide–semiconductor (MOS) transistors can reduce the gate leakage current ($I_g$) by using thicker oxide films while maintaining the same electrically equivalent oxide thickness (EOT). Lanthanum oxide (La$_2$O$_3$), which is a member of rare earth-based oxides, was classified into the next group of potential candidates to succeed conventional oxides. On the other hand, the introduction of metal gates for high-$k$ materials has been focused on choosing the right metal material for good electrical performance and best compatibility with standard complementary MOS (CMOS) processing. However, metal gate integration and its impact on high-$k$ reliability are not well understood. It is vital to understand the impact of metal gates on reliability issues such as defect density, electrical stability, and failure rate since many factors in metal gate integration (deposition, annealing, etching, etc.) can potentially affect the reliability of a high-$k$ gated CMOS device. In this work, W-gated La$_2$O$_3$ stacked structures were fabricated and the effects of high voltage stressing on their reliability characteristics were evaluated.

2. Experiments

MIS capacitors were fabricated on n-type (100) oriented silicon wafers with resistivity of 1–5 ω cm. Thin films of La$_2$O$_3$ were deposited on HF-last or hydrogen-terminated n-type silicon substrates by electron-beam evaporation using molecular beam epitaxy (MBE) system (Anelva I) at 300 °C. The pressure in the chamber during the deposition was around 1 $\times$ 10$^{-7}$ Pa. Also, in-situ sputtering of tungsten was done at 150 W rf power in a contiguous chamber immediately after the dielectric deposition in order to avoid exposure of La$_2$O$_3$ surface to the environment. Because of this, the physical thickness of La$_2$O$_3$ cannot be measured by ellipsometry but by transmission electron microscopy. During the deposition of the metal, an argon flow of 1.33 Pa was used. Patterning of the gate electrodes was done by reactive-ion etching using SF$_6$ gas with a 30 W power.

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Finally, post-metallization annealing (PMA) was done in dry N$_2$ ambient at 500 °C for 5 min. Figures 1 and 2 show capacitance–voltage ($C–V$) and current–voltage ($I–V$) characteristics of the fabricated samples respectively.

3. Results and Discussion

From $C–V$ data in Fig. 1, the as-deposited (as-depo) sample presents higher hysteresis compared to PMA sample. Also, the hysteresis loops show that hysteresis is caused by negative charge trapping which occurs during the transition from depletion to accumulation regimes. The increase in EOT after PMA is considered to be originated due to the reaction of La$_2$O$_3$ with silicon substrate into silicate that forms a lower-$k$ interfacial layer (IL) between La$_2$O$_3$ and silicon. In Fig. 2, the $I–V$ characteristics for the same W–La$_2$O$_3$ gated capacitors are presented. The as-depo samples show a continuous increase in gate leakage current density until the oxides reach breakdown for a gate voltage $V_g > 2$ V, this is followed by a progressive-breakdown (PBD) characteristic, where the breakdown spots would gradually progress with time and stress and they are considered to be associated with the increase of the oxide conductivity which has associated an increase of the total size of the percolation path created during the breakdown event. It is thought that for the non-annealed La$_2$O$_3$ sample, a higher and random density of bulk/interfacial defects would make easier for these defects to be electrically “connected” during stress so that the size of the total leakage path during breakdown increases. On the other hand, the PMA-La$_2$O$_3$ samples suddenly break down for $V_g > 4$ V, which suggests both reduction and densification of defects within La$_2$O$_3$, and thus, a breakdown event with a more discrete nature.

In Fig. 3(a), the evolution of gate leakage current $I_g$ with stressing time clearly shows that for identical stress conditions, smaller area devices will exhibit larger times to breakdown $t_{bd}$ where more severe breakdown events take place. Figure 3(b) shows the former data using gate leakage current density for comparison purposes. Different $t_{bd}$ distributions are associated with the average density of generated defects during stress, so that samples with larger area would find more sites for defect generation during the stress. Also, the post-breakdown characteristic of $I_g$ for all
samples does not show a clear relationship with device area, this suggests a highly localized nature for $I_g$ flow through the leakage spot after breakdown. Despite the disagreement about the defect generation model, there is a general consensus in considering that a critical density of bulk defects generated at random places eventually leads to the formation of a localized leakage path across the oxide layer. The former is known as the percolation model, and we think that this approach could be initially applied, at least qualitatively, to explain the degradation process occurring on these devices. This is more visible in Fig. 3(a), where the post-breakdown $I_g$ characteristics for all samples do not show a clear relationship with device area. (b) Gate leakage current density $J_g$ evolution with stressing time for W–La$_2$O$_3$ gated capacitors. The same data as in (a) is shown after area normalization for comparison purposes.

![Fig. 1. C–V curves for W–La$_2$O$_3$ capacitors before and after PMA at 500°C. EOT = 1.3 and 1.8 nm are obtained for as-depo and PMA samples respectively.](image1)

![Fig. 2. J–V curves for W–La$_2$O$_3$ capacitors before and after PMA at 500°C. Compared to the as-depo samples, the densification of the films after PMA increases gate leakage current density $J_g$ and the time-to-zero breakdown point.](image2)

![Fig. 3. Evolution of gate leakage current with stressing time for W–La$_2$O$_3$ gated capacitors: (a) For the same stressing conditions, longer times for breakdown are observed for devices with smaller areas. The post-breakdown $I_g$ characteristics for all samples do not show a clear relationship with device area. (b) Gate leakage current density $J_g$ evolution with stressing time for W–La$_2$O$_3$ gated capacitors. The same data as in (a) is shown after area normalization for comparison purposes.](image3)
gate with substrate grounded at room temperature. From that figure, it is not clear whether or not the distribution slopes depend on the area of the test structures. In addition, it cannot be concluded what is the statistical nature of these distributions. From Fig. 4(a) and by linearly extrapolating $t_{bd}$ data up to 10 years, we have found that the maximum gate voltage required for a W–La$_2$O$_3$ stack to reach breakdown is about 2.5 V for both samples. It is important to notice that these lifetime predictions are only a rough approximation because once the exponential law of voltage dependence for breakdown reaches very low voltages (compared to those used during operation conditions), the linear model will tend to approach a more power-law based model. In any case, a 10-year-long operation is guaranteed by using the very simple linear $V_g$ or reciprocal $1/V_g$ models because of the high electric fields used during the stressing of these samples. At high electric field, the linear and reciprocal models converge and that is why both models can be used here to project the lifetime of La$_2$O$_3$.

Figure 5 shows the increase in SILC density after positive stress. The increase in SILC density after stressing time is shown for the device with smaller area. The fresh $J-V$ curve represents the device before the stress is applied.
The degradation rate is occurring through all of the devices. It is thought that an increased density of new defects generated during stress adds-up to an initially uniform density of intrinsic or initial defects so that smaller area devices under the same stress conditions will end up with a higher final density of defects which in turn increases SILC (see Fig. 8). The newly generated defects can be located at the interfaces of $\text{La}_2\text{O}_3$ with silicon, interfacial layer and tungsten or at the bulk of the $\text{La}_2\text{O}_3$ itself. In Fig. 8, a very simplified model is drawn to represent this effect. It is seen that smaller area devices will produce a crowd of initial and newly generated defects during CVS as compared to devices with bigger areas. These sites would allow more SILC to flow through the oxide layer by acting as “stepping stones” for tunneling carriers. This phenomenon is often referred to as trap-assisted tunneling. This is important because even though smaller area devices produce longer lifetimes to breakdown during higher-voltage stressing conditions (see Figs. 3 and 4), the stressing of W–$\text{La}_2\text{O}_3$ stacks during lower CVS (as compared to the CVS used for lifetime projection) does not break down the oxide but the damage induced in the dielectric results in an inversely proportional dependence of SILC increase with respect to gate area. This implies that even with long-lasting lifetimes for oxides with smaller areas, their electrical degradation before breakdown will ultimately impose a serious limit towards their use for smaller-area devices.

On the other hand, the introduction of a more chemically inert metal like tungsten as gate electrode can improve some electrical characteristics of the MIS devices by reducing the formation of an IL between $\text{La}_2\text{O}_3$ and the metal itself. Nonetheless, the final thermal treatments applied to an already metallized $\text{La}_2\text{O}_3$-gated MIS device will have several effects on its physical and electrical characteristics. In this respect, the introduction of PMA compared to annealing before metallization (PDA or post-deposition annealing) for tungsten-gated $\text{La}_2\text{O}_3$ MIS devices, has resulted in better electrical characteristics both in terms of chemical stability and reliability. This been said, the electrical results presented in this paper have been obtained after introducing tungsten as the metal gate electrode atop $\text{La}_2\text{O}_3$ but mainly because of the thermal processing applied immediately after metallization of the fabricated MIS devices.

4. Conclusions

The reliability characteristics of W–$\text{La}_2\text{O}_3$-nSi gate stacks with EOT = 1.3 and 1.8 nm (after PMA) were investigated. The introduction of PMA at 500 °C improved the electrical characteristics of the oxide by reducing hysteresis in the C–V data and increasing the time-to-zero breakdown voltage during a ramped-voltage measurement. By extrapolating time to breakdown results after positive CVS measurements, the lifetime projection for the oxide was obtained. A 10-year-long operation for W–$\text{La}_2\text{O}_3$ is predicted if $V_g < 2.3$ V by using the very simple linear $V_g$ model. The dependence of device’s area on the electrical degradation and breakdown of W–$\text{La}_2\text{O}_3$ was also investigated. It is found that the post-breakdown characteristic of $I_g$ for all samples does not show a direct relationship with area, which suggests a highly localized nature the breakdown spot. Finally, even though smaller area devices produce longer lifetimes to breakdown during higher-voltage stressing conditions, the stressing with lower CVS does not breaks down the oxides but the damage induced in the dielectrics results in an inversely proportional dependence of SILC increase with respect to gate area.

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