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To cite this article: Joel Molina *et al* 2008 *Jpn. J. Appl. Phys.* **47** 7076

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Degradation and Breakdown of W–La₂O₃ Stack after Annealing in N₂

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(Received March 7, 2008; accepted May 30, 2008; published online September 12, 2008)

We report the effect of relatively high-voltage stressing (under substrate injection) on the stress-induced leakage current (SILC) and breakdown of W–La₂O₃ stacked structures. It is shown that the gate area of the metal–insulator–semiconductor (MIS) devices under evaluation influences their final degradation characteristics after stress. Once the samples reach breakdown, their post-breakdown current–voltage (*I*–*V*) characteristics suggest that leakage spots are highly localized and are caused by the accumulation of defects. [DOI: 10.1143/JJAP.47.7076]

KEYWORDS: La₂O₃, PMA, SILC, breakdown, reliability

1. Introduction

High dielectric constant materials for the gate of metal–oxide–semiconductor (MOS) transistors can reduce the gate leakage current (I_g) by using thicker oxide films while maintaining the same electrically equivalent oxide thickness (EOT). Lanthanum oxide (La₂O₃), which is a member of rare earth-based oxides, was classified into the next group of potential candidates to succeed conventional oxides.¹⁾ On the other hand, the introduction of metal gates for high-*k* materials has been focused on choosing the right metal material for good electrical performance and best compatibility with standard complementary MOS (CMOS) processing. However, metal gate integration and its impact on high-*k* reliability are not well understood. It is vitally important to understand the impact of metal gates on reliability issues such as defect density, electrical stability, and failure rate since many factors in metal gate integration (deposition, annealing, etching, etc.) can potentially affect the reliability of a high-*k* gated CMOS device. In this work, W-gated La₂O₃ stacked structures were fabricated and the effects of high voltage stressing on their reliability characteristics were evaluated.

2. Experiments

MIS capacitors were fabricated on n-type (100) oriented silicon wafers with resistivity of 1–5 Ω·cm. Thin films of La₂O₃ were deposited on HF-last or hydrogen-terminated n-type silicon substrates by electron-beam evaporation using molecular beam epitaxy (MBE) system (Anelva I) at 300 °C. The pressure in the chamber during the deposition was around 1×10^{-7} Pa. Also, *in-situ* sputtering of tungsten was done at 150 W rf power in a contiguous chamber immediately after the dielectric deposition in order to avoid exposure of La₂O₃ surface to the environment. Because of this, the physical thickness of La₂O₃ cannot be measured by ellipsometry but by transmission electron microscopy. During the deposition of the metal, an argon flow of 1.33 Pa was used. Patterning of the gate electrodes was done by reactive-ion etching using SF₆ gas with a 30 W power.

Finally, post-metallization annealing (PMA) was done in dry N₂ ambient at 500 °C for 5 min. Figures 1 and 2 show capacitance–voltage (*C*–*V*) and current–voltage (*I*–*V*) characteristics of the fabricated samples respectively.

3. Results and Discussion

From *C*–*V* data in Fig. 1, the as-deposited (as-depo) sample presents higher hysteresis compared to PMA sample. Also, the hysteresis loops show that hysteresis is caused by negative charge trapping which occurs during the transition from depletion to accumulation regimes. The increase in EOT after PMA is considered to be originated due to the reaction of La₂O₃ with silicon substrate into silicate that forms a lower-*k* interfacial layer (IL) between La₂O₃ and silicon.^{2–4)} In Fig. 2, the *I*–*V* characteristics for the same W–La₂O₃ gated capacitors are presented. The as-depo samples show a continuous increase in gate leakage current density until the oxides reach breakdown for a gate voltage $V_g > 2$ V, this is followed by a progressive-breakdown (PBD) characteristic, where the breakdown spots would gradually progress with time and stress and they are considered to be associated with the increase of the oxide conductivity which has associated an increase of the total size of the percolation path created during the breakdown event.^{5–7)} It is thought that for the non-annealed La₂O₃ sample, a higher and random density of bulk/interfacial defects would make easier for these defects to be electrically “connected” during stress so that the size of the total leakage path during breakdown increases. On the other hand, the PMA-La₂O₃ samples suddenly break down for $V_g > 4$ V, which suggests both reduction and densification of defects within La₂O₃, and thus, a breakdown event with a more discrete nature.

In Fig. 3(a), the evolution of gate leakage current I_g with stressing time clearly shows that for identical stress conditions, smaller area devices will exhibit larger times to breakdown t_{bd} where more severe breakdown events take place. Figure 3(b) shows the former data using gate leakage current density for comparison purposes. Different t_{bd} distributions are associated with the average density of generated defects during stress,⁸⁾ so that samples with larger area would find more sites for defect generation during the stress. Also, the post-breakdown characteristic of I_g for all

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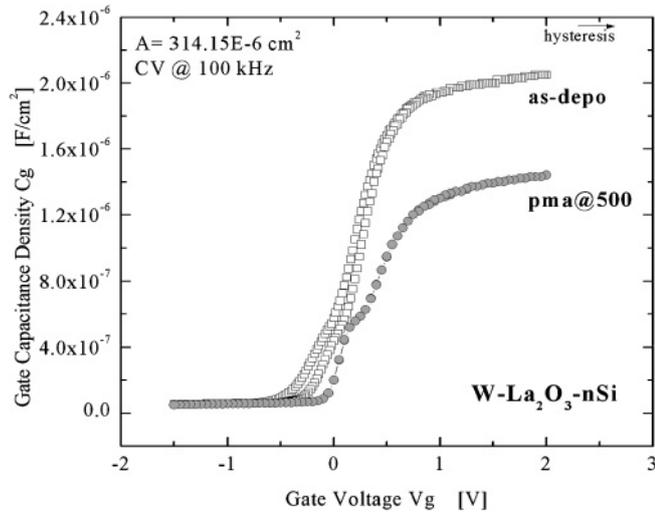


Fig. 1. C - V curves for W - La_2O_3 capacitors before and after PMA at $500^\circ C$. EOT = 1.3 and 1.8 nm are obtained for as-depo and PMA samples respectively.

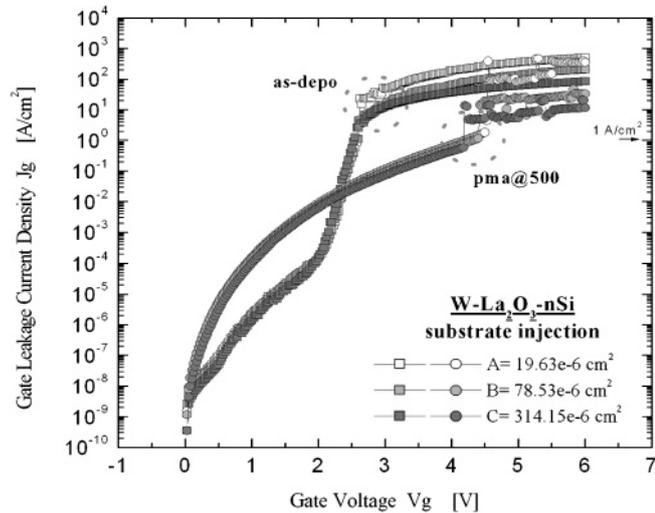
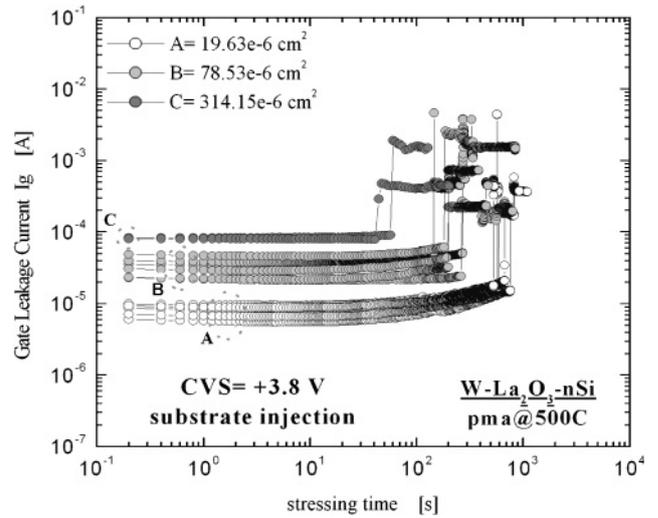
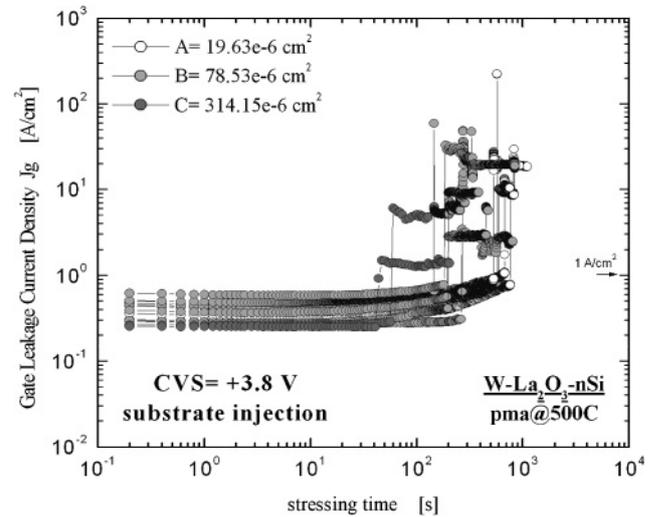


Fig. 2. J - V curves for W - La_2O_3 capacitors before and after PMA at $500^\circ C$. Compared to the as-depo samples, the densification of the films after PMA increases gate leakage current density J_g and the time-to-zero breakdown point.

samples does not show a clear relationship with device area, this suggests a highly localized nature for I_g flow through the leakage spot after breakdown.⁹⁾ Despite the disagreement about the defect generation model, there is a general consensus in considering that a critical density of bulk defects generated at random places eventually leads to the formation of a localized leakage path across the oxide layer.¹⁰⁾ The former is known as the percolation model,¹¹⁾ and we think that this approach could be initially applied, at least qualitatively, to explain the degradation process occurring on these devices. This is more visible in Fig. 3(a), where the post-breakdown characteristics of I_g do not show a direct relationship with device area. In order to quantitatively corroborate this model, the critical defect density N_{crit} must be obtained so that the relationship between breakdown statistics and defect creation can be assessed and also, a rough estimation of the defect size involved in the formation



(a)



(b)

Fig. 3. Evolution of gate leakage current with stressing time for W - La_2O_3 gated capacitors: (a) For the same stressing conditions, longer times for breakdown are observed for devices with smaller areas. The post-breakdown I_g characteristics for all samples do not show a clear relationship with device area. (b) Gate leakage current density J_g evolution with stressing time for W - La_2O_3 gated capacitors. The same data as in (a) is shown after area normalization for comparison purposes.

of the breakdown path as well. After this, the current runaway and the energy dissipation dynamics through the damaged zone would determine the severity of the event and consequently the magnitude of the leakage current. It is thought that a higher post-breakdown I_g is linked to a greater conductivity or size of the total damaged spot area which is created in the oxide by defect percolation after stress. In Fig. 4(a), the lifetime projection for the W - La_2O_3 stack is plotted based on time-dependent dielectric breakdown (TDDB) measurements with constant voltage stress (CVS) by taking into account a 63% mean time to failure. It is shown that smaller area devices will require longer times to reach breakdown even if the same applied CVS are used. Figure 4(b) shows the Weibull plot of the breakdown distributions for two different devices' areas stressed at 3.8, 4.0, and 4.2 V. The stress voltages were applied on the

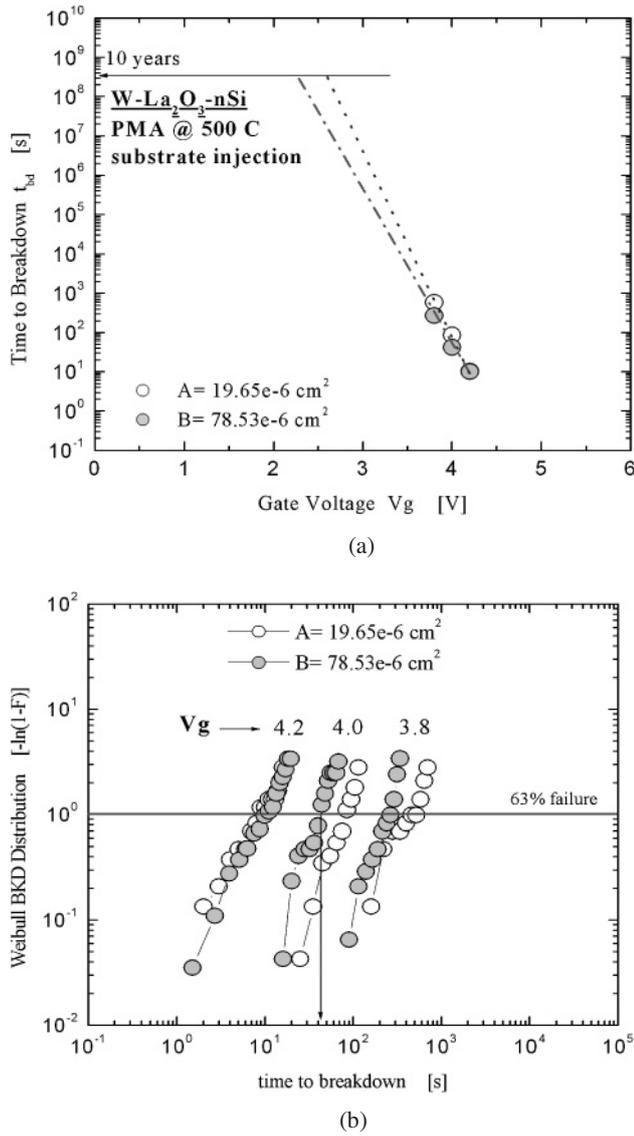


Fig. 4. Reliability data for W-La₂O₃ gated capacitors after TDDB measurements and with CVS: (a) Lifetime projection by taking into account a 63% mean time to failure. Smaller area devices present slightly longer lifetimes to breakdown. (b) Weibull distribution of breakdown for the W-La₂O₃ gated capacitors biased at three different gate voltages.

gate with substrate grounded at room temperature. From that figure, it is not clear whether or not the distribution slopes depend on the area of the test structures. In addition, it cannot be concluded what is the statistical nature of these distributions.¹²⁾ From Fig. 4(a) and by linearly extrapolating t_{bd} data up to 10 years, we have found that the maximum gate voltage required for a W-La₂O₃ stack to reach breakdown is about 2.5 V for both samples. It is important to notice that these lifetime predictions are only a rough approximation because once the exponential law of voltage dependence for breakdown reaches very low voltages (compared to those used during operation conditions), the linear model will tend to approach a more power-law based model.^{13,14)} In any case, a 10-year-long operation is guaranteed by using the very simple linear V_g or reciprocal $1/V_g$ models because of the high electric fields used during the stressing of these samples. At high electric field, the linear and reciprocal models converge and that is why

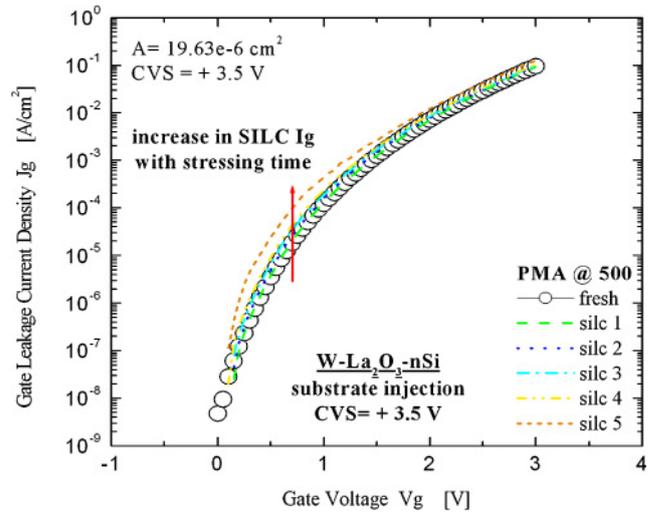


Fig. 5. (Color online) J - V characteristic of W-La₂O₃ before and after positive CVS. The increase in SILC density after stressing time is shown for the device with smaller area. The fresh J - V curve represents the device before the stress is applied.

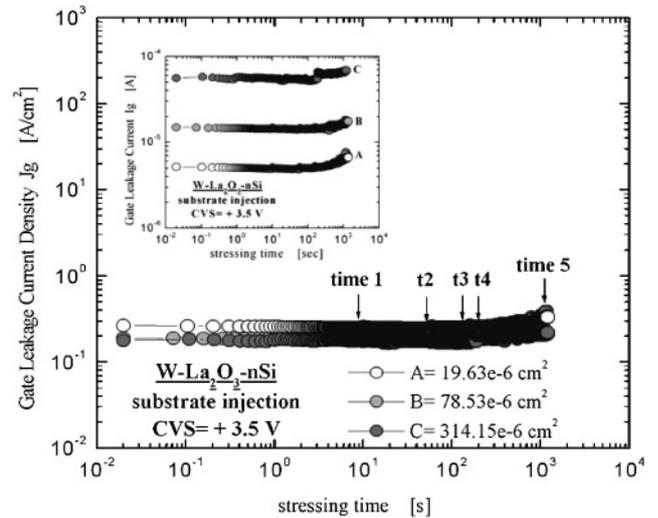


Fig. 6. Evolution of gate leakage current density J_g with stressing time. SILC measurements were performed at the same points t1, ..., t5 for all areas A, B, and C. The inset shows the same data without area normalization for comparison purposes.

both models can be used here to project the lifetime of La₂O₃.

Figure 5 shows the increase in SILC density after positive CVS. The applied gate voltage V_g , was 3.5 V during all the time of the stressing measurements. SILC was measured at the same time points for all samples during the degradation by CVS (which are shown as t1, t2, ..., t5 in Fig. 6), and this was done by applying a ramped voltage measurement with V_g less than CVS in order to avoid extra-induction of defect generation. The normalized SILC values are shown in Fig. 7. Interestingly, higher increases in SILC after stress are observed for samples with smaller area during all the range of the gate leakage current evolution with time (shown in Fig. 6). During stress, the injection of electrons into La₂O₃ is caused by the same conduction mechanism independently of the area of the device, so that we can assume that the same

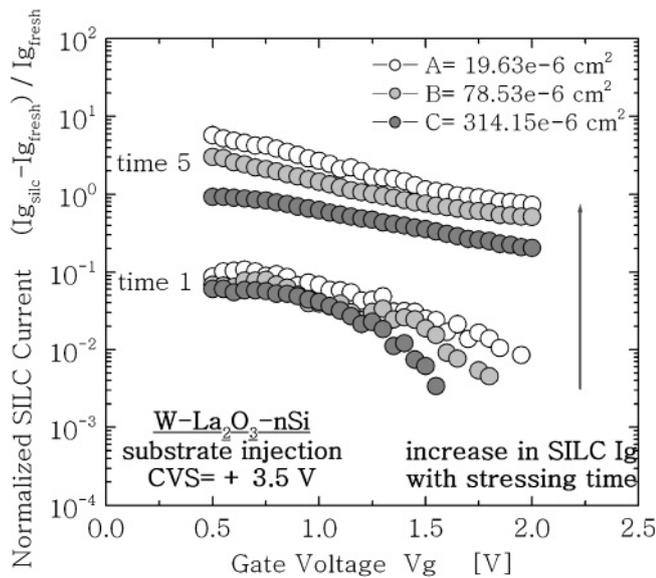


Fig. 7. Normalized SILC I_g current as a function of gate voltage and stressing time. Higher SILC-induced degradation is obtained for smaller area devices.

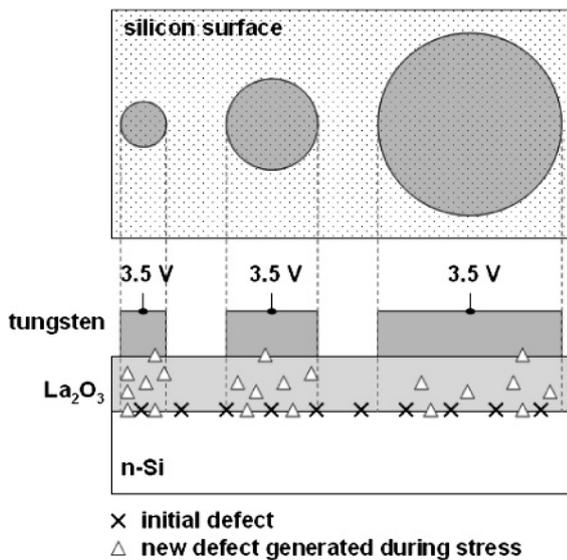


Fig. 8. Schematic model representing the generation of new defects during CVS measurements. Smaller devices get a crowded defect density after stress.

degradation rate is occurring through all of the devices. It is thought that an increased density of new defects generated during stress adds-up to an initially uniform density of intrinsic or initial defects so that smaller area devices under the same stress conditions will end up with a higher final density of defects which in turn increases SILC (see Fig. 8). The newly generated defects can be located at the interfaces of La_2O_3 with silicon, interfacial layer and tungsten or at the bulk of the La_2O_3 itself. In Fig. 8, a very simplified model is drawn to represent this effect. It is seen that smaller area devices will produce a crowd of initial and newly generated defects during CVS as compared to devices with bigger areas. These sites would allow more SILC to flow through the oxide layer by acting as “stepping stones” for tunneling

carriers. This phenomenon is often referred to as trap-assisted tunneling. This is important because even though smaller area devices produce longer lifetimes to breakdown during higher-voltage stressing conditions (see Figs. 3 and 4), the stressing of $\text{W-La}_2\text{O}_3$ stacks during lower CVS (as compared to the CVS used for lifetime projection) does not breaks down the oxide but the damage induced in the dielectric results in an inversely proportional dependence of SILC increase with respect to gate area. This implies that even with long-lasting lifetimes for oxides with smaller areas, their electrical degradation before breakdown will ultimately impose a serious limit towards their use for smaller-area devices.

On the other hand, the introduction of a more chemically inert metal like tungsten as gate electrode can improve some electrical characteristics of the MIS devices by reducing the formation of an IL between La_2O_3 and the metal itself. Nonetheless, the final thermal treatments applied to an already metallized La_2O_3 -gated MIS device will have several effects on its physical and electrical characteristics.¹⁵ In this respect, the introduction of PMA compared to annealing before metallization (PDA or post-deposition annealing) for tungsten-gated La_2O_3 MIS devices, has resulted in better electrical characteristics both in terms of chemical stability and reliability.¹⁶ This been said, the electrical results presented in this paper have been obtained after introducing tungsten as the metal gate electrode atop La_2O_3 but mainly because of the thermal processing applied immediately after metallization of the fabricated MIS devices.

4. Conclusions

The reliability characteristics of $\text{W-La}_2\text{O}_3$ -nSi gate stacks with $\text{EOT} = 1.3$ and 1.8 nm (after PMA) were investigated. The introduction of PMA at 500°C improved the electrical characteristics of the oxide by reducing hysteresis in the $C-V$ data and increasing the time-to-zero breakdown voltage during a ramped-voltage measurement. By extrapolating time to breakdown results after positive CVS measurements, the lifetime projection for the oxide was obtained. A 10-year-long operation for $\text{W-La}_2\text{O}_3$ is predicted if $V_g < 2.3$ V by using the very simple linear V_g model. The dependence of device's area on the electrical degradation and breakdown of $\text{W-La}_2\text{O}_3$ was also investigated. It is found that the post-breakdown characteristic of I_g for all samples does not show a direct relationship with area, which suggests a highly localized nature the breakdown spot. Finally, even though smaller area devices produce longer lifetimes to breakdown during higher-voltage stressing conditions, the stressing with lower CVS does not breaks down the oxides but the damage induced in the dielectrics results in an inversely proportional dependence of SILC increase with respect to gate area.

Acknowledgments

This work was partially supported by the Mexican Council for Science and Technology (CONACyT), Mexico, the Semiconductor Technology Academic Research Center (STARC) and Special Coordination Funds for Promoting Science and Technology by the Ministry of Education, Culture, Sports, Science and Technology, Japan.

- 1) G. D. Wilk, R. M. Wallace, and J. M. Anthony: *J. Appl. Phys.* **89** (2001) 5243.
- 2) K. Tachi, H. Iwai, T. Hattori, N. Sugii, K. Tsutsui, P. Ahemt, and K. Kakushima: *ECS Trans.* **3** (2006) No. 3, 425.
- 3) H. Nohira, T. Yoshida, H. Okamoto, W. Sakai, K. Nakajima, M. Suzuki, K. Kimura, J. Ng, Y. Kobayashi, S. Ohmi, H. Iwai, E. Ikenaga, K. Kobayashi, Y. Takata, and T. Hattori: *ECS Trans.* **1** (2005) No. 1, 87.
- 4) T. Gougousi, M. J. Kelly, D. B. Terry, and G. N. Parsons: *J. Appl. Phys.* **93** (2003) 1691.
- 5) F. Monsieur, E. Vincent, D. Roy, S. Bruyere, J. C. Vildeuil, G. Pananakakis, and G. Ghibaudo: *Proc. IEEE IRPS*, 2002, p. 45.
- 6) T. Hosoi, P. LoRe, Y. Kamakura, and K. Taniguchi: *IEDM Tech. Dig.*, 2002, p. 155.
- 7) E. Miranda, A. Cester, and A. Paccagnella: *Electron. Lett.* **39** (2003) 749.
- 8) S. Lombardo, A. LaMagna, C. Spinella, C. Gerardi, and F. Crupi: *J. Appl. Phys.* **86** (1999) 6382.
- 9) E. Miranda and J. Sune: *Microelectron. Reliab.* **44** (2004) 1.
- 10) B. Kaczer, R. Degraeve, A. Keersgieter, K. Van de Mierop, V. Simons, and G. Groeseneken: *IEEE Trans. Electron Devices* **49** (2002) 507.
- 11) J. H. Stathis: *J. Appl. Phys.* **86** (1999) 5757.
- 12) E. Y. Wu, W. W. Abadeer, L. K. Han, S. H. Lo, and G. R. Hueckel: *Proc. IEEE IRPS*, 1999, p. 57.
- 13) J. H. Stathis: *IBM J. Res. Dev.* **46** (2002) 265.
- 14) E. Y. Wu, E. J. Nowak, A. Vayshenker, W. L. Lai, and D. L. Harmon: *IBM J. Res. Dev.* **46** (2002) 287.
- 15) J. A. Ng, Y. Kuroki, N. Sugii, K. Kakushima, S.-I. Ohmi, K. Tsutsui, T. Hattori, H. Iwai, and H. Wong: *Microelectron. Eng.* **80** (2005) 206.
- 16) J. Molina, K. Tachi, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, and H. Iwai: *J. Electrochem. Soc.* **154** (2007) G110.