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A novel CMOS exponential transconductor operating in weak inversion

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A novel CMOS exponential transconductor which employs only three NMOS transistors operating in weak inversion, is presented. The main advantage of the proposed circuit is its wide range of exponential behaviour, which reaches up to five decades of current range, and above 10 μA to an input voltage range of 800 mV. The physical realisation is achieved in two forms: in the first one, the circuit is implemented with discrete MOS transistor arrays by CD4007 series; in the second one, the circuit is fully integrated in a 0.5 μm CMOS standard process. Simulated and experimental results of the proposed exponential transconductor are also presented.

Keywords: analogue circuits; CMOS circuits; exponential circuits; weak inversion circuits; transconductors

1. Introduction

Exponential circuits are analogue blocks which are indispensable to obtain a wide variety of signal processing functions with applications in communications, hearing instruments, log-domain filtering, etc. (Sheingold 1976; Serdijn, van der Woerd, Davidse, and van Roermund 1994; Duerden, Roberts, and Deen 2001; Yamaji, Kanou, and Ikatura 2002).

Exponential circuits are typically obtained from devices that contain some type of pn junction, because a voltage-to-current logarithmic relationship governs the performance of those devices. Several implementations which achieve exponential circuits using pn junction diodes had been reported (Sheingold 1976; Franco 1988) or bipolar junction transistors (Kumwachara, and Fujii 2000; Panagiotopoulos, Newcomb, and Singh 2000). On the other hand, exponential circuits also had been reported with realisations based on mathematical approximations employing MOS transistors operating in strong inversion; however the range is limited to one or two decades of exponential behaviour (Vlassis 2001; Yamaji 2002). Furthermore, this article is devoted to show the usefulness of using MOS transistors operating in weak inversion, because the current-voltage relation is logarithmic.

A novel exponential circuit is introduced herein, which employs only three NMOS transistors operating in weak inversion. Its high performance output feature is highlighted,

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which is maintained up to 10 μA for an input voltage range near to 800 mV. Additionally, only one bias current source is used in the exponential circuit, favouring the design of low voltage and low power circuits. Experimental results of the exponential transconductor are presented in two ways: first by using CD4007 CMOS transistor arrays, and second by employing an exponential circuit fabricated in 0.5 μm CMOS standard technology through MOSIS.

In section 2 the principle of operation of the exponential transconductor is described. In section 3, simulation results achieved with HSPICE are presented. Experimental results are shown in section 4, while the conclusions are discussed in section 5.

2. Description of the exponential circuit

An exponential circuit must fulfil the function:

$$f(x) = A \cdot e^{b \cdot x} \tag{1}$$

where A and b are positive constants, and the variable x can take real values. The structure of the novel exponential circuit is presented in Figure 1. It is implemented with three transistors M_1–M_3 operating in the weak inversion. The resistor R_0 is only used for measurement purposes.

The current source I_b maintains to M_1 in weak inversion. If the Early effect is ignored, the relationship between the drain current, I_{DS}, and V_{GS} of a MOS transistor can be described by (Geiger, Allen, and Strader 1990):

$$I_{DS} = \frac{W}{L} I_{D0} \cdot e^{\left(\frac{V_{BS}(n-1)}{nV_T}\right)\left(\frac{V_{GS}-V_{Th}}{nV_T}\right)} \left(1 - e^{\left(\frac{-V_{DS}}{V_T}\right)}\right) \tag{2}$$

where V_{Th} is the threshold voltage, $V_T = kT/q$ is the thermal voltage, V_{DS} is the drain-source voltage, n is a constant, and the current I_{D0}, which is related with the transconductance parameter k', is given by (Geiger et al. 1990):

$$I_{DO} \cong \frac{2nk'V_T^2}{e^2} \tag{3}$$

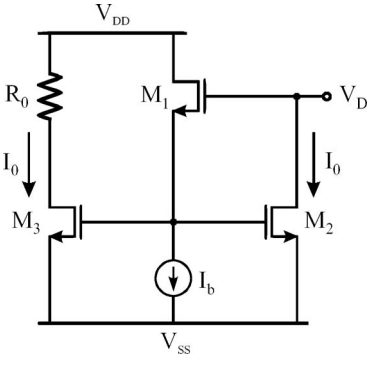

Figure 1. Proposed exponential transconductor circuit.

The relationship (3) establishes the limits of operation between both weak and strong inversion regions (Degrauwe, Marc, and Sansen Willy 1984). In this way, the MOS transistor operates in weak inversion if its drain current is smaller than $I_{D0}/8$ (Degrauwe et al. 1984). On the other hand, if $V_{DS} > 3V_T$, the MOS transistor operates in saturation region (Geiger et al. 1990), and the term e^{-V_{DS}/V_T} can be negligible, so that the equation (2) can be expressed as:

$$I_{DS} \cong \frac{W}{L} I_{DO} \cdot e^{V_{BS}\left(\frac{n-1}{nV_T}\right)} e^{\left(\frac{V_{GS}-V_{Th}}{nV_T}\right)} \tag{4}$$

In Figure 1, the exponential behaviour is generated by M_1, M_2 and I_b. V_D is the input voltage and the drain current through M_2, I_0, is the output current which is mirrored in M_3 as the final output current. R_0 is employed to extract experimentally the output current.

By applying Kirchhoff's voltage law in the loop formed by $V_D - V_{GS1} - V_{GS2}$ in Figure 1, we can obtain:

$$V_D = V_{GS1} + V_{GS2} \tag{5}$$

Further, if the body effect for M_1 is considered, then the currents through M_1 and M_2 are given by:

$$\begin{aligned} I_{DS1} &= \left(\frac{W}{L}\right)_1 I_{D0} \cdot e^{V_{BS1}\left(\frac{n-1}{nV_T}\right)} e^{\left(\frac{V_{GS1}-V_{Th}}{nV_T}\right)} \\ I_{DS2} &= \left(\frac{W}{L}\right)_2 I_{DO} \cdot e^{\left(\frac{V_{GS}-V_{Th}}{nV_T}\right)} \end{aligned} \tag{6}$$

Since M_2 and M_3 form a translinear loop, then by combining equations (5) and (6), and by considering that the currents $I_{DS1} = I_b$ and $I_{DS2} = I_0$, then the output current can be expressed as:

$$I_0 = A \cdot e^{\frac{V_D}{n^2 V_T}} \tag{7}$$

where A is a constant that depends of I_b, of the process parameters and of the geometric parameters. The constant A can be expressed as:

$$A = \frac{\left(\frac{W}{L}\right)_1 I_{D0} \cdot \left(\left(\frac{W}{L}\right)_2 I_{D0}\right)^{\frac{1}{n}}}{(I_b)^{\frac{1}{n}} \cdot e^{\frac{V_{Th}}{nV_T}\left(1+\frac{1}{n}\right)}} \tag{8}$$

As one sees, expressions (7) and (8) describe the behaviour of the proposed exponential transconductor. The factor A, which is given by equation (8), depends directly on $(W/L)_1$, and inversely to I_b. Then, if the dimensions of M_1 are big, and if I_b holds a low value, then the exponential transconductor can operate with high currents.

3. Simulation results

Post-layout simulations of the proposed exponential circuit are presented in this section. The simulations were obtained in HSPICE employing 0.5 μm AMIS process parameters.

Figure 2 shows the exponential behaviour of the proposed circuit. In this case, $V_{DD} = |V_{SS}| = 0.6$ V, and the source current value I_b is shifted from 1 to 9 μA, in 2 μA steps. The dimensions of the transistors are shown in Table 1.

In Figure 2, it can be observed that the output current presents an exponential response from 10 pA up to 10 μA, which corresponds to an input voltage range near to 800 mV. This conformity is obtained because the input transistor, M_1, presents body effect, and its characteristic also shows an exponential behaviour in the I-V relationship of the MOS transistor. As a result, the body effect improves the response of the circuit. In this form the output current preserves a wide region of work, up to five decades of current range, from 10 pA to 10 μA.

Another important aspect of the behaviour of the exponential circuits is the temperature. The expressions (7) and (8) clearly show that the output current is proportional to the exponential of V_D. Evidently, it can be observed that the output current depends on some additional terms: In the numerator, the output current depends on geometric parameters and the I_{D0} current; in the denominator; the output current depends on the current I_b and of the threshold voltage. Once the dimensions and the current I_b have been chosen, the additional terms depend on process parameters and the temperature. That happens because the current I_{DO} depends on thermal voltage, which also depends on the temperature.

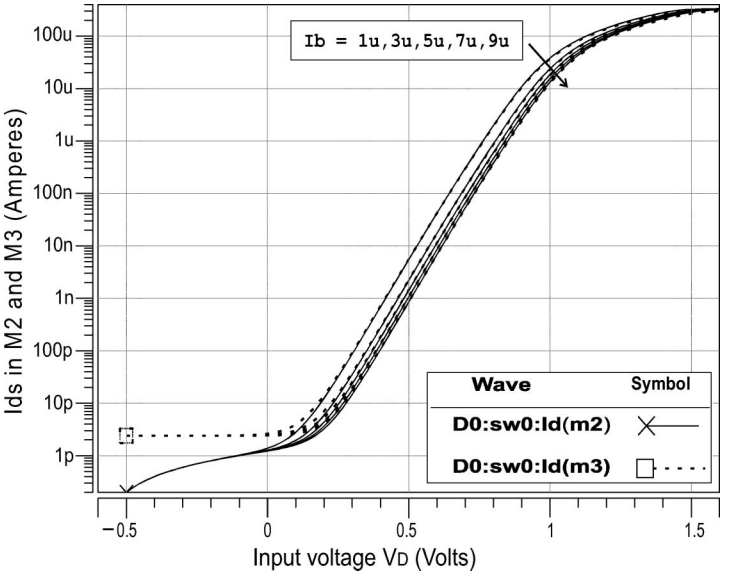

Figure 2. Post-layout simulations of the exponential circuit. I_0 ($I_{ds2,3}$) *versus* the input voltage, V_D.

Table 1. Dimensions of the transistors of the proposed exponential circuit.

	M1	M2	M3
W (μm)	18	18	18
L (μm)	0.9	0.9	0.9
m	4	1	1

m, Number of transistors in parallel.

The variation of the output current, with temperature varying from -55 up to 125°C, is shown in Figure 3. Simulations results show a small variation of the output current with temperature in the range from 10–50°C. However, for temperatures out of this range, the output response variations are more significant, because I_{D0} is directly dependent of the temperature, which is associated to the thermal voltage.

4. Experimental results

The proposed exponential circuit has been experimentally proved employing CD4007 CMOS transistor arrays. In this case, $V_{DD} = 6$ V, $V_{SS} = 0$, $R_0 = 10$ KΩ (which was used to extract the output current), and the LM334 integrated current source was employed to implement the current source I_b. Figure 4 shows the measured output current against the

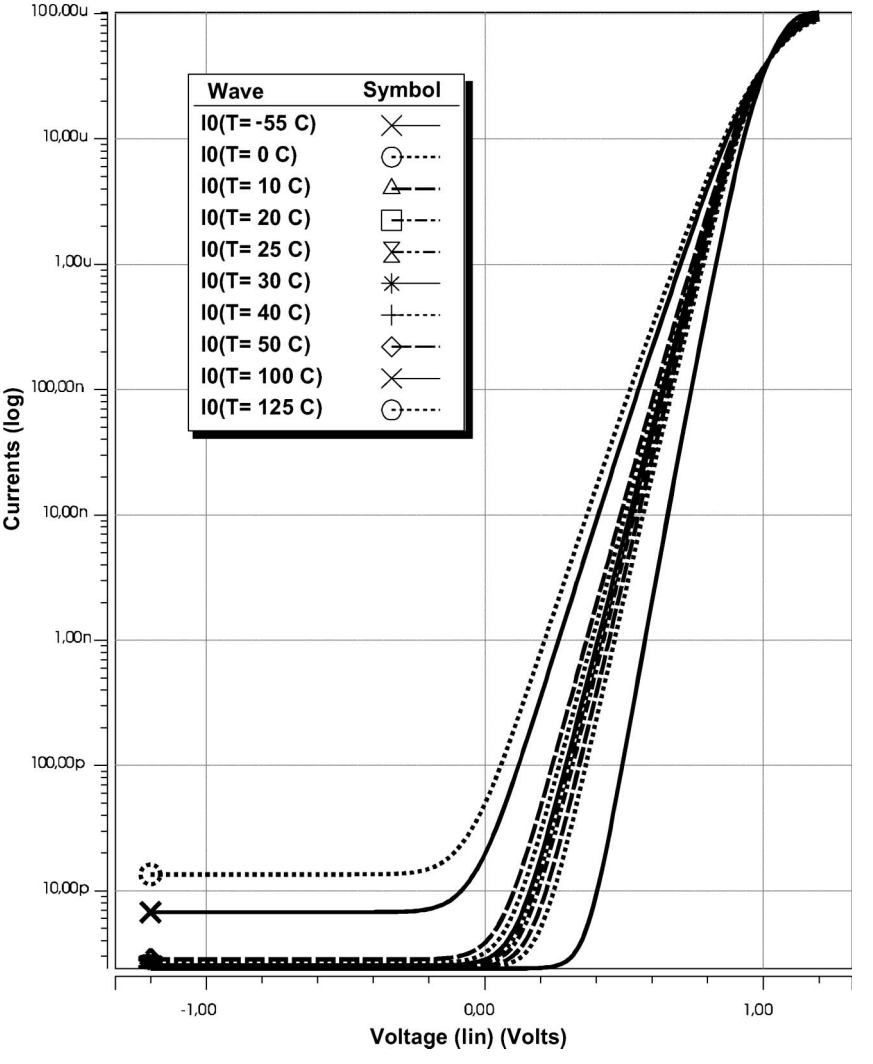

Figure 3. Variation of the output current with temperature.

input voltage in a semilog-y scale for three different values of I_b. The output current presents near to four decades (1 nA–8 μA) corresponding to an input voltage range from 3.3 V to near 4.4 V. Experimental results below 1nA cannot be obtained, mainly because of noise and the high threshold voltage in the CD4007 arrays. However, the circuit of Figure 1 can sustain an exponential behaviour beyond 5 μA.

The proposed exponential transconductor was also fabricated in a 0.5 μm CMOS standard technology of AMIS. Figure 5 shows the micro-photography of the exponential circuit. In this case, the output current was measured with a semiconductor parameter analyser HP4156A model. The experimental results are shown in Figure 6. In this case, $V_{DD} = 1.8$ V, $V_{SS} = 0$, and the input voltage was swept for different values of the current

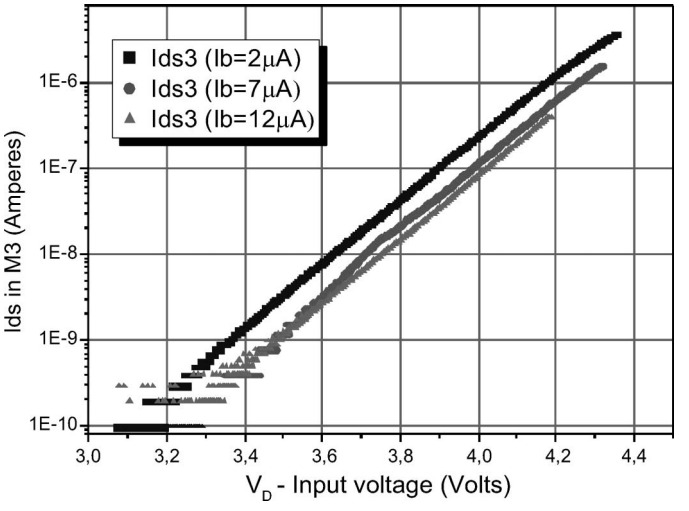

Figure 4. Experimental results of the current output against V_D in semilog scale with CD4007 MOS transistors arrays.

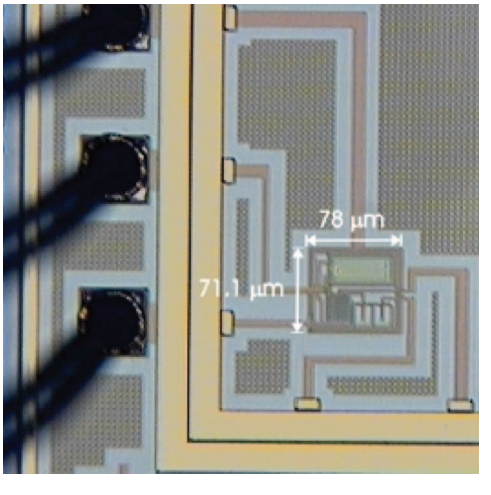

Figure 5. Micro-photography of the exponential transconductor.

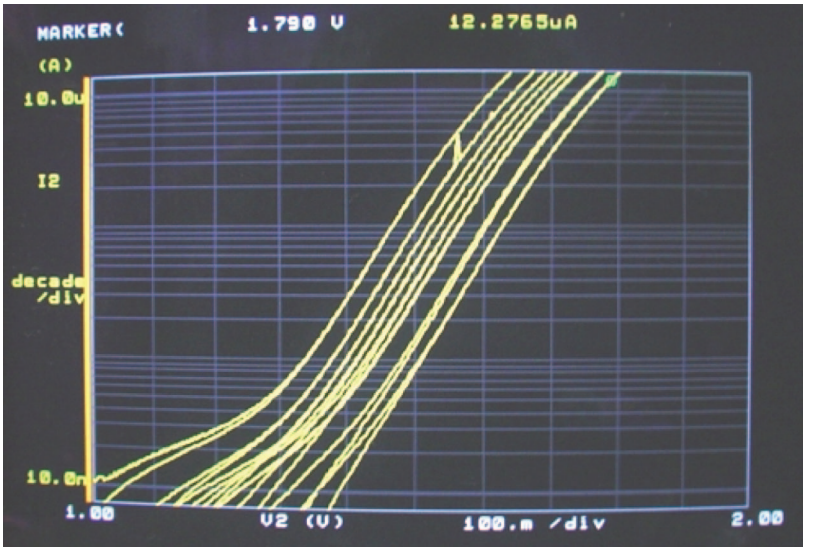

Figure 6. Experimental results of the exponential transconductor fabricated in a 0.5 μm CMOS process.

I_b (10, 20, 30, 40, 50, 100, 130 and 145 μA). As one sees, the output current shows an exponential behaviour above 10 nA and near 10 μA.

5. Conclusions

The design of a novel V-I exponential circuit has been introduced. Simulation results using HSPICE show an exponential behaviour within the region from 10 pA to 10 μA. Also, temperature variations of the current output have been presented. Experimental results, using transistor arrays CD4007, verifies the exponential operation of the proposed circuit in a wider range compared to the already presented ones. The output current presents near to four decades, from 1 nA to 8 μA, which corresponds to an input voltage range from 3.3 V to near 4.4 V. Measurements of the fabricated circuit show an exponential performance above 10 nA and near 10 μA for an input voltage range from 1 to 1.8 V approximately.

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