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Room temperature quantum tunneling and Coulomb blockade in silicon-rich oxide

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ABSTRACT

We studied the electrical properties of silicon nanocrystals (Si-ncs) with a wide size distribution embedded in an oxide matrix. A wide Coulomb gap, clear current bumps, and significant current oscillations and jumps were observed at room temperature in the current vs. voltage characteristics of an Al/silicon-rich oxide/Si MOS-like structure. These anomalies can be well explained by quantum tunneling and Coulomb blockade effects. High-frequency capacitance vs. voltage, and conductance vs. voltage curves show jumps in similar voltage range supporting this explanation. The fact that the charging energy due to the Coulomb blockade effect is much larger than the quantum level spacing weakens the strict size-dependence of the quantum tunneling. The high density of Si-ncs in the oxide layer also enables the carriers to always find Si-ncs of similar size close enough to tunnel through.

1. Introduction

Self-assembly silicon nanocrystals (Si-ncs) embedded in dielectrics have drawn much attention from many researchers recently due to their potential applications in nanoelectronics and optoelectronics. Devices such as Si-based light-emitting diodes [1,2], single electron transistors [3], single electron memories [4], ultra-violet (UV) sensors [5] and photovoltaic solar cells [6] have been proposed. The electrical properties of Si-ncs are of particular importance for their applications. To date, the electrical properties of Si-ncs have been studied extensively [7–14]. A large diversity of experimental phenomena in electrical characterizations have been reported, such as single electron charge-trapping effect [7,8], resonant tunneling transport [9,10], current oscillations [11,12] and capacitance or current switches between different levels [13,14]. The reason for such a diversity of experimental observations may be due to the differences in the microstructure of the studied materials used in the course of the different studies. The density, shape, size and locations of Si-ncs in dielectrics should play an important role for their electrical properties. These parameters depend on the fabrication techniques and the deposition conditions, e.g., the excess Si content, substrate surface morphology, film thickness, etc. However, all above-reported results, which provide useful information for the deep understanding of the electrical properties of Si-ncs, can be associated with the quantum confinement and Coulomb blockade effect in the Si-ncs.

For carrier transport perpendicularly through an oxide layer consisting of Si-ncs, the Si-ncs play a key role. The embedded Si-ncs can form percolation paths for carrier transport, and hence the current is significantly increased. At low-electrical field, the carrier transport between Si-ncs is dominated by sequential tunneling, and other transport mechanisms such as Fowler–Nordheim tunneling can be neglected [15]. Thus the transport properties are very sensitive to the Si-ncs size, size distribution and their inter-distance (or the barrier thickness). It is generally believed that uniform Si-ncs are essential for observing quantum effects; thus, many experimental approaches trying to fabricate uniform Si-ncs have been devoted. However, synthesis of uniform Si-ncs embedded in a dielectric is not an easy work although a success has been achieved by using a superlattice approach [16]. On the other hand, our recent experimental results indicate that significant quantum effect can still be observed in a self-assembled Si-ncs/SiO_2 system with large variation in Si-ncs sizes [11]. One possible reason for our samples is that the charging energy due to the Coulomb blockade effect is much larger than

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quantum level spacing, thus weakening the sensitive size-dependence of the quantum tunneling [9]. Another reason could be due to the high density of Si-ncs in oxide, which was achieved by controlling both the partial pressure ratio of the reactant gases and the substrate surface texturing.

In this article, we report significant resonant tunneling and current oscillations in an Al/silicon-rich oxide (SRO)/Si metal-oxide-semiconductor (MOS)-like structure. The SRO layer is a two-phase material with high density of Si-ncs embedded in an oxide matrix fabricated by low-pressure chemical vapor deposition (LPCVD) method. The results indicate that significant room temperature resonant tunneling and Coulomb blockade effects can be observed in a "large device" with random distributed self-assembly Si-ncs. These results are of significance in future devices made of self-assembly nanocrystalline silicon based on resonant tunneling and Coulomb blockade effects.

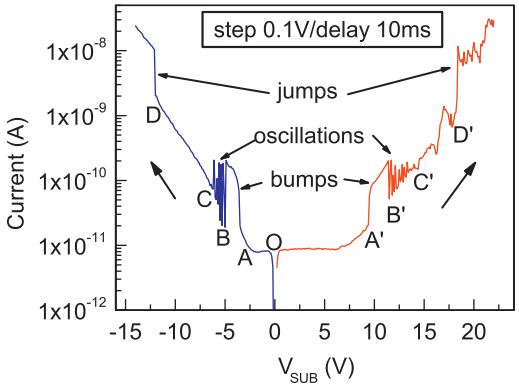

Fig. 1. Typical *I–V* curves under surface accumulation and inversion conditions. The voltage sweep directions are indicated by arrows.

2. Experiments

The samples have an Al/SRO/Si MOS-like structure, where the SRO layer is a two-phase material consisting of Si-ncs embedded in an oxide matrix. The SRO layer with a thickness of ~600 nm was deposited by LPCVD on n-type c-Si wafers with a (1 0 0) orientation and a resistivity of ~1–3 Ω-cm. The surface of the c-Si substrates was mechanically polished with 1-μm diamond sand, producing a high density of scratches and pits. The reason for the substrate surface texturing is to obtain a high density of Si-ncs in the deposited layer because the pits and scratches may act as nucleation sites. Standard RCA (Radio Corporation of America) cleaning process was performed on the substrates before putting them into the deposition chamber. The SRO layer was deposited at 725 °C with SiH_4 and N_2O as reactant gases. The partial pressure ratio Ro, which is defined as $Ro = P(N_2O)/P(SiH_4)$ was fixed to 10 during the deposition. After depositions, the films were thermally annealed at 1100 °C in N_2 for 3 h to crystallize the Si-ncs. The microstructure of the SRO layer was studied using a transmission electron microscope (TEM; Tecnai F30, PHI company) operated with an acceleration voltage of 300 kV. Front Al gate electrodes (area $A = 9.5 \times 10^{-3}\,cm^{-2}$) were evaporated on the annealed samples and back-contacts were also made by evaporating Al after etching off the native oxide layer. Dark quasi-static current vs. voltage (*I–V*) characteristics were measured using a computer-controlled Keithley 6517 electrometers. The applied voltage was swept step-by-step with variable sweep speed by changing the step voltages and delay times. High-frequency (110 kHz) capacitance vs. voltage (*C–V*), and conductance vs. voltage (*G–V*) characteristics were measured using a Keithley 590 CV analyzer. All measurements were performed at room temperature in dark with the bias voltage applied to the substrate (V_{SUB}).

3. Results

Fig. 1 shows the typical *I–V* curve of the devices. Clearly, in both bias directions similar anomalies were observed. At small bias voltages (OA, OA′), there is only a very small leakage current. At points A and A′, the current rapidly increased to high level, and this high current was kept for a period of voltage (regions AB and A′B′). The threshold voltages for the rapid current increase are $V_A = 1.75$ and 6.12 V, for negative and positive substrate biases, respectively. At points B and B′, the current jumps to a low value, forming current bumps (regions AB and A′B′) followed by random oscillations (regions BC and B′C′), the oscillations terminate at points C and C′. After that, the current smoothly increases till points D and D′ where the current shows another jump to a higher level. Sometimes, the current still shows some switches in different current levels when $V > V_D$ as shown in Fig. 1. The anomalies appear at different voltages for positive and negative biases possibly due to the asymmetric MOS-like device structure of the studied devices. When the n-type Si substrate was positively biased, it would exhaust some part of applied voltage and thus the current anomalies appeared at a larger value of voltage compared to the opposite bias direction as shown in Fig. 1.

Fig. 2 (A) and (B) shows *I–V* curves of the devices measured using different delay times and sweep directions, respectively. From Fig. 2(A), one can find that the leakage current in the voltage range of (0 to −2 V) depends on the delay time. Slower voltage sweeps produce smaller leakage current. In the case of step delay time of 3 s, the current approaches the lowest limit of the measurement system. This result indicates the leakage current is a displacement current produced by the charging of the stray capacitance of the device and measurement system, and will not be considered in the next. In this case, the drift current through the SRO layer in the voltage range of (−2 to 8 V) is zero and a wide Coulomb gap (AA′) was thus observed in Fig. 1. Another feature shown in Fig. 2(A) is that the current bump is almost independent of the step delay time. This indicates the current bump is produced by static transport of carriers through the SRO layer and some special conduction mechanisms are set up in this voltage range. However, the current oscillations in region BC depend on the step delay time. At very slow voltage sweep (step delay time 3 s), the oscillations disappear. Fig. 2(B) shows that the current jump at point D depends on the charge-trapping conditions and thus the charging history of the SRO layer. If the SRO layer traps more charges, point D moves to lower voltage. When the voltage sweeps from a large magnitude to a small one, point D appears at lower voltage because in this case more charges have been trapped in the SRO layer. Fig. 2(B) also indicates that the current bump and oscillations do not depend on the voltage sweep directions and this again confirms that they are ascribed to the carrier transport through the SRO layer via a kind of special conduction channel. This will be discussed later.

Fig. 3 shows the high-frequency *C–V* and *G–V* curves. In the voltage region where current bump and oscillations were observed (region AC), some anomalies also appear in *C–V* and *G–V* curves. The capacitance and conductance show some very regular jumps among different levels. The positions of these jumps are random, however, similar jumps were always observed in repeated measurements and in most of the devices of the wafer.

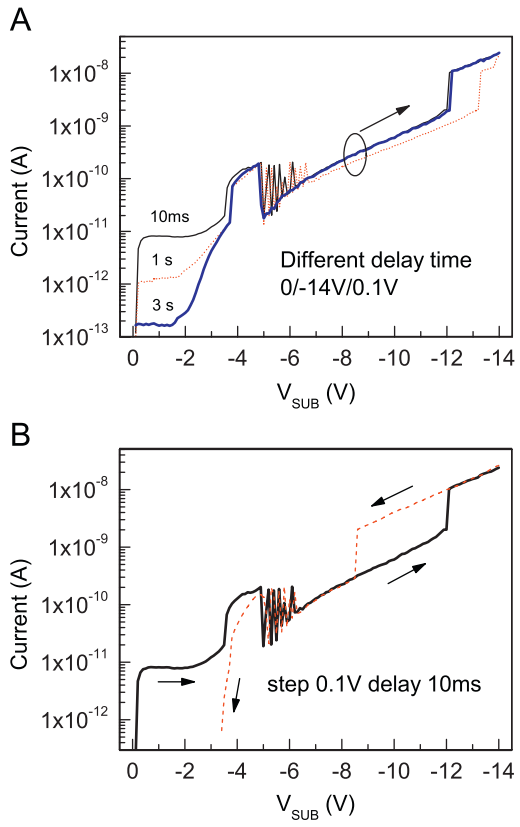

Fig. 2. *I–V* curves measured at different step delay time (A) and sweep directions (B). The step delay times are shown in (A) and the voltage sweep directions are marked by arrows in (B).

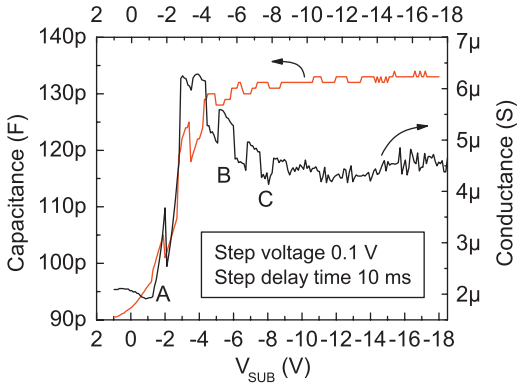

Fig. 3. High-frequency (100 kHz) *C–V* and *G–V* curves of the AI/SRO/Si devices. Random jumps appear in region AC, where the current bump and oscillations were observed.

4. Discussions

In order to understand the observed anomalies in the *I–V*, *C–V* and *G–V* curves, the microstructure of the SRO layer was investigated. Fig. 4 shows the cross-section high-resolution TEM (HRTEM) micrograph of the SRO layer. A high density (around $7.5 \times 10^{11}\,\mathrm{cm}^{-2}$) of Si-ncs dispersed in the SRO layer, which is shown in the figure, and some Si-ncs are encircled to guide the eyes. The shape and size of Si-ncs show a large diversity. The large size is around 8 nm while small one is around 2–3 nm.

The observed anomalies in *I–V* curves are associated with the high-density Si-ncs in the SRO layer because no anomaly in the

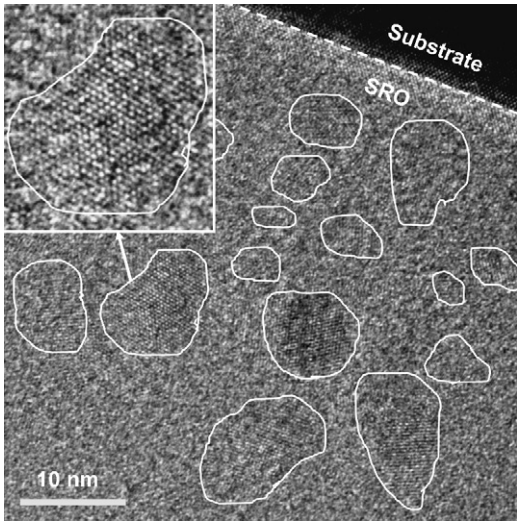

Fig. 4. HRTEM micrograph of the SRO layer. Some Si-ncs are marked to guide the easy. One Si-ne was enlarged for clarity in the inset. The dashed line indicates the Si/SRO interface.

I–V curve was observed in a control sample with a stoichiometric oxide layer instead of SRO. When a negative bias was applied to the substrate, electrons accumulate at the substrate surface. However, if the magnitude of the bias is small, the electrons cannot be injected into the Si-ncs in the SRO layer due to the interplay of quantum confinement and Coulomb blockade effects, producing a large Coulomb gap with drift current being zero. As will be discussed below, the current starts to flow through conduction paths consisting of larger Si-ncs. Thus we can estimate the threshold voltage for current flow, V_T (in the case of accumulation, the applied voltage totally drops at the SRO layer). As for the HRTEM results, the larger Si-ncs have an average size of ~8 nm and average center-to-center distance of ~15 nm. In this case, the quantum level spacing of the Si-ncs is negligible compared with their charging energy. The charging energy of a single Si-nc can be estimated $E_o = e^2/2C_o = 46\,\mathrm{meV}$ (where $C_o = 2\pi\varepsilon_{ox}d$ is the self-capacitance of a Si-nc, ε_{ox} is oxide permittivity and d is diameter of Si-nc). According to the collective effect in multi-tunneling junctions [17–19], $V_T = N \times E_o/e$ (N is the number of Si-ncs in a conduction path). Considering the thickness of SRO layer is 600 nm, a conduction path consists of ~40 larger Si-ncs in average. Thus the estimated threshold voltage for current flow is, $V_T = 1.84\,\mathrm{V}$, in a good agreement with the experimental results as shown in Fig. 1 (the experimental data $V_A = 1.75\,\mathrm{V}$).

With increasing voltage, electrons can overcome the energy barrier to be injected into the Si-ncs; thus, current starts to increase rapidly. Conduction paths consisting of a series of Si-ncs are formed where electrons sequentially tunnel between those Si-ncs at suitable voltages. The fact that the SRO layer contains a high density of Si-ncs enables an electron in a Si-nc to find another similar-sized Si-nc close enough to tunnel through because they have similar physical properties. The conduction paths consisting of larger Si-ncs are first switched on because they have lower energy barriers due to larger sizes of Si-ncs. With increasing voltage, smaller Si-ncs are involved in producing more conduction paths and the current continuously increases. It is noted that an electron in a smaller Si-nc can tunnel not only into a nearby Si-nc of similar size, but also into a nearby larger Si-nc, because a larger Si-nc has a lower energy level. In such a way, conduction paths consisting of Si-ncs of different sizes will be formed; however, in such conduction paths, the Si-ncs sizes

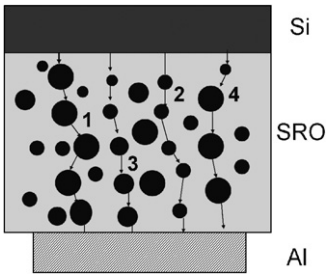

Fig. 5. Schematic of conduction paths. Conduction paths numbered 1 and 2 are formed by Si-ncs of similar sizes; while those numbered 3 and 4 consist of Si-ncs of different sizes.

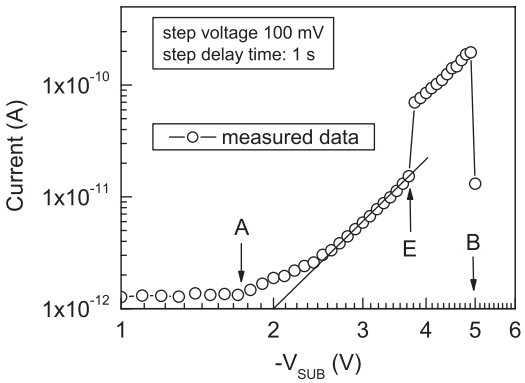

Fig. 6. The current bump in region AB. A power law can well fit the experimental data in the starting region of the bump (region AE), indicating a formation of 1D conduction paths.

should gradually increase in order to enable the sequential tunneling of electrons. The formation of conduction paths is schematically illustrated in Fig. 5.

Fig. 6 plots the typical current bump occurring in region AB in a log–log scale. It is clear that in the starting region of this bump (region AE) the current increases following a power law $I-[(V-V_T)/V_T]^{\zeta}$, where ζ is constant. $\zeta \approx 1.1$ was obtained by fitting of the experimental data, indicating a one-dimensional (1D) conduction path formation in this voltage range [17,18]. That means, the current starts to flow through a 1D conduction path consisting of a series of larger Si-ncs.

When the voltage is increased to V_B, the energy level alignment between Si-ncs in some conduction paths is broken; thus, these conduction paths are switched off and their Si-ncs are charged-up by electrons. The Coulomb blockade effect plays an important role in the rapid switching-off of the conduction paths. The Debye screening length of the SRO layer at room temperature can be estimated $L_D \approx 47$ nm if assuming the density of charged Si-ncs $n = 10^{16}\,\mathrm{cm}^{-3}$, a reasonable value being lower than the density of total Si-ncs in the SRO layer (estimated to be $7.5 \times 10^{16}\,\mathrm{cm}^{-3}$). Therefore, one charged Si-nc can influence the potential of a large cross-section area perpendicular to the transport direction; thus, it can switch off many other nearby conduction paths. The positive feedback of the screening effect rapidly spreads over the whole device and all the conduction paths were switched off very fast (if we call the first switched off conduction paths (SOCP) as 1st-generation SOCP, then the charged Si-ncs in 1st-generation SOCP switched off nearby conduction paths—2nd-generation SOCP: the charged Si-ncs in 2nd-generation SOCP further switched off other nearby conduction paths—3rd-generation SOCP, and so on). This may be the reason for the very rapid decrease of the current at point B (B′).

Two possible reasons may be associated with the current oscillations in regions BC and B′C′. One reason is the random switch on/off of some conduction paths. Because the charging and discharging of a Si-nc can influence the switch on/off of many conduction paths, current will randomly jump in different levels. Another reason may be associated with transient charge transfer between Si-ncs and the electrodes (Al gate and Si substrate) because the current oscillations depend on the step delay time, and oscillations disappear if the delay time is long (Fig. 2(A)). The Si-ncs near the Al/SRO and SRO/Si interfaces dominate this transient process. *C–V* and *G–V* results shown in Fig. 3 support this argument.

In the surface accumulation condition, the capacitance of the MOS devices equals the oxide capacitance. In region AC, both capacitance and conductance show random jumps. Because the SRO layer is a two-phase material, the oxide capacitance C_{ox} consists of an overall Si-ncs capacitance C_{nc} and an oxide matrix capacitance $C_{mx} \cdot C_{ox} = C_{nc} + C_{mx} \cdot C_{mx}$ is constant, thus the jump in C_{ox} is caused by the jump of C_{nc}, or in other words, by the random charging and discharging of the interface Si-ncs. The jumps were mainly observed in region AC because in this region the Fermi level of Si substrate is aligned or near-aligned with the energy levels of the interface Si-ncs, thus the charging and discharging of interface Si-ncs are possible. The lower conductance state (corresponding to higher capacitance state) is associated with the charged-up of the interface Si-ncs. At this state, no other electrons can be injected into the charged-up Si-ncs due to the Coulomb blockade effect. The high-conductance (lower capacitance) state is associated with the empty state of interface Si-ncs and electrons can be injected into the empty Si-ncs causing higher conductance and lower capacitance. In region BC, the energy levels are generally de-aligned; however, the superimposed small high-frequency voltage signal may stimulate the electrons to be injected into interface Si-ncs and the jumps are still observed in *C* and *G*. It is worthy to note that when the interface Si-ncs are charged-up, their equivalent capacitance C_{nc} is zero; however, the surface area occupied by the Si-ncs will work as normal oxide layer and the same area can accumulate more charges than Si-ncs because there is no Coulomb blockade effect in the oxide layer, thus producing higher capacitance. Our results differ from those in Refs. [14,20] possibly because of the different microstructures of the studied materials.

The current oscillations in region BC in *I–V* curves could also be stimulated by the small high-frequency signals. During the measurements, the voltage was scanned step-by-step. The step voltage can be decomposed into a series of high-frequency signals. Some of them may stimulate the transfer of electrons between interface Si-ncs and electrodes, producing random current oscillations. However, these decomposed high-frequency signals cannot persist for a long time, and it should be between 1 and 3 s for our samples, as shown in Fig. 2(A). It was reported that carrier transport time into or from a Si-nc embedded in a silicon nitride matrix can be as long as 0.3 s as determined by *C–V* spectroscopy [15]. Considering the higher barrier of oxide matrix in our samples compared with Ref. [15], the transport time of 1–3 s in our samples is in a good agreement with Ref. [15].

The current jump in point D is possibly associated with the delocalization of electrons in the Si-ncs. It is proposed that when the electrons have high energy, then they will be delocalized from the Si-ncs [9]. These delocalized electrons have high mobility to be transported between Si-ncs and hence 2D conduction paths can be formed, thus a current jump was observed. If the SRO layer trapped a high density of electrons, the average potential energy of electrons in the SRO layer increases. Electrons in Si-ncs will be easier to be delocalized, thus the current jump moves to smaller voltage as shown in Fig. 2(B).

5. Conclusion

Large Coulomb gap, clear current bumps, current oscillations and jumps were observed in the *I–V* characteristics of Al/SRO/Si MOS-like devices at room temperature, where the SRO layer has a large diversity of Si-ncs size distribution. These anomalies can be explained by the quantum tunneling and Coulomb blockade effects. Although the Si-ncs sizes have a wide distribution, the high density of Si-ncs enables the carriers to be transported between Si-ncs of similar sizes. The strong Coulomb blockade effect also weakens the strict requirement to Si-ncs size for resonant tunneling. *C–V* and *G–V* measurements support our explanation.

Acknowledgments

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