ResearchGate

See discussions, stats, and author profiles for this publication at: https://www.researchgate.net/publication/3426298

Fabrication and Characterization of Coplanar Waveguides on Silicon Using a Combination of SiO and...

Article *in* IEEE Transactions on Components and Packaging Technologies · October 2008

DOI: 10.1109/TCAPT.2008.922005 · Source: IEEE Xplore

CITATIONS
4

READS
77

6 authors, including:

Rebeca Leal
Universidad Politécnica de Aguascalientes
4 PUBLICATIONS **5** CITATIONS

SEE PROFILE

I. E. Zaldivar-Huerta
Instituto Nacional de Astrofísica, Óptica y Ele...
56 PUBLICATIONS **111** CITATIONS

SEE PROFILE

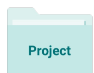
Carmen Maya
Ensenada Center for Scientific Research and ...
38 PUBLICATIONS **153** CITATIONS

SEE PROFILE

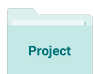
Mariano Aceves
Instituto Nacional de Astrofísica, Óptica y Ele...
176 PUBLICATIONS **753** CITATIONS

SEE PROFILE

Some of the authors of this publication are also working on these related projects:



single electron devices View project



Studies and Integration of Silicon Based Light Emitting Systems View project

All content following this page was uploaded by Rebeca Leal on 04 March 2014.

The user has requested enhancement of the downloaded file.

Fabrication and Characterization of Coplanar Waveguides on Silicon Using a Combination of SiO_2 and SRO_{20}

Rebeca Leal-Romero, José Eleazar Zuñiga-Juárez, Ignacio E. Zaldívar-Huerta, *Member, IEEE*, María del Carmen Maya-Sánchez, *Member, IEEE*, Mariano Aceves-Mijares, *Member, IEEE*, and J. Apolinar Reynoso-Hernández, *Member, IEEE*

***Abstract*—In this work, the use of silicon rich oxide (SRO) and chemical vapor deposition SiO_2 double layers as passivation films of coplanar waveguides (CPW) on high resistivity silicon (HR-Si) with an N^+ backside is studied. The microwave performance of the fabricated CPWs is evaluated by computing the attenuation loss of the devices in the 0.045–50 GHz frequency range. Experimental results show that the N^+ layer can be used without affecting CPW performance. Also, using a combined dielectric layer (SRO_{20}/SiO_2), the attenuation losses are reduced compared to single dielectric layers.**

***Index Terms*—Attenuation constant, coplanar waveguide (CPW), dielectric constant, silicon rich oxide (SRO), traveling wave.**

I. Introduction

THE increasing number of microwave functions that can be performed by semiconductor devices has contributed to the use of coplanar waveguide (CPW) and transmission lines on monolithic microwave integrated circuits (MMICs) and microwave integrated circuit (MICs). CPW allows the superficial connection of flip-chip active and passive devices reducing the cost and size of the packages [1], [2]. Researchers are now devoted to integrate all parts on the same monolithic Si chip, and many reports using silicon to develop high frequencies devices can be found in the literature. Currently, efforts are being focus on decreasing the losses of CPWs built on silicon. So in order to reduce the conductor and dielectric looses a thicker metal layer as well as thicker dielectric layer are often used [3]–[6]. However, the interface losses [5] which are due to charge carriers at the interface between the dielectric layer and silicon can not be reduced increasing the thick metal and the thick dielectric layer. Therefore the passivation layers placed between the electrodes and the substrate play a very important role, for example in [7] it is reported that the inclusion of a discontinuous SiO_2 film between the CPW metal electrodes and the HR-Si (High Resistivity Silicon) substrate reduces the DC leakage current. Fouad *et al.* [8] have proposed the use of Benzocyclobutene (BCB) dielectric as a passivation film on micromachined structures using low resistivity silicon. In [9], it was successfully demonstrated that the use of silicon rich oxide (SRO) on HR-Si substrate reduces attenuation losses. In addition, if HR-Si is used as a substrate of silicon integrated circuits a highly doped back layer is needed to make contact with the common substrate [10]. HR-Si is usually lightly type N, and an N^+ backside layer is done by implantation. However, to our knowledge the effect of the N^+ layer on the attenuation losses of the CPWs has not been studied until now. Thus, the purpose of this paper is to investigate the microwave performance of a CPW fabricated on high resistivity silicon (HR-Si) substrate with an N^+ backside layer and the use of the SRO20 as pasivation layer for reducing the losses due to charge carriers at the interface. In addition, the study includes the combination of silicon dioxide (SiO_2) and silicon rich oxide (SRO) double layers between the CPW metal conductors and the substrate. The experimental details are discussed in Section II. Section III describes the electrical characterization methods used to calculate the attenuation constant (α), the effective dielectric constant (ε_{eff}), and the characteristic impedance (Z) parameters. Section IV is devoted to showing experimental results. Finally, in Sections V and VI, the results are discussed and conclusions are drawn.

Manuscript received March 12, 2007; revised December 20, 2007. First published May 23, 2008; current version published September 17, 2008. This work was supported by INAOE-CICESE and CONACYT—México Scholarship 182340. This work was recommended for publication by Associate Editor F. Shi upon evaluation of the reviewers comments.

R. Leal-Romero is with the Centro de Investigación Científica y de Educación Superior de Ensenada (CICESE), Ensenada C. P. 22860, México. She is also with the Instituto Nacional de Astrofísica, Óptica y Electrónica (INAOE), Puebla C. P. 72000, México (e-mail: rleal@cicese.mx).

J. E. Zuñiga-Juárez, M. del Carmen Maya-Sánchez, and J. A. Reynoso-Hernández are with the Centro de Investigación Científica y de Educación Superior de Ensenada (CICESE), Ensenada C.P. 22860, México (e-mail: ezuniga@cicese.mx; mcmaya@cicese.mx; apolinar@cicese.mx).

I. E. Zaldívar-Huerta and M. Aceves-Mijares are with the Instituto Nacional de Astrofísica, Óptica y Electrónica (INAOE), Puebla C. P. 72000, México (e-mail: zaldivar@inaoep.mx; maceves@inaoep.mx).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCAPT.2008.922005

II. Fabrication Description

Fig. 1 shows the structures fabricated. In all cases high resistivity silicon (HR-Si) type N was used as a substrate. The resistivity of the wafers is 4000 Ω-cm with 400 μm of thickness and an N^+ layer is formed in the substrate's back implanting Phosphorus. Fig. 1 shows the schematic representation of the different structures built. For the structures corresponding to Fig. 1(a) and (c), the SiO_2 was obtained by the use of an atmospheric pressure chemical vapor deposition (APCVD) system, and the gases used were SiH_4, O_2 and N_2. For structures corresponding to Fig. 1(b) and (c), the SRO was obtained by

1521-3331/$25.00 © 2008 IEEE

Authorized licensed use limited to: CICESE. Downloaded on May 25,2010 at 16:44:12 UTC from IEEE Xplore. Restrictions apply.

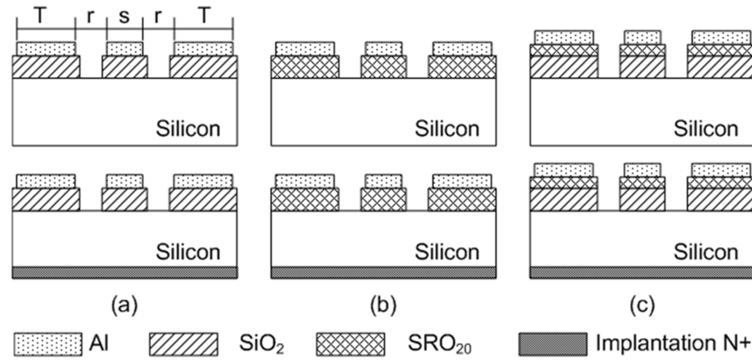


Fig. 1. Schematic of the CPW fabricated on Si HR and Si HR-N^+

TABLE I
DEPOSITIONS CONDITIONS FOR SiO_2 AND SRO_{20} AND THICKNESS MEASURED

Dielectric	Technique	Gases	Temp (ºC)	Time (min)	Thickness (µm)
SiO_2	APCVD	SiH_4, O_2, N_2	450	45	2.03
SRO_{20}	LPCVD	SiH_4, N_2O	700	125	0.67

TABLE II
CPW DIMENSIONS: MEASURED (NOMINAL)

Structure	T (µm)	s (µm)	r (µm)	Dielectric
CPW1	350 (360)	95 (100)	55 (50)	SiO_2
CPW2	350 (360)	95 (100)	55 (50)	SRO_{20}
CPW3	350 (360)	95 (100)	55 (50)	SRO_{20}/ SiO_2

the chemical reaction between SiH_4 and N_2 O in a low pressure chemical vapor deposition (LPCVD) system. The excess of silicon is determined by the gas ratio R_0 [11] ($R_0 = 3$ produces 17% silicon excess and R_0 >100 produces stoichiometric SiO_2). $R_0 = 20$ was used in this experiment. Table I shows the deposition conditions and the layer thickness obtained under those conditions. The thickness and the refractive index of the dielectric films were measured using a Gaertner ellipsometer model L117 with a 6328 Å helium neon laser and a 70° angle of incidence. Aluminum was used as a conductive layer on the strips and it was obtained by evaporation with an electron gun. The dielectric films and aluminum layer were patterned to form the ground (T) and the signal (s) strips with a gap (r) between the ground and the signal strips. The dimensions of the strips were measured using an optical microscope and a reticule with a filament. Results of the measurements are shows in Table II (the values between parentheses correspond to the dimensions of the mask used). The length of the structures is 1 and 4 mm, referred to as LA and LC, respectively. The thickness of the aluminum layer is 1.3 μm and it was measured by the use of an Alpha Step profiler.

III. THEORETICAL METHODS

In the microwave characterization of the CPW investigated, an automatic network analyzer HP85510C system (ANA), a Cascade microtech™ probe station and coplanar probes were utilized. To assess the high frequency performance of the CPW under study we use the characteristic impedance (Z_c) and the propagation constant (γ). From the knowledge of the propagation constant the dielectric constant and the line losses are determined.

A. Evaluation of the Characteristic Impedance

To determine the characteristic impedance of the CPW the S-parameters are measured. This was achieved by calibrating the ANA at the end of the probe tips using the Line-Reflect-Mach (LRM) calibration technique in the 0.045–50 GHz range. The measured S parameters are converted to a transmission matrix $(\mathbf{T})$ to determine the line impedance using the method reported in [9], [12]. The characteristic impedance (Z_L) is computed from the reflection coefficient (Γ) as [9]

$$Z_L = Z_0 \left(\frac{1+\Gamma}{1-\Gamma}\right) \tag{1}$$

Γ can be determined by the solution to the quadratic expression

$$\left(\frac{1}{\Gamma}\right)^2 t_{21} + \left(\frac{1}{\Gamma}\right)(t_{22} - t_{11}) - t_{12} \tag{2}$$

where $t_{\rm ij}$ (with $i = 1, 2$ and $j = 1, 2$) are the elements of the transmission matrix $\mathbf{T}$ of the CPW.

Authorized licensed use limited to: CICESE. Downloaded on May 25,2010 at 16:44:12 UTC from IEEE Xplore. Restrictions apply.

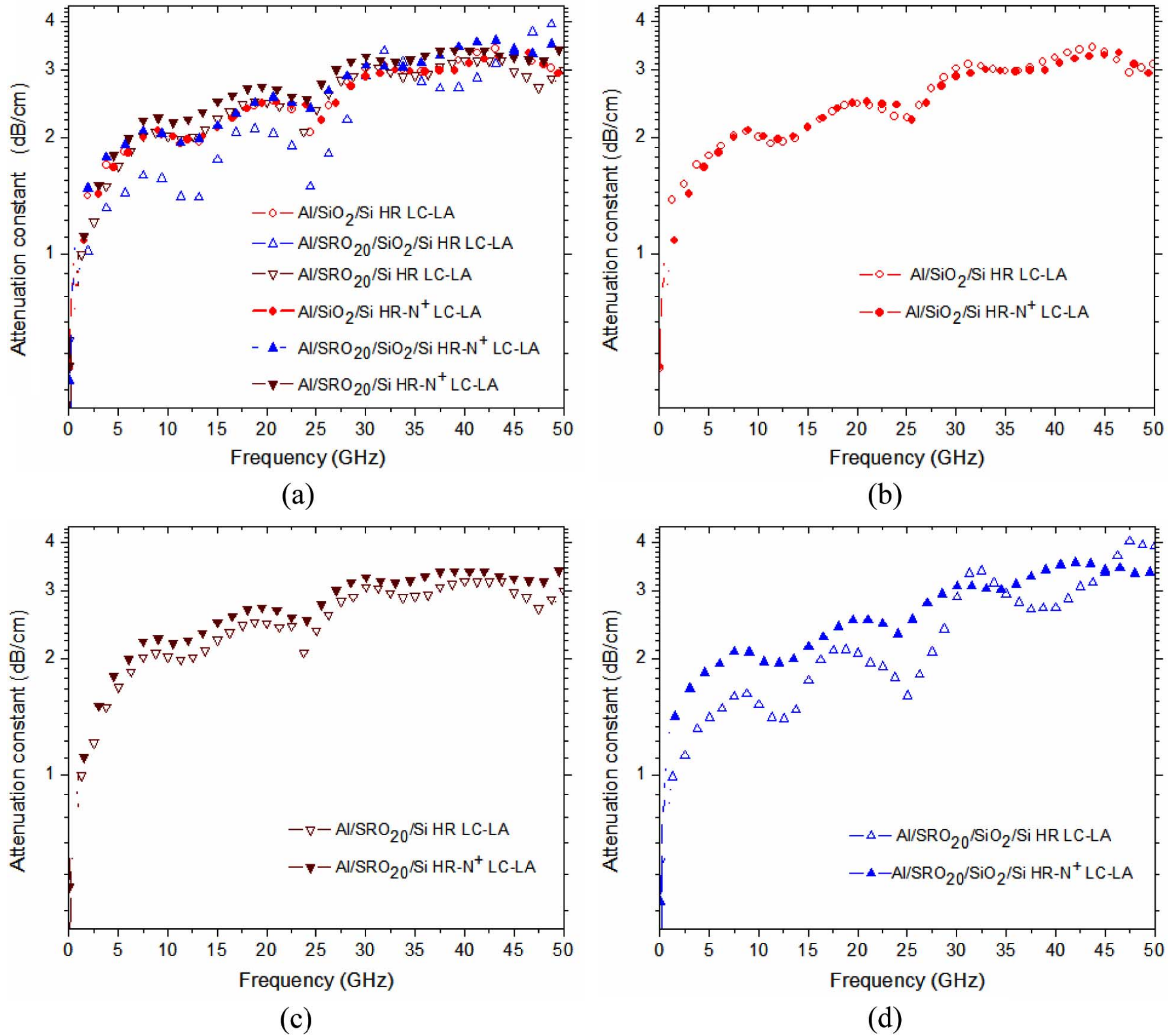


Fig. 2. CPW Losses as a function of frequency on Si HR and on Si HR-N^+ for (a) all the structures, (b) Al/SiO_2/Si, (c) Al/SRO_{20}/Si, and (d) Al/SRO_{20}/SiO_2/Si structures.

B. Evaluation of the Attenuation and the Effective Dielectric Constants

Prior to the attenuation constant and the dielectric constant estimation the line propagation constant was determined using an improved Line-Line (L–L) method [13], [14]. The main feature of the improved L-L method is that the ANA is not calibrated, and only the switching errors are corrected with the procedure reported in [15]. Indeed, the use of an uncalibrated ANA improves the measurements because residual errors generated by the non-idealities of the standards are eliminated. Then, to ascertain the attenuation constant (α) and the effective dielectric constant $(\varepsilon_{\text{eff}})$, we first determine the traveling wave (λ) of the line using the method reported in [13], [14]. Two uniform CPWs of different length but with the same characteristic impedance are used. According to the method reported in [13], [14] γ can be calculated by

$$\gamma = \frac{1}{L_2 - L_1} \ln(\lambda) \tag{3}$$

where L_2 and L_1 are the lengths of the long and the short lines, respectively, and λ can be computed using the expression (17) reported in [13]. The propagation constant (γ) is defined as

$$\gamma = \alpha + j\beta \tag{4}$$

where α is the attenuation constant (Np/m) and β is the phase constant (radians/m). On the other hand, the effective dielectric constant is given as

$$\varepsilon_{\text{eff}} = \left(\frac{\beta c}{2\pi f}\right)^2 \tag{5}$$

where c and f are the speed of light and the frequency, respectively.

IV. Experimental Results

The attenuation constant, α, and the effective dielectric constant, ε_{eff}, were computed from the knowledge of γ, as described in the Section III-B. The lines LA (1 mm) and LC (4 mm) were used as L_1 and L_2, respectively. Fig. 2 shows

Authorized licensed use limited to: CICESE. Downloaded on May 25,2010 at 16:44:12 UTC from IEEE Xplore. Restrictions apply.

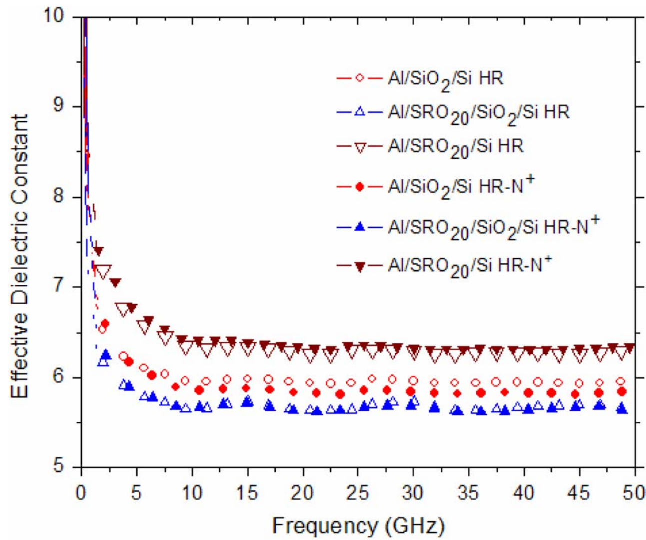


Fig. 3. CPW Effective dielectric constant versus frequency for all the structures.

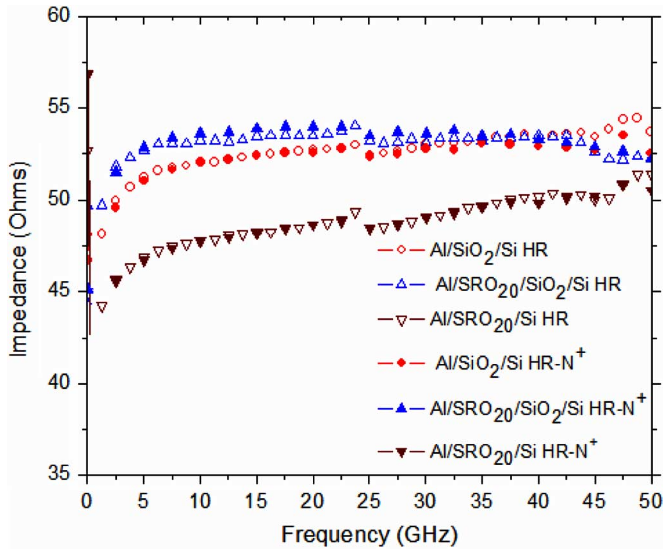


Fig. 4. CPW Characteristic impedance versus frequency for all the structures.

the frequency dependence of the attenuation constant. Fig. 2(a) compares the losses of the SiO_2, SRO_{20}, and SRO_{20}/SiO_2 structures fabricated on HR-Si substrate with and without the N^+ back layer. From Fig. 2(a) it is observed that the losses of the SRO_{20}/SiO_2 structures deposited on the HR-Si substrate without N^+ are the lowest of all. Structures made of SiO_2 and SRO_{20} single layers have similar losses and the N^+ layer has a minimum effect, as can be seen from Fig. 2(b) and (c). However, the structure SRO_{20} shows lower losses than the structure SiO_2 at low frequency. Because the SiO_2 layer is thicker than the SRO_{20} layer it would be expected that the losses in the SiO_2 structure were lower than the losses of the SRO_{20} structure. However, we observe that the SRO_{20} structure has lower losses than SiO_2 structure. This reduction of the losses can be due to an improvement of the interface losses. The SRO_{20}/SiO_2 dual layer produces the lowest losses; see Fig. 2(d). However, the N^+ layer increases the losses in this structure, but continues being similar to the single layers. Plots of the effective dielectric constant ($\varepsilon_{\rm eff}$) versus frequency for the lines fabricated on HR-Si with and without an implanted N^+ back layer are shown in Fig. 3. The frequency dependence of this parameter indicates whether a transmission line is dispersive or not. In all cases the value of $\varepsilon_{\rm eff}$ is approximately 6 and is practically constant in the measured frequency range. Significant changes are not remarkable between the two types of substrate used. Finally, Fig. 4 shows the frequency dependence of the characteristic impedance for the lines fabricated on HR-Si and HR-Si-N^+, respectively. This value is between 47 and 53 Ω. A significant difference in the line impedance between the two types of substrate is not observed. The impedance of the SRO_{20} structures is lower than for the other two types of structures. The impedance of the CPW structures depends on the dimensions (r, s and T) and the substrate characteristics. Indeed, it is expected that the characteristic impedance varies since the dielectric layer is different.

V. Conclusion

In this paper, we have evaluated and compared the attenuation coefficient, the effective dielectric constant, and the characteristic impedance of the CPWs fabricated on HR-Si substrates with and without a N^+ back layer. Different dielectric films such as SiO_2, SRO_{20}/SiO_2 and SRO_{20} were used. The double layer of SRO_{20}/SiO_2 on a HR-Si substrate has a positive impact on the CPW losses. In fact, we have found a reduction of the attenuation coefficient using this kind of dielectric compared with single layer dielectrics. On the other hand, when a high resistivity Si substrate with an N^+ back layer was used, the losses for SRO_{20}/SiO_2 structures increase. However the losses obtained are similar to those of the CPW structures using SiO_2 and SRO_{20}. The losses of SiO_2 and SRO_{20} structures do not present important changes when they are deposited on HR-Si-N^+. Therefore, the impact of the N^+ back layer in the substrate on the loss is not significant. The effective dielectric constant and the characteristic impedance do not present significant changes when the CPWs are fabricated on HR-Si or on HR-Si-N^+.

Acknowledgment

The authors would like to thank P. Alarcon for his help during the preparation of the samples and J. de Jesús Ibarra Villaseñor and B. Ramírez for device measurements.

References

[1] A. C. Reyes, S. M. El-Grazaly, S. J. Dorn, M. Dydyk, D. K. Schroder, and H. Patterson, "Coplanar waveguide and microwave inductors on silicon substrate," *IEEE Trans. Microw. Theory Tech.*, vol. 43, no. 9, pp. 2016–2022, Sep. 1995.

[2] K. C. Gupta, R. Garg, I. Bahl, and P. Bhartia, *Microstrip Lines and Slotlines*, 2nd ed. Norwood, MA: Artech house, 1996.

[3] L.-L. W. Leung, W.-C. Hon, and K. J. Chen, "Low-loss coplanar waveguide interconnects on low-resistivity silicon substrate," *IEEE Trans. Compon. Packag. Technol.*, vol. 27, no. 3, pp. 507–512, Sep. 2004.

[4] Y. Zhu, S. Wang, and H. Wu, "Multilayer coplanar waveguide transmission lines compatible with standard digital silicon technologies," in *IEEE MTT-S Int. Dig.*, 2007, pp. 1567–1570.

[5] C. Schöllhorn, W. Zhao, M. Morschbach, and E. Kasper, "Attenuation mechanisms of aluminum millimeter-wave coplanar waveguides on silicon," *IEEE Trans. Electron Devices*, vol. 50, no. 3, pp. 740–746, Mar. 2003.

Authorized licensed use limited to: CICESE. Downloaded on May 25,2010 at 16:44:12 UTC from IEEE Xplore. Restrictions apply.

[6] Y. Zhu and H. Wu, "A 10–40 GHz 7 dB directional coupler in digital CMOS technology," in *IEEE MTT-S Int. Dig.*, 2006, pp. 1551–1554.
[7] Y. Wu, H. S. Gamble, B. M. Armstrong, V. F. Fusco, and J. A. Carson Stewart, "SiO_2 interface layer effects on microwave loss of high-resistivity CPW line," *IEEE Microw. Guided Wave Lett.*, vol. 9, no. 1, pp. 10–12, Jan. 1999.
[8] F. Bouchriha, K. Grenier, D. Dubuc, P. Pons, R. Plana, and J. Graffeuil, "Minimization of passive circuits losses realized on low resistivity silicon using micro-machining techniques and thick polymer layer," in *IEEE MTT-S Int. Dig.*, Jun. 2003, pp. 959–962.
[9] J. A. Reynoso-Hernández, R. Rangel-Rojo, M. Aceves, I. Zaldivar, L. E. Sánchez, and M. Herrera, "Influence of the SRO as passivation layer on the microwave attenuation losses on the CPW's fabricated on HR-Si," *IEEE Microw. Wireless Compon. Lett.*, vol. 13, no. 12, pp. 508–510, Dec. 2003.
[10] M. Aceves-Mijares, M. Estrada, A. Cerdeira, and A. Cerdeira-Estrada, C. A. Grimes, E. C. Dickey, and M. V. Pishko, Eds., "Silicon PIN diodes as radiation detectors," *All Rights of Reproduction in any Encyclopedia al Sensors*, vol. 9, pp. 431–451, 2006.
[11] D. Dong, E. A. Irene, and D. R. Young, "Preparation and some properties of chemically vapor-deposited Si-Rich SiO_2 and Si_3N_4 films," *J. Electrochem. Soc.*, vol. 125, no. 5, pp. 819–823, May 1978.
[12] J. A. Reynoso-Hernández, R. Rangel-Rojo, M. Aceves, I. Zaldivar, L. E. Sánchez, and M. Herrera, "A method for computing the characteristic impedance of transmission lines using the wave cascade matrix formalism," in *Proc. 61st ARFTG*, Philadelphia, PA, Jun. 12–13, 2003, pp. 349–355.
[13] J. A. Reynoso-Hernández, "Unified method for determining the complex propagation constant of reflecting and nonreflecting transmission line," *IEEE Microw. Wireless Compon. Lett.*, vol. 13, no. 8, pp. 351–353, Aug. 2003.
[14] J. A. Reynoso-Hernández, F. Estrada M., T. Parra, K. Grenier, and J. Graffeuil, "An Improved for the wave propagation constant γ estimation in broadband uniform millimeter-wave transmission line," *Microw. Opt. Technol. Lett.*, vol. 22, no. 4, pp. 268–271, Aug. 1999.
[15] ARFTG, "Short Course on Measurements and Metrology for a Wireless World," San Diego, CA, Nov. 27–28, 2001.

Rebeca Leal-Romero was born in Xalapa Veracruz, Mexico, in 1980. She received the B.S. degree in electronic instrumentation engineering degree from the University of Veracruz, Xalapa, Mexico, in 2002, the M.S. degree from the National Institute of Astrophysics, Optical and Electronics (INAOE), Puebla, Mexico, in 2006, and is currently pursuing the Ph.D. degree in electronics and telecommunications at the Centro de Investigación Cientifica y de Educación Superior de Ensenada (CICESE), Tijuana-Ensenada, Mexico.

Her research interests are in the study of coplanar and microstrip transmission lines manufactured on silicon using rich silicon oxide (SRO) like passivation layer interface.

J. E Zúñiga-Juárez was born in Ensenada, Mexico, in 1977. He received the B.S. degree in electronic engineering from the University of Baja California, Tijuana, Mexico, in 1999 and the M.S. degree from the Centro de Investigacion Cientifica y de Educacion Superior de Enseanda (CICESE), Ensenada, Mexico, in 2003 where he is currently pursuing the Ph.D. degree in electronics and telecommunications.

His research interests are in high frequency on-wafer measurements, and MESFET, HEMT, and HBT device modeling.

Ignacio E. Zaldívar-Huerta (M'02) was born in Izúcar de Matamoros, Puebla, México. He received the B.S. degree in electronics engineering from Universidad Autónoma de Puebla (UAP) in 1992, the M.S. degree in microelectronics from the Instituto Nacional de Astrofísica, Óptica y Electrónica (INAOE), Puebla, in 1995, and the Ph.D. degree in sciences for the engineering from the Université de Franche-Comté, Besancon, France, in 2001.

Since February 2002, he has been an Associate Researcher with the Department of Electronics, Instituto Nacional de Astrofísica, Óptica y Electrónica in Tonantzintla, Puebla. His current research interests are primarily in fiber optics communication systems, and high-speed electro-optic devices on silicon.

María del Carmen Maya-Sánchez (M'02) was born in Mexico City, Mexico, in 1972. She received the B.S. degree in communications and electronic engineering from the Instituto Politecnico Nacional, Mexico City, in 1995, the M.Sc. degree in electronic and telecommunications from the Centro de Investigación Cientifica y de Educación Superior de Ensenada (CICESE), Ensenada, Mexico, in 1997, and the Ph.D. degree from the Universitat Politecnica de Catalunya, Barcelona, Spain, in 2003.

Since 2004, she has been a Researcher with the High Frequency Group, Electronics and Telecommunications Department, CICESE. Her research interests are in MESFET, HEMT, and HBT device modeling, noise measurements techniques, and the analysis, design, and characterization of microstrip and coplanar transmission lines.

Mariano Aceves-Mijares (M'93) has been working in the development of semiconductor devices for more than 20 years. He leads projects supported for various national and international institutions. He is author or coauthor of more than 200 papers in technical journals and proceedings. He is part of the academic staff of the postgraduate program of the National Institute of Astrophysics, Optical and Electronics (INAOE), Puebla, Mexico. He has also expended some sabbatical periods working with the national and international industry. He has developed new silicon devices and holds three patents. Currently, he is with the Microelectronics Department, INAOE.

J. Apolinar Reynoso-Hernández (A'92–M'03) received the B.S. degree in electronics and telecommunications engineering from La Escuela Superior de Ingeniería Mecánica y Electrica del Instituto Politécnico Nacional (ESIME-IPN), Mexico, in 1980, the M.Sc. degree in solid state physics from The Research and Advanced Studies Center, National Polytechnic Institute (CINVESTAV-IPN), Zacatenco, Mexico, in 1985, and the Ph.D. degree in electronics from Université Paul Sabatier-LAAS du CNRS, Toulouse, France, in 1989. His Ph.D. thesis was on low frequency noise in MESFET and HEMTs.

Since 1990, he has been a Researcher with the Electronics and Telecommunications Department, CICESE, Ensenada, Mexico. His areas of specialized research interest include, high frequency on-wafer measurements, high frequency device modeling, linear, nonlinear, and noise device modeling and switched power amplifiers.

Dr. Reynoso-Hernández received the ARFTG (2001) and ARFTG (2007) Best Paper Poster Award. He is frequently a Reviewer for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES and the IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS.

View publication stats
Authorized licensed use limited to: CICESE. Downloaded on May 25,2010 at 16:44:12 UTC from IEEE Xplore. Restrictions apply.