Development of a modeling methodology for circuits with memristors

by

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A dissertation submitted to the Electronics Department in partial fulfillment of the requirements for the degree of

D.Sc. in Electronics

at the

National Institute for Astrophysics, Optics and Electronics
February 2015
Tonantzintla, Puebla

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Resumen

A partir de la publicación revolucionaria del Profesor Chua en los años 70’s, el concepto del memristor ha sido introducido. Sin embargo, tuvo que transcurrir un periodo aproximadamente de 40 años para que la concepción física del memristor se llevara a cabo por los laboratorios HP en el 2008. Hoy en día, este dispositivo emergente ha sido empleado en nuevas aplicaciones; las cuales abarcan desde el desarrollo de memorias modernas hasta circuitos analógicos en combinación con elementos convencionales para obtener funcionalidades novedosas. Lo anterior ha provocado la necesidad de modelos apropiados del memristor para llevar a cabo simulaciones de circuitos con el propósito de ayudar en el flujo de diseño de circuitos y sistemas memristivos. La presente tesis introduce una novedosa metodología de modelado para generar expresiones semi-simbólicas del memristor en forma de modelos orientados a la simulación de circuitos en los dominios de DC y tiempo. Estos modelos son expresados mediante relaciones de rama voltaje-corriente; es decir, modelos funcionales del memristor. Además, una atención especial es dedicada durante el proceso de generación para verificar que las principales señas de identidad del memristor sean cumplidas; lo cual significa que los modelos propuestos poseen las propiedades para ser considerados verdaderos memristores. Los modelos han sido caracterizados detalladamente con respecto a varios parámetros del dispositivo - asumiendo los valores del laboratorio de HP. En el último paso de la metodología, los modelos son establecidos mediante bloques funcionales; los cuales se pueden utilizar por las herramientas industriales de simulación de circuitos integrados, tales como SPICE. Los modelos del memristor han sido probados mediante una serie de circuitos con resultados satisfactorios.
Abstract

Since the seminal paper of Prof. Chua in the early 70’s when the concept of the memristor was introduced, a period of nearly 40 years has passed in order to have a real memristor device in 2008 at the HP Labs. Nowadays, this emerging device has been already used in novel applications that span from the development of modern memories to analog circuit applications in combination with traditional electronics to obtain novel functionalities. As a direct consequence, especially suited models for the memristor are needed that can be used in circuit simulation applications to help the design flow of memristive circuits and systems. This work introduces a novel modeling methodology in order to generate semi-symbolical expressions in the form of circuit simulation-oriented memristor models in the DC and time domains. The generated models are expressed in the form of an $i$-$v$ constitutive branch relationship, i.e. a functional memristor model. Special attention during the generation process has been devoted to verify that the fingerprints of the memristor are fulfilled, which means that the proposed models posses the main properties stipulated for a device to be considered a memristor. The models have been thoroughly characterized versus several parameters of the device - assuming the HP Lab values. In the last step of the methodology, the models are recast in functional blocks that can be used within industrial IC simulation frameworks such as SPICE. The generated memristor models have been tested in a series of bench-mark circuits with excellent results.
# Contents

Resumen ii  
Abstract iv  

1 Introduction 3  
1.1 Original concept . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 3  
1.2 Finding the missing memristor . . . . . . . . . . . . . . . . . . . . . . . . 6  
1.3 Fingerprints of the memristor . . . . . . . . . . . . . . . . . . . . . . . . . 9  
1.4 Other mem-elements . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 14  
1.4.1 Memcapacitor . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 15  
1.4.2 Meminductor . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 15  
1.4.3 Memcapacitive and meminductive systems . . . . . . . . . . . . . . 17  
1.5 Motivation . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 19  
1.6 Objective of the thesis . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 20  

2 State of the art of memristor models 27  
2.1 Why is modeling necessary? . . . . . . . . . . . . . . . . . . . . . . . . . . 27  
2.1.1 The memristor needs to be modeled . . . . . . . . . . . . . . . . . . . 28  
2.2 Analysis domain . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 28  
2.2.1 DC-model . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 28  
2.2.2 Transient-model . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 29  
2.2.3 Frequency-model . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 30  
2.3 Hierarchy of design . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 30  
2.3.1 Physical model . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 30  
2.3.2 Circuital model . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 31  
2.3.3 Behavioral model . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 32  
2.4 Discussion . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 32
3 Development of DC memristor models
  3.1 DC memristor model ............................................. 41
    3.1.1 PWL approximation ........................................ 41
    3.1.2 Voltage-controlled memristive system ..................... 43
    3.1.3 Current-controlled memristive system ..................... 45
    3.1.4 Variations of the PWL parameters ......................... 47
  3.2 Generation of the $v-i$ branch relationship .................. 49
  3.3 A glimpse to DC analysis of memristive circuits ............... 52
  3.4 Cases of study ................................................. 54
    3.4.1 A single-memristor circuit .............................. 54
    3.4.2 A two-memristor circuit ................................. 57

4 Transient memristor model ........................................ 63
  4.1 Polynomial-based model ....................................... 63
    4.1.1 Mathematical description ................................ 63
    4.1.2 Characteristic of the memristor model ................... 65
  4.2 Homotopy-based model ......................................... 66
    4.2.1 Homotopy perturbation method ............................ 66
    4.2.2 Memristor model using HPM .............................. 68
    4.2.3 Numerical analysis ....................................... 68
    4.2.4 Symbolical analysis ...................................... 71
    4.2.5 Parameter variation ...................................... 76
    4.2.6 Characteristic of the memristor model ................... 82
  4.3 Discussion ...................................................... 83

5 Circuit applications .............................................. 87
  5.1 Nullor-based examples ........................................ 87
    5.1.1 Trans-memresistance amplifier ............................ 92
    5.1.2 Trans-memconductance amplifier .......................... 108
  5.2 Opamp-based examples ......................................... 124
    5.2.1 Memristor-based inverter amplifier ....................... 124
    5.2.2 Memristor-based noninverter amplifier .................... 136
    5.2.3 Conclusions .............................................. 143
  5.3 Mem-elements emulator circuits ................................ 145
    5.3.1 Memcapacitor and meminductor grounded .................. 145
    5.3.2 Mutator using current conveyor and OTA .................. 148
    5.3.3 Emulator using single-output current conveyor .......... 150
5.3.4 Meminductor emulator ........................................... 152

6 Conclusions ......................................................... 157

A Nonlinear boundary of HP memristor ............................. 159

B Transient memristor model ......................................... 161
List of Figures

1.1 The four fundamental two-terminal electric elements . . . . . . . . . . . . . 4
1.2 The general structure of HP memristor . . . . . . . . . . . . . . . . . . . . 6
1.3 $V-J$ characteristic curve of the unipolar switching . . . . . . . . . . . . . 7
1.4 The positive instantaneous power areas . . . . . . . . . . . . . . . . . . . . 10
1.5 Lissajous figures . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 10
1.6 Memristor fingerprint: Pinched hysteresis loop . . . . . . . . . . . . . . . . 11
1.7 Memristor fingerprint: Hysteresis lobe area . . . . . . . . . . . . . . . . . . 12
1.8 Frequency response of Lissajous figures . . . . . . . . . . . . . . . . . . . . 12
1.9 Memristor fingerprint: Shrunken hysteresis loop . . . . . . . . . . . . . . . 13
1.10 Circuit elements with memory and conventional elements . . . . . . . . . . 14
1.11 Characteristic curves of the memcapacitive system . . . . . . . . . . . . . . 18

3.1 PWL representation of the memristive system . . . . . . . . . . . . . . . . . 42
3.2 PWL functions for the voltage-controlled memristive system . . . . . . . . . 43
3.3 Circuit with voltage-controlled memristive system . . . . . . . . . . . . . . . 44
3.4 DC-responses of the voltage-controlled memristive systems . . . . . . . . . 44
3.5 PWL functions for the current-controlled memristive system . . . . . . . . . 45
3.6 Circuit with current-controlled memristive system . . . . . . . . . . . . . . . 46
3.7 DC-responses of the current-controlled memristive systems . . . . . . . . . 46
3.8 Scheme of variations for memristive slopes . . . . . . . . . . . . . . . . . . . 47
3.9 Simulation results using the variations of $M_1$ coefficient . . . . . . . . . . 48
3.10 Simulation results using the variations of $M_2$ coefficient . . . . . . . . . . 48
3.11 Scheme of variations for hyperplane position . . . . . . . . . . . . . . . . . 49
3.12 Simulation results using the variations of the hyperplane $V_T$ . . . . . . . 49
3.13 Methodology for DC analysis of memristors . . . . . . . . . . . . . . . . . . 50
3.14 DC memristive circuit . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 54
3.15 DC-response of different memristor characteristics . . . . . . . . . . . . . . 55
3.16 DC two-memristor circuit . . . . . . . . . . . . . . . . . . . . . . . . . . . 57
<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.17</td>
<td>DC-response of the $M_1$ and $M_2$ memristors</td>
<td>57</td>
</tr>
<tr>
<td>4.1</td>
<td>Hysteresis loops of the memristor model</td>
<td>65</td>
</tr>
<tr>
<td>4.2</td>
<td>Memristance of the memristor model</td>
<td>65</td>
</tr>
<tr>
<td>4.3</td>
<td>General procedure of the approximate solution using HPM</td>
<td>67</td>
</tr>
<tr>
<td>4.4</td>
<td>RMSE using different homotopy orders</td>
<td>69</td>
</tr>
<tr>
<td>4.5</td>
<td>HPM and RK4 curves of the solution $x(t)$ using the homotopy order 6.</td>
<td>70</td>
</tr>
<tr>
<td>4.6</td>
<td>RMSE using different frequency values. The HPM order is 6.</td>
<td>70</td>
</tr>
<tr>
<td>4.7</td>
<td>Symbolical state variable $x(t)$ using different $\omega$ values</td>
<td>74</td>
</tr>
<tr>
<td>4.8</td>
<td>Symbolical memristance $M$ using different $\omega$ values</td>
<td>75</td>
</tr>
<tr>
<td>4.9</td>
<td>Analysis of $x(t)$ using different values of current amplitude.</td>
<td>77</td>
</tr>
<tr>
<td>4.10</td>
<td>$M$-$i$ and $v$-$i$ characteristic using not possible value of parameter $A$.</td>
<td>78</td>
</tr>
<tr>
<td>4.11</td>
<td>Analysis of window function coefficient using different values.</td>
<td>79</td>
</tr>
<tr>
<td>4.12</td>
<td>RMSE using different window function coefficient values</td>
<td>80</td>
</tr>
<tr>
<td>4.13</td>
<td>$M$-$i$ and $v$-$i$ characteristic curves using different values of parameter $a$.</td>
<td>80</td>
</tr>
<tr>
<td>4.14</td>
<td>Hysteresis loops of the memristor model</td>
<td>82</td>
</tr>
<tr>
<td>4.15</td>
<td>Memristance of the memristor model</td>
<td>82</td>
</tr>
<tr>
<td>5.1</td>
<td>The nullor</td>
<td>87</td>
</tr>
<tr>
<td>5.2</td>
<td>The asymptotic-gain model</td>
<td>88</td>
</tr>
<tr>
<td>5.3</td>
<td>Negative-feedback amplifiers</td>
<td>89</td>
</tr>
<tr>
<td>5.4</td>
<td>Negative-feedback trans-mem amplifiers</td>
<td>90</td>
</tr>
<tr>
<td>5.5</td>
<td>Nullor synthesis by MOS-equivalent</td>
<td>91</td>
</tr>
<tr>
<td>5.6</td>
<td>Nullor synthesis by Memistor realization</td>
<td>91</td>
</tr>
<tr>
<td>5.7</td>
<td>Trans-memresistance amplifier with nullor</td>
<td>92</td>
</tr>
<tr>
<td>5.8</td>
<td>$u_o(t)$ curves for the trans-memresistance amplifier with nullor using polynomial memristor model</td>
<td>93</td>
</tr>
<tr>
<td>5.9</td>
<td>Transmem-resistance $i_r$-$u_o$ hysteresis with nullor using polynomial memristor model</td>
<td>93</td>
</tr>
<tr>
<td>5.10</td>
<td>$u_o(t)$ curves for the trans-memresistance amplifier with nullor using HPM memristor model</td>
<td>94</td>
</tr>
<tr>
<td>5.11</td>
<td>Transmem-resistance $i_r$-$u_o$ hysteresis with HPM memristor model</td>
<td>95</td>
</tr>
<tr>
<td>5.12</td>
<td>Trans-memresistance amplifier with MOS-equivalent</td>
<td>96</td>
</tr>
<tr>
<td>5.13</td>
<td>$u_o(t)$ curves for the trans-memresistance amplifier with MOS-equivalent using polynomial memristor model</td>
<td>96</td>
</tr>
<tr>
<td>5.14</td>
<td>Transmem-resistance $i_r$-$u_o$ hysteresis with MOS-equivalent using polynomial memristor model</td>
<td>97</td>
</tr>
<tr>
<td>Figure</td>
<td>Description</td>
<td></td>
</tr>
<tr>
<td>--------</td>
<td>-------------</td>
<td></td>
</tr>
<tr>
<td>5.15</td>
<td>Transmission curves for Analysis I.</td>
<td></td>
</tr>
<tr>
<td>5.16</td>
<td>Transmission curves for Analysis II.</td>
<td></td>
</tr>
<tr>
<td>5.17</td>
<td>$u_o(t)$ curves for the trans-memresistance amplifier with MOS-equivalent using HPM memristor model.</td>
<td></td>
</tr>
<tr>
<td>5.18</td>
<td>Transmem-resistance $i_t$-$u_o$ hysteresis with MOS-equivalent using HPM memristor model.</td>
<td></td>
</tr>
<tr>
<td>5.19</td>
<td>Transmission curves for Analysis I.</td>
<td></td>
</tr>
<tr>
<td>5.20</td>
<td>Transmission curves for Analysis II.</td>
<td></td>
</tr>
<tr>
<td>5.21</td>
<td>Transmemresistance amplifier with Memistor realization.</td>
<td></td>
</tr>
<tr>
<td>5.22</td>
<td>$u_o(t)$ curves for the trans-memresistance amplifier with Memistor realization using polynomial memristor model.</td>
<td></td>
</tr>
<tr>
<td>5.23</td>
<td>Transmem-resistance $i_t$-$u_o$ hysteresis (black) and memristor hysteresis (red) for Memistor realization using polynomial memristor model.</td>
<td></td>
</tr>
<tr>
<td>5.24</td>
<td>$u_o(t)$ curves for the trans-memresistance amplifier with Memistor realization using HPM memristor model.</td>
<td></td>
</tr>
<tr>
<td>5.25</td>
<td>Transmem-resistance $i_t$-$u_o$ hysteresis (black) and memristor hysteresis (blue) for Memistor realization using HPM memristor model.</td>
<td></td>
</tr>
<tr>
<td>5.26</td>
<td>Trans-memconductance amplifier with nullor.</td>
<td></td>
</tr>
<tr>
<td>5.27</td>
<td>$i_o(t)$ curves for the trans-memconductance amplifier with nullor using polynomial memristor model.</td>
<td></td>
</tr>
<tr>
<td>5.28</td>
<td>Transmem-conductance $u_t$-$i_o$ hysteresis with nullor using polynomial memristor model.</td>
<td></td>
</tr>
<tr>
<td>5.29</td>
<td>$i_o(t)$ curves for the trans-memconductance amplifier with nullor using HPM memristor model.</td>
<td></td>
</tr>
<tr>
<td>5.30</td>
<td>Transmem-conductance $u_t$-$i_o$ hysteresis with nullor using HPM memristor model.</td>
<td></td>
</tr>
<tr>
<td>5.31</td>
<td>Trans-memconductance amplifier with MOS-equivalent.</td>
<td></td>
</tr>
<tr>
<td>5.32</td>
<td>$i_o(t)$ curves for the trans-memconductance amplifier with MOS-equivalent using polynomial memristor model.</td>
<td></td>
</tr>
<tr>
<td>5.33</td>
<td>Transmem-conductance $u_t$-$i_o$ hysteresis with MOS-equivalent using polynomial memristor model.</td>
<td></td>
</tr>
<tr>
<td>5.34</td>
<td>Transmission curves for Analysis I.</td>
<td></td>
</tr>
<tr>
<td>5.35</td>
<td>Transmission curves for Analysis II.</td>
<td></td>
</tr>
<tr>
<td>5.36</td>
<td>$i_o(t)$ curves for the trans-memconductance amplifier with MOS-equivalent using HPM memristor model.</td>
<td></td>
</tr>
</tbody>
</table>
5.37 Transmem-conductance $u_i-i_o$ hysteresis with MOS-equivalent using HPM memristor model ........................................ 116
5.38 Transmission curves for Analysis I. ........................................ 117
5.39 Transmission curves for Analysis II. ........................................ 118
5.40 Trans-memconductance amplifier with Memistor realization .......... 119
5.41 $i_o(t)$ curves for the trans-memconductance amplifier with Memistor realization using polynomial memristor model .......... 119
5.42 Transmem-conductance $u_i-i_o$ hysteresis (black) and memristor hysteresis (red) for Memistor realization using polynomial memristor model ......... 120
5.43 $i_o(t)$ curves for the trans-memconductance amplifier with Memistor realization using HPM memristor model ............................ 121
5.44 Transmem-conductance $u_i-i_o$ hysteresis (black) and memristor hysteresis (blue) for Memistor realization using HPM memristor model .......... 121
5.45 Memristor-based inverter amplifier ........................................ 124
5.46 $t-A_v$ characteristic curves using different memristor models ............ 125
5.47 Transmission characteristic curves using different memristor models .... 126
5.48 HSPICE and AnalogInsydes simulation results ............................ 126
5.49 Memristor-based inverter amplifier ........................................ 127
5.50 $t-A_v$ characteristic curves using different memristor models ............ 127
5.51 Transmission characteristic curves using different memristor models .... 128
5.52 HSPICE and AnalogInsydes simulation results ............................ 128
5.53 Gain-THD curves using the HPM memristor model ........................ 131
5.54 Gain-THD curves using the polynomial memristor model .................. 132
5.55 Memristor-based inverter amplifier ........................................ 133
5.56 $t-A_v$ characteristic curves using different memristor models ............ 134
5.57 Transmission characteristic curves using different memristor models .... 134
5.58 HSPICE and AnalogInsydes simulation results ............................ 135
5.59 Memristor-based noninverter amplifier ..................................... 136
5.60 $t-A_v$ characteristic curves using different memristor models ............ 136
5.61 Transmission characteristic curves using different memristor models .... 137
5.62 HSPICE and AnalogInsydes simulation results ............................ 137
5.63 Memristor-based noninverter amplifier ..................................... 138
5.64 $t-A_v$ characteristic curves using different memristor models ............ 138
5.65 Transmission characteristic curves using different memristor models .... 139
5.66 HSPICE and AnalogInsydes simulation results ............................ 139
5.67 Gain-THD curves using the HPM memristor model ........................ 140
5.68 Gain-THD curves using the polynomial memristor model ............... 141
5.69 Memristor-based noninverter amplifier ........................................... 142
5.70 $t-A_v$ characteristic curves using different memristor models ............. 142
5.71 Transmission characteristic curves using different memristor models .... 143
5.72 HSPICE and AnalogInsydes simulation results ................................. 143
5.73 Memcapacitor and meminductor emulators ....................................... 145
5.74 $V_{in}$ and $V_{out}$ curves for the memcapacitor emulator ....................... 146
5.75 $V_{in}$ and $V_{out}$ curves for the meminductor emulator ....................... 146
5.76 The capacitance $C(t)$ using different memristor models ..................... 147
5.77 The inductance $L(t)$ using different memristor models ...................... 147
5.78 Mutator $M_R$ to $M_C$ using CCII+ and OTA .................................. 148
5.79 $q$ and $I_{Mc}$ curves for the memcapacitor using polynomial memristor model 148
5.80 $V_{in}$-Capacitance characteristic curves using polynomial memristor model 149
5.81 $q$ and $I_{Mc}$ curves for the memcapacitor using HPM memristor model .... 149
5.82 $V_{in}$-Capacitance characteristic curves using HPM memristor model .... 149
5.83 Floating memcapacitor ................................................................. 150
5.84 Memcapacitor characteristic-curves using polynomial memristor model ... 150
5.85 Memcapacitor characteristic-curves using HPM memristor model ........... 151
5.86 Floating meminductor ................................................................. 152
5.87 Meminductor characteristic-curves using polynomial memristor model .... 152
5.88 Meminductor characteristic-curves using HPM memristor model .......... 153
A.1 The HP memristor structure using nonlinear boundary ......................... 159
Chapter 1

Introduction

The idea of the memristor, the missing circuit element that relates the electrical variables of charge and flux, has represented a revolution in electronics and a key piece of the grandest technology challenges: mimicking the functions of the brain. The history of the memristor has two remarkable milestones [1, 2]: the first one [1] in 1971 when Professor L. O. Chua introduced the mathematical existence of the device as the fourth basic electric circuit element, and the second one [2] in 2008 when researches of HP Labs were able to fabricate the memristor, i.e. the memristor as a real device. This introductory chapter presents, firstly, an overview of the fundamental concepts introduced by Chua with special emphasis in pointing out the main properties of the memristor. Naturally, attention is also devoted to the discovery of the device and to the open possibilities for electronic design incorporating the memristor. In addition, the most important fingerprints of the device are addressed and discussed. Furthermore, the expansion of the original concept of the memristor to circuit elements with memory is presented in order to define the new family of memory passive elements. Hereafter, the motivation for tackling the problem of memristor modeling is justified and the global objectives of this thesis are introduced.

1.1 Original concept

At the end of 1971, Chua [1] introduced a new two-terminal circuit element that closed the loop around the four main electrical variables of Circuit Theory, namely, electric charge $q$, voltage $v$, current $i$, and flux linkage $\varphi$. This new fundamental circuit element was called memristor (a contraction for memory resistor) because it behaves as a resistor with memory. The memristor constituted the missing electric element that established a direct branch relationship between the electric charge and the flux linkage. Figure 1.1 shows the concept explained above.
Chapter 1. Introduction

Figure 1.1: The four fundamental two-terminal electric elements

In the Figure 1.1, the crossed lines denote the time-dependent derivative of charge and flux, the so-called charge-conservation and flux-conservation laws, which are expressed as:

\[
\frac{dq(t)}{dt} = i(t) \quad \text{or} \quad q(t) = \int_{-\infty}^{t} i(\tau)d\tau
\]

and

\[
\frac{d\varphi(t)}{dt} = v(t) \quad \text{or} \quad \varphi(t) = \int_{-\infty}^{t} v(\tau)d\tau
\]

respectively.

Chua mathematically predicted that there is a solid-state device, which defines the missing relationship between four basic variables [1]. This relationship establishes that the memristor can be either flux-controlled or charge-controlled:

\[
q(t) = g_M(\varphi) \quad \varphi(t) = f_M(q)
\]

flux-controlled charge-controlled

(1.1)

After differentiating with respect to \( t \), both terms of (1.1), it yields

\[
i(t) \triangleq \frac{dq(t)}{dt} = \frac{dg_M(\varphi)}{d\varphi} \frac{d\varphi}{dt} \quad v(t) \triangleq \frac{d\varphi(t)}{dt} = \frac{df_M(q)}{dq} \frac{dq}{dt}
\]

By applying the chain rule to the expressions above, it is possible to obtain

\[
i(t) = \frac{dg_M(\varphi)}{d\varphi} \frac{d\varphi}{dt} \quad v(t) = \frac{df_M(q)}{dq} \frac{dq}{dt}
\]

Therefore, the current of a flux-controlled memristor and the voltage of a charge-controlled memristor are given by
1.1. Original concept

\[ i(t) = \frac{dg_M(\varphi)}{d\varphi} v(t) \quad \quad v(t) = \frac{df_M(q)}{dq} i(t) \]

The expressions can be defined as

\[ i(t) = W(\varphi)v(t) \quad \quad v(t) = M(q)i(t) \] \hspace{1cm} (1.2)

where \( W(\varphi) \) is called memconductance and \( M(q) \) is called memresistance.

In 1976, Chua and Kang [3] considered the \textbf{memristor} as a particular case of a general class of dynamical systems, called \textbf{memristive systems} and defined by

\[
\begin{align*}
\dot{x} &= f(x, \varsigma, t) \\
y &= g(x, \varsigma, t) \varsigma
\end{align*}
\] \hspace{1cm} (1.3)

where \( x \) represents the state of the system, and the output and input of the system are represented by \( y \) and \( \varsigma \) respectively.

The equation system of (1.3) opens the possibility for two different types of memristive system: voltage and current controlled. The current-controlled and the voltage-controlled memristive systems are represented by

\[
\begin{align*}
\dot{x} &= f(x, i, t) \quad \quad \dot{x} &= f(x, v, t) \\
v &= R(x, i, t)i \quad \quad \quad \quad \ \quad i &= G(x, v, t)v
\end{align*}
\] \hspace{1cm} (1.4)

where \( v \) and \( i \) denote the voltage and current port, respectively.

The original conception of the memristor was demonstrated by building operational laboratory models with the help of active circuits [1]. The M-R Mutator was used to transform the \( v-i \) characteristic curve of the nonlinear resistor into the corresponding \( \varphi-q \) characteristic curve of the memristor. The absence of a physical device was the major drawback for demonstrating the properties and potential applications of memristors.

The first conceptual application of the memristor was introduced by Chua and Tseng [4] in 1974. The dynamical behavior of the real diode under reverse, forward and sinusoidal operating modes was simulated using a circuital model, called memristive diode model. This model was compared with existing models for diodes as: the Two-Capacitor model [5], the Barna-Horelick model [6], the Linvill’s multi-lumped model [7] and the Wang-Branin model [8]. The simulation results indicated that the memristors are useful for modeling devices with charge-storage and conductivity modulation effects.
Chapter 1. Introduction

The memristor also was considered as a new bond graph element [9] in order to simulate mechanical and electrochemical systems with memristors.

The theory of the memristor carried out by Chua had to wait over thirty years until the scale of electronic devices would allow the observation of the memristive behavior.

1.2 Finding the missing memristor

The memristive behavior had been previously reported [10] to the original conception of the memristor. These anomalous behaviors in the $v$-$i$ characteristic curves of micro and nano-scale devices have been observed in different materials and by various types of physical mechanisms [11, 12, 13, 14, 15, 16, 17, 18].

In 2008, HP Labs presented a physical model of a two-terminal electrical device which behaves like a memristor [2, 19]. The HP memristor is a nanometric scale thin film of TiO$_2$ which can be divided by two main regions: the undoped region with high resistance $R_{OFF}$ and the doped region with low resistance $R_{ON}$.

Figure 1.2 shows the general structure of the HP memristor, where $D$ is the total length of the device and $w$ is the length of doped region. In this thesis, the boundary of the two regions of the memristor is considered as an one-dimensional problem; i.e. the boundary is linear. A simple proposal in order to tackled the nonlinear boundary is shown in Appendix A.

The application of an external bias $v(t)$ across the memristor has the effect of displacing the boundary between the two regions. The length of doped region is a charge-dependent function and is responsible for the memristive behavior of the device.

The above explanation has been modeled by the linear dopant drift model. This model is based on the following equation
where $\mu_V$ is the average ion mobility.

Integrating the above expression with respect to $t$, it yields

$$w(t) = \mu_V \frac{R_{ON}}{D} q(t)$$ (1.6)

By inserting the expression 1.6 into the following $v$-$i$ relationship,

$$v(t) = \left( R_{ON} \frac{w(t)}{D} + R_{OFF} \left( 1 - \frac{w(t)}{D} \right) \right) i(t)$$ (1.7)

It is possible to obtain

$$M(q) = R_{OFF} \left( 1 - \frac{\mu_V R_{ON}}{D^2} q(t) \right)$$ (1.8)

where $M(q)$ is the memresistance.

The $q$-dependent term indicates that the HP memristor is a charge-controlled memristor. According to the charge-conservation law, shown in equation 1.1, the HP memristor can also be considered as a current-controlled memristor.

The HP memristor is considered a bipolar switching memristive system because of both voltage polarities are required to switch a device from a low resistance state (ON) to a high resistance state (OFF) and back. However, there is another type of switching memristive system reported in the literature: the unipolar switching memristive systems. The unipolar switching is defined by two voltages: the set (driving OFF$\rightarrow$ON transition) and the reset (driving ON$\rightarrow$OFF transition) voltages, as shown in Figure 1.3.

![V-I characteristic curve of the unipolar switching](image-url)
This resistance switching is considered by some authors [20] to be based on a thermal effect. Physically, a weak conducting filament with a controlled resistance is formed in the electroforming process. During the reset operation, this filament is partially destroyed because of the large amount of heat released, similarly to a traditional house-hold fuse [20]. In the set operation, the filament is reconstructed again. The nanoscale filament formation has been observed experimentally in such material as TiO$_2$ [21] and NiO [22].

In this thesis, the bipolar switching memristive system is resorted in order to carry out the study of the memristive systems.

The physical realization of the memristor by HP Labs opens the possibility for including memristors and memristive systems into ICs. This possibility has the advantage of extending the functionality of the circuits. The conception of a hybrid chip composed of transistors and memristors can improve the performance of circuits without the need for reducing the size of the devices [23].

Among others, memristors are promising devices for a wide range of potential uses [24], such as

**Non-volatile memory** The memristors can retain memory states and data without requiring external biasing. Nonvolatile characteristic, nano-scale geometry and compatibility with CMOS technology are properties of the memristors that increase the density of memory cells and reduce the power dissipation. Besides, the memristors provide new approaches for managing and reducing the power by disabling of CAM (Content Addressable Memory) cell blocks without loss of stored data [25].

**Dynamic load** Recent advances in the development of new devices have allowed the implementation of the memristor as a dynamic load, e.g. the programmable gain amplifier using the memristor as a variable resistor [26]. The memristors fulfill the need of programmable resistors in high-frequency circuits for the purpose of adapting to particular applications or compensating PVT variations. Programmable comparators, Schmitt triggers and Oscillators [27] have also been developed using memristors.

**Neuromorphic* and biological systems** The physical conception of the memristor has created excitement in the community of neuromorphic researchers. The dynamics of the memristor is correlated with the behavior of the chemical synapses in neuromorphic systems [28]. Electronic circuits based on LC and memristors networks have recently been constructed and used to model the adaptive behavior of unicellular organisms [29]. Moreover, the memristor can be used for modeling the electrical properties of the human skin [30].
Crossbar latches The high power consumption of transistors has been a major barrier to miniaturization and development of microprocessors. Solid-state memristors can be combined into devices called Crossbar latches [31], which can replace transistors in future computing systems using a much smaller area.

1.3 Fingerprints of the memristor

The anomalous behavior in the $v$-$i$ characteristic curves of micron and nano-scale devices and the advent of the HP memristor has contributed to a misunderstanding about the interpretation of the general characteristics of the memristor.

The analysis of the results reported as memristive behavior reveals that some devices or systems are not memristors in the sense of the original definition [1] but are memristive systems according to the more general definition [3]. Moreover, there are systems or devices that behave as memristors or memristive systems solely under special conditions.

The concept of fingerprints has been introduced [32, 33, 34] for the purpose of identifying the memristive nature of the systems and therefore to determine the violation of the principle of operation for memristors and memristive systems. The fingerprints can be classified as: DC-domain fingerprints and time-domain fingerprints.

Time-domain fingerprints

The fingerprints in the time-domain that a device or system should exhibit in order to be classified as a memristor, are the following

- Pinched hysteresis loop
- Hysteresis lobe area
- Shrunken hysteresis loop

Pinched hysteresis loop

The pinched hysteresis loop fingerprint implies that the hysteresis loop must pass through the intersection $(0,0)$ of the $v$-$i$ characteristic curve for any possible amplitude $A$ and frequency $\omega$ values of the sinusoidal input-signal. Besides, this signature must be fulfilled for any value of the state variable $x$. This fingerprint is based on three fundamental

*This is a term used to describe VLSI circuits containing analog systems which mimic neurobiological architectures present in the nervous system.
properties of the memristors [3], called: passivity criterion, no energy discharge and double-valued Lissajous figure.

The passivity criterion establishes that the memristors are passive elements when $G(x, v) \geq 0$ for any input voltage $v(t)$ or $R(x, i) \geq 0$ for any input current $i(t)$, for all $t \geq t_0$; i.e. the output ($v$ or $i$) is zero whenever the input ($i$ or $v$) is zero, regardless of the state variable $x$. Therefore, this property is depicted as a zero-crossing in the $v$-$i$ characteristic curve.

The property of no energy discharge implies that because $G(x, v) \geq 0$ (or $R(x, i) \geq 0$) the instantaneous power ($p(t) = v(t)i(t)$) is always positive for memristors, i.e. the $v$-$i$ characteristic curve is located in the first and third quadrant, as shown in Figure 1.4, in order to satisfy the principle of a positive instantaneous power.

![Figure 1.4: The positive instantaneous power areas](image)

The property of double-valued Lissajous figure establishes that, under periodic operation, the memristors always exhibit a $v$-$i$ Lissajous figure whose the current $i$ (or voltage $v$) is at most a double-valued function of $v$ (or $i$).

![Figure 1.5: Lissajous figures](image)
1.3. Fingerprints of the memristor

The Lissajous figure 1.5a corresponds to a memristor because any value of one axis belongs to at most two values of the other axis. Figure 1.5b shows an impossible Lissajous figure for a memristor because the dashed-line intersects more than two points.

The waveform of Figure 1.6 is related to a double-valued function. This type of function implies that the output variable and the state variable show no additional transient phenomena to the input-signal; and therefore ensures that the device is a pure memristor.

\[ i(t) \]
\[ v(t) \]

\[ v(t) \]
\[ M \]

\[ i(t) \]

Figure 1.6: Memristor fingerprint: Pinched hysteresis loop

The memristive systems and the pure memristors can be distinguished by two different types of pinched hysteresis loops, called self-crossing and not self-crossing [35]. These types of crossings are related to the path of the pinched hysteresis loop. The pure memristors generate pinched hysteresis loop of type self-crossing (black arrows in Figure 1.6). The not self-crossing type (red arrows in Figure 1.6) is associated to the memristive systems.

Moreover, the \( v(t)-M \) characteristic curve is depicted in Figure 1.6(right-side). The pinched hysteresis loop causes the \( v(t)-M \) characteristic curve is located in the first and second quadrant.

**Hysteresis lobe area**

The hysteresis lobe area fingerprint implies that the area of the pinched hysteresis lobe decreases monotonically as the frequency \( \omega \) of the input-signal tends to infinity.

Figure 1.7(left-side) shows two hysteresis lobe areas using different frequency values. The solid-line represents the hysteresis lobe area for \( \omega_1 \) and the dashed-line displays the hysteresis lobe area for \( \omega_2 = 10\omega_1 \).
The area of the lobe in the $i$-$v$ characteristic curve is related to the corresponding part of memristive potential in the $q$-$\varphi$ plane. The lobe area of the pinched hysteresis loop has been widely analyzed [36, 37, 38] in order to understand the hysteresis effects in circuits employing memristors. This fingerprint causes that the range of memristance is reduced as the area of the pinched hysteresis lobe decreases monotonically, as shown in Figure 1.7(right-side).

**Shrunken hysteresis loop**

The shrunken hysteresis loop fingerprint implies that the shape of the pinched hysteresis loop tends to a single-valued function as the frequency $\omega$ approaches infinity. This fingerprint is based on one fundamental property of the memristors [3], called: limiting linear characteristic.

---

**Figure 1.7: Memristor fingerprint: Hysteresis lobe area**

**Figure 1.8: Frequency response of Lissajous figures**
1.3. Fingerprints of the memristor

The limiting linear characteristic establishes that the memristors, under periodic operation, degenerate into a linear time-invariant resistor as the excitation frequency increases toward infinity. This property is illustrated in Figure 1.8.

Figure 1.9 shows the pinched and shrunken hysteresis loops. The solid-line represents the pinched hysteresis loop for \( \omega_1 \) and the dashed-line displays the shrunken hysteresis loop for \( \omega_2=\infty \).

\[ \omega_1 \omega_2 \]

\[ i(t) \]

\[ v(t) \]

\[ M \]

\[ v(t) \]

\[ \omega_1 \omega_2 \]

\[ i(t) \]

Figure 1.9: Memristor fingerprint: Shrunken hysteresis loop

The waveforms of Figure 1.9 indicate that as the frequency \( \omega \) of the input-signal increases to infinity, the state variable converges to a constant value and establishes a linear relationship between the input variable and the output variable. Therefore, the effect of the pinched hysteresis loop disappears.

Furthermore, the \( v(t) \)-\( M \) characteristic curve is depicted in Figure 1.9(right-side). The shrunken hysteresis loop causes the \( v(t) \)-\( M \) characteristic curve is shrunken with a fixed value of memristance.

The physical interpretation of this phenomenon [39] is that the system possesses certain inertia and can not respond as rapidly as the fast variation in the excitation waveform and therefore must settle to some equilibrium state. This implies that the hysteresis effect of the memristive system decreases as the frequency increases and hence it eventually degenerates into a purely resistive system.

**DC-domain fingerprint**

The fingerprint in DC-domain is based on the fundamental property of the memristors [3], called: DC characteristic. For dc operation, the \( v-i \) characteristic curves behave as
Chapter 1. Introduction

time-independent no linear resistors; i.e., the derivative of the state variable, shown in (1.3), is used in the time-independent version.

This property implies that the state variable \( x \) is considered not time dependent and causes that the value of the derivative is equal to zero. Then, the output variable depends only on the input variable. Therefore, a value of the input variable gives a value of the output variable.

In DC-domain, the nullor has been considered as equivalent element of the behavior of the memristors [33].

1.4 Other mem-elements

The idea of the memristor has been extended to capacitive and inductive elements, called memcapacitor and meminductor [40]. The coexistence between the passive non-memory elements and the mem-elements is shown in Figure 1.10.

These new circuit elements with memory show pinched hysteresis loops in the two constitutive variables that define them: charge-voltage for the memcapacitor, and current-flux for the meminductor. Hereafter, the concepts of memcapacitor and meminductor are developed mathematically for the purpose of determining the relationship between the constitutive variables and comparing with the conventional circuit elements.
1.4. Memcapacitor

The capacitor with memory or memcapacitor is a two-terminals element which constitutive relationship is represented by

\[
\int_{-\infty}^{t} q(\tau) d\tau = \sigma^\dagger = f(\varphi) \tag{1.9}
\]

Differentiating with respect to time \( t \), both terms of (1.9), it yields

\[
q(t) \triangleq \frac{d\sigma}{dt} = \frac{df(\varphi)}{dt}
\]

By applying the \textit{chain rule} to the expression above, it is possible to obtain

\[
q(t) = \frac{df(\varphi)}{d\varphi} \frac{d\varphi}{dt}
\tag{1.10}
\]

The equation (1.10) can be rearranged in two different forms

\[
q(t) = \frac{d\sigma}{d\varphi} \frac{d\varphi}{dt} = \frac{d\varphi}{d\sigma} q(t)
\]

The above expressions can be simplified as

\[
q(t) \triangleq C(\varphi)v(t) \quad v(t) \triangleq D(\sigma)q(t)
\]

where \( C(\varphi) = \frac{d\sigma}{d\varphi} \) and \( D(\sigma) = \frac{d\varphi}{d\sigma} \) are called memcapacitance and memelastance, respectively.

1.4.2 Meminductor

The meminductor or inductor with memory is a two-terminals element which constitutive variables are related by

\[
\int_{-\infty}^{t} \varphi(\tau) d\tau = \rho^\ddagger = f(q) \tag{1.11}
\]

\(^\dagger\)This term has been introduced by Chua \([41]\) in order to assign a symbol to the time-domain integral of charge

\(^\ddagger\)This term has been introduced by Chua \([41]\) in order to assign a symbol to the time-domain integral of flux
After applying some derivative steps with respect to time $t$, both terms of (1.11), it yields

$$\phi(t) \triangleq \frac{d\rho}{dt} = \frac{df(q)}{dt}$$

The chain rule is used into the expression above in order to obtain

$$\phi(t) = \frac{df(q)}{dq} \frac{dq}{dt} = \frac{dq}{d\rho} \phi(t) \tag{1.12}$$

The equation (1.12) is realigned in two different forms

$$\phi(t) = \frac{d\rho}{dq} \frac{dq}{dt} \frac{dq}{d\rho} \phi(t)$$

These expressions are abbreviated as

$$\phi(t) \triangleq L(q)i(t) \quad i(t) \triangleq \Gamma(\rho)\phi(t)$$

where

$$L(q) = \frac{d\rho}{dq} \quad \Gamma(\rho) = \frac{dq}{d\rho}$$

are called meminductance and memreluctance, respectively.

In order to compare the circuit elements with memory, the conventional circuit elements, namely, resistor, capacitor and inductor can be represented by

**Resistor**

$$v(t) = Ri(t) \quad i(t) = Gv(t) \tag{1.13}$$

**Capacitor**

$$q(t) = Cv(t) \quad v(t) = Dq(t) \tag{1.14}$$
1.4. Other mem-elements

Inductor

\[
\varphi(t) = Li(t) \quad i(t) = \Gamma \varphi(t)
\]

current-controlled \quad flux-controlled \quad (1.15)

Table 1.1 resumes the circuit elements: resistor (R), capacitor (C), inductor (I), memristor (\(M_R\)), memcapacitor (\(M_C\)) and meminductor (\(M_I\)) with the respective controlled variable: voltage-controlled, current-controlled, charge-controlled and flux-controlled.

Table 1.1: Duality between conventional and mem-elements

<table>
<thead>
<tr>
<th>conventional elements</th>
<th>mem-elements</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>(v = Ri)</td>
</tr>
<tr>
<td></td>
<td>(voltage-controlled)</td>
</tr>
<tr>
<td>C</td>
<td>(q = Cv)</td>
</tr>
<tr>
<td></td>
<td>(charge-controlled)</td>
</tr>
<tr>
<td>L</td>
<td>(\varphi = Li)</td>
</tr>
<tr>
<td></td>
<td>(flux-controlled)</td>
</tr>
</tbody>
</table>

1.4.3 Memcapacitive and meminductive systems

Similarly that the memristor is considered as a particular case of a general class of dynamical systems, called memristive systems; the memcapacitor and meminductor are particular instances of more extensive dynamical systems, called memcapacitive and meminductive systems.

The general class of \(n\)th-order \(u\)-controlled memory devices [42] can be described by

\[
\dot{x} = f(x, u, t) \quad y(t) = g(x, u, t)u(t) \quad (1.16)
\]

where \(x\) is a vector representing \(n\) internal state variables, \(y(t)\) and \(u(t)\) are output/input variables (i.e., current, charge, voltage, or flux), \(g\) is a generalized response and \(f\) is a continuous \(n\)-dimensional vector function.

Memcapacitive and meminductive systems are particular cases of 1.16, where the constitutive variables are charge and voltage for the memcapacitance and flux and current for the meminductance.

1.4.3.1 Memcapacitive system

The \(n\)th-order memcapacitive system charge and voltage-controlled can be defined by
\begin{equation}
\dot{x} = f(x, q, t) \quad \dot{x} = f(x, V_C, t) \tag{1.17}
\end{equation}

\begin{equation}
V_C(t) = D(x, q, t)q(t) \quad q(t) = C(x, V_C, t)V_C(t)
\end{equation}

where \(D\) and \(C\) are called memelastance and memcapitance, respectively. \(V_C(t)\) and \(q(t)\) are the voltage and the charge on the memcapacitive system at time \(t\).

Figure 1.11: Characteristic curves of the memcapacitive system

Figure 1.11 shows the \(v_C(t)-q(t)\) and \(v_C(t)-C\) characteristic curves of the memcapacitive system. The memcapacitive system behaves as a linear capacitor in the limit of infinite frequency and displays the pinched hysteresis loop in the \(v_C(t)-q(t)\) characteristic curve.

### 1.4.3.2 Meminductive system

The \(n\)th-order meminductive system flux and current-controlled can be defined by

\begin{equation}
\dot{x} = f(x, \varphi, t) \quad \dot{x} = f(x, I_L, t) \tag{1.18}
\end{equation}

\begin{equation}
I_L(t) = \Gamma(x, \varphi, t)\varphi(t) \quad \varphi(t) = L(x, I_L, t)I_L(t)
\end{equation}

where \(\Gamma\) and \(L\) are called memreluctance and meminductance, respectively. \(I_L(t)\) and \(\varphi(t)\) are the current and the flux on the meminductive system at time \(t\).

The meminductive system can be modeled similarly to the memcapacitive system presented above. The meminductive system presents the pinched hysteresis loop in the \(i_L(t)\)-\(\varphi(t)\) characteristic curve and the \(i_L(t)\)-\(L\) characteristic curve tends to a fixed value as the
frequency approaches infinity.

Table 1.2 resumes the systems with memory: memristive system \((M_{RS})\), memcapacitive system \((M_{CS})\) and meminductive system \((M_{LS})\) with the respective controlled variable: voltage-controlled \((VC)\), current-controlled \((CC)\), charge-controlled \((QC)\) and flux-controlled \((FC)\).

<table>
<thead>
<tr>
<th>System</th>
<th>Port equation</th>
<th>State equation</th>
</tr>
</thead>
<tbody>
<tr>
<td>(CCM_{RS})</td>
<td>(v = M(x,i,t)i)</td>
<td>(\dot{x} = f(x,i,t))</td>
</tr>
<tr>
<td>(VCM_{RS})</td>
<td>(i = W(x,v,t)v)</td>
<td>(\dot{x} = f(x,v,t))</td>
</tr>
<tr>
<td>(VCM_{CS})</td>
<td>(q = C(x,v,t)v)</td>
<td>(\dot{x} = f(x,v,t))</td>
</tr>
<tr>
<td>(QCM_{CS})</td>
<td>(v = D(x,q,t)q)</td>
<td>(\dot{x} = f(x,q,t))</td>
</tr>
<tr>
<td>(CCM_{LS})</td>
<td>(\varphi = L(x,i,t)i)</td>
<td>(\dot{x} = f(x,i,t))</td>
</tr>
<tr>
<td>(FCM_{LS})</td>
<td>(i = \Gamma(x,\varphi,t)\varphi)</td>
<td>(\dot{x} = f(x,\varphi,t))</td>
</tr>
</tbody>
</table>

The circuit elements with memory can be used for non-volatile memory and promise to allow simulation of learning, adaptation and spontaneous behavior. These kind of devices are common at nano-scale [43, 44, 45, 46, 47] where the dynamical properties of electrons and ions depend on the history of the system during certain time scales [48].

## 1.5 Motivation

The theoretical conception of the memristor opens the possibility of simulating hybrid circuits, i.e. circuits with conventional and memory elements. The design of hybrid circuits and systems based on conventional and memory elements require rethinking of fundamental circuit analysis, i.e. conventional circuit analysis with modified nodal analysis (MNA) cannot consider mem-elements such as memristor together with the traditional devices. Therefore, the incorporation of the memristor in a simulation scheme represents a major part in order to improve the properties of the new circuit element with the conventional devices.

The physical conception of the memristor by HP Labs has motivated a great interest for modeling the memristive behavior of the device. A lot of work has been done with the purpose of obtaining a SPICE model or macro-model of the memristor [49, 50, 51, 52, 53, 54]. Macro-models or SPICE models have the major drawback of using a large number of nodes or circuit elements to mimic the behavior of the memristor in a particular analysis domain, instead of using a two-terminal model that accomplishes the principal fingerprints of the memristor.
In addition, the system of equations that represents the memristive behavior must be solved by a numerical integration method. This type of numerical method has the major disadvantage of employing a long CPU time to obtain the numerical values at each instant of time.

1.6 Objective of the thesis

The research area of this thesis is focused on modeling the memristor in order to be included in a simulation procedure for circuits with memristors. Therefore, the objective of this thesis is

- Generating memristor models for different domain analysis (DC, time and frequency domain) in order to be included in a simulation procedure for circuits with memristors.
Bibliography


Chapter 2

State of the art of memristor models

The discovery of the physical memristor has caused widespread interest for modeling the memristive behavior in order to include the device in a simulation procedure. The principal goal of the memristive models is showing the eight-shape or the bow tie-shape in the $v$-$i$ characteristic curve. However, the pinched hysteresis loop is not sufficient for validating the memristive model. The behavior of the memristance respect to current, voltage, charge, flux or state variable must be reviewed in order to ensure the reliability of the memristive model. This chapter presents a brief introduction about the need for modeling in the electronic circuit design and introduces different types of memristive models by classifying three principal areas. Firstly, the analysis-domain classification is presented. In addition, the hierarchy of design is used as classification of the memristor models. Furthermore, the memristor models are organized based on the mathematical expressions. Hereafter, the advantages and disadvantages of the memristive models are discussed with the purpose of obtaining the necessary features for modeling these kind of devices.

2.1 Why is modeling necessary?

Modeling is a major step in the electronic circuit design. The principal purpose consists of generating equivalent approximations that allow to carry out the simulation tasks of analysis and synthesis. The process of conceiving and selecting suitable models is a problem of central importance in the design and simulation of electronic circuits [1]. Besides, the assignment of proper numerical values to the model parameters are keys to the successful computer-aided analysis of a circuit [1].

The adequacy of the models in the simulation tasks involves three principal commitments [2]: agreement between the simulation results and the actual performance of the physically implemented circuit, compromise between computational complexity and in-
Chapter 2. State of the art of memristor models

herent inaccuracy; and choosing which physically phenomena should be incorporated in the model and which are to be neglected.

2.1.1 The memristor needs to be modeled

The design of hybrid circuits and systems based on conventional elements and memristors is not possible without the generation of models for memristors. The modeling of the new fundamental circuit element allow to carry out the simulation of novel electronic circuits that contain memory elements and traditional devices.

2.2 Analysis domain

The electrical circuits are broken down in three different analysis domains [2, 1, 3]: DC, transient and frequency. DC-analysis is based on the response of the circuit for time-invariant excitation sources and is referred to the determination of operating points. The time-variable responses established in circuits under periodic operation of excitation sources are treated in the transient-analysis. The transfer characteristics of electrical circuits, e.g. amplitude, phase and delay, as functions of frequency are examined in the frequency-analysis.

2.2.1 DC-model

DC-analysis is the starting point for circuit simulators. The fundamental problem consists of finding DC operating points, which are used as initial states in other types of analysis.

The behavior of the memristor in the DC-domain has been poorly studied in the literature. In [4], the DC-model of the memristor is developed by considering current contributions arising from different conduction mechanisms. The proposed circuit model is obtained by fitting the filament-assisted tunneling currents from different regions of the \( v-i \) characteristic curve of the memristor. The parametric representation of the currents is performed by polynomial functions which depend on the voltage applied to the device.

In [5], the DC-model of the memristor is based on movement of the dopant boundary \( w \). The memristor is considered a constant resistance which tends either \( R_{ON} \) or \( R_{OFF} \) in a time required, called resistance saturation time. The time required for resistance saturation depends on the sign and the value of the voltage in the device.

In [6], the DC-response of the memristor is represented by the waveform of the current, the time after which the current reaches the equilibrium value and the decaying
curve as time increases. The behavior of the memristor in DC-regime is related to the decomposition of the hysteresis characteristic curve as the frequency tends to decrease.

The fundamental properties of the memristive systems [7] establish that under DC-operation the memristive systems are equivalent to nonlinear resistors. However, this property has not been tackled in the literature.

2.2.2 Transient-model

The transient-domain is the most widely used to model the behavior of the memristor. In this domain, the three most important features of the memristive systems can be displayed: the pinched hysteresis loop in the $i$-$v$ characteristic curve, the behavior of the memristance and the waveform of the state variable.

In [8], the memristor is based on a single internal state variable. The rate of system resistance change (R changes between two limiting values) is characterized by a PWL function with two segments and one hyperplane. Besides, the piece-wise linear approximation has been used for establishing the $q$-$\varphi$ relationship [9, 10], the state variable of memristive devices [8] and the pinched hysteresis loop in the $v$-$i$ characteristic curve of the memristor [11]. The numerical calculations of this kind of models are performed using a numerical integration method in order to show the characteristic curves of the memristor.

In [12], the memristor is based on the movement of the boundary between two regions with different dopant concentration. This model is called linear drift model. The linear drift velocity of the memristor is described by a normalized state variable. The state variable is proportional to the charge that passes through the device. However, this model is not bounded to the physical limits of the device and the nonlinear behavior of the transport mechanism is not incorporated. Therefore, the linear drift model has been extended to the nonlinear drift model. The system of equations for the nonlinear model is similar to the linear model except by the adding of a term to the state equation, called window function [12, 13, 14, 15]. This function bounds the normalized state variable within zero and unity, i.e. the velocity changes based on the position of the boundary. The concept of the window function has been carried out with propose of incorporating the nonlinear behavior into the state variable equation.

In [16, 17, 18], the memristor has been modeled using emulators or SPICE models. These models are composed of individual elements which together can display the principal characteristics of the memristors. Moreover, the incorporation of new elements in these kind of models contributes to represent additional phenomena in the device.

The principal properties [19, 7] and fingerprints [20, 21, 22, 23] of the memristors have been established in the time-domain in order to ensure the reliability of the models.
2.2.3 Frequency-model

The modeling of the memristor in the frequency-domain is closely related to the behavior of the memristor in the time-domain, e.g. the collapse of the pinched hysteresis loop is observed in the time-domain despite of being an effect caused by the variation of the frequency. This correlation of analysis domain has led to low interest for making memristor models in the frequency-domain.

In [24], the memristor is considered a device that generates passive second and higher harmonics signals. This feature is incorporated into the memristor model for harmonic generation in combination with active circuits.

In [25], the memristor is represented by the Fourier response of the current in the device. The Fourier series of the memristor current contains sine-type components and no DC component. These characteristics are related with the pinched hysteresis loop and the odd-symmetry of the memristor.

In [26], the discrete Fourier transform is used to explain the properties of the memristor current in terms of time evolution of the width and the memconductance in the device. The Fourier analysis shows that the shape of the hysteresis curve is related to the weights of the harmonics.

2.3 Hierarchy of design

The automated design of analog systems has been structured over three principal levels of hierarchy [27]: behavioral, circuital and physical. Behavioral-level is used to represent the general idea of the system. The generation of architectures composed of circuit elements in order to mimic the behavior of the system is treated in the circuital-level. Physical-level is related to the behavior of real devices.

2.3.1 Physical model

The physical models reflect the physical phenomena taking place into memristor devices [28, 29, 30]. The goal of this kind of models is to obtain physical insight into the transport process responsible for memristive behavior. These models are validated with the experimental data from real devices.

In [29], the memristor model is based on numerical solutions of coupled drift-diffusion equations for electrons and ions with appropriate boundary conditions. The dynamics of the memristive device is simulated by a semiconductor thin film with mobile dopants that are partially compensated using a small amount of immobile acceptors. This model
2.3. Hierarchy of design

presents different conclusions about the behavior of a thin film semiconductor memristive device. First, the ON and nearby low-resistance states have ohmic $v$-$i$ characteristics, but as the zero-bias resistance of the device increases toward the OFF state, the $v$-$i$ curves become increasingly nonlinear because of the npn potential barrier that develops in the semiconductor. Second, for the same magnitude but opposite polarity of applied voltage, the speed of switching ON will be significantly faster than switching OFF. This is related to the electric field and the dopant concentration gradients. Finally, it is possible to invert the switching polarity of a device; for example, applying an ON-switching voltage for a long enough time will eventually cause ions from the grounded side of the device to drift toward the center of the film, thus turning the device OFF.

In [28], the behavior of the memristor device is modeled from classical macroscopic viewpoint, which is represented by the electron density distribution inside the device. The memristor model is based on classic ion transportation theory and composed of three regions, namely, the conductive region, the transition region and the insulating region. The conductive region corresponds to the region of filaments while the transition region connects the filaments and the remaining insulating region. The formation or dissolution of the filament is simulated as the ion surface motion within the transition region. The parameters $w$, $\lambda$ and $D$ are used in order to denote the lengths of the conductive region, the transition region, and the entire device, respectively.

In [30], a general model is proposed in order to explain the memristive switching behavior of nanodevices. This model suggests that the switching involves changes in the electronic barrier at the Pt/TiO$_2$ interface induced by drift of oxygen vacancies under an applied electric field. When vacancies drift towards the interface, they create conducting channels that short-circuit the electronic barrier. When vacancies drift away from the interface they eliminate these channels, restoring the original electronic barrier. This model fits the experimentally measured $I$-$V$ characteristic curve of the memristor using an equation comprising of two terms. The first term is used to approximate the ON-state behavior of the memristor due to the electron tunneling. The second term represents the approximation of the OFF-state behavior of the memristor similar to a P-N junction.

2.3.2 Circuital model

The circuital models allow the optimization of the memristive behavior of the devices by adjusting circuit elements and bias conditions [31]. These type of models are used for building macro-models or SPICE models. The macro and SPICE models have been widely used in order to mimic the memristive behavior of the device built by HP Labs.

On one hand, the SPICE memristor models have been developed for different appli-
cations, such as: chaos and oscillation [32, 33], arithmetic and logic [33, 34, 35, 36, 37], amplifier [38, 39] and filter [40]; and different areas of knowledge, such as: neuromorphic systems [41], biological systems [42] and electronics [42]. On the other hand, the SPICE memristor models have been implemented with three [43], four [44, 45, 46], five [47, 48], six [46], eight [49] and ten [50] internal nodes using passive elements and eight [46] internal nodes using active elements.

2.3.3 Behavioral model

The behavioral models provide an overview of the expected memristive characteristic [51]. The classical procedure in order to build behavioral models consist of using mathematical expressions to represent the general behavior of the device.

In [12], the behavior of the memristor has been modeled using the state variable equation of the boundary between two regions (doped and undoped) of the HP memristor. Moreover, this mathematical expression has been modified by adding one term to the state variable equation, called window function [52].

In [53], the piece-wise linear approximation has been used for modeling the behavior of the memristor in biological applications.

2.4 Discussion

The memristor models classified by analysis domain and hierarchy of design can be located in more than one category. In [54], the memristor model is performed using behavioral approaches and then it is transformed into a SPICE model. In [4], the dc memristor model is based on the behavioral approximation of the \(i-v\) characteristic curve and it is represented by the polynomial function of the current response across the device. In [55], the fundamental concept of memristor is used to develop behavioral models of non-volatile resistance switching memory devices. Therefore, the memristor models have been built to cover different design levels in different analysis domains. However, in the literature there is not memristor model or memristive model that can be used in the three domains of analysis: DC, transient and frequency.

The possible causes of the lack of memristor models using the three domains of analysis include: the principal fingerprints [20, 21, 22, 23] are displayed in the time-domain, the absence of analytical expressions to represent the behavior of the memristor and the misunderstanding of the dc response of the memristor.

The macro and SPICE models have been constantly proposed in order to incorporate
2.4. Discussion

the memristor in a simulation procedure. However, these models present two major drawbacks: the number of nodes employed and the validity of the model by using the pinched hysteresis loop in the \( v-i \) characteristic curve as the unique fingerprint of the device.

In [12], the memristor model is described by using the state variable equation and represents the linear diffusion of dopants through the device. However, this model has no physical boundaries in the frontiers; i.e., the normalized state variable can be increased above the unity, which means that the boundary of the doped region has exceeded the length of the device. The memristor models in [13, 14, 15] solve the problem of the physical boundaries by adding a term to the equation of the state variable, called window function. The window function restricts the diffusion of dopants into the physical limits of the device; i.e., the normalized state variable can not exceed the boundaries of the device. This model provides an adequate approximation of the memristive behavior. However, the principal drawback is the need for a numerical integration method to solve the system of equations.

The memristor model of [30] is considered a closer approach to the real behavior of the memristor device due to the use of mathematical expressions related to physical phenomena present in the device. However, there are many parameters that can be adjusted and do not represent realistic values of the memristive characteristic.

The PWL memristor models [8, 9, 10, 11] are used to represent the rate of memristance, state variable and resistance change. These models are useful to represent switching mechanism because of the piece-wise linear representation is composed of slopes and hyperplanes. However, the necessity of numerical integration methods and the inability to include nonlinear effects represent two principal disadvantages of these models.
Bibliography


Bibliography


Chapter 3

Development of DC memristor models

In DC-domain, the calculation of the operating points has been regarded as the most important simulation stage because it represents the starting point for other types of analysis. The incorporation of the memristor opens the possibility of studying the influence of the memristive behavior in the operating points of circuits with memristors. This chapter presents, firstly, a simple model of the memristor based on the piece-wise linear (PWL) approximation. In addition, the influence of the parameters of the PWL approximation in the $v$-$i$ characteristic curve is studied. Furthermore, the methodology for obtaining the $v$-$i$ characteristic is explained. Hereafter, the existence of multiple operation points is treated by two cases of study.

3.1 DC memristor model

In this section, a DC model is developed from the original dynamic formulation of a memristive system.

3.1.1 PWL approximation

The memristive systems are represented by

$$\begin{align*}
\dot{x} &= f(x, i) \\
v &= R(x, i)i \\
i &= G(x, v)v \\
\end{align*}$$

(3.1)

The PWL approximation can be used to establish the branch-characteristic of the
memristive elements. The general representation of the memristive system using the first and the third quadrant is depicted in Figure 3.1.

![Figure 3.1: PWL representation of the memristive system](image)

This representation is composed of the slopes $M_1$, $M_2$, $M_3$ and the break points $V_{T_1}$, $V_{T_2}$. Additionally, the blue dashed-line is incorporated into the PWL representation to complete a possible path between the first and third quadrant and therefore establish a pinched hysteresis loop.

According to the literature, this representation can be carried out using the general explicit piece-wise linear function of Chua and Kang [1]. The formal definition of this canonical PWL function is expressed as [1]:

$$f(x) = a_0 + a_1 x + \sum_{j=1}^{n} \{b_j |x - x_j| + c_j \text{sgn}(x - x_j)\}$$

(3.2)

The characteristic of the blue dashed-line in Figure 3.1 may cause, under certain conditions, problems with the canonical PWL function of (3.2). In order to overcome that problem, the decomposed formulation based on the hyperplane unbending has been proposed [2].

In this part of the thesis, the particular explicit piece-wise linear function of Chua and Kang [3] has been resorted in order to represent the memristive behavior. Furthermore, the analysis is focused to the first quadrant of the PWL representation in Figure 3.1. However, the proposed methodology can be applied to the third quadrant.

The formal definition of the particular PWL function is expressed as [4]:
3.1. DC memristor model

\[ f(x) = a + Bx + \sum_{i=1}^{\sigma} c_i |(\alpha_i, x) - \beta_i| \]  \hspace{1cm} (3.3)

This function is capable of modeling the change of slopes and the break point which are essential conditions for carrying out the memristive effect.

3.1.2 Voltage-controlled memristive system

The voltage-controlled memristive systems can be divided in two different cases: memristive state and memconductive state. These cases are described by

\[
\begin{align*}
\dot{x} &= f(V_M) \\
I_M &= \frac{V_M}{x(V_M)} \\
& \text{memristive-state} \\
\dot{x} &= f(V_M) \\
I_M &= x(V_M)V_M \\
& \text{memconductive-state}
\end{align*}
\]  \hspace{1cm} (3.4)

where the state variable \(\dot{x}\) is established as the function that governs the change in memristive or memconductive value of the system and \(V_M\) denotes the voltage across the memristive system.

The state equations are defined by the canonical formulation of (3.3), compounded of two lineal-segments and one hyperplane, as shown in Figure 3.2.

Figure 3.2: PWL functions for the voltage-controlled memristive system

The state equations are expressed as

\[
\begin{align*}
\dot{x} &= a_0 + a_1 V_M + b_1 |V_M - V_T| \\
a_0 &= -\frac{1}{2}(M_2 - M_1)|V_T| \\
a_1 &= M_1 + \frac{1}{2}(M_2 - M_1) \\
b_1 &= \frac{1}{2}(M_2 - M_1) \\
& \text{memristive-state} \\
\dot{x} &= a_0 + a_1 V_M + b_1 |V_M - V_T| \\
a_0 &= -\frac{1}{2}(W_2 - W_1)|V_T| \\
a_1 &= W_1 + \frac{1}{2}(W_2 - W_1) \\
b_1 &= \frac{1}{2}(W_2 - W_1) \\
& \text{memconductive-state}
\end{align*}
\]  \hspace{1cm} (3.5)
where $M_1$ and $M_2$ are the memristive slopes, $W_1$ and $W_2$ are the memconductive slopes and $V_T$ represents the position of the hyperplane.

The voltage-controlled memristive systems established in (3.4) and (3.5) are used to simulate the circuit shown in Figure 3.3.

\[ \begin{align*}
I_M \\
\text{V} \quad \pm \\
\text{M} \quad \text{+} \\
\text{W} \quad \text{M} \\
\text{W} \quad \text{M} \\
\end{align*} \]

Figure 3.3: Circuit with voltage-controlled memristive system

where $V=2V$. The hyperplane position is $V_T=0.5$ and the values of $M_1$, $M_2$, $W_1$ and $W_2$ are listed in Table 3.1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_1$</td>
<td>0.5 kΩ</td>
</tr>
<tr>
<td>$M_2$</td>
<td>1 kΩ</td>
</tr>
<tr>
<td>$W_1$</td>
<td>2 m℧</td>
</tr>
<tr>
<td>$W_2$</td>
<td>1 m℧</td>
</tr>
</tbody>
</table>

Table 3.1: Parameter values

The values of the parameters $M_1$, $M_2$, $W_1$ and $W_2$ have been established to fulfill the PWL function for the voltage-controlled memristive system, as shown in Figure 3.2. In the case of memristive-state, the value of $M_2$ is the double of the $M_1$ value in order to ensure the change of slope in the memristor. For the case of memconductive-state, the value of $W_2$ is the half of $W_1$ value.

\[ \begin{align*}
\text{Current(mA)} \\
\text{Voltage(V)} \\
\end{align*} \]

Figure 3.4: DC-responses of the voltage-controlled memristive systems

Figure 3.4 shows the dc-responses of the voltage-controlled memristive systems. The
3.1. DC memristor model

Simulation results have been obtained by sweeping the power supply $V$ of the electrical circuit shown in Figure 3.3. In each value of voltage, the system of equations of the voltage-controlled memristive system has been resolved using a numerical integration method. On one hand, the dashed-line represents the monotonically increasing curve of the voltage-controlled memristive system using the memconductive-state. On the other hand, the solid-line represents the non-monotonically increasing curve of the voltage-controlled memristive system using the memristive-state.

### 3.1.3 Current-controlled memristive system

In the case of the current-controlled memristive systems, the memristive-state and the memconductive-state are described by

\[
\begin{align*}
\dot{x} &= f(I_M) \\
V_M &= x(I_M)I_M \quad \text{memristive-state} \\
\dot{x} &= f(I_M) \\
V_M &= \frac{I_M}{x(I_M)} \quad \text{memconductive-state}
\end{align*}
\]

where $\dot{x}$ is the state variable and $I_M$ denotes the current across the memristive system.

The state equations are defined by the canonical formulation of (3.3), as shown in Figure 3.5.

![PWL functions for the current-controlled memristive system](image)

The state equations are expressed as

\[
\begin{align*}
\dot{x} &= a_0 + a_1 I_M + b_1 |I_M - I_T| \\
\dot{x} &= a_0 + a_1 I_M + b_1 |I_M - I_T| \\
a_0 &= -\frac{1}{2}(M_2 - M_1)|I_T| \\
a_0 &= -\frac{1}{2}(W_2 - W_1)|I_T| \\
a_1 &= M_1 + \frac{1}{2}(M_2 - M_1) \\
a_1 &= W_1 + \frac{1}{2}(W_2 - W_1) \\
b_1 &= \frac{1}{2}(M_2 - M_1) \\
b_1 &= \frac{1}{2}(W_2 - W_1)
\end{align*}
\]

(3.7)
where $M_1$ and $M_2$ are the memristive slopes, $W_1$ and $W_2$ are the memconductive slopes and $I_T$ represents the position of the hyperplane.

The current-controlled memristive systems established in (3.6) and (3.7) are used to simulate the circuit shown in Figure 3.6.

![Figure 3.6: Circuit with current-controlled memristive system](image)

where $I=2\text{mA}$. The hyperplane position is $I_T=0.5\text{mA}$ and the values of $M_1$, $M_2$, $W_1$ and $W_2$ are listed in Table 3.1. The values of the parameters $M_1$, $M_2$, $W_1$ and $W_2$ have been established according to the criteria for the case of voltage-controlled PWL function.

![Figure 3.7: DC-responses of the current-controlled memristive systems](image)

Figure 3.7 shows the dc-responses of the current-controlled memristive systems. The procedure for obtaining the simulation results is similar to the case of voltage-controlled memristive systems with the difference that the power supply in Figure 3.6 is current-mode. On one hand, the dashed-line represents the monotonically increasing curve of the current-controlled memristive system using the memristive-state. On the other hand, the solid-line represents the non-monotonically increasing curve of the current-controlled memristive system using the memconductive-state.

In summary, the Figures 3.4 and 3.7 show that the DC-response curve of the memristive system, under certain conditions, exhibits a non-monotonically increasing curve and therefore it is possible to cause multiple operating points.
3.1.4 Variations of the PWL parameters

The parameters $M_1$, $M_2$ and $V_T$ of the PWL memristor model can be related with the memristive behavior of the device. In the bipolar switching memristive systems, the hysteresis process often is of a threshold type: while a high applied voltage is needed to change the device state, at low applied voltages the resistance of the device remains unchanged. This is very often associated [5] with ionic transport and electrochemical reactions. The experimental work of [6] assumes that the rate of the resistance change is small below a threshold voltage $V_T$ and fast above $V_T$.

The location, concentration and distribution of oxygen vacancies in the TiO$_2$ film control the conductance, rectification and switching polarity of the device [7]. Moreover, the ratio $\frac{M_2}{M_1}$ is dependent of the thickness of the TiO$_x$/TiO$_2$ layers [8].

Hereafter, the effects in the voltage-current characteristic of the memristive systems at DC-regime caused by the parameters $M_1$, $M_2$ and $V_T$ of the PWL memristor model are determined using the systematically variations of the parameter values. The variations of parameters are principal focused on two issues: variations of memristive slopes and variations of hyperplane position.

Variations of memristive slopes

In order to assesses the effects of the memristive slopes $M_1$ and $M_2$ in the voltage-current characteristic, the scheme of variations in Figure 3.8 is proposed.

![Figure 3.8: Scheme of variations for memristive slopes](image)

The previous scheme causes two different cases. The first case consists of varying the memristive slope $M_1$ for the following values (in KΩ): 0.1, 0.25, 0.5, 0.75, 1, 1.5, 2, 3, 4 and 5; while $M_2=1$KΩ.

The resulting family of $V$-$I$ curves are depicted in Figure 3.9. These simulation results have been obtained using the numerical integration method of Runge-Kutta for each value
of the memristive slope $M_1$. In plain words, it can be established that $M_1$ affects the asymptotic $V$-$I$ characteristics by flattening the curve and locating the peak closer to zero as $M_1$ increases.

![Figure 3.9: Simulation results using the variations of $M_1$ coefficient](image)

In the second case, the memristive slope $M_2$ is varied for the following values (in KΩ): 0.1, 0.25, 0.5, 0.75, 1, 1.5, 2, 3, 4 and 5; while $M_1$=1KΩ.

In similar way, the resulting $V$-$I$ DC branch relationships are depicted in the family of curves of Figure 3.10. It can be established that $M_2$ affects the asymptotic $V$-$I$ characteristics by lowering the curve at high voltages (for $V > V_T$ approximately) as $M_2$ increases. Besides $M_1$ has no further effect at low voltages and the peak remains basically unchanged.

![Figure 3.10: Simulation results using the variations of $M_2$ coefficient](image)
Variations of hyperplane position

For assessing the effect that the hyperplane position $V_T$ has on the voltage-current characteristic of the memristive system, the scheme of variations in Figure 3.11 is proposed.

![Diagram](image)

Figure 3.11: Scheme of variations for hyperplane position

In this case, the hyperplane position is varied for the following values (in V): 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9 and 1; while $M_1=500\Omega$ and $M_2=1K\Omega$.

The resulting family of characteristic curves $V$-$I$ are depicted in Figure 3.12. It can be established that the position of hyperplane $V_T$ affects the asymptotic characteristic curve $V$-$I$ by lowering the curve at voltages above $V_T$.

![Graph](image)

Figure 3.12: Simulation results using the variations of the hyperplane $V_T$

In summary, it could be noticed that the variations on the PWL parameters affect the shape of the resulting $v$-$i$ curves.

### 3.2 Generation of the $v$-$i$ branch relationship

The main goal of the methodology is to obtain a $v$-$i$ branch relationship that constitutes the memristor model in DC. This methodology is shown in Figure 3.13.
Input parameters

In this initial stage, the voltage-controlled characteristic is given by a PWL function that consists of two lines segments separated by a hyperplane at $V_T$. The slopes of the segments are $M_1$ and $M_2$.

PWL description

The PWL function is based on the well-known canonical representation of (3.3). In the case of the voltage-controlled memristive system, the PWL description is established as (3.4) and (3.5).

Expression of DC characteristic

The state equation of (3.5) is used for obtaining the current-voltage characteristic of the memristive system. In order to do this, the numerical integration formula of the fourth-order Runge-Kutta method is resorted. The formula of RK4 [9] is expressed as

$$x_{n+1} = x_n + \frac{h}{6}(k_1 + 2k_2 + 2k_3 + k_4)$$

using
3.2. Generation of the $v$-$i$ branch relationship

\begin{align*}
k_1 &= f(V_M) \\
k_2 &= f(V_M + \frac{1}{2}k_1h) \\
k_3 &= f(V_M + \frac{1}{2}k_2h) \\
k_4 &= f(V_M + k_3h)
\end{align*}

This method approaches the solution of the ordinary differential equation using an iterative process where the numerical solution $x_{n+1}$ is determined by the present value $x_n$ plus the weighted average of the products of the size of the interval $h$ and an estimated slope. Besides, the RK4 method is a fourth-order method meaning that the local truncation error is on the order of $O(h^5)$ and the total accumulated error is on order of $O(h^4)$. Runge-Kutta methods have local truncation error of the same order of Taylor methods, but do not use the calculation and evaluation of the derivatives of the function [9]. Because of these characteristics and the use only of monotonically increasing curves to represent the memristive system in the DC-domain, the RK4 method is resorted to approach the solution of the ODE. The results of the integration procedure are recast in the output equation of (3.4).

At this point, the process of constructing a mathematical function that fit the series of data points from the output variable of the memristive system is performed using the command \texttt{Fit} from \textit{Wolfram Mathematica} [10]. This curve fitting procedure is applied in order to approximate the current-voltage characteristic to a polynomial function of the form:

\[
\hat{i}(V_M) = a_nV_M^n + a_{n-1}V_M^{n-1} + \ldots + a_2V_M^2 + a_1V_M + a_0
\]

(3.8)

The expression of (3.8) represents the constitutive branch relationship of the memristive system that will be used for DC analysis in the simulation procedure. In particular, special attention is devoted to assess the existence of multiple DC operating points because the expression in (3.8) may be a non monotonically increasing characteristic.

Simulation procedure

In the simulation procedure an input netlist is used to establish the equilibrium equation that will be placed in a homotopy solver for obtaining the multiple DC solutions. The input netlist is oriented to input the circuit description containing components as voltage and current independent-sources, linear resistors and memristors. The equilibrium equation is formulated by using a slightly changed version of the modified nodal analysis
formulation that incorporates the current-voltage characteristics of the memristive systems as a separated nonlinear current vector, as follows:

\[
f(x) = Y_{mna}X_{mna} + \hat{i}(V_M) - S = 0
\]

where, \(X_{mna}\) represents the unknowns as the MNA variables, \(S\) is the stimuli vector and \(\hat{i}(V_M)\) is the vector of the voltage-controlled memristor branch relationships.

Because Newton-Rhapson methods face several convergence problems especially when dealing with equations emanating from memristive systems, the homotopy methods are resorted. Homotopy methods formulate an associated equation to the original system of non-linear equations by adding an extra parameter, the homotopy parameter \(\lambda\). The homotopy formula is represented by

\[
H(f(x), \lambda) = f(x) + (\lambda - 1)f(x_0) = 0
\]

The solutions are found on the homotopy path.

### 3.3 A glimpse to DC analysis of memristive circuits

In general, the problem of finding the DC operating point is important because it is the starting point for other kinds of analysis such as the small signal and transient analysis. The work of finding the DC operating consists in solving the nonlinear algebraic equations (NAEs) emanating from circuits.

The complete solution to the general DC problem of nonlinear circuits focusses on the next aspects [11]: determining whether or not the uniqueness of the dc solution is guaranteed, establishing an upper bond on the number of dc solutions, and as last step calculating all of them, as well as determining their conditions for stability.

As for nonlinear resistive circuits, the resulting equilibrium equation for memristive circuits at dc regime has the form of system of NAEs:

\[
f(x) = 0
\]  

(3.9)

where \(x\) is the set of unknowns node voltages and currents of the non-NA compatible elements.

For memristor circuits, the highly nonlinear resulting curves impose serious convergence problems when using the well-known Newton-Raphson method for solving the system of NAEs in (3.9). Besides, Newton-Raphson methods are locally convergent, it means that they usually fail to converge to a solution when the starting point is not close enough to
3.3. A glimpse to DC analysis of memristive circuits

the solution.

Homotopy methods have proved its usefulness not only to overcome this drawback but also to find more than one DC solutions. They are based on establishing an auxiliary scheme in order to convert the problem of finding the roots of the system in (3.9) a static problem into a problem of finding the solution of an associated ordinary differential equation (a dynamic problem) [12, 13].

The homotopy equation is formed by adding a parameter to the original equation:

$$\mathcal{H}(f(x), \lambda) = 0$$

where $\lambda$ is the homotopy parameter, and $\mathcal{H}$ is the resulting homotopy formula.

However, the homotopy methods exhibit three principal drawbacks, such as: the initial point where the homotopy starts to trace the solution, the stop criterion to decide when to stop seeking for more solutions and the path tracking to ensure the trajectory of the solution curve.

In [13], a homotopy scheme that overcomes the problem of the stop criterion for these kinds of methods has been introduced and it will be applied to solve the equilibrium equations of memristive circuits. This homotopy method is called the double-bounded homotopy (DBH) and is defined by

$$\mathcal{H}(f(x), \lambda) = CQ + e^Q \ln(Df^2(x) + 1)$$

where $f(x)$ is the function to solve, $\lambda$ is the homotopy parameter, $a$ and $b$ are the values of the double bounding lines, $C$ and $D$ are positive constants of the homotopy, and $Q$ is given by:

$$(\lambda - a)(\lambda - b)$$

Hereafter, the DBH method is employed to find the solutions in the memristive circuits at dc-regimen.
3.4 Cases of study

3.4.1 A single-memristor circuit

The first example consists of the memristive circuit shown in Figure 3.14.

\[
I_M = 0.0505V_M + 0.00933V_M^2 - 1.045V_M^3 + 4.1928V_M^4 - 8.6192V_M^5 + 10.9289V_M^6 \\
- 9.0108V_M^7 + 4.8515V_M^8 - 1.647V_M^9 + 0.320V_M^{10} - 0.0272V_M^{11} \tag{3.10}
\]

\[
I_M = 0.0547V_M + 0.099V_M^2 - 0.6338V_M^3 + 3.5221V_M^4 - 8.2V_M^5 + 11.1881V_M^6 \\
- 9.6988V_M^7 + 5.419V_M^8 - 1.8937V_M^9 + 0.3769V_M^{10} - 0.0326V_M^{11} \tag{3.11}
\]

\[
I_M = 0.057V_M - 0.1689V_M^2 - 0.2551V_M^3 + 2.462V_M^4 - 6.351V_M^5 + 9.054V_M^6 \\
- 8.0449V_M^7 + 4.5671V_M^8 - 1.6142V_M^9 + 0.324V_M^{10} - 0.0282V_M^{11} \tag{3.12}
\]

Figure 3.14: DC memristive circuit

where \( V = 2V \) and \( R = 400\Omega \). The voltage-controlled memristor \( M \) is given by three different \( I-V \) expressions with the purpose of inspecting the impact of parameter variation on the amount of solutions for memristive circuits. These expressions are obtained using the methodology for generating the \( v-i \) characteristics as shown in Figure 3.13 and are defined as follow.

As it can be seen, the order of the \( I-V \) expressions is set to a value of 11 in order to obtain greater accuracy with respect to the numerical solution from the process of integration. In addition, a lower order of the expression compromises the tolerance with respect to the original curve of the memristive system.

According to the expression of the memristor, three different cases of DC-response can emerge. These cases are the result of the intersection between the asymptotic \( I-V \) memristor characteristic and the load line -defined by the values of \( V \) and \( R \). DC-responses
are depicted in Figure 3.15.

The first case is shown in Figure 3.15a with $M_1=500$ and $M_2=500$. In this circumstance, a Newton-Rapshon scheme can find the solution provided the Jacobian of the system remains non-singular. This case uses the $I-V$ expression of (3.10).

The second case uses the $I-V$ expression of (3.11) with $M_1=810$ and $M_2=500$. In this case, Newton-like methods are able to reach only the first solution (at low voltages) but they experience serious convergence problems when assessing the second solution (when the load line is tangent to the $I-V$ characteristic). Figure 3.15b shows the DC-response of this case.

The third case is shown in Figure 3.15c with $M_1=1000$ and $M_2=100$. In this case, Newton-Raphson methods are able to find only one solution depending on the selection of the starting guess of the method. The $I-V$ expression of (3.12) is used for this case.

![Figure 3.15: DC-response of different memristor characteristics](image)

Table 3.2 shows the operating points of the three cases explained above. The cases of multiple solutions, Figures 3.15b and 3.15c, have been addressed by resorting to the DBH method.
In the following, the stability of the DC solutions for each case is addressed.

**First case** Herein, the system possesses a single DC operating point. This can be straightforwardly solved by using the traditional Newton method. The solution lies on a positive -slope region of the $v$-$i$ memristor DC characteristic, which means that the solution is stable.

**Second case** Here, two solutions are found. $S_1$ is stable while $S_2$ is unstable.

**Third case** In this case three solutions appear. $S_1$ and $S_3$ are stable while $S_2$ is unstable.

### Table 3.2: Summary of the operating points of the three cases

<table>
<thead>
<tr>
<th>Sol.</th>
<th>$V_M$ (V)</th>
<th>$I_M$ (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>0.108692</td>
<td>0.00472827</td>
</tr>
<tr>
<td>$S_1$</td>
<td>0.124707</td>
<td>0.00468823</td>
</tr>
<tr>
<td>$S_2$</td>
<td>0.860166</td>
<td>0.00284958</td>
</tr>
<tr>
<td>$S_1$</td>
<td>0.140453</td>
<td>0.00464887</td>
</tr>
<tr>
<td>$S_2$</td>
<td>0.393065</td>
<td>0.00401734</td>
</tr>
<tr>
<td>$S_3$</td>
<td>1.03058</td>
<td>0.00242355</td>
</tr>
</tbody>
</table>

Additional comparative information of the three cases are summarized in Table 3.3.

### Table 3.3: Analysis of the operating points of the DC memristive circuit

<table>
<thead>
<tr>
<th>Sol.</th>
<th>$V_R$</th>
<th>$I_R$</th>
<th>$V_M$</th>
<th>$I_M$</th>
<th>$P_R$</th>
<th>$P_M$</th>
<th>$\sum V I$</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>0.00472827</td>
<td>1.89131</td>
<td>0.00472827</td>
<td>0.108692</td>
<td>0.00945654</td>
<td>0.00894261</td>
<td>2.81893x10⁻¹⁸</td>
</tr>
<tr>
<td>$S_1$</td>
<td>0.00468823</td>
<td>1.87529</td>
<td>0.00468823</td>
<td>0.124707</td>
<td>0.00937646</td>
<td>0.00879181</td>
<td>-4.3361x10⁻¹⁹</td>
</tr>
<tr>
<td>$S_2$</td>
<td>0.00284958</td>
<td>1.13983</td>
<td>0.00284958</td>
<td>0.860166</td>
<td>0.00568465</td>
<td>0.00241312</td>
<td>-5.7278x10⁻¹⁵</td>
</tr>
<tr>
<td>$S_1$</td>
<td>0.00464887</td>
<td>1.85955</td>
<td>0.00464887</td>
<td>0.140453</td>
<td>0.00929774</td>
<td>0.00844119</td>
<td>-1.6263x10⁻¹⁸</td>
</tr>
<tr>
<td>$S_2$</td>
<td>0.00401734</td>
<td>1.60693</td>
<td>0.00401734</td>
<td>0.393065</td>
<td>0.00541499</td>
<td>0.00241312</td>
<td>-8.0231x10⁻¹⁸</td>
</tr>
<tr>
<td>$S_3$</td>
<td>0.00242355</td>
<td>0.96942</td>
<td>0.00242355</td>
<td>1.03058</td>
<td>0.0048471</td>
<td>0.00234944</td>
<td>-7.2307x10⁻¹⁵</td>
</tr>
</tbody>
</table>
3.4.2 A two-memristor circuit

The second example consists of a two-memristor circuit [14], as shown in Figure 3.16.

\[ I_{M1} = 0.05417(V_b - V_c) - 0.0822(V_b - V_c)^2 - 0.7455(V_b - V_c)^3 + 3.9447(V_b - V_c)^4 
- 9.1982(V_b - V_c)^5 + 12.6736(V_b - V_c)^6 - 11.11(V_b - V_c)^7 + 6.273(V_b - V_c)^8 
- 2.2124(V_b - V_c)^9 + 0.4438(V_b - V_c)^{10} - 0.0386(V_b - V_c)^{11} \]  
(3.13)

\[ I_{M2} = 0.057V_c - 0.1689V_c^2 - 0.2551V_c^3 + 2.462V_c^4 - 6.351V_c^5 + 9.0546V_c^6 
- 8.0449V_c^7 + 4.5671V_c^8 - 1.6142V_c^9 + 0.324V_c^{10} - 0.0282V_c^{11} \]

Figure 3.17 shows the DC-responses of the \( M_1 \) and \( M_2 \) memristors. The memristive characteristics of \( M_1 \) and \( M_2 \) present three intersections with the load line. Table 3.4 shows the operating points of the memristors \( M_1 \) and \( M_2 \).
Table 3.4: Summary of the operating points of $M_1$ and $M_2$

<table>
<thead>
<tr>
<th>Sol.</th>
<th>$V_M$ (V)</th>
<th>$I_M$ (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_1$</td>
<td>0.1220</td>
<td>4.6949</td>
</tr>
<tr>
<td>$S_2$</td>
<td>0.7397</td>
<td>3.1507</td>
</tr>
<tr>
<td>$S_3$</td>
<td>1.0811</td>
<td>2.2970</td>
</tr>
<tr>
<td>$S_4$</td>
<td>0.1410</td>
<td>4.6472</td>
</tr>
<tr>
<td>$S_5$</td>
<td>0.3880</td>
<td>4.0297</td>
</tr>
<tr>
<td>$S_6$</td>
<td>1.0661</td>
<td>2.3345</td>
</tr>
</tbody>
</table>

The branch electrical-variables of $M_1$ and $M_2$ are shown in Table 3.5.

Table 3.5: Analysis of the operating points of $M_1$ and $M_2$

<table>
<thead>
<tr>
<th>Sol.</th>
<th>$V_M$ (V)</th>
<th>$I_M$ (mA)</th>
<th>$I_M'(V_M) = G_M(S)$</th>
<th>$R_M(\Omega) = G_M^{-1}$</th>
<th>$P_M$ (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_1$</td>
<td>0.1220229859979923</td>
<td>4.694942535005002</td>
<td>0.0211003</td>
<td>47.39269</td>
<td>0.572891</td>
</tr>
<tr>
<td>$S_2$</td>
<td>0.739714187344127</td>
<td>3.1507145316396826</td>
<td>-0.00407294</td>
<td>-245.52289</td>
<td>2.33063</td>
</tr>
<tr>
<td>$S_3$</td>
<td>1.0811665470000758</td>
<td>2.297076632498105</td>
<td>-0.00019711</td>
<td>-5.073x10^{-3}</td>
<td>2.48353</td>
</tr>
<tr>
<td>$S_4$</td>
<td>0.14109989090191406</td>
<td>4.6472472727452149</td>
<td>0.00118107</td>
<td>84.60898</td>
<td>0.655722</td>
</tr>
<tr>
<td>$S_5$</td>
<td>0.388011511346674</td>
<td>4.029797122163331</td>
<td>-0.00666631</td>
<td>-151.37043</td>
<td>1.56389</td>
</tr>
<tr>
<td>$S_6$</td>
<td>1.0661612891168126</td>
<td>2.334596772079685</td>
<td>-0.000998819</td>
<td>-1.001x10^{-3}</td>
<td>2.46906</td>
</tr>
</tbody>
</table>

With the purpose of obtaining the solutions of circuit in Figure 3.16, the DBH method is resorted. Table 3.6 shows the operating points of the circuit compounded of $M_1$ and $M_2$ memristors. Besides, the branch electrical-variables of the operation points are shown in Table 3.7.

Table 3.6: Solutions using the DBH method

<table>
<thead>
<tr>
<th>Soluciones</th>
<th>$V_b$ (V)</th>
<th>$V_c$ (V)</th>
<th>$I_v$ (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_1$</td>
<td>1.2082259570272</td>
<td>1.4078452267629</td>
<td>-1.9794351074322</td>
</tr>
<tr>
<td>$S_2$</td>
<td>0.041500014955818</td>
<td>0.25237891076774</td>
<td>-4.8062499626355</td>
</tr>
<tr>
<td>$S_3$</td>
<td>0.23403114962084</td>
<td>0.12430622762259</td>
<td>-4.4149221250480</td>
</tr>
<tr>
<td>$S_4$</td>
<td>0.920681999991821</td>
<td>0.057622615964098</td>
<td>-2.6982950002045</td>
</tr>
<tr>
<td>$S_5$</td>
<td>1.0567255225081</td>
<td>0.04870250321150</td>
<td>-2.3581811937297</td>
</tr>
<tr>
<td>$S_6$</td>
<td>0.52990240876302</td>
<td>0.44637855425860</td>
<td>-3.6752439780925</td>
</tr>
<tr>
<td>$S_7$</td>
<td>1.033478006494494</td>
<td>0.98384546118236</td>
<td>-2.4163049837640</td>
</tr>
</tbody>
</table>
### 3.4. Cases of study

#### Table 3.7: Analysis of the solutions using DBH method

<table>
<thead>
<tr>
<th>Sol.</th>
<th>V_E</th>
<th>I_E</th>
<th>V_R</th>
<th>I_R</th>
<th>V_M</th>
<th>I_M</th>
<th>V_M</th>
<th>I_M</th>
<th>V_M</th>
<th>I_M</th>
<th>P_E</th>
<th>P_R</th>
<th>P_M</th>
<th>P_M</th>
<th>∑Vf</th>
</tr>
</thead>
<tbody>
<tr>
<td>S_1</td>
<td>2</td>
<td>-0.00197944</td>
<td>0.791774</td>
<td>0.00197944</td>
<td>-0.199619</td>
<td>0.00197944</td>
<td>1.40785</td>
<td>0.00197944</td>
<td>-0.00395887</td>
<td>0.00156727</td>
<td>-0.000395133</td>
<td>0.00278674</td>
<td>-5.2448x10^{-11}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S_2</td>
<td>2</td>
<td>-0.00197944</td>
<td>1.9585</td>
<td>0.00197944</td>
<td>-0.210879</td>
<td>0.00197944</td>
<td>2.52379</td>
<td>0.00197944</td>
<td>-0.00597925</td>
<td>0.00058901</td>
<td>-0.00103252</td>
<td>0.00123571</td>
<td>-1.37078x10^{-10}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S_3</td>
<td>2</td>
<td>-0.00197944</td>
<td>1.76597</td>
<td>0.00197944</td>
<td>-0.199725</td>
<td>0.00197944</td>
<td>1.21436</td>
<td>0.00197944</td>
<td>-0.008882984</td>
<td>0.00079661</td>
<td>0.000484427</td>
<td>0.000548802</td>
<td>-1.11586x10^{-14}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S_4</td>
<td>2</td>
<td>-0.00266983</td>
<td>1.07932</td>
<td>0.00266983</td>
<td>0.863059</td>
<td>0.00266983</td>
<td>0.0576226</td>
<td>0.00266983</td>
<td>-0.00589659</td>
<td>0.00291232</td>
<td>0.0022879</td>
<td>0.000155483</td>
<td>2.15945x10^{-13}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S_5</td>
<td>2</td>
<td>-0.00235818</td>
<td>0.94272</td>
<td>0.00235818</td>
<td>1.00803</td>
<td>0.00235818</td>
<td>0.0487025</td>
<td>0.00235818</td>
<td>-0.004761636</td>
<td>0.00222441</td>
<td>0.00237711</td>
<td>0.000114849</td>
<td>1.36692x10^{-9}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S_6</td>
<td>2</td>
<td>-0.00367524</td>
<td>1.4701</td>
<td>0.00367524</td>
<td>0.0835239</td>
<td>0.00367524</td>
<td>0.446379</td>
<td>0.00367524</td>
<td>-0.00735049</td>
<td>0.00540297</td>
<td>0.000306971</td>
<td>0.00164056</td>
<td>1.02618x10^{-11}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S_7</td>
<td>2</td>
<td>-0.0024163</td>
<td>0.966522</td>
<td>0.0024163</td>
<td>0.0496325</td>
<td>0.0024163</td>
<td>0.983845</td>
<td>0.0024163</td>
<td>-0.00483261</td>
<td>0.00235441</td>
<td>0.00019927</td>
<td>0.0027727</td>
<td>4.2659x10^{-13}</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Chapter 3. Development of DC memristor models
Bibliography


Chapter 4

Transient memristor model

The principal properties and fingerprints of the memristors have been established in the time-domain. The models of the memristors have been generated using SPICE-models, mathematical-models and behavioral-models. However, these kind of models do not fulfill the fundamental characteristics of the memristive systems.

From the point of view of CAD, the modeling of the memristor must comply with the following requirements: two-terminal model, full-symbolical expression and the capacity of showing the principal variables of the memristive systems.

This chapter presents two memristor models using two different methods in order to generate the $v$-$i$ expressions that satisfy the properties and fingerprints of the memristors. The first one is based on the polynomial approximation of the constitutive variables of the memristor. The second one is based on the solution of the memristive system from the HP memristor using the homotopy perturbation method.

4.1 Polynomial-based model

In this part, the memristor model is obtained using the polynomial expression. The mathematical description is presented in order to establish the connection between the $q$-$\varphi$ curve and the $v$-$i$ expression of the model. Besides, the memristor model is simulated with the purpose of showing the behavior in the time-domain.

4.1.1 Mathematical description

The memristor can be either $q$-controlled or $\varphi$-controlled. Therefore, the memristor can be described by the following function
\[ \varphi(t) = M_1 q(t) + M_2 q(t)^2 \]  \hspace{1cm} (4.1)\]

where \( M_1 \) and \( M_2 \) are the memristance values defined as

\[ M_1 = R_{OFF} \quad M_2 = \frac{R_{ON} - R_{OFF}}{4} \]

where \( R_{OFF} \) and \( R_{ON} \) are the OFF-state and ON-state resistance, respectively. The order of the polynomial function shown in (4.1) is set to a value of two for the purpose of maintaining simplicity in the formulation without performing complex calculations. In addition, a higher order of the polynomial expression involves a faster switching time between the values of \( R_{OFF} \) and \( R_{ON} \) of the memristor. This area of study is not addressed in this thesis and therefore the order selected in (4.1) is useful.

The current across the memristor is defined by

\[ i(t) = A \sin(\omega t) \]  \hspace{1cm} (4.2)\]

where \( A \) is the current amplitude and \( \omega \) represents the frequency. By integrating (4.2), the electric charge \( q(t) \) is obtained

\[ q(t) = \int_0^t A \sin(\omega \tau) d\tau = \frac{A}{\omega} [1 - \cos(\omega t)] \]  \hspace{1cm} (4.3)\]

A new expression for the flux is obtained, after substituting (4.3) in (4.1)

\[ \varphi(t) = \frac{A}{\omega} (1 - \cos(\omega t)) \left[M_1 + M_2 \frac{A}{\omega} (1 - \cos(\omega t)) \right] \]

Because the time-derivative of the flux is the voltage, it is possible obtain an expression for the voltage

\[ v(t) = \left[M_1 + 2M_2 \frac{A}{\omega} (1 - \cos(\omega t)) \right] i(t) \]  \hspace{1cm} (4.4)\]

The expression of (4.4) constitutes in fact an \( v-i \) branch relationship that models the memristor, and it can be recast as a functional model for simulation purposes. It clearly results that the memristance is given as:

\[ M = \left[M_1 + 2M_2 \frac{A}{\omega} (1 - \cos(\omega t)) \right] \]  \hspace{1cm} (4.5)\]

It is important to notice, that the limit value of the memristance at high frequency is:

\[ M_\infty = \lim_{\omega \to \infty} (M) = M_1 = R_{OFF} \]
i.e. the value of the OFF-state resistance

### 4.1.2 Characteristic of the memristor model

The polynomial memristor model is established using the expression of (4.4). This memristor model is evaluated for discrete values of the frequency at \( \omega = 1, 2, 10 \), and the corresponding hysteresis loops are shown in Figure 4.1. It possesses the main fingerprints of a passive memristor, such as: pinched hysteresis loop, hysteresis lobe area and shrunken hysteresis loop. The curves have been obtained for \( R_{OFF} = 14.41 \text{ K}\Omega \), \( R_{ON} = 1.4 \text{ K}\Omega \) and \( A = 1 \).

![Figure 4.1: Hysteresis loops of the memristor model](image)

Besides, the waveform of the memristance given by (4.5) is depicted in Figure 4.2. The loci traced out by \((M,v(t))\) is a hysteresis loop, but it is not pinched since \( M > 0 \) for all times.

![Figure 4.2: Memristance of the memristor model](image)
4.2 Homotopy-based model

In this part, the memristor model is obtained using the homotopy perturbation method (HPM). Firstly, a brief glimpse of the HPM procedure is introduced. Then, the relation between the system of equations of the HP memristor and the homotopy equation is presented. Hereafter, the numerical and symbolical analysis of the solutions from the HPM procedure is realized in order to establish the behavior of the principal characteristics of the memristor model. Moreover, the variation of the parameter is addressed with the purpose of finding the range of usefulness of the memristor model. Finally, the memristor model is simulated with the purpose of showing the behavior in the time-domain.

4.2.1 Homotopy perturbation method

The homotopy perturbation method (HPM) is employed to obtain an approximate solution for the nonlinear differential equations \([1, 2, 3]\). HPM introduces a homotopy parameter \(p\), which takes values ranging from 0 up to 1.

The nonlinear differential equation, for the case of HPM, can be expressed as

\[
L(v) + N(v) - f(r) = 0
\]

where \(L\) and \(N\) are the linear and nonlinear operators, and \(f(r)\) is a known analytic function.

The homotopy formulation can be established as

\[
H(v, p) = (1 - p)[L(v) - L(u_0)] + p[L(v) + N(v) - f(r)] = 0
\]

(4.6)

where \(u_0\) is the initial approximation for the solution of (4.6), and \(p\) is known as the perturbation homotopy parameter.

Assuming that the solution of (4.6) can be represented as a power series of \(p\)

\[
v = p^0v_0 + p^1v_1 + p^2v_2 + \cdots
\]

Therefore, the approximate solution of (4.6) can be of the form

\[
v = v_0 + v_1 + v_2 + \cdots
\]

(4.7)

The general procedure for the approximate solution of the nonlinear differential equation using HPM is shown in Figure 4.3. This procedure consists of formulating the homotopy equation with the nonlinear differential equation. Then, the order of approximation
$n^*$ should be set to generate the power series of $p$. This power series is substituted in the homotopy equation with the purpose of obtaining terms in function of the homotopy parameter. The coefficient of the power $n$ homotopy parameter is used as the nonlinear differential equation and the solution is considered the particular case of the power $n$ homotopy parameter. Hereafter, the particular solutions of the nonlinear differential equations using the coefficient of the power $n$ homotopy parameter are obtained until the power $n$ equals to the order of approximation $n^*$. Finally, the general solution is composed of the sum of all the particular solutions.

Figure 4.3: General procedure of the approximate solution using HPM
4.2.2 Memristor model using HPM

The HP memristor can be represented by the following system of equations

\[
\frac{dw(t)}{dt} = \mu_V \frac{R_{ON}}{D} i(t) f(w(t))
\]

\[
f(w(t)) = aw(t)^5 - 2aw(t)^3 + aw(t)
\]

\[
v(t) = \left( R_{ON} \frac{w(t)}{D} + R_{OFF} \left( 1 - \frac{w(t)}{D} \right) \right) i(t)
\]

(4.8)

where \( \mu_V \) is the average ion mobility, \( D \) is the full length of the device, \( R_{ON} \) and \( R_{OFF} \) are the ON and OFF state resistances, \( w(t) \) is the state variable that represents the length of the doped region, \( f(w(t)) \) is the window function and \( a \) is the window function coefficient.

The current across the memristor \( i(t) \) is represented by the following expression

\[ i(t) = A \sin(\omega t) \]

where \( A \) is the current amplitude and \( \omega \) is the angular frequency.

The state variable equation of (4.8) can be re-written as

\[
\frac{dx(t)}{dt} = \mu_V \frac{R_{ON}}{D^2} i(t) f(x(t))
\]

(4.9)

where \( x(t) = \frac{w(t)}{D} \) is the normalized state variable.

The nonlinear equation of (4.9) is substituted in the homotopy formulation of (4.6)

\[
H(x(t), p) = (1 - p) \left[ \frac{dx(t)}{dt} \right] + p \left[ \frac{dx(t)}{dt} - \mu_V \frac{R_{ON}}{D^2} i(t) f(x(t)) \right] = 0
\]

(4.10)

The expression of (4.10) is developed using the general procedure of HPM shown in Figure 4.3. Hereafter, the approximate solutions of the homotopy formulation are evaluated using two principal types of analysis: numerical and symbolical analysis.

4.2.3 Numerical analysis

The numerical analysis is based on the choice of the homotopy order by comparing the margin of error between HPM procedure and the numerical integration method. Moreover, the behavior of the margin of error as the frequency tends to infinity is studied. The numerical analysis is carried out using the parameter values of \( x_0=0.1, a=3, A=400 \times 10^{-7}, \mu=1 \times 10^{-14}, R_{ON}=100, \alpha=160 \) and \( D=10 \times 10^{-9} \).
Homotopy order

The principal objective is to find the most suitable homotopy order in order to carry out the symbolical analysis. The way to do this is comparing the solution $x(t)$ from HPM and the solution $x^*(t)$ from the four-order Runge-Kutta integration method (RK4). The comparison procedure is performed by assessing the root-mean-square error (RMSE).

The RMSE can be determined by

$$\text{RMSE} = \sqrt{\frac{1}{n} \sum_{i=1}^{n} (x^*(t) - x(t))^2}$$

(4.11)

where $n$ is the number of samples.

Figure 4.4: RMSE using different homotopy orders

Figure 4.4 shows the RMSE values for different homotopy orders. The lowest RMSE values are located in the 19 and 32 homotopy orders. However, these homotopy orders generate solutions $x(t)$ with significant amount of terms. Therefore, the homotopy order should be less than 19.

The values of homotopy order under 19 present wide dispersion of RMSE values, as shown in Figure 4.4. However, the homotopy orders of 6 and 15 remain with low values of RMSE. Besides, the number of terms in the solution $x(t)$ using the homotopy order of 6 is negligible compared to the 15, 19 and 32 homotopy orders values. This feature represents an advantage, from the point of view of modeling, because with a minor amount of terms; the behavior of the HP memristor can be modeled.

Assuming that, the difference between the curve of the solution $x(t)$ from HPM procedure and the curve of the solution $x^*(t)$ from the RK4 procedure is not significant, as shown in Figure 4.5, the homotopy order 6 is chosen to carry out the symbolical analysis.
Figure 4.5: HPM and RK4 curves of the solution $x(t)$ using the homotopy order 6.

**Frequency**

The purpose of the frequency variation is to analyze the RMSE values as the frequency tends to infinity. This part of the numerical analysis is carried out using the mathematical expression of (4.11) and the homotopy order of 6. Moreover, the frequency value is varied from 1 to 100.

Table 4.1: RMSE values using different frequency values. The HPM order is 6.

<table>
<thead>
<tr>
<th>Frequency</th>
<th>RMSE</th>
<th>Frequency</th>
<th>RMSE</th>
<th>Frequency</th>
<th>RMSE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.008607500</td>
<td>35</td>
<td>0.008532501</td>
<td>70</td>
<td>0.000818259</td>
</tr>
<tr>
<td>5</td>
<td>0.001047520</td>
<td>40</td>
<td>0.000841938</td>
<td>75</td>
<td>0.000818259</td>
</tr>
<tr>
<td>10</td>
<td>0.000931147</td>
<td>45</td>
<td>0.000844512</td>
<td>80</td>
<td>0.000818259</td>
</tr>
<tr>
<td>15</td>
<td>0.000895380</td>
<td>50</td>
<td>0.000827569</td>
<td>85</td>
<td>0.000818259</td>
</tr>
<tr>
<td>20</td>
<td>0.000870859</td>
<td>55</td>
<td>0.000818259</td>
<td>90</td>
<td>0.000818259</td>
</tr>
<tr>
<td>25</td>
<td>0.000853746</td>
<td>60</td>
<td>0.000818259</td>
<td>95</td>
<td>0.000818259</td>
</tr>
<tr>
<td>30</td>
<td>0.000859321</td>
<td>65</td>
<td>0.000818259</td>
<td>100</td>
<td>0.000771825</td>
</tr>
</tbody>
</table>

Figure 4.6: RMSE using different frequency values. The HPM order is 6.

Table 4.1 show the RMSE values between the solutions $x(t)$ and $x^*(t)$ as the frequency tends to infinity. As it can be seen, the RMSE value decreases as the frequency increases.
Besides, the behavior of the RMSE values is depicted in Figure 4.6 from 1 to 100 frequency values.

The simulation results show two principal behaviors. Firstly, the RMSE value decreases rapidly as the frequency increases the double of the value. After that, the RMSE value decreases gradually as the frequency continuously increasing. The reduction of the RMSE is related to the form of the solution \( x(t) \) as the frequency approaches infinity. The waveform of the solution \( x(t) \) is an asymmetrical and periodical curve which has a margin of error with respect to the solution \( x^*(t) \) from the numerical integration method. This difference is reduced as the frequency increases because the solutions of the \( x(t) \) and \( x^*(t) \) curves become symmetrical and periodical waveforms and therefore the error tends to zero.

### 4.2.4 Symbolical analysis

The symbolical analysis is based on the composition of the symbolical solution \( x(t) \) using the homotopy order established in the numerical analysis. Moreover, the symbolical memristance \( M(x(t)) \) is studied in order to establish the mathematical expression that models the memristor. Finally, the behavior of the \( x(t) \) and \( M(x(t)) \) symbolical expressions as the frequency increases is studied in order to establish the dependency of the frequency.

#### Symbolical solution \( x(t) \)

The symbolical solution \( x(t) \) is obtained from HPM procedure using the mathematical expression of (4.10) and the homotopy order of 6. This symbolical expression is represented by

\[
x(t) = x_0 + \frac{C_h a A \mu R_{ON}}{\omega D^2} + \frac{C_h a R_{ON}^2}{\omega^2 D^4} + \frac{C_h a^3 \mu^3 R_{ON}^3}{\omega^3 D^6} + \frac{C_h a^4 A^4 \mu^4 R_{ON}^4}{\omega^4 D^8} - \frac{C_h a^5 A^5 \mu^5 R_{ON}^5}{\omega^5 D^{10}} - \frac{C_h a^6 A^6 \mu^6 R_{ON}^6}{\omega^6 D^{12}} \\
+ \cos(\omega t) \left[ - \frac{C_h a A \mu R_{ON}}{\omega D^2} - \frac{C_h a^2 A^2 \mu^2 R_{ON}^2}{\omega^2 D^4} - \frac{C_h a^3 A^3 \mu^3 R_{ON}^3}{\omega^3 D^6} + \frac{C_h a^4 A^4 \mu^4 R_{ON}^4}{\omega^4 D^8} - \frac{C_h a^5 A^5 \mu^5 R_{ON}^5}{\omega^5 D^{10}} + \frac{C_h a^6 A^6 \mu^6 R_{ON}^6}{\omega^6 D^{12}} \right] \\
+ \cos(2\omega t) \left[ - \frac{C_h a A \mu R_{ON}}{\omega D^2} + \frac{C_h a^3 A^3 \mu^3 R_{ON}^3}{\omega^3 D^6} + \frac{C_h a^4 A^4 \mu^4 R_{ON}^4}{\omega^4 D^8} - \frac{C_h a^5 A^5 \mu^5 R_{ON}^5}{\omega^5 D^{10}} - \frac{C_h a^6 A^6 \mu^6 R_{ON}^6}{\omega^6 D^{12}} \right] \\
+ \cos(3\omega t) \left[ - \frac{C_h a A \mu R_{ON}}{\omega D^2} - \frac{C_h a^2 A^2 \mu^2 R_{ON}^2}{\omega^2 D^4} - \frac{C_h a^3 A^3 \mu^3 R_{ON}^3}{\omega^3 D^6} + \frac{C_h a^4 A^4 \mu^4 R_{ON}^4}{\omega^4 D^8} + \frac{C_h a^5 A^5 \mu^5 R_{ON}^5}{\omega^5 D^{10}} \right]
\]
Chapter 4. Transient memristor model

The total number of harmonics is 6, as shown in (4.12).

\[ \text{Symbolical memristance } M(x(t)) \]

The symbolical memristance \( M(x(t)) \) is represented by

\[
M(x(t)) = R_{ON}x(t) + \alpha R_{ON}(1 - x(t))
\]

(4.13)

In the case of the homotopy order of 6, the solution \( x(t) \) is composed of 7 terms and the total number of harmonics is 6, as shown in (4.12).

where \( x_0 \) is the initial width and \( C_h \) is a constant of the homotopy.

The solution \( x(t) \) from HPM is composed of \( (p + 1) \) terms, where \( p \) is the homotopy order. The first term is called DC. The second term is called the fundamental. The following terms are called the harmonics. The total number of harmonics depends on the value of \( p \).

Substituting the symbolical solution \( x(t) \) in (4.13), the symbolical memristance \( M(x(t)) \) can be re-written as

\[
M(x(t)) = x_0 R_{ON} + R_{ON} \alpha (1 - x_0) + \frac{C_h a A \mu R_{ON}^2}{\omega D^2} + \frac{C_h a^2 A^2 \mu^2 R_{ON}^3}{\omega^2 D^4} + \frac{C_h a^3 A^3 \mu^3 R_{ON}^4}{\omega^3 D^6} + \frac{C_h a^4 A^4 \mu^4 R_{ON}^5}{\omega^4 D^8} + \frac{C_h a^5 A^5 \mu^5 R_{ON}^6}{\omega^5 D^{10}} + \frac{C_h a^6 A^6 \mu^6 R_{ON}^7}{\omega^6 D^{12}}
\]  

(4.12)

\[ + \cos(\omega t) \left[ + \frac{C_h a A \mu R_{ON}^2}{\omega D^2} - \frac{C_h a^2 A^2 \mu^2 R_{ON}^3}{\omega^2 D^4} + \frac{C_h a^3 A^3 \mu^3 R_{ON}^4}{\omega^3 D^6} - \frac{C_h a^4 A^4 \mu^4 R_{ON}^5}{\omega^4 D^8} + \frac{C_h a^5 A^5 \mu^5 R_{ON}^6}{\omega^5 D^{10}} - \frac{C_h a^6 A^6 \mu^6 R_{ON}^7}{\omega^6 D^{12}} \right] \]

72


The symbolical memristance \( M(x(t)) \) from HPM is composed of \((p + 1)\) terms. These terms are called DC and the harmonics. In the case of the homotopy order of 6, the symbolical memristance is composed of 7 terms and the total number of harmonics is 6.

The symbolical expression of (4.14) constitutes in fact an \( v-i \) branch relationship that models the memristor, and it can be recast as a functional model for simulation purposes.

\( x(t) \) and \( M(x(t)) \) frequency dependency

In order to determine the influence of the frequency in the solution \( x(t) \) and memristance \( M(x(t)) \) symbolical expressions, the parameters are replaced with the following values: \( x_0=0.1, \, a=3, \, A=400\times10^{-7}, \, \mu=1\times10^{-14}, \, R_{ON}=100, \, \alpha=160 \) and \( D=10\times10^{-9} \).

The symbolical solution \( x(t) \) of (4.12) can be simplified as

\[
x(t) = 0.1 - \frac{0.0241758}{\omega^6} - \frac{0.015989}{\omega^5} + \frac{0.0106446}{\omega^4} + \frac{0.0542583}{\omega^3} + \frac{0.0995527}{\omega^2} + \frac{0.117612}{\omega^1} + \cos(\omega t) \left[ + \frac{0.0444442}{\omega^6} + \frac{0.0266483}{\omega^5} - \frac{0.0170313}{\omega^4} - \frac{0.0813875}{\omega^3} - \frac{0.132737}{\omega^2} \right]
\]
Chapter 4. Transient memristor model

\[- \frac{0.117612}{\omega} \]
\[+ \cos(2\omega t) \left\{ \begin{array}{c} - \frac{0.0259026}{\omega^6} - \frac{0.0152276}{\omega^5} + \frac{0.00851566}{\omega^4} + \frac{0.032555}{\omega^3} + \frac{0.0331842}{\omega^2} \\ + \frac{0.0115123}{\omega^6} + \frac{0.00571034}{\omega^5} - \frac{0.00243304}{\omega^4} - \frac{0.00542583}{\omega^3} \\ + \frac{0.00345368}{\omega^6} - \frac{0.00126897}{\omega^5} + \frac{0.000304131}{\omega^4} \\ + \frac{0.000627942}{\omega^6} + \frac{0.000126897}{\omega^5} \\ + \frac{0.0000523285}{\omega^6} \end{array} \right\} \]

The expression of (4.15) is dependent of the frequency and establishes that as \( \omega \) tends to infinity the solution \( x(t) \) approaches to the value of \( x_0 \). This behavior can be observed by simulating, separately, each one of the terms that constitute the symbolical solution \( x(t) \).

Figure 4.7 shows the behavior of the DC, the fundamental and the harmonics terms as \( \omega \) tends to infinity. The DC term tends to the value of 0.1 as \( \omega \) tends to infinity, as shown in Figure 4.7a. The fundamental and the harmonic terms tends to zero as \( \omega \) tends to infinity, as shown in Figures 4.7a and 4.7b. Therefore, the DC term is the dominant term in accordance \( \omega \) tends to infinity. In general can be concluded that as \( \omega \) tends to infinity, the symbolical solution \( x(t) \) approaches to the value of \( x_0 \).

The symbolical memristance \( M(x(t)) \) of (4.14) can be simplified as
4.2. Homotopy-based model

\[ M(x(t)) = 14410 + \frac{384.395}{\omega^6} + \frac{254.225}{\omega^5} - \frac{169.249}{\omega^4} - \frac{862.707}{\omega^3} - \frac{1582.89}{\omega^2} - \frac{1870.03}{\omega} + \cos(\omega t) \left[ -\frac{658.963}{\omega^6} - \frac{423.708}{\omega^5} + \frac{270.798}{\omega^4} + \frac{1294.06}{\omega^3} + \frac{2110.52}{\omega^2} \right] + \frac{1870.03}{\omega} \]

\[ + \cos(2\omega t) \left[ +\frac{411.852}{\omega^6} + \frac{242.119}{\omega^5} - \frac{135.399}{\omega^4} - \frac{517.624}{\omega^3} - \frac{527.629}{\omega^2} \right] \]

\[ + \cos(3\omega t) \left[ -\frac{183.045}{\omega^6} - \frac{90.7945}{\omega^5} + \frac{38.6854}{\omega^4} + \frac{86.2707}{\omega^3} \right] \]

\[ + \cos(4\omega t) \left[ +\frac{54.9136}{\omega^6} + \frac{20.1765}{\omega^5} - \frac{4.83568}{\omega^4} \right] \]

\[ + \cos(5\omega t) \left[ -\frac{9.98428}{\omega^6} - \frac{2.01765}{\omega^5} \right] \]

\[ + \cos(6\omega t) \left[ +\frac{0.832024}{\omega^6} \right] \] (4.16)

The expression of (4.16) establishes that as \( \omega \) tends to infinity the memristance \( M(x(t)) \) approaches to the following expression

\[ M(x(t))_{\omega \to \infty} = R_{ON}x_0 + \alpha R_{ON}(1 - x_0) \] (4.17)

This behavior can be observed by simulating, separately, each one of the terms that constitute the symbolical memristance \( M(x(t)) \).

![Figure 4.8: Symbolical memristance \( M \) using different \( \omega \) values](image)

Figure 4.8 shows the behavior of the DC, the fundamental and the harmonics terms as \( \omega \) tends to infinity. The DC term tends to the value of 14.41 kΩ as \( \omega \) tends to infinity, as
shown in Figure 4.8a. The fundamental and the harmonic terms tends to zero as $\omega$ tends to infinity, as shown in the figures 4.8a and 4.8b. Therefore, the DC term is the dominant term in accordance $\omega$ tends to infinity. In general can be concluded that as $\omega$ tends to infinity, the symbolic memristance $M(x(t))$ is dependent on the variables $\alpha$, $R_{ON}$ and $x_0$.

### 4.2.5 Parameter variation

In this part of the analysis, the impact of the variation of the parameters: current amplitude $A$, the window function coefficient $a$, the resistive factor $\alpha$ and the initial width $x_0$ is studied with the purpose of finding the solution $x(t)$ from HPM that approaches to the solution $x^*(t)$ using the RK4 integration method in order to achieve the widest memristance range. The RMSE value is used to measure the differences between the solutions $x(t)$ and $x^*(t)$.

The parameters are replaced with the following values: $x_0=0.1$, $a=3$, $A=400 \times 10^{-7}$, $\mu=1 \times 10^{-14}$, $R_{ON}=100$, $\alpha=160$ and $D=10 \times 10^{-9}$. In the case of the parameters are not varied remain with the starting values.

**Current Amplitude ($A$)**

The current amplitude ($A$) is varied for the following values (in $\mu$A):

<table>
<thead>
<tr>
<th>$A$</th>
<th>RMSE</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>0.000278065</td>
</tr>
<tr>
<td>20</td>
<td>0.000787793</td>
</tr>
<tr>
<td>30</td>
<td>0.003571840</td>
</tr>
<tr>
<td>40</td>
<td>0.008607500</td>
</tr>
<tr>
<td>50</td>
<td>0.034329900</td>
</tr>
<tr>
<td>60</td>
<td>0.250248000</td>
</tr>
<tr>
<td>70</td>
<td>0.896945000</td>
</tr>
<tr>
<td>80</td>
<td>2.381120000</td>
</tr>
<tr>
<td>90</td>
<td>5.315490000</td>
</tr>
<tr>
<td>100</td>
<td>10.57850000</td>
</tr>
</tbody>
</table>

The current amplitude $A$ values with the corresponding RMSE values are shown in Table 4.2. The behavior of the data shows that the maximum value of the current amplitude, before the RMSE value increases considerably, is located in the range from 40$\mu$A to 50$\mu$A.

**Table 4.2: RMSE values for the variation of the current amplitude $A$**

<table>
<thead>
<tr>
<th>$A$</th>
<th>RMSE</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>0.000278065</td>
</tr>
<tr>
<td>20</td>
<td>0.000787793</td>
</tr>
<tr>
<td>30</td>
<td>0.003571840</td>
</tr>
<tr>
<td>40</td>
<td>0.008607500</td>
</tr>
<tr>
<td>50</td>
<td>0.034329900</td>
</tr>
</tbody>
</table>

The value of the parameter $A$ impacts, significantly, the range of memristance in the memristor because it modifies the value of the state variable $x(t)$; i.e., as the current amplitude increases the range of the state variable increases and therefore the range of memristance increases too.
4.2. Homotopy-based model

Figure 4.9: Analysis of $x(t)$ using different values of current amplitude.

Figure 4.9 shows the differences between the solutions $x(t)$ from the HPM procedure (blue line) and the RK4 integration method (red line). These series of frames confirm the range of acceptable current amplitude and also establish that as the value of the parameter $A$ increases above 50$\mu$A the curve of the variable $x(t)$ is deformed to achieve physical values not allowed.

The problems caused by the use of physical values not allowed are shown in Figure 4.10. The principal drawback is located in the $v$-$i$ characteristic curve. According to the
fundamental properties of the memristive systems is impossible to obtain the performance of the curve in the enclosed area -black arrows-, as shown in Figure 4.10. Moreover, the $M-i$ characteristic curve reaches the maximum values of memristance above the physical limits allowed.

![Figure 4.10: M-i and v-i characteristic using not possible value of parameter $A$.](image)

As it can be seen, the pinched hysteresis loop and the range of memristance suffer disturbances in particular areas. These areas correspond to phenomena unrelated to the behavior of the memristor. Therefore, the curves shown in Figures 4.10a and 4.10b do not represent the performance of the memristive system.

**Window function coefficient ($a$)**

The equation of the window function has the form

$$f(x(t)) = a[x(t)]^5 - 2a[x(t)]^3 + ax(t)$$  \hspace{1cm} (4.18)

where $a$ is called the window function coefficient.

The window function coefficient is used for modifying proportionally the behavior of the window function. The range of operation for the window function can be established as

$$1 \geq f(x(t)) \geq 0$$

$$1 \geq x(t) \geq 0$$  \hspace{1cm} (4.19)

According to (4.18) and (4.19) the maximum value for the window function coefficient $a$ is 3.55.

The window function coefficient ($a$) is varied for the following values:
4.2. Homotopy-based model

The values of the window function coefficient $a$ with the corresponding RMSE values are shown in Table 4.3. The behavior of the data establishes that as the window function coefficient increases, the RMSE increases too.

Table 4.3: RMSE values for the variation of the window function coefficient $a$

<table>
<thead>
<tr>
<th>$a$</th>
<th>RMSE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.000409124</td>
</tr>
<tr>
<td>1.5</td>
<td>0.000787793</td>
</tr>
<tr>
<td>2</td>
<td>0.002062800</td>
</tr>
<tr>
<td>2.5</td>
<td>0.005648360</td>
</tr>
<tr>
<td>3</td>
<td>0.008607500</td>
</tr>
<tr>
<td>3.5</td>
<td>0.012122600</td>
</tr>
</tbody>
</table>

According to (4.8), the window function coefficient adjusts the amount of current across the memristor and therefore modifies the value of the state variable $x(t)$.

Figure 4.11: Analysis of window function coefficient using different values.

Figure 4.11 shows the differences between the solutions $x(t)$ from the HPM procedure (blue line) and the RK4 integration method (red line). The maximum value of the state variable $x(t)$ is located for a window function coefficient $a$ of 3.5. However, the value of 3.5 presents the maximum RMSE value, as shown in Figure 4.12.

The reason that the value of 3.5 causes the maximum RMSE is the presence of the disturbance at the top of the solution $x(t)$ from the HPM procedure, as shown in Figure
4.11f. The appropriate window function coefficient is one that approaches the solution \( x(t) \) to the unity value for achieving the widest memristance range.

According to Figures 4.11 and 4.12 the widest memristance range is caused by a window function coefficient value of 3.3. The value of 3.3 has the same amount of RMSE that a value of 2.7 as shown in Figure 4.12.

![Figure 4.12: RMSE using different window function coefficient values](image)

The consequences of varying the parameter \( a \) can be observed in the \( v-i \) and \( M-i \) characteristic curves. The lobe area of the pinched hysteresis loop and the range of memristance increase as the value of the window function coefficient increases, as shown in Figure 4.13.

![Figure 4.13: \( M-i \) and \( v-i \) characteristic curves using different values of parameter \( a \).](image)
4.2. Homotopy-based model

**Resistive factor (α)**

The resistive factor \( α \) establishes the resistive ratio.

\[
α = \frac{R_{OFF}}{R_{ON}} \tag{4.20}
\]

The fixed value of \( R_{ON} \) causes that \( R_{OFF} \) assumes the unique value according to (4.20). The resistive factor \( α \) is varied for the following values:

\[
\begin{array}{cccccccc}
100 & 120 & 140 & 160 & 180 & 200 & 220 \\
\end{array}
\]

The values of the resistive factor \( α \) with the corresponding \( M_{Max} \), \( M_{Min} \) and \( M_{ω→∞} \) values are shown in Table 4.4. The variations of the parameter \( α \) does not lead to changes for the solution \( x(t) \).

<table>
<thead>
<tr>
<th>( α )</th>
<th>( M_{Max} )</th>
<th>( M_{Min} )</th>
<th>( M_{ω→∞} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>9010</td>
<td>3653</td>
<td>9010</td>
</tr>
<tr>
<td>120</td>
<td>10810</td>
<td>4370</td>
<td>10810</td>
</tr>
<tr>
<td>140</td>
<td>12610</td>
<td>5088</td>
<td>12610</td>
</tr>
<tr>
<td>160</td>
<td>14410</td>
<td>5806</td>
<td>14410</td>
</tr>
<tr>
<td>180</td>
<td>16210</td>
<td>6524</td>
<td>16210</td>
</tr>
<tr>
<td>200</td>
<td>18010</td>
<td>7241</td>
<td>18010</td>
</tr>
<tr>
<td>220</td>
<td>19810</td>
<td>7959</td>
<td>19810</td>
</tr>
</tbody>
</table>

This behavior is caused because the resistive factor is not related to the state variable of (4.8). The mathematical expression of (4.17) establishes that the resistive factor affects the maximum and minimum values of memristance.

**Initial width (\( x_0 \))**

The initial width \( (x_0) \) is varied for the following values:

\[
\begin{array}{cccccccc}
0.1 & 0.2 & 0.3 & 0.4 & 0.5 & 0.6 & 0.7 & 0.8 & 0.9 \\
\end{array}
\]

The behavior of the data establishes that as the parameter \( x_0 \) increases, the low value of the state variable increases and therefore the range of the solution \( x(t) \) is reduced. This reduction in the range of the solution \( x(t) \) causes that the range of memristance is reduced considerably.
4.2.6 Characteristic of the memristor model

The HPM memristor model is established using the expression of (4.14). This memristor model is evaluated for discrete values of the frequency at $\omega = 1, 2, 10$, and the corresponding hysteresis loops are shown in Figure 4.14. It possesses the main fingerprints of a passive memristor, such as: pinched hysteresis loop, hysteresis lobe area and shrunken hysteresis loop. The curves have been obtained for $x_0=0.1, a=3, A=400\times10^{-7}, \mu=1\times10^{-14}, R_{ON}=100, R_{OFF}=16\Omega$ and $D=10\times10^{-9}$.

![Hysteresis loops of the memristor model](image)

Figure 4.14: Hysteresis loops of the memristor model

Moreover, the waveform of the memristance is shown in Figure 4.15.

![Memristance of the memristor model](image)

Figure 4.15: Memristance of the memristor model
4.3 Discussion

The conventional memristor models [4, 5] use mathematical expressions in order to simulate the behavior of the memristive systems. These models present the principal drawback of requiring a numerical integration method to solve the system of equations. The necessity of using a large amount of memristors causes problems in the execution speed of the computer programs. Therefore, this part of the thesis proposes the use of behavioral modeling of the memristor as alternative path for obtaining the memristive characteristic.

The polynomial model of the memristor is based on the approximation of the \( q-\varphi \) curve by using the polynomial function. This function uses the \( R_{ON} \) and \( R_{OFF} \) parameters to bound the range of the memristance in the device. However, this model uses the theoretical conception of the memristive behavior in order to include the memristor in the simulation procedure; i.e. the polynomial approximation of the memristive characteristic does not use the physical parameters to adjust the behavior and the boundary conditions of the device. Thus, the polynomial model is useful to carry out new studies in circuits with conventional elements in order to investigate the response of the systems with the insertion of the memristor.

The novel HPM memristor model is based on the full-symbolical expression of the memristive behavior using the physical parameters of the HP memristor. This feature represents the principal advantage with respect to the numerical integration methods. The numerical integration methods present errors as the time-variable increases, called local truncation error and total accumulated error [6]. These errors do not occur in the new memristor model because the numerical integration method is not necessary to display the characteristic curves of the memristive behavior. Moreover, the expression of the HPM memristor model is composed of terms classified as fundamental and harmonic elements. This feature provides a particular vision to understand the collapse of the \( v-i \) characteristic, the state variable and the memristance curve as frequency approaches infinity.

The summary of the characteristics of the polynomial memristor model and the HPM memristor model is exposed in Table 4.5. This summary is based on the following characteristics: memristive values, parameters of control, number of terms and the characteristic curves of the \( v-i \), memristance and state-variable. Firstly, the memristive values consist of establishing the values of the parameters in the memristor model in order to display memristive behavior. Then, parameters of control mention the parameters used in the mathematical expression of the model. After that, number of terms specifies the amount of elements that constitutes the mathematical approximation of the model. Finally, the characteristic curves of the memristive behavior are incorporated into the summary of the
memristor models.

Table 4.5: Summary of the characteristics of the memristor models

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Polynomial memristor model</th>
<th>HPM memristor model</th>
</tr>
</thead>
<tbody>
<tr>
<td>memristive behavior</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>parameters of control</td>
<td></td>
<td></td>
</tr>
<tr>
<td>number of terms</td>
<td>2</td>
<td>7</td>
</tr>
<tr>
<td>v-i characteristic curve</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>M characteristic curve</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

The classical figure of performance for memristor models shows the pinched hysteresis loop in the $v$-$i$ characteristic curve. The novel HPM memristor model presents the classical figure of performance and also shows the state variable $w$ and the memristance $M$ characteristic curves in order to ensure the memristive behavior of the device. Besides, the memristive characteristic curves tends to be a straight line as the frequency approaches infinity.

However, the HPM memristor model operates in a bounded range. The range of usefulness is established by comparing the response of the HPM memristor model and the response from the RK4 integration method. This range is set out in Table B.6 and ensures that the RMSE value is less than 1% with respect to the numerical integration method. Finally, the HPM memristor model presents two principal drawback: the range of usefulness and the inability of incorporate the phenomenon of the state variable’s drift speed as $w$ approaches to the boundaries. These disadvantages are caused by HPM procedure problems.
Bibliography


Chapter 5

Circuit applications

The incorporation of the memristor in the simulation procedure represents a new vision for generating novel types of circuits and systems. Moreover, the new fundamental circuit element breaks the arbitrary restriction of electronic circuit theory to linear systems. This chapter describes the use of the HPM and polynomial memristor models in different types of applications, such as: negative feedback amplifiers, opamp-based circuits and mem-elements emulator circuits.

5.1 Nullor-based examples

The nullor is a two-port singular element used in the structured design methodology for the design of amplifier circuits [1, 2]. This electric component is composed of a nullator (input port) and a norator (output port), as shown in the Figure 5.1.

\[ i_i = 0 \quad v_i = 0 \]

The values of current and voltage of the nullator are by definition zero

\[ i_o \quad v_o \]

The values of current and voltage of the norator can be arbitrary
There are many forms to describe a nullor, but the most convenient one is the chain matrix $K$, because we are focused on its amplification properties. This matrix has the form

$$K = \begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}$$

which establishes the following definitions of transfer functions:

$$A = \left. \frac{u_i}{u_o} \right|_{i_o=0} = 0 \quad B = \left. \frac{u_i}{i_o} \right|_{u_o=0} = 0$$

$$C = \left. \frac{i_i}{u_o} \right|_{i_o=0} = 0 \quad D = \left. \frac{i_i}{i_o} \right|_{u_o=0} = 0$$

(5.1)

Therefore, the nullor possesses infinite-gains for all four basic amplifiers, i.e. the nullor represents the ideal infinite gain plant to be controlled by the feedback network which is usually constituted by passive components. This description yields the asymptotic-gain model of negative-feedback amplifiers [2, 3], as shown in Figure 5.2.

In this way, the four types of amplifiers can be obtained when a passive feedback network is connected with the nullor in a single negative-feedback loop [1, 4] as shown in Figure 5.3.

The ideal closed-loop gains for the negative-feedback amplifiers above are given as
5.1. Nullor-based examples

\begin{align*}
A_V &= 1 + \frac{R_2}{R_1} & A_G &= -G \\
A_R &= -R & A_I &= 1 + \frac{R_2}{R_1}
\end{align*}

(5.2)

where $A_V$, $A_G$, $A_R$ and $A_I$ are the voltage, transconductance, transresistance and current gains, respectively.

The existence of the memristor opens the possibility for introducing a novel family of memristive transfer functions that are obtained by substituting the resistors of the passive feedback network by memristors. The resulting configurations are shown in Figure 5.4.

Besides, depending on the selection made of the components of the feedback network, a specific member of the family emerges, as listed in Table 5.1.

In order to demonstrate the feasibility of achieving a memristive transfer function, the nullor part of the amplifiers is implemented by appropriated active devices. In this thesis, two different nullor implementations are carried out: MOS-realization and Memistor*-realization.

*The attentive reader should notice the word memistor. It is not a mistake, it is a 3-terminal device different from the memristor.
The MOS implementation

The MOS in common-source (CS) configuration is used for implementing the nullor since this configuration has the best approximation to small entries in the chain matrix $\mathbf{K}$. The nullor implemented by a first-order small-signal model of the CS-stage is shown in Figure 5.5.

The chain matrix $\mathbf{K}$ is given as

$$
\mathbf{K}_{CS} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \left(-\frac{g_m}{g_{ds}}\right)^{-1} & (-g_m)^{-1} \\ 0 & 0 \end{bmatrix}
$$

where $g_m$ is the transconductance and $g_{ds}$ is the drain-source conductance.

Because no capacitors are included in the model, the maximum possible stage gain is

Table 5.1: Family of Trans-memristive Amplifiers

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Feedback network</th>
<th>Member</th>
</tr>
</thead>
<tbody>
<tr>
<td>voltage</td>
<td>$M_1 - M_2$</td>
<td>pure transmem-voltage amplifier</td>
</tr>
<tr>
<td>$M_1 - R_2$</td>
<td>transmem-voltage amplifier type I</td>
<td></td>
</tr>
<tr>
<td>$R_1 - M_2$</td>
<td>transmem-voltage amplifier type II</td>
<td></td>
</tr>
<tr>
<td>transconductance</td>
<td>$W$</td>
<td>transmem-conductance amplifier</td>
</tr>
<tr>
<td>transresistance</td>
<td>$M$</td>
<td>transmem-resistance amplifier</td>
</tr>
<tr>
<td>current</td>
<td>$M_1 - M_2$</td>
<td>pure transmem-current amplifier</td>
</tr>
<tr>
<td>$M_1 - R_2$</td>
<td>transmem-current amplifier type I</td>
<td></td>
</tr>
<tr>
<td>$R_1 - M_2$</td>
<td>transmem-current amplifier type II</td>
<td></td>
</tr>
</tbody>
</table>
5.1. Nullor-based examples

Figure 5.5: Nullor synthesis by MOS-equivalent

given as \( \frac{g_m}{g_{ds}} \) [5], which is also refereed as the DC-gain expressed usually as:

\[
\text{DC-gain(dBs)} = 20 \log \left( \frac{g_m}{g_{ds}} \right)
\]  

(5.4)

In this thesis, the single MOS-stage is resorted in order to carry out the methodology of the structured electronic design. This method [1] assumes that it is possible to design analog circuits in a well-defined way and therefore the best performing circuits are found.

**Memistor characterization**

Another way of implementing the nullor with an active device is by using a memistor. The memistor is a three-terminal device in which the current entering in the control terminal modulates the resistance between the other two terminals [6, 7]. The memistor can be obtained by a back-to-back series connection of two memristors, as shown in Figure 5.6.

In fact, the memristor is the ‘fundamental element’ while the memistor is the ‘derived circuit element’. By implementing the nullor with the memistor, fully-memristor versions of the trans-memristive amplifiers can be obtained.

Hereafter, the HPM and polynomial memristor models are used to carry out the circuit-level simulation of the trans-memresistance and trans-memconductance amplifiers.
5.1.1 Trans-memresistance amplifier

5.1.1.1 Nullor-based design

The circuit shown in Figure 5.7 represents the trans-memresistance amplifier using the nullor as the plant to be controlled. This negative-feedback amplifier is simulated by using the polynomial and HPM memristor models.

![Figure 5.7: Trans-memresistance amplifier with nullor](image)

where $i_i = A \sin \omega t$, $A = 40 \mu A$, $R_L = 1 \Omega$ and $M$ is characterized by the parameter values of the memristor model.

### Polynomial model

The polynomial memristor model is characterized by the parameter values shown in Table 5.2. The memristor model is incorporated in the feedback loop of the amplifier, as shown in Figure 5.7. This circuit is simulated in order to examine the behavior of the output variable and the transfer ratio of the amplifier.

**Table 5.2: $M$ parameter values using polynomial memristor model**

<table>
<thead>
<tr>
<th>$M$ (Ω)</th>
<th>$M_{min}$</th>
<th>$M_{max}$</th>
<th>$\alpha$</th>
<th>$M(\omega \rightarrow \infty)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M$</td>
<td>16000-100</td>
<td>100Ω</td>
<td>1600Ω</td>
<td>160</td>
</tr>
</tbody>
</table>

**Results**

The simulation result of the output voltage $u_o(t)$ of the amplifier for two discrete values of the frequency $\omega = 1, 10$ is shown in Figure 5.8. Besides, in order to gain insight on the dynamics of the amplifier, simulations were also carried out by substituting the memristor
$M$ for linear resistors having the minimum and maximum memristance values that the memristor can reach, namely $M_{\text{min}}$ and $M_{\text{max}}$ respectively.

![Figure 5.8: $u_o(t)$ curves for the trans-memresistance amplifier with nullor using polynomial memristor model](image)

The corresponding curves shown in Figure 5.8 denote $u_o$ with the memristor by the red lines, and the black lines are associated to the simulations with $M_{\text{min}}$ and $M_{\text{max}}$. Clearly it can be noticed that the $u_o$ curve jumps from the lower to the upper limits at low-frequency and it sticks to the upper limit at high frequencies, i.e. the amplifier reaches the maximum trans-memresistance value. The label $\times 10^{-2}$ means that the curve of $M_{\text{min}}$ has been increased one hundred times of the original value in order to be displayed.

![Figure 5.9: Transmem-resistance $i_i$-$u_o$ hysteresis with nullor using polynomial memristor model](image)

Another result of the simulations is the transmission curves ($\frac{u_o}{i_i}$) of the amplifier for the same frequency values that are shown in Figure 5.8. The memristive transresistance ratio ($\frac{u_o}{i_i}$) shows the typical eight-shape of the memristor hysteresis, tending to a straight-line at high frequencies, as shown in Figure 5.9. Table 5.3 shows the breakdown of the memristive transresistance ratio by reducing the memristive range as the frequency increases.
Table 5.3: Memristive transresistance ratio using different frequency values

<table>
<thead>
<tr>
<th>$\omega$</th>
<th>$\frac{u_i}{v_i}(\text{K}\Omega)$</th>
<th>$\omega$</th>
<th>$\frac{u_i}{v_i}(\text{K}\Omega)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>16-0.010</td>
<td>6</td>
<td>16-13.35</td>
</tr>
<tr>
<td>2</td>
<td>16-8.050</td>
<td>7</td>
<td>16-13.72</td>
</tr>
<tr>
<td>3</td>
<td>16-10.70</td>
<td>8</td>
<td>16-14.01</td>
</tr>
<tr>
<td>4</td>
<td>16-12.02</td>
<td>9</td>
<td>16-14.23</td>
</tr>
<tr>
<td>5</td>
<td>16-12.82</td>
<td>10</td>
<td>16-14.41</td>
</tr>
</tbody>
</table>

HPM model

The HPM memristor model is characterized by the parameter values shown in Table 5.4. Now, the circuit shown in Figure 5.7 is performed by using the HPM memristor model. This circuit is simulated in order to examine the behavior of the output variable and the transfer ratio of the amplifier.

Table 5.4: $M$ parameter values using HPM memristor model

<table>
<thead>
<tr>
<th>$M(\Omega)$</th>
<th>$x_0$</th>
<th>$a$</th>
<th>$A$</th>
<th>$\alpha$</th>
<th>$M_{\text{min}}$</th>
<th>$M_{\text{max}}$</th>
<th>$M(\omega \to \infty)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M$</td>
<td>14410-5806</td>
<td>0.1</td>
<td>3</td>
<td>$40\mu A$</td>
<td>160</td>
<td>5806$\Omega$</td>
<td>14410$\Omega$</td>
</tr>
</tbody>
</table>

Results

The simulation result of the output voltage $u_o(t)$ of the amplifier for two discrete values of the frequency $\omega = 1, 10$ is shown in Figure 5.10.

Figure 5.10: $u_o(t)$ curves for the trans-memresistance amplifier with nullor using HPM memristor model

In this case, the corresponding curves shown in Figure 5.10 denote $u_o$ with the memristor by the blue lines, and the black lines are associated to the simulations with the $M_{\text{min}}$ and the $M_{\text{max}}$ reached by the memristor.
5.1. Nullor-based examples

Figure 5.11: Transmem-resistance $i_r-u_o$ hysteresis with nullor using HPM memristor model

The transmission curves ($u_o/i_i$) of the amplifier are shown in Figure 5.11. Table 5.5 shows the behavior of the trans-memresistance values as the frequency increases.

Table 5.5: Memristive transresistance ratio using different frequency values

<table>
<thead>
<tr>
<th>$\omega$</th>
<th>$\frac{u_o}{i_i}$ (KΩ)</th>
<th>$\omega$</th>
<th>$\frac{u_o}{i_i}$ (KΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>14.41-5.806</td>
<td>6</td>
<td>14.41-13.65</td>
</tr>
<tr>
<td>2</td>
<td>14.41-11.15</td>
<td>7</td>
<td>14.41-13.78</td>
</tr>
<tr>
<td>3</td>
<td>14.41-12.59</td>
<td>8</td>
<td>14.41-13.87</td>
</tr>
</tbody>
</table>
5.1.1.2 MOS-based design

The circuit shown in Figure 5.12 represents the trans-memresistance amplifier using the nullor implementation of the MOS in common-source configuration. This implementation is simulated by using the polynomial and HPM memristor models.

![Memristor Circuit Diagram](image)

Figure 5.12: Trans-memresistance amplifier with MOS-equivalent

The values of the amplifier are: \( i_i = A \sin \omega t, \ A = 40 \mu A, \ R_L = 1 \Omega, \ g_m = 320 \frac{\mu A}{V}, \ g_{ds} = 320 \text{nS} \) and \( M \) is characterized by the parameter values of the memristor model.

### Polynomial model

The polynomial memristor model is characterized by the parameter values shown in Table 5.2. By following the same procedure as in the previous implementation, the circuit of Figure 5.12 is simulated.

### Results

![Voltage-Time Graphs](image)

Figure 5.13: \( u_o(t) \) curves for the trans-memresistance amplifier with MOS-equivalent using polynomial memristor model
The simulation result of the output voltage $u_o(t)$ are shown in Figure 5.13. In low-frequency, the trans-memresistance amplifier displays a negative trans-memresistance region. This region is related to the performance of the equation that governs the trans-memresistance amplifier. Note that, the negative trans-memresistance values disappear as the frequency tends to infinity because of the range of memristance is reduced.

![Graph](image)

Figure 5.14: Transmem-resistance $i_i-u_o$ hysteresis with MOS-equivalent using polynomial memristor model

For this implementation, the resulting $i_i-u_o$ hysteresis loops (in black) and the hysteresis loops of the memristor (in red) are shown in Figure 5.14.

It clearly result that the trans-memresistance is smaller than the memresistance at the feedback, which can be explained by the fact that the implemented nullor does not have zeroes in its chain matrix. Table 5.6 shows the memristive transresistance ratio with the MOS-equivalent as the frequency increases.

<table>
<thead>
<tr>
<th>$\omega$ (KΩ)</th>
<th>$\omega_M$ (KΩ)</th>
<th>$\omega_i$ (KΩ)</th>
<th>$\omega$ (KΩ)</th>
<th>$\omega_M$ (KΩ)</th>
<th>$\omega_i$ (KΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 16-0.010</td>
<td>12.86-3.021</td>
<td>6 16-13.35</td>
<td>12.86-10.21</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 16-8.050</td>
<td>12.86-4.920</td>
<td>7 16-13.72</td>
<td>12.86-10.59</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3 16-10.70</td>
<td>12.86-7.567</td>
<td>8 16-14.01</td>
<td>12.86-10.87</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4 16-12.02</td>
<td>12.86-8.891</td>
<td>9 16-14.23</td>
<td>12.86-11.09</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5 16-12.82</td>
<td>12.86-9.685</td>
<td>10 16-14.41</td>
<td>12.86-11.27</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Effect of the DC-gain**

In this part, further analysis of the amplifier is achieved for several values of the DC-gain. This important parameter expresses how closer the MOS-model is to the nullor. Because the DC-gain depends on $g_{ds}$ and $g_m$, separate analysis are carried out by varying $g_{ds}$ and $g_m$. 

97
Analysis I: Effect of $g_{ds}$

In this analysis, the output conductance $g_{ds}$ is varied while the transconductance $g_m$ remains fixed. The trans-memresistance $i_i - u_o$ hystereses are shown in Figure 5.15 for DC-gain values of 60dB, 40dB and 20dB.

![Figure 5.15: Transmission curves for Analysis I.](image)

Another form of looking at the simulation results is recast in Table 5.7. Herein, the values associated to $g_{ds}$ in order to produce the DC-gain values above yield a limit trans-memresistance value at $\omega = \infty$, that is to say high frequencies. Decreasing the DC-gain (increasing $g_{ds}$) causes a small reduction in this limit.

<table>
<thead>
<tr>
<th>DC-gain (dB)</th>
<th>$g_m \left(10^{-6} \text{A} \right)$</th>
<th>$g_{ds}(\bar{b})$</th>
<th>$\frac{g_m}{\omega}(\text{k}\Omega)$ for $\omega = \infty$</th>
</tr>
</thead>
<tbody>
<tr>
<td>60</td>
<td>320</td>
<td>$320 \times 10^{-9}$</td>
<td>12.86</td>
</tr>
<tr>
<td>40</td>
<td>320</td>
<td>$320 \times 10^{-8}$</td>
<td>12.74</td>
</tr>
<tr>
<td>20</td>
<td>320</td>
<td>$320 \times 10^{-7}$</td>
<td>11.70</td>
</tr>
</tbody>
</table>
Analysis II: Effect of $g_m$

In this analysis, $g_m$ is varied while $g_{ds}$ is fixed. The resulting trans-memresistance $i_t-u_o$ hystereses are shown in Figure 5.16 for the same DC-gain values of the previous analysis.

![Figure 5.16: Transmission curves for Analysis II.](image)

The summary of the effect of $g_m$ is shown in Table 5.8. Now, the values associated to $g_m$ produce a limit trans-memresistance value at $\omega=\infty$. Note that, the variation of $g_m$ causes negative trans-memresistance values even though the frequency tends to infinity.

<table>
<thead>
<tr>
<th>DC-gain (dB)</th>
<th>$g_m$</th>
<th>$g_{ds}(10^{-5}) \Omega$</th>
<th>$\frac{2\pi}{\omega_i}(k\Omega)$</th>
<th>$\omega = \infty$</th>
</tr>
</thead>
<tbody>
<tr>
<td>60</td>
<td>$320 \times 10^{-6}$</td>
<td>320</td>
<td>12.86</td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>$320 \times 10^{-7}$</td>
<td>320</td>
<td>-15.09</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>$320 \times 10^{-8}$</td>
<td>320</td>
<td>-269.5</td>
<td></td>
</tr>
</tbody>
</table>

HPM model

The HPM memristor model is characterized by the parameter values shown in Table 5.4. By following the same procedure as in the previous implementation, the circuit of Figure 5.12 is simulated in order to examine the behavior of the output variable and the transfer ratio of the amplifier.

Results

The simulation result of the output voltage $u_o(t)$ of the amplifier for two discrete values of the frequency $\omega = 1, 10$ is shown in Figure 5.17. For this implementation, the resulting $i_t-u_o$ hysteresis loops (in black) and the hysteresis loops of the memristor (in blue) are shown in Figure 5.18.
Figure 5.17: $u_o(t)$ curves for the trans-memresistance amplifier with MOS-equivalent using HPM memristor model

Figure 5.18: Transmem-resistance $i_t-u_o$ hysteresis with MOS-equivalent using HPM memristor model

Table 5.9: Memristive transresistance ratio using different frequency values

<table>
<thead>
<tr>
<th>$\omega$</th>
<th>$M$(KΩ)</th>
<th>$\frac{u_o}{i_t}$(KΩ)</th>
<th>$\omega$</th>
<th>$M$(KΩ)</th>
<th>$\frac{u_o}{i_t}$(KΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>14.41-5.806</td>
<td>11.27-2.678</td>
<td>6</td>
<td>14.41-13.65</td>
<td>11.27-10.52</td>
</tr>
</tbody>
</table>

Note that, the negative trans-memresistance values are not present by using the HPM memristor. Table 5.9 shows the memristive transresistance ratio with the MOS-equivalent as the frequency increases.
Effect of the DC-gain

The analysis of the amplifier is achieved for several values of the DC-gain. Because the DC-gain depends on \( g_{ds} \) and \( g_m \), separate analysis are carried out by varying \( g_{ds} \) and \( g_m \).

Analysis I: Effect of \( g_{ds} \)

The conductance \( g_{ds} \) is varied while the transconductance \( g_m \) remains fixed.

![Transmission curves for Analysis I](image)

Figure 5.19: Transmission curves for Analysis I.

The trans-memresistance \( i_i-u_o \) hystereses are shown in Figure 5.19 for DC-gain values of 60dB, 40dB and 20dB.

Table 5.10: Summary of Analysis I

| DC-gain (dB) | \( g_m \times 10^7 \) | \( g_{ds}(10^{-8})\) | \( \frac{Z_{mR}}{|\omega|} \) for \( \omega = \infty \) |
|--------------|-----------------|-----------------|-----------------|
| 60 | 320×10^{-6} | 320 | 11.27 |
| 40 | 320×10^{-7} | 320 | 11.17 |
| 20 | 320×10^{-8} | 320 | 10.25 |

In Table 5.10, the values associated to \( g_{ds} \) in order to produce the DC-gain values above yield a limit trans-memresistance value at \( \omega=\infty \), that is to say high frequencies. Decreasing the DC-gain (increasing \( g_{ds} \)) causes a small reduction in this limit.
Analysis II: Effect of \( g_m \)

In this analysis, \( g_m \) is varied while \( g_{ds} \) is fixed.

\[ \text{DC-gain (dB)} \quad g_m \quad g_{ds}(10^{-9}) \Omega \quad \frac{g_{ds}}{i_c}(k\Omega) \text{ for } \omega = \infty \]

<table>
<thead>
<tr>
<th>DC-gain (dB)</th>
<th>( g_m )</th>
<th>( g_{ds}(10^{-9}) \Omega )</th>
<th>( \frac{g_{ds}}{i_c}(k\Omega) \text{ for } \omega = \infty )</th>
</tr>
</thead>
<tbody>
<tr>
<td>60</td>
<td>( 320 \times 10^{-8} )</td>
<td>320</td>
<td>11.27</td>
</tr>
<tr>
<td>40</td>
<td>( 320 \times 10^{-7} )</td>
<td>320</td>
<td>-16.67</td>
</tr>
<tr>
<td>20</td>
<td>( 320 \times 10^{-8} )</td>
<td>320</td>
<td>-270.9</td>
</tr>
</tbody>
</table>

Note that, in spite of using the HPM memristor model, the variation of \( g_m \) causes negative trans-memresistance values even though the frequency tends to infinity.
5.1.3 Memistor-based design

The circuit shown in Figure 5.21 represents the trans-memresistance amplifier using the nullor implementation of the memistor. This implementation is simulated by using the polynomial and HPM memristor models.

![Trans-memresistance amplifier with Memistor realization](image)

where \( i_i = A \sin \omega t \), \( A = 40 \mu A \) and \( R_L = 1 \text{M} \Omega \). The memristor \( M \) and the memistor are characterized by the parameter values of the memristor model.

**Polynomial model**

The polynomial memristor model is characterized by the parameter values shown in Table 5.2. By following the same procedure as in the previous implementation, the circuit of Figure 5.21 is simulated.

**Results**

![u_o(t) curves for the trans-memresistance amplifier with Memistor realization using polynomial memristor model](image)
The simulation result of the output voltage $u_o(t)$ of the amplifier for two discrete values of the frequency $\omega = 1, 10$ is shown in Figure 5.22. For this implementation, the resulting $i_i-u_o$ hysteresis loops (in black) and the hysteresis loops of the memristor (in red) are shown in Figure 5.23.

![Figure 5.23: Transmem-resistance $i_i-u_o$ hysteresis (black) and memristor hysteresis (red) for Memistor realization using polynomial memristor model](image)

Table 5.12: Memristive transresistance ratio using different frequency values

<table>
<thead>
<tr>
<th>$\omega$</th>
<th>$M$(KΩ)</th>
<th>$\frac{u_o}{i_i}$(KΩ)</th>
<th>$\omega$</th>
<th>$M$(KΩ)</th>
<th>$\frac{u_o}{i_i}$(KΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>16-0.010</td>
<td>5.333-0.033</td>
<td>6</td>
<td>16-13.35</td>
<td>5.333-4.450</td>
</tr>
<tr>
<td>2</td>
<td>16-8.050</td>
<td>5.333-2.683</td>
<td>7</td>
<td>16-13.72</td>
<td>5.333-4.576</td>
</tr>
<tr>
<td>3</td>
<td>16-10.70</td>
<td>5.333-3.566</td>
<td>8</td>
<td>16-14.01</td>
<td>5.333-4.670</td>
</tr>
<tr>
<td>4</td>
<td>16-12.02</td>
<td>5.333-4.008</td>
<td>9</td>
<td>16-14.23</td>
<td>5.333-4.744</td>
</tr>
<tr>
<td>5</td>
<td>16-12.82</td>
<td>5.333-4.273</td>
<td>10</td>
<td>16-14.41</td>
<td>5.333-4.803</td>
</tr>
</tbody>
</table>

Table 5.12 shows the memristive transresistance ratio with the Memistor-realization as the frequency increases.

**HPM model**

The HPM memristor model is characterized by the parameter values shown in Table 5.4. By following the same procedure as in the previous implementation, the circuit of Figure 5.21 is simulated in order to examine the behavior of the output variable and the transfer ratio of the amplifier.

**Results**

The simulation result of the output voltage $u_o(t)$ of the amplifier for two discrete values of the frequency $\omega = 1, 10$ is shown in Figure 5.24.
5.1. Nullor-based examples

Figure 5.24: $u_o(t)$ curves for the trans-memresistance amplifier with Memistor realization using HPM memristor model

For this implementation, the resulting $i_{i-u_o}$ hysteresis loops (in black) and the hysteresis loops of the memristor (in blue) are shown in Figure 5.25. The trans-memresistance and the memresistance at the feedback remain the same behavior as the previous analysis using the polynomial memristor model.

Figure 5.25: Transmem-resistance $i_{i-u_o}$ hysteresis (black) and memristor hysteresis (blue) for Memistor realization using HPM memristor model

Table 5.13 shows the memristive transresistance ratio with the Memistor-realization as the frequency increases.
Table 5.13: Memristive transresistance ratio using different frequency values

<table>
<thead>
<tr>
<th>ω</th>
<th>$M(KΩ)$</th>
<th>$\frac{u_o}{u_i}(KΩ)$</th>
<th>ω</th>
<th>$M(KΩ)$</th>
<th>$\frac{u_o}{u_i}(KΩ)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>14.41-5.806</td>
<td>4.803-1.935</td>
<td>6</td>
<td>14.41-13.65</td>
<td>4.803-4.552</td>
</tr>
</tbody>
</table>

5.1.1.4 Conclusions

The feasibility of input-output characteristics that exhibit the typical memristive hysteresis has been proved by the analysis of the trans-memresistance amplifier amplifiers using the polynomial and the HPM memristor models. The simulation results show that the pinched hysteresis loop of the memristor has been transmitted to the input-output transfer characteristics which indicates a memristive behavior of the amplifier.

The nullor has been implemented in two forms, namely a MOS-realization and a novel Memistor-realization. On the one hand, the first implementation allow us to foresee that hybrid (MOS/memristor) circuits can be used for this type of application. On the other hand, the second implementation opens the possibility to obtain full-memristor realizations for these circuits. Besides, the results on the analysis of the effect of the DC-gain when the nullor is implemented by a MOS-stage are in concordance with the basic concepts of the design of nullor-based negative feedback amplifiers.

Table 5.14: Summary of data from the trans-memresistance amplifier using the polynomial memristor model

<table>
<thead>
<tr>
<th>Trans-memresistance amplifier</th>
<th>$M(KΩ)$ for $ω=∞$</th>
<th>$u_M(V)$</th>
<th>$\frac{u_o}{u_i}(KΩ)$ for $ω=1$</th>
<th>$\frac{u_o}{u_i}(KΩ)$ for $ω=∞$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nullor-based</td>
<td>16</td>
<td>0.61</td>
<td>16-0.100</td>
<td>16</td>
</tr>
<tr>
<td>MOS-equivalent</td>
<td>16</td>
<td>0.48</td>
<td>12.86-3.021</td>
<td>12.86</td>
</tr>
<tr>
<td>Memistor-implementation</td>
<td>16</td>
<td>0.20</td>
<td>5.33-0.033</td>
<td>5.33</td>
</tr>
</tbody>
</table>

Table 5.15: Summary of data from the trans-memresistance amplifier using the HPM memristor model

<table>
<thead>
<tr>
<th>Trans-memresistance amplifier</th>
<th>$M(KΩ)$ for $ω=∞$</th>
<th>$u_M(V)$</th>
<th>$\frac{u_o}{u_i}(KΩ)$ for $ω=1$</th>
<th>$\frac{u_o}{u_i}(KΩ)$ for $ω=∞$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nullor-based</td>
<td>14.41</td>
<td>0.57</td>
<td>14.41-5.806</td>
<td>14.41</td>
</tr>
<tr>
<td>MOS-equivalent</td>
<td>14.41</td>
<td>0.44</td>
<td>11.27-2.678</td>
<td>11.27</td>
</tr>
<tr>
<td>Memistor-implementation</td>
<td>14.41</td>
<td>0.19</td>
<td>4.803-1.935</td>
<td>4.803</td>
</tr>
</tbody>
</table>

The differences on the simulation results in the case of using Nullor-based, MOS-equivalent and Memistor-implementation in the trans-memresistance amplifier are recast in Table 5.14 and Table 5.15.
The information establishes that the active part of the trans-memresistance amplifier contributes significantly to the performance of the amplifier. The use of non-ideal blocks in the active part causes the value of the memristive transmission decreases as the frequency tends to infinity, i.e. the gain of the amplifier is reduced. Moreover, the memristive behavior of the transfer ratios has not disappeared in the case of MOS-implementation and Memistor-implementation which suggests the usefulness of the memristor as feedback element.
5.1.2 Trans-memconductance amplifier

5.1.2.1 Nullor-based design

The circuit shown in Figure 5.26 represents the trans-memconductance amplifier using the nullor as the plant to be controlled. This negative-feedback amplifier is simulated by using the polynomial and HPM memristor models.

\[ u_i = A \sin \omega t, \quad A=1 \text{V}, \quad R_L=1 \Omega \]

where \( u_i = A \sin \omega t \), \( A=1 \text{V} \), \( R_L=1 \Omega \) and \( W \) is characterized by the parameter values of the memristor model.

Polynomial model

The polynomial memristor model is characterized by the parameter values shown in Table 5.16.

<table>
<thead>
<tr>
<th>( W(10^{-4} \text{S}) )</th>
<th>( W_{\text{max}}(\text{S}) )</th>
<th>( W_{\text{min}}(\text{S}) )</th>
<th>( \alpha )</th>
<th>( W(\omega \to \infty)(\text{S}) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( W )</td>
<td>( 6.25\times10^{-4} )</td>
<td>( 1\times10^{-2} )</td>
<td>( 6.25\times10^{-5} )</td>
<td>160</td>
</tr>
</tbody>
</table>

The memristor model is incorporated in the feedback loop of the amplifier, as shown in Figure 5.26. This circuit is simulated in order to examine the behavior of the output variable and the transfer ratio of the amplifier.

Results

The simulation result of the output current \( i_o(t) \) of the amplifier for two discrete values of the frequency \( \omega = 1, 10 \) is shown in Figure 5.27.
Besides, in order to gain insight on the dynamics of the amplifier, simulations were also carried out by substituting the memristor \( W \) for linear conductances having the minimum and maximum memconductances values that the memristor can reach, namely \( W_{\text{min}} \) and \( W_{\text{max}} \) respectively.

The corresponding curves shown in Figure 5.27 denote \( i_o \) with the memristor by the red lines, and the black lines are associated to the simulations with \( W_{\text{min}} \) and \( W_{\text{max}} \). Clearly it can be noticed that the \( i_o \) curve jumps from the lower to the upper limits at low-frequency and it sticks to the lower limit at high frequencies, i.e. the amplifier reaches the minimum trans-memconductance value. The label \( \times 10 \) means that the curve of \( W_{\text{max}} \) has been reduced to one tenth of the original value in order to be displayed.

Another results of the simulations are the transmission curves \( \left( \frac{u}{i_o} \right) \) of the amplifier, as shown in Figure 5.28. These curves show the typical eight-shape of the memristor hysteresis, tending to a straight-line at high frequencies.

\[\frac{i_o}{\text{mA}} \quad \frac{u}{\text{V}}\]

Figure 5.27: \( i_o(t) \) curves for the trans-memconductance amplifier with nullor using polynomial memristor model

Figure 5.28: Transmem-conductance \( u-i_o \) hysteresis with nullor using polynomial memristor model
Table 5.17 shows the breakdown of the memristive transconductance ratio by reducing the memristive range as the frequency increases.

Table 5.17: Memristive transconductance ratio using different frequency values

<table>
<thead>
<tr>
<th>ω</th>
<th>( \omega_i ) (x10^{-5}S)</th>
<th>ω</th>
<th>( \omega_o ) (x10^{-5}S)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>6.250-1000</td>
<td>6</td>
<td>6.250-7.490</td>
</tr>
<tr>
<td>2</td>
<td>6.250-12.42</td>
<td>7</td>
<td>6.250-7.284</td>
</tr>
<tr>
<td>5</td>
<td>6.250-7.800</td>
<td>10</td>
<td>6.250-6.939</td>
</tr>
</tbody>
</table>

**HPM model**

The HPM memristor model is characterized by the parameter values shown in Table 5.18.

Table 5.18: \( W \) parameter values using HPM memristor model

<table>
<thead>
<tr>
<th>( W(10^{-5}S) )</th>
<th>( x_0 )</th>
<th>( a )</th>
<th>( A )</th>
<th>( \alpha )</th>
<th>( W_{max}(S) )</th>
<th>( W_{min}(S) )</th>
<th>( W(\omega \to \infty)(S) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.939-17.22</td>
<td>0.1</td>
<td>3</td>
<td>40( \mu )A</td>
<td>160</td>
<td>1.722\times10^{-1}</td>
<td>6.939\times10^{-5}</td>
<td>6.939\times10^{-5}</td>
</tr>
</tbody>
</table>

Now, the circuit shown in Figure 5.26 is performed by using the HPM memristor model.

**Results**

The simulation result of the output voltage \( i_o(t) \) of the amplifier for two discrete values of the frequency \( \omega = 1, 10 \) is shown in Figure 5.29.

![Figure 5.29: \( i_o(t) \) curves for the trans-memconductance amplifier with nullor using HPM memristor model](image-url)
In this case, the corresponding curves shown in Figure 5.29 denote \( i_o \) with the memristor by the blue lines, and the black lines are associated to the simulations with the \( W_{min} \) and the \( W_{max} \) reached by the memristor.

![Figure 5.30: Transmem-conductance \( u_i - i_o \) hysteresis with nullor using HPM memristor model](image)

The transmission curves (\( \frac{i_o}{u_i} \)) of the amplifier are shown in Figure 5.30. The memristive transconductance ratio (\( \frac{i_o}{u_i} \)) shows the typical eight-shape of the memristor hysteresis, tending to a straight-line at high frequencies, as shown in Figure 5.30. Table 5.19 shows the behavior of the memristive range as the frequency increases.

<table>
<thead>
<tr>
<th>( \omega )</th>
<th>( \frac{i_o}{u_i} \times 10^{-5} )S</th>
<th>( \omega )</th>
<th>( \frac{i_o}{u_i} \times 10^{-5} )S</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>6.939-17.22</td>
<td>6</td>
<td>6.939-7.322</td>
</tr>
<tr>
<td>5</td>
<td>6.939-7.423</td>
<td>10</td>
<td>6.939-7.147</td>
</tr>
</tbody>
</table>
5.1.2.2 MOS-based design

The circuit shown in Figure 5.31 represents the trans-memconductance amplifier using the
nullor implementation of the MOS in common-source configuration. This implementation
is simulated by using the polynomial and HPM memristor models.

\[ u_i = A \sin \omega t, \quad A = 1V, \quad R_L = 1\Omega, \quad g_m = 320 \frac{\mu A}{V}, \quad g_{ds} = 320nS \]
and \( W \) is characterized by

the parameter values of the memristor model.

Polynomial model

The polynomial memristor model is characterized by the parameter values shown in Table
5.16. By following the same procedure as in the previous implementation, the circuit of
Figure 5.31 is simulated.

Results

\[ i_o(t) \] curves for the trans-memconductance amplifier with MOS-equivalent

using polynomial memristor model

\[ i_o(t) \] curves for the trans-memconductance amplifier with MOS-equivalent

using polynomial memristor model

\[ i_o(t) \] curves for the trans-memconductance amplifier with MOS-equivalent

using polynomial memristor model

\[ i_o(t) \] curves for the trans-memconductance amplifier with MOS-equivalent

using polynomial memristor model
By following the same procedure as in the previous implementation, the curves $i_o(t)$ are obtained and shown in Figure 5.32.

![Figure 5.33: Transmem-conductance $u_i-i_o$ hysteresis with MOS-equivalent using polynomial memristor model](image)

For this implementation, the Figure 5.33 shows the resulting $u_i-i_o$ hysteresis loops (in black) and the hysteresis loops of the memristor are also shown (in red).

It clearly result that the trans-memconductance is smaller than the memconductance at the feedback, which can be explained by the fact that the implemented nullor does not have zeroes in its chain matrix. Table 5.20 shows the memristive transconductance ratio with the MOS-equivalent as the frequency increases.

Table 5.20: Memristive transconductance ratio using different frequency values

<table>
<thead>
<tr>
<th>$\omega$</th>
<th>$W$ (x10$^{-5}$S)</th>
<th>$\frac{i_o}{i_i}$ (x10$^{-5}$S)</th>
<th>$\omega$</th>
<th>$W$ (x10$^{-5}$S)</th>
<th>$\frac{i_o}{i_i}$ (x10$^{-5}$S)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>6.250-1000</td>
<td>5.224-31.00</td>
<td>6</td>
<td>6.250-7.490</td>
<td>5.224-6.064</td>
</tr>
<tr>
<td>5</td>
<td>6.250-7.800</td>
<td>5.224-6.266</td>
<td>10</td>
<td>6.250-6.939</td>
<td>5.224-5.698</td>
</tr>
</tbody>
</table>

**Effect of the DC-gain**

In this part, further analysis of the amplifier is achieved for several values of the DC-gain. This important parameter expresses how closer the MOS-model is to the nullor. Because the DC-gain depends on $g_{ds}$ and $g_m$, separate analysis are carried out by varying $g_{ds}$ and $g_m$. 
Analysis I: Effect of $g_{ds}$

In this analysis, the output conductance $g_{ds}$ is varied while the transconductance $g_m$ remains fixed.

![Figure 5.34: Transmission curves for Analysis I.](image)

The trans-memconductance $u_i - i_o$ hystereses are shown in Figure 5.34 for DC-gain values of 60dB, 40dB and 20dB.

Another form of looking at the simulation results is recast in Table 5.21. Herein, the values associated to $g_{ds}$ in order to produce the DC-gain values above yield a limit trans-memconductance value at $\omega = \infty$, that is to say high frequencies. Decreasing the DC-gain (increasing $g_{ds}$) causes a small reduction in this limit.

Table 5.21: Summary of Analysis I

<table>
<thead>
<tr>
<th>DC-gain (dB)</th>
<th>$g_m$ ($10^{-6}$A/V)</th>
<th>$g_{ds}$ (℧)</th>
<th>$\frac{u_i}{g_m} (℧)$ for $\omega = \infty$</th>
</tr>
</thead>
<tbody>
<tr>
<td>60</td>
<td>320</td>
<td>320×10^{-9}</td>
<td>5.224×10^{-8}</td>
</tr>
<tr>
<td>40</td>
<td>320</td>
<td>320×10^{-8}</td>
<td>5.185×10^{-5}</td>
</tr>
<tr>
<td>20</td>
<td>320</td>
<td>320×10^{-7}</td>
<td>4.825×10^{-5}</td>
</tr>
</tbody>
</table>
Analysis II: Effect of $g_m$

In this analysis, $g_m$ is varied while $g_{ds}$ is fixed.

![Graphs showing transmission curves for Analysis II](image)

Figure 5.35: Transmission curves for Analysis II.

The resulting trans-memconductance $u_i-i_o$ hystereses are shown in Figure 5.35 for the same DC-gain values of the previous analysis.

The summary of the effect of $g_m$ is shown in Table 5.22. Now, the values associated to $g_m$ produce a limit trans-memresistance value at $\omega=\infty$.

Table 5.22: Summary of Analysis II

<table>
<thead>
<tr>
<th>DC-gain (dB)</th>
<th>$g_m$</th>
<th>$g_{ds}(10^{-9})\Omega$</th>
<th>$\frac{\mu_{u_i}}{g_m}(\Omega)$ for $\omega = \infty$</th>
</tr>
</thead>
<tbody>
<tr>
<td>60</td>
<td>$320 \times 10^{-6}$</td>
<td>320</td>
<td>$5.224 \times 10^{-5}$</td>
</tr>
<tr>
<td>40</td>
<td>$320 \times 10^{-7}$</td>
<td>320</td>
<td>$2.100 \times 10^{-5}$</td>
</tr>
<tr>
<td>20</td>
<td>$320 \times 10^{-8}$</td>
<td>320</td>
<td>$3.029 \times 10^{-6}$</td>
</tr>
</tbody>
</table>

HPM model

The HPM memristor model is characterized by the parameter values shown in Table 5.18. By following the same procedure as in the previous implementation, the circuit of Figure 5.31 is simulated in order to examine the behavior of the output variable and the transfer ratio of the amplifier.

**Results**

The simulation result of the output current $i_o(t)$ of the amplifier for two discrete values of the frequency $\omega = 1, 10$ is shown in Figure 5.36. The resulting $u_i-i_o$ hysteresis loops (in black) and the hysteresis loops of the memristor (in blue) are shown in Figure 5.37.
The trans-memconductance and the memconductance at the feedback remain the same behavior as the previous analysis using the polynomial memristor model. Table 5.23 shows the memristive transconductance ratio with the MOS-equivalent as the frequency increases.

Table 5.23: Memristive transconductance ratio using different frequency values

<table>
<thead>
<tr>
<th>ω</th>
<th>W(x10^{-5}S)</th>
<th>\frac{\Delta W}{\Delta t}(x10^{-5}S)</th>
<th>ω</th>
<th>W(x10^{-5}S)</th>
<th>\frac{\Delta W}{\Delta t}(x10^{-5}S)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>6.939-17.22</td>
<td>5.698-11.18</td>
<td>6</td>
<td>6.939-7.322</td>
<td>5.698-5.954</td>
</tr>
</tbody>
</table>
Effect of the DC-gain

The analysis of the amplifier is achieved for several values of the DC-gain. Because the DC-gain depends on $g_{ds}$ and $g_m$, separate analysis are carried out by varying $g_{ds}$ and $g_m$.

Analysis I: Effect of $g_{ds}$

The conductance $g_{ds}$ is varied while the transconductance $g_m$ remains fixed.

![Figure 5.38: Transmission curves for Analysis I.](image)

The trans-memconductance $u_t-i_o$ hystereses are shown in Figure 5.38 for DC-gain values of 60dB, 40dB and 20dB.

In Table 5.24, the values associated to $g_{ds}$ in order to produce the DC-gain values above yield a limit trans-memconductance value at $\omega=\infty$, that is to say high frequencies. Decreasing the DC-gain (increasing $g_{ds}$) causes a small reduction in this limit.

<table>
<thead>
<tr>
<th>DC-gain (dB)</th>
<th>$g_m$ ($10^{-6}\Omega$)</th>
<th>$g_{ds}(\Omega)$</th>
<th>$\frac{g_{ds}(\Omega)}{g_m}$ for $\omega=100$</th>
</tr>
</thead>
<tbody>
<tr>
<td>60</td>
<td>320</td>
<td>$320 \times 10^{-9}$</td>
<td>$5.698 \times 10^{-5}$</td>
</tr>
<tr>
<td>40</td>
<td>320</td>
<td>$320 \times 10^{-8}$</td>
<td>$5.656 \times 10^{-5}$</td>
</tr>
<tr>
<td>20</td>
<td>320</td>
<td>$320 \times 10^{-7}$</td>
<td>$5.269 \times 10^{-5}$</td>
</tr>
</tbody>
</table>
Analysis II: Effect of \( g_m \)

In this analysis, \( g_m \) is varied while \( g_{ds} \) is fixed.

![Graph](image)

Figure 5.39: Transmission curves for Analysis II.

The resulting trans-memconductance \( u_i - i_o \) hystereses are shown in Figure 5.39 for the same DC-gain values of the previous analysis.

The summary of the effect of \( g_m \) is shown in Table 5.25. Now, the values associated to \( g_m \) produce a limit trans-memconductance value at \( \omega=\infty \).

Table 5.25: Summary of Analysis II

<table>
<thead>
<tr>
<th>DC-gain (dB)</th>
<th>( g_m ) ( \mu )</th>
<th>( g_{ds} ) (( \times 10^{-\nu} ))Ω</th>
<th>( \frac{g_{ds}}{g_m} ) (( \Omega )) for ( \omega=\infty )</th>
</tr>
</thead>
<tbody>
<tr>
<td>60</td>
<td>( 320 \times 10^{-6} )</td>
<td>320</td>
<td>( 5.698 \times 10^{-3} )</td>
</tr>
<tr>
<td>40</td>
<td>( 320 \times 10^{-7} )</td>
<td>320</td>
<td>( 2.183 \times 10^{-5} )</td>
</tr>
<tr>
<td>20</td>
<td>( 320 \times 10^{-8} )</td>
<td>320</td>
<td>( 3.045 \times 10^{-6} )</td>
</tr>
</tbody>
</table>
5.1.2.3 Memistor-based design

The circuit shown in Figure 5.40 represents the trans-memconductance amplifier using the nullor implementation of the memistor. This implementation is simulated by using the polynomial and HPM memristor models.

![Circuit diagram for trans-memconductance amplifier](image)

Figure 5.40: Trans-memconductance amplifier with Memistor realization

where \( u_i = A \sin \omega t \), \( A = 1 \text{V} \) and \( R_L = 1 \Omega \). The memristor \( W \) and the memristors that constitutes the memistor are characterized by the parameter of the memristor model.

**Polynomial model**

The polynomial memristor model is characterized by the parameter values shown in Table 5.16. By following the same procedure as in the previous implementation, the circuit of Figure 5.40 is simulated.

**Results**

![Plot of i_o(t) curves](image)

Figure 5.41: \( i_o(t) \) curves for the trans-memconductance amplifier with Memistor realization using polynomial memristor model
The simulation result of the output voltage \( u_o(t) \) of the amplifier for two discrete values of the frequency \( \omega = 1, 10 \) is shown in Figure 5.41. The label \( @x10^{-1} \) means that the curve of \( W_{\text{max}} \) has been increased ten times of the original value in order to be displayed.

![Figure 5.42: Transmem-conductance \( u_i-\!i_o \) hysteresis (black) and memristor hysteresis (red) for Memistor realization using polynomial memristor model](image)

For this implementation, the resulting \( u_i-\!i_o \) hysteresis loops (in black) and the hysteresis loops of the memristor (in red) are shown in Figure 5.42. Table 5.26 shows the memristive transconductance ratio with the Memistor-implementation as the frequency increases.

<table>
<thead>
<tr>
<th>( \omega )</th>
<th>( W(\times10^{-5}\text{S}) )</th>
<th>( \frac{\mu_W}{\mu_i}(\times10^{-5}\text{S}) )</th>
<th>( \omega )</th>
<th>( W(\times10^{-5}\text{S}) )</th>
<th>( \frac{\mu_W}{\mu_i}(\times10^{-5}\text{S}) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>6.250-1000</td>
<td>2.083-333.33</td>
<td>6</td>
<td>6.250-7.390</td>
<td>2.083-2.496</td>
</tr>
</tbody>
</table>

**HPM model**

The HPM memristor model is characterized by the parameter values shown in Table 5.18. By following the same procedure as in the previous implementation, the circuit of Figure 5.40 is simulated.

**Results**

The simulation result of the output current \( i_o(t) \) of the amplifier for two discrete values of the frequency \( \omega = 1, 10 \) is shown in Figure 5.43. For this implementation, the resulting
$u_i - i_o$ hysteresis loops (in black) and the hysteresis loops of the memristor (in blue) are shown in Figure 5.44.

![Figure 5.43](image-url) **Figure 5.43:** $i_o(t)$ curves for the trans-memconductance amplifier with Memistor realization using HPM memristor model

![Figure 5.44](image-url) **Figure 5.44:** Transmem-conductance $u_i - i_o$ hysteresis (black) and memristor hysteresis (blue) for Memistor realization using HPM memristor model

<table>
<thead>
<tr>
<th>$\omega$</th>
<th>$W(x10^{-3}S)$</th>
<th>$\frac{dW}{d\omega}(x10^{-5}S)$</th>
<th>$\omega$</th>
<th>$W(x10^{-3}S)$</th>
<th>$\frac{dW}{d\omega}(x10^{-5}S)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>6.939-17.22</td>
<td>2.313-5.740</td>
<td>6</td>
<td>6.939-7.322</td>
<td>2.313-2.440</td>
</tr>
</tbody>
</table>

The trans-memconductance and the memconductance at the feedback remain the same behavior as the previous analysis using the polynomial memristor model. Table 5.27
shows the memristive transconductance ratio with the Memistor-implementation as the frequency increases.

5.1.2.4 Conclusions

The feasibility of input-output characteristics that exhibit the typical memristive hysteresis has been proved by the analysis of the trans-memconductance amplifiers. The simulation results show that the pinched hysteresis loop of the memristor has been transmitted to the input-output transfer characteristics which indicates a memristive behavior of the amplifier.

The nullor has been implemented in two forms, namely a MOS-realization and a novel Memistor-realization. On the one hand, the first implementation allow us to foresee that hybrid (MOS/memristor) circuits can be used for this type of application. On the other hand, the second implementation opens the possibility to obtain full-memristor realizations for these circuits. Besides, the results on the analysis of the effect of the DC-gain when the nullor is implemented by a MOS-stage are in concordance with the basic concepts of the design of nullor-based negative feedback amplifiers.

The differences on the simulation results in the case of using Nullor-based, MOS-equivalent and Memistor-implementation in the trans-memconductance amplifier are re-cast in Table 5.28 and Table 5.29.

Table 5.28: Summary of data from the trans-memconductance amplifier using the polynomial memristor model

<table>
<thead>
<tr>
<th>Trans-memconductance amplifier</th>
<th>$W(\mu S)$ for $\omega=\infty$</th>
<th>$u_w(V)$</th>
<th>$\frac{u_m}{u_i}(\mu \Omega)$ for $\omega=1$</th>
<th>$\frac{u_m}{u_i}(\mu \Omega)$ for $\omega=\infty$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nullor-based</td>
<td>62.5</td>
<td>1</td>
<td>$10 \times 10^4 - 62.5$</td>
<td>62.5</td>
</tr>
<tr>
<td>MOS-equivalent</td>
<td>62.5</td>
<td>0.83</td>
<td>310 - 54.6</td>
<td>54.6</td>
</tr>
<tr>
<td>Memistor-implementation</td>
<td>62.5</td>
<td>0.33</td>
<td>$3.333 \times 10^3 - 20.8$</td>
<td>20.8</td>
</tr>
</tbody>
</table>

Table 5.29: Summary of data from the trans-memconductance amplifier using the HPM memristor model

<table>
<thead>
<tr>
<th>Trans-memconductance amplifier</th>
<th>$W(\mu S)$ for $\omega=\infty$</th>
<th>$u_w(V)$</th>
<th>$\frac{u_m}{u_i}(\mu \Omega)$ for $\omega=1$</th>
<th>$\frac{u_m}{u_i}(\mu \Omega)$ for $\omega=\infty$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nullor-based</td>
<td>69.39</td>
<td>1</td>
<td>172.2 - 69.39</td>
<td>69.39</td>
</tr>
<tr>
<td>MOS-equivalent</td>
<td>69.39</td>
<td>0.83</td>
<td>111.8 - 56.98</td>
<td>56.98</td>
</tr>
<tr>
<td>Memistor-implementation</td>
<td>69.39</td>
<td>0.33</td>
<td>57.40 - 23.13</td>
<td>23.13</td>
</tr>
</tbody>
</table>

The information establishes that the active part of the trans-memconductance amplifier contributes significantly to the performance of the amplifier. The use of non-ideal blocks in the active part causes the value of the memristive transmission decreases as the frequency
tends to infinity, i.e. the gain of the amplifier is reduced. Moreover, the memristive behavior of the transfer ratios has not disappeared in the case of MOS-implementation and Memistor-implementation which suggests the usefulness of the memristor as feedback element.
5.2 Opamp-based examples

The op-amp is a differential amplifier that exhibits a large voltage gain, low output impedance and high input impedance. In the conventional inverter and noninverter amplifiers, the op-amp is connected using two resistors $R_1$ and $R_2$.

The existence of the memristor provides the opportunity to use memristors instead of resistors. Besides, depending of the resistor replaced; a new configuration of the memristor-based amplifier emerges. These new configurations are listed in Table 5.30.

Table 5.30: New configurations of memristor-based amplifiers

<table>
<thead>
<tr>
<th>Amplifier</th>
<th>Feedback network</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>inverter</td>
<td>$M - M$</td>
<td>$\frac{M}{M}$ configuration</td>
</tr>
<tr>
<td></td>
<td>$M - R$</td>
<td>$\frac{M}{R}$ configuration</td>
</tr>
<tr>
<td></td>
<td>$R - M$</td>
<td>$\frac{R}{M}$ configuration</td>
</tr>
<tr>
<td>noninverter</td>
<td>$M - M$</td>
<td>$\frac{M}{M}$ configuration</td>
</tr>
<tr>
<td></td>
<td>$M - R$</td>
<td>$\frac{M}{R}$ configuration</td>
</tr>
<tr>
<td></td>
<td>$R - M$</td>
<td>$\frac{R}{M}$ configuration</td>
</tr>
</tbody>
</table>

In this thesis, the ideal functional-model of the operational amplifier is resorted in order to accomplish the point of view of the structured electronic design. Moreover, the analysis of the composition of fundamental and harmonic terms in the case of $\frac{M}{R}$ configuration inverter and noninverter amplifiers in order to determine the total harmonic distortion (THD).

Hereafter, the HPM and polynomial memristor models are used to carry out the circuit-level simulation of the inverter and noninverter amplifiers.

5.2.1 Memristor-based inverter amplifier

$\frac{M_1}{M_2}$ configuration

![Figure 5.45: Memristor-based inverter amplifier](image-url)
The transmission characteristic of the circuit shown in the Figure 5.45, can be established as

$$A_v = \frac{V_{out}}{V_{in}} = -\frac{M_1}{M_2}$$ (5.5)

The memristors $M_1$ and $M_2$ are characterized with the parameter values shown in Table 5.32 and Table 5.31 for the polynomial and HPM memristor model, respectively.

Table 5.31: $M_1$ and $M_2$ parameter values using polynomial memristor model

<table>
<thead>
<tr>
<th>$M$</th>
<th>$R_{ON}$</th>
<th>$R_{OFF}$</th>
<th>$\alpha$</th>
<th>$M(\omega \to \infty)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_1$</td>
<td>38000-100</td>
<td>100</td>
<td>380</td>
<td>38000</td>
</tr>
<tr>
<td>$M_2$</td>
<td>16000-100</td>
<td>100</td>
<td>160</td>
<td>16000</td>
</tr>
</tbody>
</table>

Table 5.32: $M_1$ and $M_2$ parameter values using HPM memristor model

<table>
<thead>
<tr>
<th>$M$</th>
<th>$x_0$</th>
<th>$a$</th>
<th>$A$</th>
<th>$\alpha$</th>
<th>$M(\omega \to \infty)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_1$</td>
<td>14410-9385</td>
<td>0.1</td>
<td>2</td>
<td>40\mu A</td>
<td>160</td>
</tr>
<tr>
<td>$M_2$</td>
<td>14410-5806</td>
<td>0.1</td>
<td>3</td>
<td>40\mu A</td>
<td>160</td>
</tr>
</tbody>
</table>

Figure 5.46: $t-A_v$ characteristic curves using different memristor models

The Figure 5.46 shows the $t-A_v$ curve using the $\frac{M_1}{M_2}$ configuration. The gain $A_v$ exhibits a periodical variation in different instants of time. Besides, the gain $A_v$ tends to a fixed value according $\omega$ approaches to infinity.

The Figure 5.47 shows the transmission curve using the $\frac{M_1}{M_2}$ configuration. The transmission curve exhibits a pinched hysteresis loop. Moreover, the transmission curve tends to be a straight line according $\omega$ approaches to infinity.
The memristors $M_1$ and $M_2$ have been incorporated to Verilog-A modules in order to be employed in a HSPICE simulation procedure. A comparison of HSPICE and AnalogInsydes simulation results is depicted in Figure 5.48.
5.2. Opamp-based examples

5.2.1.1 $\frac{M_2}{R}$ configuration

![Figure 5.49: Memristor-based inverter amplifier](image)

The transmission characteristic of the circuit shown in the Figure 5.49, can be established as

$$A_v = \frac{V_{out}}{V_{in}} = -\frac{M_2}{R}$$ \hspace{1cm} (5.6)

where $R=5\text{K}\Omega$

![Figure 5.50: $t$-$A_v$ characteristic curves using different memristor models](image)

The Figure 5.50 shows the $t$-$A_v$ curve using the $\frac{M_2}{R}$ configuration. The gain $A_v$ exhibits a periodical variation in different instants of time. Besides, the gain $A_v$ tends to a fixed value according $\omega$ approaches to infinity.

The Figure 5.51 shows the transmission curve using the $\frac{M_2}{R}$ configuration. The transmission curve exhibits a pinched hysteresis loop. Moreover, the transmission curve tends to be a straight line according $\omega$ approaches to infinity.
Chapter 5. Circuit applications

\[ R = \begin{bmatrix} 1 & 100 \\ -1.0 & -0.5 \\ 0.0 & 0.5 \\ -1.0 & -0.5 \\ 0.0 & 0.5 \\ -1.0 & -0.5 \\ 0.0 & 0.5 \\ -1.0 & -0.5 \\ 0.0 & 0.5 \end{bmatrix} \]

\[ V_{\text{in}}(t) = \begin{bmatrix} v_1(t) \\ v_2(t) \\ v_3(t) \end{bmatrix} \]

\[ V_{\text{out}}(t) = \begin{bmatrix} v_1(t) \\ v_2(t) \\ v_3(t) \end{bmatrix} \]

(a) Polynomial memristor model

(b) HPM memristor model

Figure 5.51: Transmission characteristic curves using different memristor models

The memristor \( M_2 \) has been incorporated to Verilog-A module in order to be employed in a HSPICE simulation procedure. A comparison of HSPICE and AnalogInsydes simulation results is depicted in Figure 5.52.

**THD**

The total harmonic distortion, or THD, is the sum of all harmonic components compared against the fundamental component. In the case of memristor-based inverter amplifiers, THD is the ratio of the sum of all harmonic components of the output voltage to the fundamental component of the output voltage.

THD can be expressed as

\[ \text{THD} = \sqrt{\frac{v_2^2 + v_3^2 + v_4^2 + \ldots + v_n^2}{v_1}} \]  \hspace{1cm} (5.7)
where \( n \) is the maximum harmonic component, \( v_k \) is the output voltage of the \( k \)-th harmonic and \( k=1 \) is the output voltage of the fundamental frequency.

The result of the equation 5.7 is a comparison of the output voltages of all harmonic components and the output voltage of the fundamental component.

The output voltage of the memristor-based inverter amplifier in the \( \frac{M}{R} \) configuration, are given by

\[
v_{out} = -\frac{M}{R}v_{in} \tag{5.8}
\]

where \( v_{in} = A \sin(\omega t) \).

In the case of HPM memristor model, the memristance \( M \) is defined by

\[
M = C_1 + C_2 \cos(\omega t) + C_3 \cos(2\omega t) + C_4 \cos(3\omega t) \\
+ C_5 \cos(4\omega t) + C_6 \cos(5\omega t) + C_7 \cos(6\omega t) \tag{5.9}
\]

where \( C_1, C_2, C_3, C_4, C_5, C_6 \) and \( C_7 \) are constants from the physical parameters and the homotopy perturbation method.

Substituting the above expression in the equation 5.8

\[
v_{out} = -\left[ \frac{C_1}{R} \sin(\omega t) + \frac{C_2}{R} \cos(\omega t) \sin(\omega t) + \frac{C_3}{R} \cos(2\omega t) \sin(\omega t) \\
+ \frac{C_4}{R} \cos(3\omega t) \sin(\omega t) + \frac{C_5}{R} \cos(4\omega t) \sin(\omega t) \\
+ \frac{C_6}{R} \cos(5\omega t) \sin(\omega t) + \frac{C_7}{R} \cos(6\omega t) \sin(\omega t) \right] \tag{5.10}
\]

Applying some trigonometric identities

\[
v_{out} = -\left[ \left( \frac{C_1}{R} - \frac{C_3}{2R} \right) \sin(\omega t) + \left( \frac{C_2}{2R} - \frac{C_4}{2R} \right) \sin(2\omega t) \\
+ \left( \frac{C_3}{2R} - \frac{C_5}{2R} \right) \sin(3\omega t) + \left( \frac{C_4}{2R} - \frac{C_6}{2R} \right) \sin(4\omega t) \\
+ \left( \frac{C_5}{2R} - \frac{C_7}{2R} \right) \sin(5\omega t) + \frac{C_6}{2R} \sin(6\omega t) + \frac{C_7}{2R} \sin(7\omega t) \right] \tag{5.11}
\]

The above expression establishes the \( v_{out} \) voltage using the frequency components: fundamental, second, third, fourth, fifth, sixth and seventh harmonic.

The equation 5.7 can be rewritten as
\[
THD = \sqrt{\frac{v_2^2 + v_3^2 + v_4^2 + v_5^2 + v_6^2 + v_7^2}{v_1}}
\] (5.12)

where the \(v_1, v_2, v_3, v_4, v_5, v_6\) and \(v_7\) expression of voltage are described as

\[
\begin{align*}
  v_1 &= \left( \frac{C_1}{R} - \frac{C_3}{2R} \right) \sin(\omega t) \\
  v_2 &= \left( \frac{C_2}{2R} - \frac{C_4}{2R} \right) \sin(2\omega t) \\
  v_3 &= \left( \frac{C_3}{2R} - \frac{C_5}{2R} \right) \sin(3\omega t) \\
  v_4 &= \left( \frac{C_4}{2R} - \frac{C_6}{2R} \right) \sin(4\omega t) \\
  v_5 &= \left( \frac{C_5}{2R} - \frac{C_7}{2R} \right) \sin(5\omega t) \\
  v_6 &= \left( \frac{C_6}{2R} \right) \sin(6\omega t) \\
  v_7 &= \left( \frac{C_7}{2R} \right) \sin(7\omega t)
\end{align*}
\]

THD can be calculated by substituting the \(v_{out}\) voltage of each frequency component in the equation 5.12.

In the case of polynomial memristor model, the memristance \(M\) is defined by

\[
M = B_1 + B_2 \cos(\omega t)
\] (5.13)

where \(B_1\) and \(B_2\) are constants from the physical parameters and the polynomial memristor model.

Substituting the above expression in the equation 5.8

\[
v_{out} = - \left[ \frac{B_1}{R} \sin(\omega t) + \frac{B_2}{R} \cos(\omega t) \sin(\omega t) \right]
\] (5.14)

Applying some trigonometric identities

\[
v_{out} = - \left[ \left( \frac{B_1}{R} \right) \sin(\omega t) + \left( \frac{B_2}{2R} \right) \sin(2\omega t) \right]
\] (5.15)
The above expression establishes the $v_{out}$ voltage using the frequency components: fundamental and second harmonic.

The equation 5.7 can be rewritten as

$$\text{THD} = \frac{\sqrt{v_2^2}}{v_1}$$

(5.16)

where the $v_1$ and $v_2$ expression of voltage are described as

$$v_1 = \left( \frac{B_1}{R} \right) \sin(\omega t)$$

$$v_2 = \left( \frac{B_2}{2R} \right) \sin(2\omega t)$$

THD can be calculated by substituting the $v_{out}$ voltage of each frequency component in the equation 5.16.

Figure 5.53: Gain-THD curves using the HPM memristor model

Figure 5.53 shows the Gain-THD curves using different angular frequency values. The
behavior of the Gain-THD curves establishes that the THD value decreases as the angular frequency tends to infinity. Furthermore, the gain value for the minimum value of THD tends to a fixed point as the angular frequency approaches infinity. The gain value at $\omega = \infty$ is a fixed point with a THD value of zero.

Table 5.33: Parameter values using different frequency values

<table>
<thead>
<tr>
<th>$\omega$</th>
<th>$M_{\text{max}}$ (kΩ)</th>
<th>$M_{\text{min}}$ (kΩ)</th>
<th>Gain$_{\text{max}}$ (dBs)</th>
<th>Gain$_{\text{min}}$ (dBs)</th>
<th>THD$_{\text{max}}$ (%)</th>
<th>THD$_{\text{min}}$ (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>16</td>
<td>0.1</td>
<td>10.1</td>
<td>-33.97</td>
<td>98.75</td>
<td>0.02</td>
</tr>
<tr>
<td>2</td>
<td>16</td>
<td>8.05</td>
<td>10.1</td>
<td>4.13</td>
<td>33.05</td>
<td>0.092</td>
</tr>
<tr>
<td>5</td>
<td>16</td>
<td>12.82</td>
<td>10.1</td>
<td>8.17</td>
<td>11.03</td>
<td>0.0087315</td>
</tr>
<tr>
<td>10</td>
<td>16</td>
<td>14.41</td>
<td>10.1</td>
<td>9.19</td>
<td>5.22</td>
<td>0.0041113</td>
</tr>
</tbody>
</table>

Table 5.33 shows the maximum memristance, the minimum memristance, the maximum gain, the minimum gain, the maximum THD and the minimum THD values as the frequency increases.

Figure 5.54: Gain-THD curves using the polynomial memristor model

Figure 5.54 shows the Gain-THD curves using different angular frequency values. The behavior of the Gain-THD curves establishes that the THD value decreases as the angular frequency tends to infinity. Furthermore, the gain value for the minimum value of THD
tends to a fixed point as the angular frequency approaches infinity. The gain value at \( \omega=\infty \) is a fixed point with a THD value of zero.

Table 5.34: Parameter values using different frequency values

<table>
<thead>
<tr>
<th>( \omega )</th>
<th>( M_{\text{max}}(k\Omega) )</th>
<th>( M_{\text{min}}(k\Omega) )</th>
<th>( \text{Gain}_{\text{max}}(\text{dBs}) )</th>
<th>( \text{Gain}_{\text{min}}(\text{dBs}) )</th>
<th>THD(_{\text{max}})(%)</th>
<th>THD(_{\text{min}})(%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>14.41</td>
<td>5.80</td>
<td>9.19</td>
<td>1.29</td>
<td>43.49</td>
<td>2.77</td>
</tr>
<tr>
<td>2</td>
<td>14.41</td>
<td>11.15</td>
<td>9.19</td>
<td>6.97</td>
<td>12.51</td>
<td>0.73</td>
</tr>
<tr>
<td>5</td>
<td>14.41</td>
<td>13.47</td>
<td>9.19</td>
<td>8.60</td>
<td>3.36</td>
<td>0.09075</td>
</tr>
<tr>
<td>10</td>
<td>14.41</td>
<td>13.99</td>
<td>9.19</td>
<td>8.93</td>
<td>1.47</td>
<td>0.02045</td>
</tr>
</tbody>
</table>

Table 5.34 shows the maximum memristance, the minimum memristance, the maximum gain, the minimum gain, the maximum THD and the minimum THD values as the frequency increases.

5.2.1.2 \( \frac{R}{M_2} \) configuration

![Figure 5.55: Memristor-based inverter amplifier](image)

The transmission characteristic of the circuit shown in the Figure 5.55, can be established as

\[
A_v = \frac{V_{out}}{V_{in}} = -\frac{R}{M_2}
\]

(5.17)

where \( R=5K\Omega \)
Figure 5.56: $t-A_v$ characteristic curves using different memristor models

Figure 5.56 shows the $t-A_v$ curve using the $\frac{R}{M_2}$ configuration. The gain $A_v$ exhibits a periodical variation in different instants of time. Besides, the gain $A_v$ tends to a fixed value according $\omega$ approaches to infinity.

Figure 5.57: Transmission characteristic curves using different memristor models

Figure 5.57 shows the transmission curve using the $\frac{R}{M_2}$ configuration. The transmission curve exhibits a pinched hysteresis loop. Moreover, the transmission curve tends to be a straight line according $\omega$ approaches to infinity.
5.2. Opamp-based examples

Figure 5.58: HSPICE and AnalogInsydes simulation results

The memristor $M_2$ has been incorporated to Verilog-A module in order to be employed in a HSPICE simulation procedure. A comparison of HSPICE and AnalogInsydes simulation results is depicted in Figure 5.58.
5.2.2 Memristor-based noninverter amplifier

\[ \frac{M_1}{M_2} \] configuration

![Diagram of memristor-based noninverter amplifier]

Figure 5.59: Memristor-based noninverter amplifier

The transmission characteristic of the circuit shown in the Figure 5.59, can be established as

\[ A_v = \frac{V_{out}}{V_{in}} = 1 + \frac{M_1}{M_2} \] (5.18)

The memristors \( M_1 \) and \( M_2 \) are characterized with the parameter values shown in Table 5.32 and Table 5.31 for the polynomial and HPM memristor model, respectively.

Figure 5.60 shows the \( t-A_v \) curve using the \( \frac{M_1}{M_2} \) configuration. The gain \( A_v \) exhibits a periodical variation in different instants of time. Besides, the gain \( A_v \) tends to a fixed value according \( \omega \) approaches to infinity.

![Graphs showing \( t-A_v \) curves]

(a) Polynomial memristor model  
(b) HPM memristor model

Figure 5.60: \( t-A_v \) characteristic curves using different memristor models

Figure 5.61 shows the transmission curve using the \( \frac{M_1}{M_2} \) configuration. The transmission
curve exhibits a pinched hysteresis loop. Moreover, the transmission curve tends to be a straight line according $\omega$ approaches to infinity.

![Diagram](image1.png)

(a) Polynomial memristor model  
(b) HPM memristor model

Figure 5.61: Transmission characteristic curves using different memristor models

The memristors $M_1$ and $M_2$ have been incorporated to Verilog-A modules in order to be employed in a HSPICE simulation procedure. A comparison of HSPICE and AnalogInsydes simulation results is depicted in Figure 5.62.

![Diagram](image2.png)

(a) Polynomial memristor model  
(b) HPM memristor model

Figure 5.62: HSPICE and AnalogInsydes simulation results
5.2.2.1 $\frac{M_2}{R}$ configuration

![Memristor-based noninverter amplifier](image)

Figure 5.63: Memristor-based noninverter amplifier

The transmission characteristic of the circuit shown in the Figure 5.63, can be established as

$$A_v = \frac{V_{out}}{V_{in}} = 1 + \frac{M_2}{R}$$  \hspace{1cm} (5.19)

where $R=5\text{K}\Omega$

![t-A_v characteristic curves](image)

(a) Polynomial memristor model  \hspace{1cm} (b) HPM memristor model

Figure 5.64: $t-A_v$ characteristic curves using different memristor models

Figure 5.64 shows the $t-A_v$ curve using the $\frac{M_2}{R}$ configuration. The gain $A_v$ exhibits a periodical variation in different instants of time. Besides, the gain $A_v$ tends to a fixed value according $\omega$ approaches to infinity.
The Figure 5.65 shows the transmission curve using the \( \frac{M_2}{\pi} \) configuration. The transmission curve exhibits a pinched hysteresis loop. Moreover, the transmission curve tends to be a straight line according \( \omega \) approaches to infinity.

The memristor \( M_2 \) has been incorporated to Verilog-A module in order to be employed in a HSPICE simulation procedure. A comparison of HSPICE and AnalogInsydes simulation results is depicted in Figure 5.66.
THD

By following the same procedure of the memristor-based inverter amplifier, the THD analysis is realized.

![Figure 5.67: Gain-THD curves using the HPM memristor model](image)

Figure 5.67 shows the Gain-THD curves using different angular frequency values. The behavior of the Gain-THD curves establishes that the THD value decreases as the angular frequency tends to infinity. Furthermore, the gain value for the minimum value of THD tends to a fixed point as the angular frequency approaches infinity. The gain value at $\omega = \infty$ is a fixed point with a THD value of zero.

Table 5.35: Parameter values using different frequency values

<table>
<thead>
<tr>
<th>$\omega$</th>
<th>$M_{\text{max}}$ (kΩ)</th>
<th>$M_{\text{min}}$ (kΩ)</th>
<th>Gain$_{\text{max}}$ (dBs)</th>
<th>Gain$_{\text{min}}$ (dBs)</th>
<th>THD$_{\text{max}}$(%)</th>
<th>THD$_{\text{min}}$(%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>14.41</td>
<td>5.80</td>
<td>11.78</td>
<td>6.69</td>
<td>29.75</td>
<td>1.89</td>
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<tr>
<td>2</td>
<td>14.41</td>
<td>11.15</td>
<td>11.78</td>
<td>10.18</td>
<td>9.05</td>
<td>0.53</td>
</tr>
<tr>
<td>5</td>
<td>14.41</td>
<td>13.47</td>
<td>11.78</td>
<td>11.35</td>
<td>2.47</td>
<td>0.066</td>
</tr>
<tr>
<td>10</td>
<td>14.41</td>
<td>13.99</td>
<td>11.78</td>
<td>11.59</td>
<td>1.69</td>
<td>0.015</td>
</tr>
</tbody>
</table>

Table 5.35 shows the maximum memristance, the minimum memristance, the maxi-
5.2. Opamp-based examples

maximum gain, the minimum gain, the maximum THD and the minimum THD values as the frequency increases.

![Graphs showing Gain-THD curves](image)

Figure 5.68: Gain-THD curves using the polynomial memristor model

Figure 5.68 shows the Gain-THD curves using different angular frequency values. The behavior of the Gain-THD curves establishes that the THD value decreases as the angular frequency tends to infinity. Furthermore, the gain value for the minimum value of THD tends to a fixed point as the angular frequency approaches infinity. The gain value at $\omega=\infty$ is a fixed point with a THD value of zero.

<table>
<thead>
<tr>
<th>$\omega$</th>
<th>$M_{\text{max}}$ (kΩ)</th>
<th>$M_{\text{min}}$ (kΩ)</th>
<th>Gain_{max} (dBs)</th>
<th>Gain_{min} (dBs)</th>
<th>THD_{max} (%)</th>
<th>THD_{min} (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>16</td>
<td>0.1</td>
<td>12.46</td>
<td>0.1720</td>
<td>60.91</td>
<td>0.0124</td>
</tr>
<tr>
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<td>8.3328</td>
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<td>12.46</td>
<td>11.7811</td>
<td>3.93</td>
<td>0.0030</td>
</tr>
</tbody>
</table>

Table 5.36: Parameter values using different frequency values

Table 5.36 shows the maximum memristance, the minimum memristance, the maximum gain, the minimum gain, the maximum THD and the minimum THD values as the frequency increases.
5.2.2.2 $\frac{R}{M_2}$ configuration

![Diagram of circuit with $V_{in}$, $R$, $M_2$, and $V_{out}$]

Figure 5.69: Memristor-based noninverter amplifier

The transmission characteristic of the circuit shown in the Figure 5.69, can be established as

$$A_v = \frac{V_{out}}{V_{in}} = 1 + \frac{R}{M_2}$$  \hspace{1cm} (5.20)

where $R=5\text{K}\Omega$

![Graphs showing $t-A_v$ curves with polynomial and HPM memristor models]

(a) Polynomial memristor model  \hspace{1cm} (b) HPM memristor model

Figure 5.70: $t-A_v$ characteristic curves using different memristor models

Figure 5.70 shows the $t-A_v$ curve using the $\frac{R}{M_2}$ configuration. The gain $A_v$ exhibits a periodical variation in different instants of time. Besides, the gain $A_v$ tends to a fixed value according $\omega$ approaches to infinity.
5.2. Opamp-based examples

\[ \Omega = 1 \]

\[ V_{\text{out}}(V) = V_{\text{in}}(V) \]

(a) Polynomial memristor model

(b) HPM memristor model

Figure 5.71: Transmission characteristic curves using different memristor models

Figure 5.71 shows the transmission curve using the \( \frac{R}{M_2} \) configuration. The transmission curve exhibits a pinched hysteresis loop. Moreover, the transmission curve tends to be a straight line according \( \omega \) approaches to infinity.

The memristor \( M_2 \) has been incorporated to Verilog-A module in order to be employed in a HSPICE simulation procedure. A comparison of HSPICE and AnalogInsydes simulation results is depicted in Figure 5.72.

5.2.3 Conclusions

The simulation results show that the pinched hysteresis loop of the memristor has been transmitted to the amplifier causing a memristive behavior in the gain characteristic curve. Further, the simulation results have been compared with a HSPICE simulation procedure using Verilog-A modules.
The advantage of using the novel polynomial and HPM memristor models in amplifiers is the ability to locate the gain value over the time, which is not achieved with a PWL function-based memristor model [8].

The composition of fundamental and harmonic terms in the novel polynomial and HPM memristor models facilitates the mathematical analysis of the total harmonic distortion. The THD in the memristor-based inverter and noninverter amplifiers has been discussed in [9]. The novel memristor models confirms that the THD is worse in the lower gain values [9].
5.3 Mem-elements emulator circuits

The concept of memristance, i.e. the property of an element whose resistance depends on the memory of the system state, has been extended to inductance and capacitance [10], which has brought us to the concept of meminductance and memcapacitance. The associated memory elements are called meminductor and memcapacitor, respectively.

In this part of the thesis, the polynomial and HPM memristor models are used to carry out the circuit-level simulation of these emulation circuits.

5.3.1 Memcapacitor and meminductor grounded

The memcapacitor emulator [11] consists of a memristor $M$, a capacitor $C$ and a resistor $R$ connected to an operational amplifier as shown in Figure 5.73. The expression of the capacitance is determined by

$$C(t) = \frac{M(t)C}{R}$$

(5.21)

On the other hand, the meminductor emulator [11] is similar to the design of a gyrator with a memristor replacing a resistor as shown in Figure 5.73. The equivalent inductance is determined by

$$L(t) = RM(t)C$$

(5.22)

Figure 5.73: Memcapacitor and meminductor emulators

The parameter values for the memcapacitor and meminductor emulators are: $R=480\Omega$, $C=10\mu\text{A}$ and $M$ is characterized by the parameter values shown in Table 5.37 and Table 5.38. The input signal is a square function.

The simulation results are shown in the waveforms of Figures 5.74 and 5.75. It shows the input voltage (solid line) and the voltage at the output of the operational amplifier...
Table 5.37: $M$ parameter values using HPM memristor model

<table>
<thead>
<tr>
<th>$M$</th>
<th>$x_0$</th>
<th>$a$</th>
<th>$A$</th>
<th>$\alpha$</th>
<th>$M_{\text{min}}$</th>
<th>$M_{\text{max}}$</th>
<th>$M(\omega \to \infty)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>14410-9385</td>
<td>0.1</td>
<td>2</td>
<td>40$\mu$A</td>
<td>160</td>
<td>9385</td>
<td>14410</td>
<td>14410</td>
</tr>
</tbody>
</table>

Table 5.38: $M$ parameter values using polynomial memristor model

<table>
<thead>
<tr>
<th>$M$</th>
<th>$M_{\text{min}}$</th>
<th>$R_{\text{max}}$</th>
<th>$\alpha$</th>
<th>$M(\omega \to \infty)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>16000-100</td>
<td>100</td>
<td>16000</td>
<td>160</td>
<td>16000</td>
</tr>
</tbody>
</table>

(dashed line) which represents the voltage of the emulate memcapacitor and meminductor. The waveforms agree with those reported in [11].

Figure 5.74: $V_{in}$ and $V_{out}$ curves for the memcapacitor emulator.

Figure 5.75: $V_{in}$ and $V_{out}$ curves for the meminductor emulator.

Besides, the equivalent capacitance $C(t)$ and inductance $L(t)$ are displayed in Figures 5.76 and 5.77. The simulation results confirm the presence of hysteresis loops in the
capacitance and inductance as a function of voltage. The behavior of the typical property in memory circuit elements is observed: the hysteresis loop is much smaller as the frequency tends to infinity.

![Figure 5.76](image1)

(a) HPM memristor model  
(b) Polynomial memristor model

Figure 5.76: The capacitance $C(t)$ using different memristor models.

![Figure 5.77](image2)

(a) HPM memristor model  
(b) Polynomial memristor model

Figure 5.77: The inductance $L(t)$ using different memristor models.
5.3.2 Mutator using current conveyor and OTA

The mutator consists of a memristor $M$, a capacitor $C$, an operational transconductance amplifier (OTA) and a current conveyor (CCII+). The implementation of the mutator [12] is shown in Figure 5.78.

![Figure 5.78: Mutator $M_R$ to $M_C$ using CCII+ and OTA](image)

According to [12], the CCII+ current conveyor transforms voltage $v_2$ into voltage $v_1$; i.e. $v_1 = v_2$. The current $i_1$ is conveyed to the z terminal causing a voltage drop on the capacitor $C$ which is proportional to the time-domain integral of this current. This voltage is then transformed using the OTA with the transconductance $g_m$ into current $i_M$.

The parameter values of the memristor to memcapacitor mutator are: $C = 10\mu F$, $g_m = 100\mu A/V$ and $M$ is characterized by the parameter values shown in Table 5.37 and Table 5.38. The input port is exited by the voltage source $v_{in}$ of sinusoidal waveform with the amplitude of 2V and the frequency of 1Hz.

![Figure 5.79: $q$ and $I_{M_c}$ curves for the memcapacitor using polynomial memristor model](image)

The simulation results are shown in the waveforms of Figures 5.79 and 5.80. Figure 5.79 shows the behavior of the charge and the current across the memcapacitor mutator. Moreover, Figure 5.80 shows the behavior of the $V_{in}$-Capacitance characteristic curve as frequency tends to infinity.
5.3. Mem-elements emulator circuits

In the case of using HPM memristor model, the simulation results are shown in the waveforms of Figures 5.81 and 5.82. Figure 5.81 shows the behavior of the charge and the current across the memcapacitor mutator.

Moreover, Figure 5.82 shows the behavior of the $V_{in}$-Capacitance characteristic curve as frequency tends to infinity.

---

Figure 5.80: $V_{in}$-Capacitance characteristic curves using polynomial memristor model

Figure 5.81: $q$ and $I_{Mc}$ curves for the memcapacitor using HPM memristor model

Figure 5.82: $V_{in}$-Capacitance characteristic curves using HPM memristor model
5.3.3 Emulator using single-output current conveyor

The implementation of the memcapacitor emulator [13] is shown in Figure 5.83. This emulator consists of a memristor $M$, a inductor $L$, a resistor $R$ and four current conveyors (CCII+).

![Figure 5.83: Floating memcapacitor](image)

The parameter values of the memcapacitor emulator are: $L=10\text{mH}$, $R=480\Omega$ and $M$ is characterized by the parameter values shown in Table 5.37 and Table 5.38. The input port is exited by the voltage source $v_{in}$ of sinusoidal waveform with the amplitude of 1V and the frequency of 1Hz.

![Figure 5.84: Memcapacitor characteristic-curves using polynomial memristor model](image)

(a) $V_C$-$q$ characteristic curves  (b) $V_C$-$C$ characteristic curves

The simulation results are shown in the waveforms of Figure 5.84. Figure 5.84a shows the parametric graph of the charge and the voltage across the memcapacitor emulator. Moreover, Figure 5.84b shows the behavior of the $V_C$-$C$ characteristic curve of the memcapacitor emulator.
5.3. Mem-elements emulator circuits

Figure 5.85: Memcapacitor characteristic-curves using HPM memristor model

In the case of using HPM memristor model, the simulation results are shown in the waveforms of Figure 5.85. Figure 5.85a shows the parametric graph of the charge and the voltage across the memcapacitor emulator. Moreover, Figure 5.85b shows the behavior of the $V_C$-$C$ characteristic curve of the memcapacitor emulator.
5.3.4 Meminductor emulator

The implementation of the meminductor emulator [13] is shown in Figure 5.86. This emulator consists of a memristor $M$, a capacitor $C$, a resistor $R$ and four current conveyors (CCII+).

![Diagram of meminductor emulator](image)

Figure 5.86: Floating meminductor

The parameter values of the meminductor emulator are: $C=1\text{nF}$, $R=480\Omega$ and $M$ is characterized by the parameter values shown in Table 5.37 and Table 5.38. The input port is exited by the voltage source $v_{in}$ of sinusoidal waveform with the amplitude of $1\text{V}$ and the frequency of $1\text{Hz}$.

![Characteristics curves](image)

Figure 5.87: Meminductor characteristic-curves using polynomial memristor model

The simulation results are shown in the waveforms of Figure 5.87. Figure 5.87a shows the parametric graph of the flux and the current across the meminductor emulator. Moreover, Figure 5.87b shows the behavior of the $I_L-L$ characteristic curve of the meminductor emulator.
In the case of using HPM memristor model, the simulation results are shown in the waveforms of Figure 5.88. Figure 5.88a shows the parametric graph of the flux and the current across the meminductor emulator. Moreover, Figure 5.88b shows the behavior of the $I_L-L$ characteristic curve of the meminductor emulator.
Bibliography


Chapter 6

Conclusions

A methodology for the generation of circuit simulation-oriented memristor models in the DC and time domains has been developed. In both cases the generated models are recast in the form of current-voltage branch relationships.

The methodology for the generation of the DC models starts from the state variable formulation of the memristive system given through a piece-wise linear (PWL) definition. A numerical integration method yields the solution of the ODE which is treated by a curve fitting procedure in order to obtain a polynomial $i-v$ characteristic. The dependence of the characteristics on the parameters of the PWL definition has been studied. As a result, the problem of the occurrence of multiple DC operating points in memristive DC circuits has been established. The multiple solutions of the DC memristive equilibrium equations have been assessed by resorting to a homotopy method for two cases study, namely a single- and two-memristor circuit.

The methodology for the generation of the time-domain models has been focused on generating to two different models. Firstly, a polynomial model has been developed from the $\varphi-q$ branch relationship of a generic memristor. In second place, a semi-symbolical memristor model has been developed from the ODE that expresses the linear drift mechanism of the device with the parameters of the HP memristor. This model has been generated by using the homotopy perturbation method (HPM). The impact of the parameters of the HPM memristor model has been determined by symbolical and numerical analyzes. Both, the polynomial and the HPM models comply with the properties and fingerprints that a memristor must posses.

Both models have been used in circuit applications. When the memristor is used in negative-feedback amplifier schemes, a new family of trans-mem amplification ratios has been established. The results are presented in the form of pinched hysteresis loops for the amplifier gains and the analysis of the composition of fundamental and harmonic terms.
in the case of using the HP memristor model in order to determine the total harmonic
distortion (THD). Another usage of these models has been in circuits for emulating mem-
capacitors and meminductors.

**Future work**

The methodology can be extended to memristors with different physical parameters be-
cause the starting definition in this work is based on the physical behavior of the device
by using the linear drift mechanism.

The memristor models should be able to unify the analysis domain of DC and time in
order to provide continuity in the simulation procedure with traditional elements. This
problem has been caused by using functional models which are approximations that depend
on the analysis domain and the validity of the variable range. However, from the computer-
aided circuit analysis point of view, the insertion of the memristor requires a reformulating
of the normal form equations by using the computationally efficient *tableau* approach,
where each memristor can be represented simply by three equations; namely, \( \frac{d\phi}{dt} = v \), \( \frac{dq}{dt} = i \),
and \( \phi = \phi(q) \).

The insertion of the fundamental variables of the memristor, namely the electric charge
and the flux-linkage in the matrix representation employed in circuit simulators involves
a dramatic change in the paradigm of circuital simulation, and it clearly constitutes a
different approach from the current work.
Appendix A

Nonlinear boundary of HP memristor

This appendix is focused on carrying out a simple proposal in order to tackle the problem of the nonlinear boundary between the two regions of the HP memristor. This problem is depicted in Figure A.1.

![Figure A.1: The HP memristor structure using nonlinear boundary](image)

The nonlinear boundary can be included into the following $v$-$i$ relationship as a two-dimensional problem

$$v(t) = \left( R_{ON} \left( wL + \frac{\Delta L}{2} \right) + R_{OFF} \left( DL - \left( wL + \frac{\Delta L}{2} \right) \right) \right) i(t) \quad (A.1)$$

According to the expression of (A.1), the $R_{ON}$ and $R_{OFF}$ parameters must be expressed in units of area.
Appendix A. Nonlinear boundary of HP memristor
Table B.1: RMSE values for the variation of $x_0$ and $a$.

<table>
<thead>
<tr>
<th>$x_0$</th>
<th>$a$</th>
<th>RMSE</th>
<th>$a$</th>
<th>RMSE</th>
<th>$a$</th>
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<td>2</td>
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### Appendix B. Transient memristor model

Table B.4: RMSE values for the variation of $x_0$, $A$, and $d = 10$. 

The table above shows the root mean square error (RMSE) for different values of $x_0$, $A$, and $d = 10$. The values are given for different increments of $a$. The RMSE values are calculated for various values of $x_0$ ranging from 10 to 100, with increments of 10. The values of $A$ range from 0.0001 to 0.001, and $d = 10$. The RMSE values are given for different increments of $a$. The table is organized in a way that allows for easy comparison of the RMSE values across different values of $x_0$, $A$, and $d = 10$. The RMSE values are given in a numeric format, and the table is designed to be easily readable and interpretable.
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Table B.5: RMSE values for the variation of $x_0$ and $a = 100$. 
## Appendix B. Transient memristor model

### Table B.6: Range of the parameters $x_0$, $A$, and $a$.

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Table B.7: Range of memristance using different parameter values. $\omega = 1$.

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## Appendix B. Transient memristor model

### Table B.8: Range of memristance using different parameter values. $\omega = 10$

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Table B.9: Range of memristance using different parameter values ω=100.

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