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Nanotechnology **20** (2009) 045201 (7pp) doi:10.1088/0957-4484/20/4/045201

The mechanism of electrical annihilation of conductive paths and charge trapping in silicon-rich oxides

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Received 31 July 2008, in final form 13 November 2008
Published 18 December 2008
Online at stacks.iop.org/Nano/20/045201

Abstract

The electrical properties of silicon-rich oxide (SRO) films in metal–oxide–semiconductor-like structures were analysed by current versus voltage (I–V) and capacitance versus voltage (C–V) techniques. SRO films were thermally annealed to activate the agglomeration of the silicon excess in the form of nanoparticles (Si-nps). High current was observed at low negative and positive voltages, and then at a certain voltage (V_{drop}), the current dropped to a low conduction state until a high electric field again activated a high conduction state. C–V measurements demonstrated a capacitance reduction at the same time as the current dropped, but without appreciable flat-band voltage (V_{FB}) shifting. The reduction in capacitance and current was also observed after applying an electrical stress. These effects are ascribed to the annihilation of conductive paths created by Si-nps. An equivalent circuit is used to explain the capacitance and current reductions. Finally, the conduction mechanism is also analysed by making use of trap assisted tunnelling and Fowler–Nordheim tunnelling at low and high electric fields, respectively.

1. Introduction

Potential applications of nanostructured silicon either embedded in a SiO_2 or Si_3N_4 matrix have attracted a great interest between researchers. Silicon-based light emitters (LED's) [1–3], detectors [4], and memories [5–7] are some of their interesting characteristics demonstrated. Different techniques have been reported in order to obtain silicon nanoparticles (Si-nps). However, compatible techniques with complementary metal–oxide–semiconductor (CMOS) technology are desired to obtain Si-nps, therefore plasma enhanced chemical vapour deposition (PECVD) [1–3, 8], low pressure chemical vapour deposition (LPCVD) [4–6, 9] and silicon ion implantation into silicon-based dielectrics [7, 10, 11] are the most commonly technologies used.

Silicon-rich oxide (SRO) films are easily deposited by PECVD and LPCVD techniques using nitrous oxide (N_2O) and silane (SiH_4) as reactant gasses. After SRO films are thermally annealed at high temperature, phase separation between Si and SiO_2 occur creating Si-nps [1–7]. Light emission and charge trapping properties of SRO films depend on the Si-np's size. SRO films containing big Si-nps (∼5 nm) exhibit a strong charge trapping and luminescence of low intensity [6, 12], meanwhile SRO films containing smaller Si-nps (∼2 nm) exhibit single electron trapping effects and a strong luminescence [12, 13].

In recent studies, SRO films deposited by LPCVD (SRO–LPCVD) with low silicon excess have shown more intense photoluminescence (PL) than with high silicon excess [12, 14]. Indeed, a spectroscopical analysis has revealed the amorphous nature of the Si-nps embedded in SRO films with low silicon excess [12]. Studies on amorphous silicon nanoparticles obtained by PECVD (SRO–PECVD) have demonstrated interesting electrical and electro-optical properties [3]. However, SRO-PECVD films must be thermally annealed at a higher temperature than SRO-LPCVD films in order to obtain intense PL. Moreover, SRO–LPCVD films emit a stronger PL than SRO–PECVD and Si implanted SiO_2 films [14, 15]. Additionally, in Si-nps-based LEDs, thin SRO films are needed to obtain low voltages of operation.

However, PECVD have a limitation in the deposition rate (r); r in PECVD is faster than in LPCVD, so LPCVD process—compared with PECVD—allows a much better control of the deposited layers' thickness. Nevertheless, in order to get functional and novel devices based on thin SRO–LPCVD films, a study on their electrical properties is still necessary.

In this work, the electrical properties of SRO films deposited by LPCVD with low silicon excess and thermally annealed at 1100 °C are studied. Current versus voltage (I–V) and capacitance versus voltage (C–V) characteristics of SRO films were measured using MOS-like structures with three different gate areas. Several operating regimes have been observed upon characterization. These regimes can be related to the presence and annihilation of conduction paths created by Si-clusters (Si-cls) within the silica matrix, where the formation of neutral defects (E′ centres [16]) can be playing an important role.

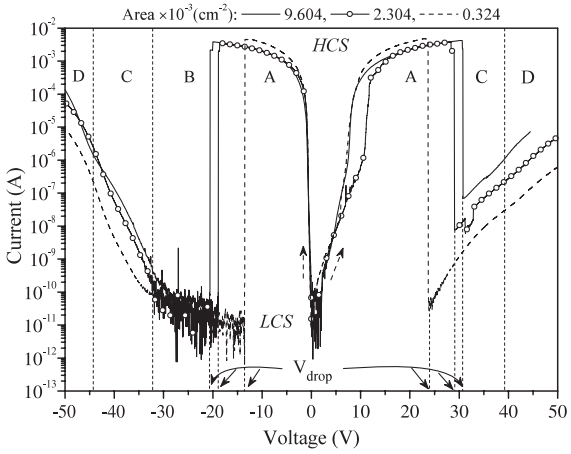

Figure 1. I–V curve measured with a sweep rate of 0.1 V s^{-1} on as-fabricated MOS-like structures with different gate area. Sweep direction is indicated by the dashed arrows.

2. Experiment

SRO films with expected thickness of 50 nm were deposited using a LPCVD hot wall reactor on (100), 0.1–1.4 Ω cm p-type silicon wafers. Nitrous oxide (N_2O) and 5%-nitrogen (N_2) diluted silane (SiH_4) were used as the reactant gasses. Si-excess in the deposited films is controlled by the ratio of partial pressure of the reactant gases, as equation (1).

$$R_0 = \frac{P(N_2O)}{P(SiH_4)} \tag{1}$$

$R_0 = 30$ was used for this experiment. The deposited SRO film contains an average silicon excess of about 4 at.% as estimated from XPS measurements [12]. After deposition, a thermal annealing at 1100 °C in N_2 atmosphere was carried out for 3 h in order to induce the Si-excess agglomeration. The thickness of the annealed SRO films, measured with a Gaertner L117 ellipsometer (incident laser wavelength of 632.8 nm), is about 53 ± 3 nm.

1 μm thick Al/Cu backside contacts were formed by sputtering and a 350 nm thick n+ polysilicon gate was deposited to form MOS-like structures, Si/SRO/PSi. Three different gate areas were patterned. The area of gate electrodes are 9.604×10^{-3}, 2.304×10^{-3}, and 3.24×10^{-4} cm^2.

Current–voltage (I–V) measurements were done using a HP4155B semiconductor parameter analyzer. All high frequency capacitance–voltage (C–V) measurements were performed from inversion to accumulation at 100 kHz (sine wave with 30 mV of amplitude) using a computer-controlled HP4192A impedance analyzer. I–V and C–V measurements were done alternately, as well as before and after applying a constant gate voltage $V_G = V_{drop}$. All the electric measurements were carried out at room temperature in dark using a Karl Suss PA200 probe system.

3. Results

Figure 1 exhibits the typical I–V curve measured in as-fabricated devices with different gate areas. A high current conduction is measured at low voltages, at both negative (forward bias, FB) and positive bias (reverse bias, RB). However, at certain voltage (V_{drop}) the current drops (regardless on the sweep rate) from a high conduction state (HCS) to a low conduction state (LCS). Afterwards, the current enters in a high electric field conduction regime. At FB, four different regions can be identified as A, B, C, and D corresponding to [0 to ∼−21 V], [∼−21 to ∼−32 V], [∼−32 to ∼−44 V] and [∼−44 to ∼−50 V], respectively, for a gate area of 9.604×10^{-3} cm^2. The B zone is the region where the current remains at some pA (LCS) after dropping from 10^{-3} A. Additionally, in C region, a steady current increase behaviour with bias is observed, which is continued on D with a slightly different slope. At RB, the A, C and D zones are also present. Furthermore, in reverse bias, drop of current occurs at higher voltages compared to that at forward bias. In the A zone (low electric fields) the current exhibits a strong dependence on the gate voltage. In this region, tunnelling mechanisms such as Fowler–Nordheim (FN) [6, 10] or Pool–Frenkel (PF) [3, 10] should be excluded because of the SRO thickness. Therefore, other conduction mechanism should be responsible for that current observed; the trap assisted tunnelling (TAT) [18] being the most probable. Meanwhile, in C and D zones the electric field inside the oxide is strong enough (>6 MV cm^{-1}) to cause a strong band bending, so electrons tunnel through a triangular barrier from the polysilicon gate towards the silicon substrate.

Figure 2(a) shows the voltage of occurrence of each zone at FB as a function of the gate area. The gate voltage at which current drops (V_{drop}), which splits A and B zones, is observed at a more negative gate voltage (higher $|V_{drop}|$) as the gate area becomes larger; meanwhile C and D zones does not seem to depend on the gate area. As observed, the V_{drop} mean values are −23, −18 and −13 V for each gate area of 9.604×10^{-3}, 2.304×10^{-3}, and 3.24×10^{-4} cm^2, respectively.

The time dependence of current through the SRO MOS-like devices, biased at $V_G = V_{drop}$ can be seen in figure 2(b). A HCS (∼10^{-3} A) is observed during 40.7, 25.8 and 10.3 s before it drops to a LCS for each gate area, respectively. Therefore, the current dropping can be obtained either during the voltage sweep or by applying a fixed gate voltage $V_G = V_{drop}$.

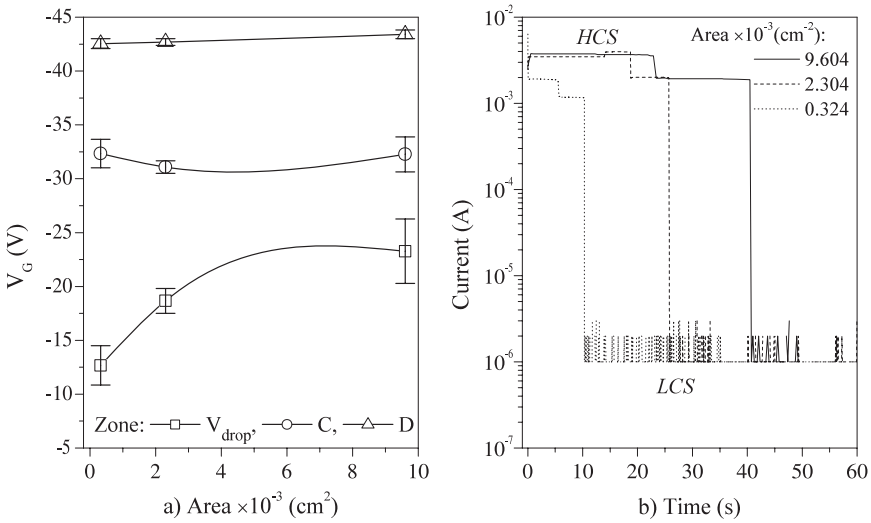

Figure 2. (a) Voltage of occurrence of the different zones as a function of the gate area (lines are plotted as an eye-guide), and (b) I–t curves at a gate voltage $V_G = V_{drop}$ of different MOS-like structures.

The switching behaviour between the HCS and LCS has been observed previously by other authors and it is known as negative differential resistance (NDR) [8]. Theoretical studies on the transport properties through a clusters' array have shown similar results [17]. A '*Coulomb Blockade Gap*' (CBG) was observed, similar to the B zone in figure 1. Its origin was attributed to the formation of a trapped-electron configuration or the stationary charge configuration (SCC) where charge trapped on the Si-nps blocks the electrical conduction. Then, a charge trapping phenomenon could be affecting the current of the devices in this work.

In order to estimate the electrical influence on the Si-nps embedded in the SRO films, C–V hysteresis curves were performed (not shown) with the voltage swept in both directions, that is, from inversion to accumulation and back to inversion. However, no flat-band voltage shifting was observed as one should expect from an oxide layer with nanoparticles [5, 6]. Rather than being trapped charges seem to flow through the SRO films. Then, C–V measurements were repeated in pursue of a charge trapping effect. This time a constant gate voltage $V_G = V_{drop}$ was applied on as-fabricated devices; the variations of the C–V curves are resumed in figure 3.

Measurements done on devices without any electrical stress showed a maximum capacitance of 732.3, 275.6, and 208.5 pF for each gate area of 9.604×10^{-3}, 2.304×10^{-3}, and 3.24×10^{-4} cm^2, respectively. After stressing the devices with a gate voltage of $V_G = V_{drop}$, the capacitance drops, homogeneously, to a lower value, for all bias. Hence current and capacitance dropping are directly correlated. Although such capacitance reduction might be related to a charge trapping phenomenon, no changes have been measured on the flat-band voltage (V_{FB}).

Figure 4(a) shows the typical I–V curves measured from devices with gate area of 9.604×10^{-3} cm^2, before and after the current has dropped. First, in as-fabricated devices, the current exhibits the same behaviour as reported in figure 1. However, a subsequent I–V measurement, on the same device, exhibits a very low level current of about 10^{-12} A in both A and B zones. This effect could be explained by the annihilation of conductive paths in the SRO film, which connect the silicon substrate

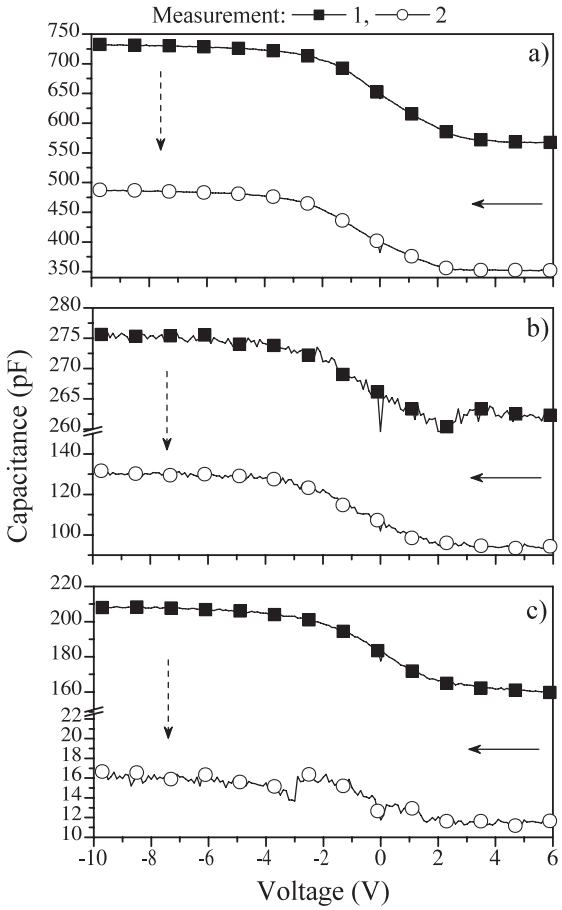

Figure 3. C–V characteristic (1) before and (2) after applying a constant electrical stress $V_G = V_{drop}$ for 60 s on the MOS-like structures with gate area of (a) 9.604×10^{-3} cm^2, (b) 2.304×10^{-3} cm^2, and (c) 3.24×10^{-4} cm^2. All measures were done from inversion to accumulation at 100 kHz and with a sweep rate of 0.1 V s^{-1}.

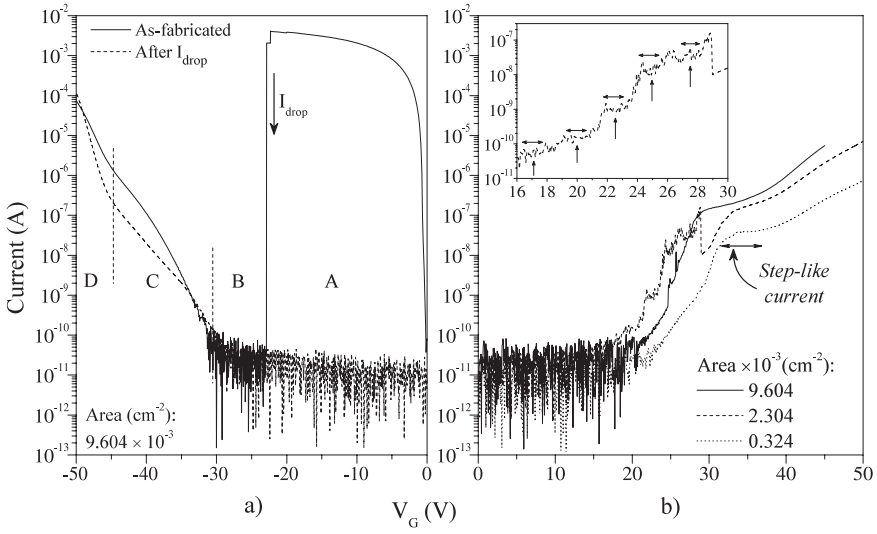

Figure 4. I–V characteristic of (a) MOS-like devices with gate area of 9.604×10^{-3} cm^2 under accumulation, before and after the current drop and on the (b) MOS-like devices with different gate area under inversion after applying a constant electrical stress $V_G = V_{drop}$ for 60 s. Inset shows the staircase-like current measured for the structure with gate area of 2.304×10^{-3} cm^2. All measures were done with a sweep rate of 0.1 V s^{-1}.

with the polysilicon gate. As the gate voltage becomes more negative, C and D regions are obtained.

Figure 4(b) shows the I–V curves from MOS-like devices with different gate areas after applying a constant electrical stress $V_G = V_{drop}$ for 60 s. The applied gate voltage $V_G = V_{drop}$ was -23, -18 and -13 V for each gate area of 9.604×10^{-3}, 2.304×10^{-3}, and 3.24×10^{-4} cm^2, respectively. This current behaviour was obtained with a positive voltage sweep after the current had already dropped. At low voltages ($<$20 V), the current oscillates at a low level ($<10^{-10}$ A) for all gate areas. For gate voltages $V_G \geqslant 20$ V, the current increases until a step-like behaviour is observed at about 29 V for devices with the largest gate area (9.604×10^{-3} cm^2) and about 32 V for the two smaller ones. This step-like current is almost constant (as marked by the arrow in figure) until entering into the high field conduction regime. Similar current behaviours have been reported [2, 3] and ascribed to charge trapping in a Si-ncs layer through tunnelling and a consequent Coulomb blockade effect on the charges trying to tunnel behind. Then, in these SRO films charges could be getting trapped during the sweep voltage. In fact, the I–V curve measured from the device with gate area of 2.304×10^{-3} cm^2 exhibits a clear staircase-like behaviour between 16 and 28 V, as shown in the inset of figure 4(b). A slightly staircase current can be also observed for the MOS-like devices with the largest gate area. This quantum phenomenon is due to Coulomb blockade (CB) effects as a result of single electron trapping in the silicon nanoparticles embedded in the SRO film [9, 13].

4. Discussion

Si nanoparticles in SRO films are produced by the diffusion and agglomeration of Si-excess at high temperature. That is, when SRO films are thermally annealed, the silicon atoms diffuse creating silicon clusters [nanoparticles (Si$_n$, $n \geqslant 3$)] at nucleation sites [14, 15].

Annealed SRO films with Si-excess similar to this experiment have been shown to contain embedded Si-nps with $\sim$1 nm estimated size [13]. However, due to the low silicon excess and assuming a dispersion in the Si-nps' size, other very small Si-nps (with few Si atoms bonded, $<$1 nm) could exist. Then, in order to understand our results, we differentiate nanostructures in: small ones ($<$1 nm) 'clusters' and big ones ($\geqslant$1 nm) 'nanoparticles'. It is expected that all of these Si-nps and Si-clusters (Si-cls) could be randomly distributed; such as a mix in which some of the Si-cls could be located between Si-nps. In this model, we assume that the tunnelling current is not uniformly distributed through the whole capacitor area, instead of this; it flows through narrow conductive paths within the oxide.

In C–V curves, a vertical shift of capacitance was obtained after the current dropped, but no shift was observed in the flat-band voltage (V_{FB}). Similar effects have been observed by other authors [7] ascribing them mainly to charge trapping in Si-ncs. However, if charge gets trapped in a SiO_2 matrix with embedded Si-nps, it should produce a V_{FB} shifting in the C–V curves [5, 6]. In this experiment, a V_{FB} shifting was obtained only when the devices were biased right after the current had dropped.

Figures 5(a) and (b) display, respectively, the C–V curves and the flat-band voltage before and after electrical stressing MOS-like devices with gate area of 9.604×10^{-3} cm^2. When the as-fabricated device is stressed with a gate voltage of $V_G = V_{drop}$ (-25 V in this case), the capacitance reduces, as shown in figure 5(a). After that, the same device was biased at several gate voltages and two trends can be clearly observed: first, the C–V curve exhibits a positive shift for electrical stresses of $V_G = 20$–30 V, indicating electrons trapping. Coincidently this voltage range correlates with that where the staircase current was observed (see the inset of figure 4(b)). Therefore, that behaviour can be related to electrons trapped in Si-nps.

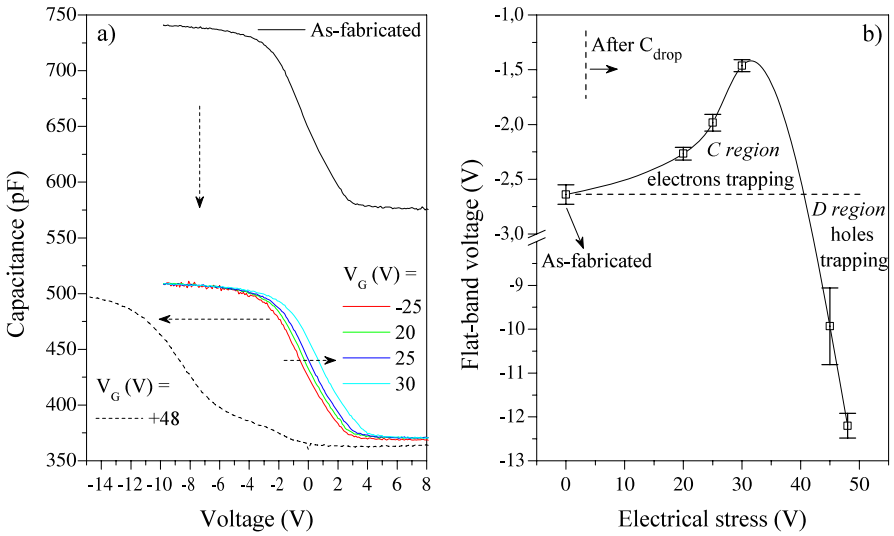

Figure 5. (a) C–V curves and (b) flat-band voltage before and after applying a constant electrical stress for 60 s on the MOS-like structure with gate area of 9.604×10^{-3} cm^2. All measures were done from inversion to accumulation at 100 kHz with a sweep rate of 0.1 V s^{-1}. (This figure is in colour only in the electronic version)

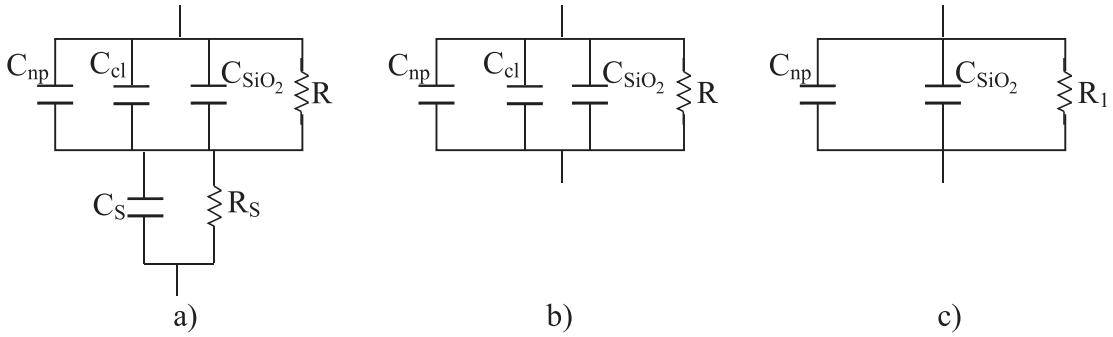

Figure 6. Equivalent circuits of SRO MOS-like structures (a) without any electrical stress and in accumulation region (b) before and (c) after the current and capacitance dropping.

Second, the C–V curve shifts toward negative voltages when a higher electrical stress ($V_G = +48$ V) is applied, indicating that holes are trapped. Charge trapping can be correlated with C and D zones, as marked in figure 5(b). Both electrons' and holes' trapping seem to occur in Si-nps which remain after the current drops. The size of these remaining Si-nps into the SRO films from this work can be also estimated from the stair width of the staircase current observed in the inset of figure 4(b) using the equations reported in [13]. The mean value of the stair width (V_{stair}) is $\sim$1.21 $\pm$ 0.06 V. If the distance between Si-nps (t_{np-np}) is close to $\sim$10 nm, then the size of Si-nps is about 1.15 $\pm$ 0.06 nm, which is a value close to the reported before [13].

On the other hand, in as-fabricated devices, if the distance between Si-nps and Si-cls is quite small, they can act as nodes for electrical conduction paths between the polysilicon gate and the Si-substrate making possible the high current conduction at low voltages. Therefore, the only possible reason for the capacitance and current reduction is a change in the conductivity of the films by the annihilation of such conductive paths. A particular case may be depicted by the E′ centres formation in SRO films [16]. E′ centres can be created in the SRO films when charges are injected into the film breaking-off Si–Si bonds during a voltage sweep or an electrical stress. It has been reported that most of E′ centres in SiO_2 are neutral [19]. This would explain why the capacitance drops without a noticeable V_{FB} shifting.

Table 1. Experimental accumulation capacitance of MOS-like structures before and after an electrical stress. The theoretical maximum capacitance of a SiO_2 film with the same thickness than the SRO film is also reported.

	Experimental C_{SRO} (pF)		
Gate area (cm^2)	Measure 1 As-fabricated	Measure 2 After $V_G = V_{drop}$	Theoretical C_{SiO_2} (pF)
9.604×10^{-3}	708 ± 26	495 ± 7	621
2.304×10^{-3}	269 ± 7	131 ± 1	149
3.24×10^{-4}	212 ± 7	18 ± 2	21

The values of the mean capacitance in accumulation measured before and after stressing the MOS-like structures are listed in table 1.

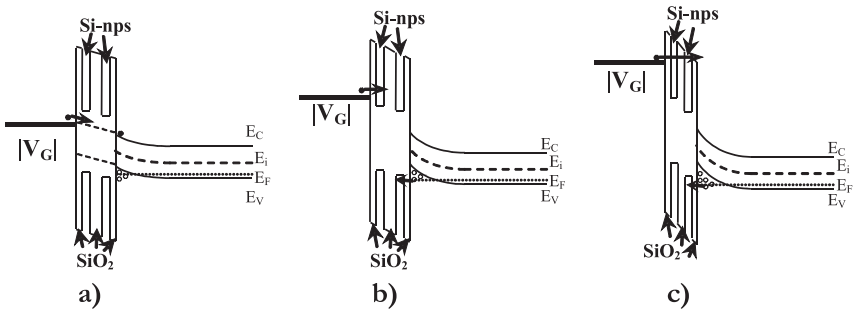

Figure 7. Band energy diagram of the SRO MOS-like structure at forward bias and gate voltages of (a) $|V_G| < |V_{drop}|$ (A region), (b) $|V_G| > |V_{drop}|$ (C region), and (c) $|V_G| \gg |V_{drop}|$ (D region).

The theoretical values of the silicon oxide capacitance of equivalent MOS-like structures (C_{SiO_2}) are also listed in table 1 being 621, 149 and 21 pF for each gate area of 9.604×10^{-3}, 2.304×10^{-3}, and 3.24×10^{-4} cm^2, respectively. These values of capacitance for a SiO_2 film, as calculated for each gate area, are smaller than the SRO capacitance measured from as-fabricated devices. Nevertheless, the theoretical capacitance is slightly close to the mean value of the capacitance measured after applying a $V_G = V_{drop}$ (measure 2), as reported in table 1.

Therefore, the total capacitance (C_T) of these MOS-like structures might be given by the combination of the capacitance of the SRO film (C_{SRO}) in series with the capacitance of silicon substrate surface (C_S), where C_{SRO} represents the sum of the Si-nps (C_{np}), Si-cls (C_{cl}), and SiO_2 (C_{SiO_2}) capacitances as depicted in the equivalent circuit shown in figure 6(a), where the total capacitance is given by:

$$C_T = \frac{C_{SRO}C_S}{C_{SRO} + C_S} = \frac{\left(C_{np} + C_{cl} + C_{SiO_2}\right) C_S}{C_{np} + C_{cl} + C_{SiO_2} + C_S}. \qquad (2)$$

At negative gate voltages ($V_G < 0$), that is, when the devices are in accumulation region, C_S is much higher than C_{SRO} and thus, the total capacitance is dominated by the SRO capacitance, i.e., $C_T = C_{SRO} = C_{np} + C_{cl} + C_{SiO_2}$, as depicted in figure 6(b), where the resistance R is the sum of Si-nps, Si-cls, and SiO_2 resistances as $R^{-1} = R_{np}^{-1} + R_{cl}^{-1} + R_{SiO_2}^{-1}$. As the silica resistance is expected to be quite high, $R_{cl} < R_{np} \ll R_{SiO_2}$, we can assume that the Si-nps and Si-cls contribution to the total resistance should be prevalent, such as $R = \sim(R_{np} + R_{cl})$.

In as-fabricated devices there is a plenty of Si-nps and Si-cls which contribute increasing the capacitance. However, an electrical anneal, which drastically diminishes the Si-cls contribution (E′ centres formation), can be produced by applying $V_G = V_{drop}$ for 60 s or during a sweep voltage in I–V measurements. As a result, C_{cl} becomes very small or annihilated and the total capacitance is consequently decreased, getting close to C_{SiO_2}, as shown in figure 3 and depicted by the equivalent circuit from figure 6(c). Now, $R = R_1 = \sim(R_{np} + R_{SiO_2})$. Then, R increases and the capacitance effect in the MOS-like devices becomes dominant, which is corroborated by the shift of V_{FB}.

Depending on the operation voltage zone, three different conduction mechanisms (A, C and D) can be identified. Figure 7 shows the energy band diagram of MOS-like structures for each of these regions. In A zone, for as-fabricated devices, the current exhibited a strong dependence on the gate voltage. Then, Si-cls could act as traps near to the mid-gap of SRO film making possible the high current conduction at low voltages, as shown in figure 1 and schematized by the energy band diagram in figure 7(a). In this zone, current fits well to the TAT model as [18]:

$$J = J_0 e^{(B/E)} \qquad (3)$$

where E is the electric field through the SRO film. For the MOS-like structure with the largest gate area (9.604×10^{-3} cm^2), values of $J_0 = 0.6$ and 3.2 A cm^{-2} and $B = 1.435$ and 9.82 MV cm^{-1} were found for negative and positive bias, respectively.

During the sweep at negative (positive) voltages, electrons from polysilicon gate (Si-substrate) tunnel into the SRO film through the conductive paths. When charges are flowing through the Si-cls, they break-off some of the Si–Si bonds (E′ centre), annihilating in that way the conductive paths and leading to current drops. The difference between the voltage needed to obtain the current dropping at forward and reverse bias is related to the P-type Si-substrate. As observed before, V_{drop} increases as the gate area becomes larger. Then, V_{drop} could be directly related to the number of conductive paths. As the gate area is increased, the number of conductive paths increases as well and a larger voltage is needed to annihilate them.

Once the current has dropped (at V_{drop}), the SRO conductivity changes. Conductive paths are now available only through more stable Si-nps (∼1.15 nm in size), and higher voltages are required to inject charge through the SRO film.

For high voltages—C and D regions—at both forward and reverse biases, Fowler–Nordheim plots were used to fit data, see figure 8. Data fits quite well at both C and D regions with FN conduction regimes for both FB and RB, as shown in figures 8(a) and (b), respectively.

At C region, the conduction is dominated by the flow of electrons from the polysilicon gate (Si-substrate) towards the Si-substrate (polysilicon gate) as illustrated in figure 7(b); meanwhile as the gate voltage becomes higher (D region), electrons tunnel directly toward the Si-substrate from the polysilicon and the flow of holes is enhanced increasing the conductivity, see figure 7(c). At these regions, some electrons

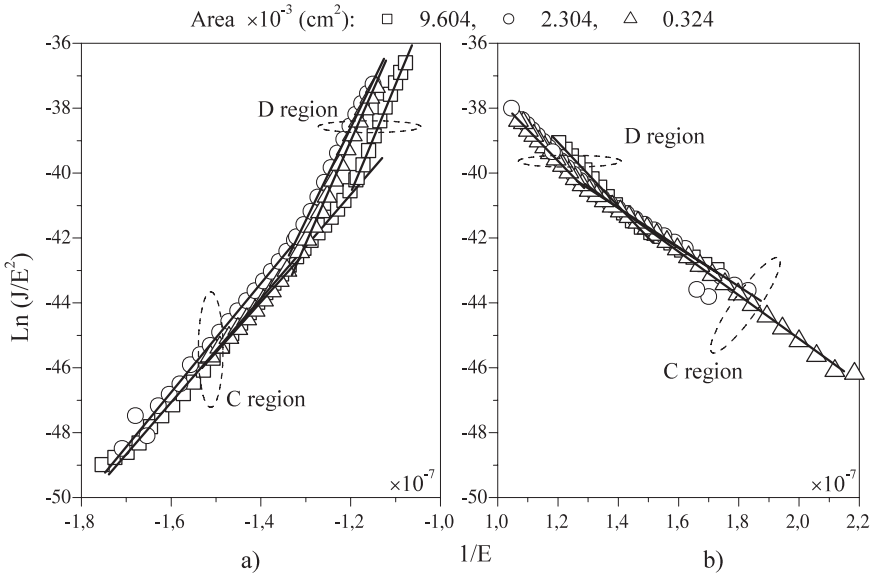

Figure 8. FN plots at (a) forward and (b) reverse bias from devices with three different gate areas where a linear region in high voltages is observed. Symbols and lines are the experimental data and linear fits, respectively.

(C region) and holes (D region) can get trapped in Si-nps resulting in the shift of the flat-band voltage (see figure 5). Once the current has dropped, the conduction observed at high electric fields fits as well the Fowler–Nordheim tunnelling model.

5. Conclusion

Electrical properties of annealed silicon-rich oxide films were studied and analysed using MOS-like structures with different gate areas. Reduction of current and capacitance was observed at specific voltages. A clear correlation between the reduction in capacitance and current was observed. This phenomenon was the result of an electrical anneal of the SRO layers, and was produced by the annihilation of conductive paths. Moreover, this anneal was related to the creation of E′ defects in the SRO layer. Charge trapping was only observed after the capacitance reduction. The current conduction mechanism though the SRO film was also analysed. The high current measured in low voltages was related to trap assisted tunnelling, meanwhile for high voltages Fowler–Nordheim tunnelling was observed.

Acknowledgments

Mr A Morales-Sánchez and Mr J Barreto acknowledge the grants received from CONACYT and CSIC (I3P), respectively. This work has been partially supported by the project TEC2006-13907/MIC, financed by the Spanish Ministry of Education and Science and P2005MX03 financed by the CSIC/CONACYT.

References

[1] Barreto J, Perálvarez M, Rodríguez J A, Morales A, Riera M, López M, Garrido B, Lechuga L and Domínguez C 2007 *Physica* E **38** 193
[2] Franzò G, Irrera A, Moreira E C, Miritello M, Iacona F, Sanfilippo D, Di Stefano G, Fallica P G and Priolo F 2002 *Appl. Phys.* A **74** 1
[3] Irrera A *et al* 2006 *Nanotechnology* **17** 1428
[4] Berman-Mendoza D, Aceves-Mijares M, Berriel-Valdos L, Domínguez-Horna C, Pedraza J, Falcony C and Carranza J 2005 *Nanotechnology* **3** 313
[5] Salonidou A, Nassiopoulou A G, Giannakopoulos K, Travlos A, Ioannou-Sougleridis V and Tsoi E 2004 *Nanotechnology* **15** 1233
[6] Kouvatsos D N, Ioannou-Sougleridis V and Nassiopoulou A G 2003 *Mater. Sci. Eng.* B **101** 270
[7] Ng C Y, Liu Y, Chen T P and Tse M S 2006 *Smart Mater. Struct.* **15** S43
[8] Park N M, Kim S H, Maeng S and Park S J 2006 *Appl. Phys. Lett.* **89** 153117
[9] Yu Z, Aceves M and Ipiña M A 2006 *Nanotechnology* **17** 3962
[10] Kameda E, Matsuda T, Emura Y and Ohzone T 1998 *Solid-State Electron.* **42** 2105
[11] Barreto J, Perálvarez M, Morales A, Garrido B, Montserrat J and Domínguez C 2008 *J. Mater. Res.* **23** 1513
[12] Morales A, Domínguez C, Barreto J, Riera M, Aceves M, Luna J A, Yu Z and Kiebach R 2007 *Rev. Mex. Fís.* S **53** 279
[13] Morales-S ánchez A, Barreto J, Domínguez C, Aceves M, Yu Z and Luna-López J A 2008 *Nanotechnology* **19** 165401
[14] Morales A, Barreto J, Domínguez C, Riera M, Aceves M and Carrillo J 2007 *Physica* E **38** 54
[15] Flores F, Aceves M, Carrillo J, Domínguez C and Falcony C 2005 *Superficies y Vacío* **18** 7
[16] Lelis A J and Oldhan T R 1994 *IEEE Trans. Nucl. Sci.* **41** 1835
[17] Shin M, Lee S, Park K W and Lee E H 1999 *Phys. Rev.* B **59** 3160
[18] Perera R, Ikeda A, Hattori R and Kuroki Y 2003 *Microelectron. Eng.* **65** 357
[19] Afanas'ev V V and Stesmans A 2000 *J. Phys.: Condens. Matter* **12** 2285