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Analysis of the impact of the drain-junction tunneling effect on a microwave MOSFET from *S*-parameter measurements

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ABSTRACT

A procedure to analyze the effect of the MOSFET drain-bulk junction tunneling current at high frequencies is presented. This procedure allows identifying the presence of band-to-band tunneling in short channel-length MOSFETs at different drain-to-source voltages. Since this analysis is based on experimental *S*-parameters performed to a single MOSFET, the procedure is not affected by the variations occurring in devices with different geometries. Excellent correlation between simulated and experimental output impedance for a 0.1 μm channel-length bulk MOSFET up to 40 GHz demonstrates the validity of the proposed technique.

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1. Introduction

Nowadays, MOSFET characterization is important among several aspects to improve compact models, to optimize device and circuit design, and to reduce the leakage currents reducing the power efficiency of electronic systems. As pointed out in recently published literature [1], the reduction of the leakage current plays a fundamental role in the transistor and circuit design for low-power CMOS applications. Moreover, due to the increased demand for high-speed electronics products, the accurate modeling of the MOSFET at high frequencies (HF) is necessary to represent the behavior of this device in microwave circuits and systems [2]. However, as the operation frequency continues to increase and the channel length to reduce, higher order effects make increasingly difficult to represent the electrical behavior of the MOSFET at HF. In this case, one of the characteristics that has to be accurately represented is the output impedance [3]. Several parameters that influence the MOSFET's output characteristics have been previously analyzed in the literature, such as the source/drain parasitic resistances, and the substrate impedance [4–6]. In fact, some of the effects that become apparent at HF have been directly associated to these parameters to keep the modeling simple and analytical [7].

As is well known, the MOSFET HF characterization based on the measurement of two-port *S*-parameters allows the determination of the equivalent-circuit model parameters, and several techniques have been reported to obtain MOSFET's intrinsic and extrinsic parameters. Therefore, using an *S*-parameter measurement-based characterization helps to identify the effects occurring within the device when associating the model parameters with physical phenomena. As the MOSFET dimensions shrink, more of these effects become apparent and have important influence in the device performance. Thus, the proper determination of the associated parameters is necessary to accurately predict the device's behavior under a wide variety of conditions. One of these high-order effects taking importance as the channel-length shrinks to nanometric dimensions is the band-to-band tunneling (BTBT) occurring in the drain-bulk junction. Thus, using measured *S*-parameters to obtain the model parameters associated with this effect is desirable to assess the performance of the device, but also to represent the corresponding behavior under a small-signal regime. The importance of the BTBT effect relies on the fact that the MOSFET's output characteristics are affected with the corresponding tunneling current at relatively high drain-to-source voltages, which considerably affects the performance of short-channel devices. In fact, previously reported experimental analyses have considered this effect in SOI MOSFETs [8] and in field-induced band-to-band tunneling effect transistors (FIBTET) [9]. These previous analyses of the BTBT effect have been performed using regression methods applied to DC measurements of several devices, assuming that this effect remains

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constant with the channel length. Until now, however, the potential of S-parameter measurements performed to single devices to carry out an analysis of the BTBT effect has not been explored.

In this paper, we use small-signal S-parameter measurements to identify and quantitatively determine the impact of BTBT originated at the drain-bulk junction of a MOSFET. We confirmed the presence of the BTBT effect through an exhaustive analysis of the experimental MOSFET's small-signal parameters up to 40 GHz. For this reason, we also propose a straightforward parameter extraction procedure that allows identifying the dominant effects influencing the device's output impedance. The proposed method is based on S-parameter measurements performed to a device biased at V_{gs} = 0 V and V_{ds} > 0 V. Using this method, we observe that an additional admittance must be included in the MOSFET HF equivalent-circuit model when considering BTBT. This admittance accounts for the current introduced by the band-to-band carrier tunneling effect occurring at the drain junction in short-channel devices [7], and allows a considerable improvement of the small-signal modeling of a MOSFET at high frequencies. The proposed methodology is validated through a correlation between simulated and experimental data for microwave MOSFETs fabricated in a 0.1 μm CMOS technology.

2. Experiments

A calibrated vector network analyzer was used to measure S-parameters to four common-source/bulk nMOSFETs fabricated on a p-type Si substrate. These devices have a channel mask length, L_m = 0.1 μm, two gate fingers (NF = 2), and finger widths W_f = 5, 10, 15, and 20 μm, respectively. Additional open and short dummy structures were used to correct the measurements from pad parasitics. The S-parameters were taken at V_{gs} = 0 V and V_{ds} = 0.3, 0.55, 0.8, and 1.05 V. The top view of the layout of the MOSFET RF test structure is presented in Fig. 1. Due to the lack of channel formation under the V_{gs} = 0 V condition, the impact of the parasitic currents flowing between drain and source when there is no channel can be analyzed using an equivalent-circuit approach explained hereafter.

3. Method formulation

Fig. 2 shows the model of a MOSFET biased at V_{gs} = 0 V that includes the intrinsic and extrinsic components. In this model, the source and drain parasitic resistances (R_s and R_d, respectively), the drain and source junction capacitances (C_{jd} and C_{js}, respectively), the gate resistance (R_g), and the substrate resistance (R_b) are considered as extrinsic elements, whereas the intrinsic part of the MOSFET is represented by means of three capacitances

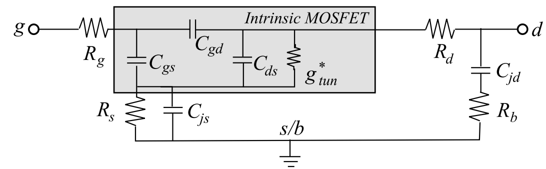

Fig. 2. Equivalent-circuit model for a MOSFET biased at V_{gs} = 0 V and V_{ds} > 0 V.

and a complex admittance (g^*_{tun}). The later is associated with the drain to bulk BTBT effect.

In the model presented in Fig. 2, all the extrinsic elements are considered as drain-bias independent. This assumption is valid for the source and drain parasitic resistances since the spreading and the accumulation resistances do not present a considerable variation with V_{ds} at V_{gs} = 0 [10]. For the case of the drain and source junction capacitances, and for the substrate resistance, this assumption is also reasonable due to the high doping of the p–n junction associated with the drain and source regions. Besides, accurate results have been obtained when assuming drain-to-source voltage independence of the substrate parameters [5].

In order to determine the substrate parameters, the equivalent circuit of Fig. 2 can be used. When V_{ds} = 0 V is assumed, the effect of g^*_{tun} can be neglected, and the typical assumptions considered under zero-bias cold-FET conditions allow to arrange the equation associated with the real part of Z_{22} in the form [5]

$$\frac{\omega^2}{\mathrm{Re}(1/Z_{22})} \approx R_b\omega^2 + \frac{1}{C_{jd}^2 R_b} \quad (1)$$

where ω is the angular frequency in radians. Thus, R_b and C_{jd} can be determined, respectively, from the slope and the intercept with the abscises of a linear regression of the experimental ω^2/Re(1/Z_{22}) versus ω^2 data.

Once R_b and C_{jd} have been obtained, the corresponding effect is removed from the experimental data by applying the following equation:

$$\mathbf{Y}_A = \mathbf{Y}_{meas} - \begin{bmatrix} 0 & 0 \\ 0 & \frac{\omega^2 C_{jd}^2 R_b}{1+\omega^2 C_{jd}^2 R_b^2} + \frac{j\omega C_{jd}}{1+\omega^2 C_{jd}^2 R_b^2} \end{bmatrix} \quad (2)$$

where $\mathbf{Y}_{meas}$ represents the Y-parameter matrix obtained from the direct transformation of measured S-parameters into Y-parameter data, whereas $\mathbf{Y}_A$ represents the Y-parameter matrix after the effect of R_b and C_{jd} has been removed from the measurements.

In [11], a procedure to obtain the source and drain resistances was proposed. Using this method, the bias-dependent series resistances were determined allowing good simulation-experiment correlation as presented in the results section. Thus, after R_s and

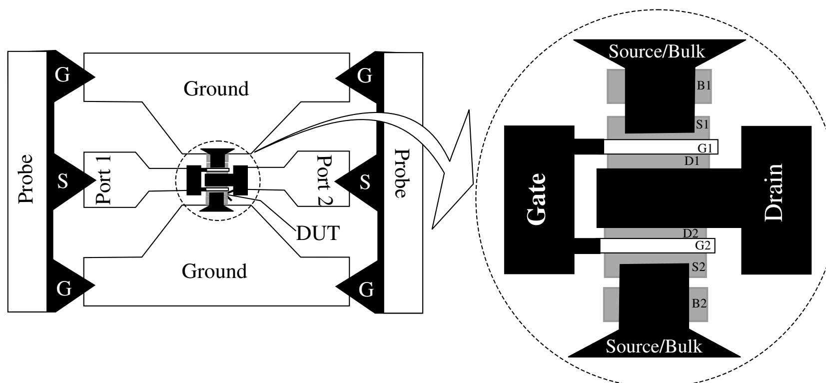

Fig. 1. Sketch showing the top view of the MOSFET RF test structure.

R_d are extracted, the corresponding effects are de-embedded from the experimental data by applying the following equation:

$$\mathbf{Z}^* = \mathbf{Z}_A - \begin{bmatrix} R_g & X - j\omega C_{js}R_sX \\ X - j\omega C_{js}R_sX & R_d \end{bmatrix} \quad (3)$$

where

$$X = \frac{R_s}{1 + \omega^2 C_{js}^2 R_s^2} \quad (4)$$

$\mathbf{Z}_A$ is the Z-parameter transformation of $\mathbf{Y}_A$ and $\mathbf{Z}^*$ is the corresponding Z-parameter matrix after removing the effect of the extrinsic resistances. In the Eq. (3), $C_{jd} \approx C_{js}$ is considered since, as can be seen in Fig. 1, the devices under investigation were designed to be symmetrical (i.e. the total area and perimeter of the drain junctions are the same to those of the source junctions).

After removing the effect of the extrinsic parameters from the measured data, the reference plane of the experimental data is shifted down to the MOSFET's intrinsic part. In this case, previously reported simplified approaches consider the intrinsic behavior of the device as purely capacitive even for high values of V_{ds}. This means that the real part of the Y-parameters associated with the MOSFET intrinsic part should be approximately equal to zero. However, as shown in Fig. 3, a sinusoidal behavior of the experimentally determined real part of the intrinsic Y_{22}^* parameter is observed when plotted versus frequency. This suggests that an additional current flow from the intrinsic drain to source (in parallel with C_{ds}) has to be considered. According to the analysis presented in the results section, this current is associated with the BTBT effect occurring in the depletion region at the drain side [7]. The following theoretical analysis allows verifying the implications of this current when the MOSFET operates at high frequencies.

According to Fig. 2, when the admittance g_{tun}^* is connected in parallel with C_{ds}, Y_{22}^* can be expressed by means of

$$Y_{22}^* = g_{tun}^* + j\omega(C_{ds} + C_{gd}) \quad (5)$$

where g_{tun}^* is associated with the BTBT charge flow and is given by [12]

$$g_{tun}^* = g_{tun} e^{-j(\omega\tau_0 - \pi/2)} \quad (6)$$

In this equation, g_{tun} and τ_0 are, respectively, the magnitude and the phase delay introduced by the BTBT effect.

Notice that the Eq. (5) can be expanded in real and imaginary parts, which yields

$$\begin{aligned} g_{tun}^* &= g_{tun}\left[\cos\left(\omega\tau_0 - \frac{\pi}{2}\right) - j\sin\left(\omega\tau_0 - \frac{\pi}{2}\right)\right] \\ &= g_{tun}[\sin(\omega\tau_0) + j\cos(\omega\tau_0)] \end{aligned} \quad (7)$$

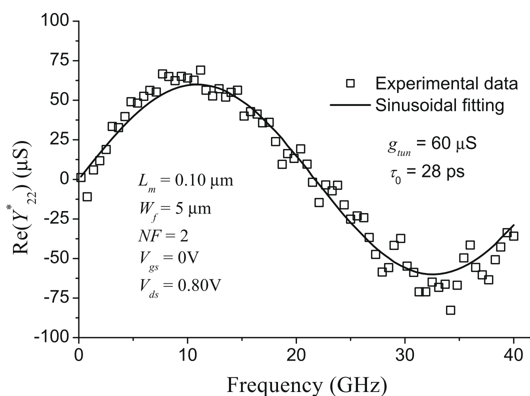

Fig. 3. Experimental Re(Y_{22}^*) versus frequency data showing a sinusoidal behavior. The solid line represents the fitting used to determine g_{tun} and τ_0.

Thus, the combination of (5) and (6) allows confirming that the real part of Y_{22}^* presents a sinusoidal form expressed by

$$\mathrm{Re}(Y_{22}^*) = g_{tun}\sin(\omega\tau_0) \quad (8)$$

As can be noticed, g_{tun} and τ_0 can be directly determined from the magnitude and phase velocity of a sinusoidal fitting of the experimental Re(Y_{22}^*) versus frequency data. This extraction is illustrated in Fig. 3.

Once g_{tun} and τ_0 have been determined, the intrinsic capacitances are directly obtained from the imaginary part of the intrinsic Y-parameters.

4. Results and discussion

Firstly, it is necessary to confirm that the V_{ds}-dependent g_{tun}^* is associated with tunneling of carriers at the drain junction as reported in [7]. This effect can be modeled by means of an expression that relates the tunneling current and the applied reverse voltage to the drain-bulk p–n junction. In this case, the BTBT current is given by [13]

$$J_{b-b} = \frac{\sqrt{2m^*}q^3 E V_{ds}}{4\pi^3\hbar E_g^{1/2}} \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3qE\hbar}\right) \quad (9)$$

In Eq. (8), q is the fundamental charge, m^* is the electron effective mass, $\hbar$ is the Plank constant, E_g is the energy bandgap, and

$$E = \sqrt{\frac{2qN_a(V_{ds} + \psi_{bi})}{\varepsilon_{Si}}} \quad (10)$$

where N_a is the bulk doping concentration, ε_{Si} is the relative permittivity of silicon, and Ψ_{bi} is the built-in potential of the drain-bulk junction.

In order to verify that at V_{gs} = 0 V the V_{ds}-dependent current occurring between drain and source is originated by the BTBT effect, Eq. (8) is correlated with measured current–voltage DC curves. In this case, the measurement of the DC terminal currents was performed at V_{gs} = V_{bs} = 0 V and V_{ds} varying from 0.1 to 1 V to devices with separated connections for the gate, drain, source and bulk terminals. Notice the importance of measuring devices with separate source and bulk terminals since common-source/bulk structures do not allow the measurement of the source and bulk currents. To obtain the BTBT current it is necessary to measure the different currents associated with the MOSFET as shown in Fig. 4. Because of the lack of channel at V_{gs} = 0 V and V_{ds} > 0, the effect of a parasitic bipolar transistor becomes apparent in the intrinsic part of the MOSFET as can be seen in Fig. 4. Notice that when the base of this

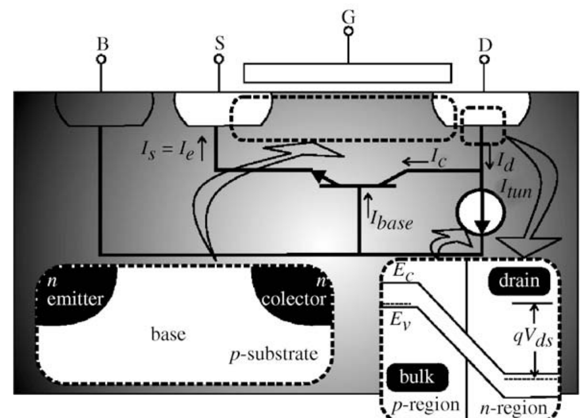

Fig. 4. Model for the MOSFET biased at V_{gs} = 0 V and V_{ds} > 0 V showing the different currents associated with the structure.

transistor is fed by a current, an additional parasitic current flows from drain to source. Thus, if a current originated by the carrier tunneling feeds the base of the transistor, this tunneling current will be scaled by a factor β (i.e. the gain of the transistor) and can be measured in the drain and source terminals. Moreover, this parasitic current at the collector of the bipolar transistor can be modeled by the Eq. (8) just by including this factor β. At this point it is worthwhile to point out the fact that the collector current of the bipolar transistor is that associated with the parameter g^*_{tun} in the small-signal model of Fig. 2.

In accordance to Fig. 4, the drain and source currents are defined, respectively, as $I_d = I_c + I_{tun}$ and $I_s = I_e$. Thus if $\beta \gg 1$, $I_c \approx I_e$ then $I_d - I_s = I_{tun}$. When comparing this experimentally determined current with the curve obtained after applying (9), a good correlation is achieved as shown in Fig. 5, which points out the fact that the BTBT effect is originating the parasitic current flowing from drain to source at $V_{gs} = 0$ V. Moreover, notice that this effect is evident in a 60 nm MOSFET.

In Fig. 6, the extracted g_{tun} and τ_0 versus the total gate width ($W_T = NF \cdot W_f$) data is plotted. As expected, g_{tun} is proportional to W_T since the current flowing from drain to source will increase as the device's width increases. For the case of τ_0, no dependence with W_T is observed, which is also physically expected since this parameter is associated with a time delay of the carriers flowing between the intrinsic drain and source regions. Thus, τ_0 would be dependent on the separation between drain and source and low sensitive to width variations.

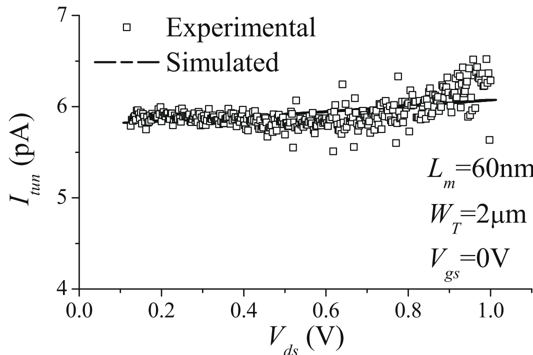

Fig. 5. Good correlation achieved between experimental and simulated data demonstrates the BTBT effect for a $(W/L) = (2\ \mu m/60\ nm)$ MOSFET.

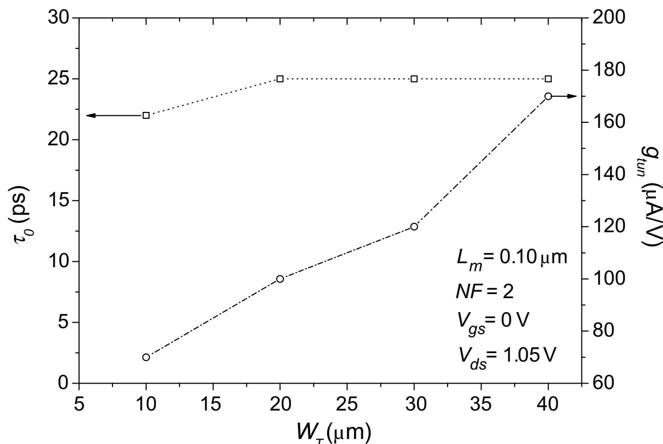

Fig. 6. Extracted τ_0 and g_{tun} versus W_T data showing a physically expected trend.

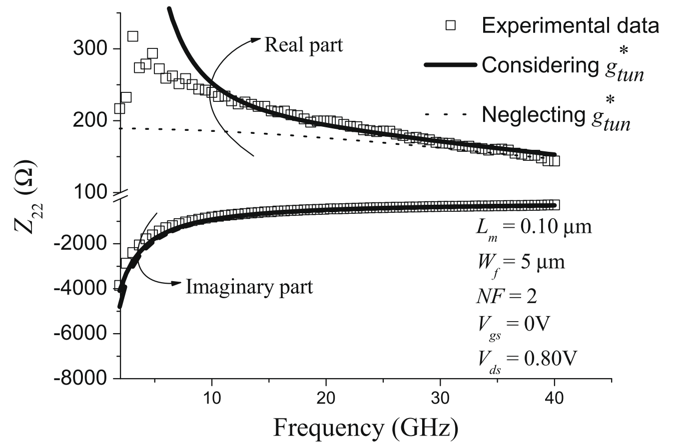

Fig. 7. Comparison between the simulated and experimental output impedance showing the improved modeling when considering g^*_{tun}.

Finally, in order to validate the proposed parameter extraction procedure, in Fig. 7 the simulated real and imaginary parts of the MOSFET output impedance are compared with experimental data. The simulations were performed with HSPICE after each small-signal MOSFET model parameter was obtained following the proposed procedure. As can be seen in Fig. 7, the simulation is considerably improved for Re(Z_{22}) above 10 GHz when the current source associated with the current tunneling is considered, whereas an almost frequency independent curve is obtained when ignoring this effect. In contrast, notice that below 10 GHz the MOSFET intrinsic part presents higher impedance when biased at $V_{ds} > 0$ V, which is not considered in the traditional models and yields an underestimation of this parameter. In the case of the curve obtained when considering the tunneling current source, the simulation presents the correct trend. Nevertheless, the inclusion of additional elements may be necessary to improve the simulation for this specific low frequency range. Work is currently underway in this direction, so that the extraction not only can be used to monitor the BTBT effect, but also to represent the behavior of microwave MOSFETs even at relatively low frequencies.

5. Conclusions

An analytical method for the extraction of the small-signal MOSFET parameters including BTBT effects was presented and demonstrated. The extracted methodology represents a valuable tool to assess the influence of BTBT effects in nanometric devices from *S*-parameter measurements. These measurements are performed to a single MOSFET avoiding dependence of the variation of the electrical characteristics with the device geometry. Furthermore, the proposed method allows the determination of the parameters to accurate represent the intrinsic behavior of MOSFETs at high frequencies. Excellent simulation-experiment correlation was achieved up to 40 GHz, and physically expected trend of the extracted parameters was observed when plotted versus channel width. Furthermore, the small-signal model for a MOSFET can be considerably improved when considering this additional effect when operating within the microwave range.

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References

[1] Mi-Chang C, Chih-Sheng C, Chih-Ping C, Ken-Ichi G, Ieong M, Lee-Chung L, et al. Transistor- and circuit-design optimization for low-power CMOS. IEEE Trans Electron Dev 2008;55(January):84–95.
[2] Doan CH, Emami S, Niknejad AM, Brodersen RW. Millimeter-wave CMOS design. IEEE J Solid-State Circ 2005;40(January):144–5.
[3] Cheng Y, Deen MJ, Chih-Hung C. MOSFET modeling for RF IC design. IEEE Trans Electron Dev 2005;529(July):1286–303.
[4] Gao X, Liou JJ, Bernier J, Croft G. An improved model for substrate current of submicron MOSFETs. Solid-State Electron 2002;46:1395–8.
[5] Torres-Torres R, Murphy-Artega R, Torres-Jacome A. An improved substrate-loss model to determine MOSFET drain, source and substrate elements. Microw Opt Tech Lett 2004;43(October):126–30.
[6] Mahalingam U, Rustagi SC, Samudra GS. Direct extraction of substrate network parameters for RF MOSFET modeling using a simple test structure. IEEE Electron Dev Lett 2006;27(February):130–2.
[7] Solomon PM, Frank DJ, Jopling J, D'Emic C, Dokumaci O, Ronsheim P, et al. Tunnel current measurements on P/N junction diodes and implications for future device design. IEDM Tech Dig 2003:233–6.
[8] Lolivier J, Jehl X, Rafhay Q, Poiroux T, Vinet M, Previtali B, et al. Experimental characterization of source-to-drain tunneling in 10 nm SOI devices. IEEE international SOI conference; 2005. p. 34–5.
[9] Kim KR, Kim DH, Ki-Whan S, Baek G, Kim HH, Huh JI, et al. Silicon-based field-induced band-to-band tunneling effect transistor. IEEE Electron Dev Lett 2004;25(June):439–41.
[10] Lim KY, Zhou X. A physically based semi-empirical series resistance model for deep-submicron MOSFT *I–V* modeling. IEEE Trans Electron Dev 2000;47(June):1300–2.
[11] Torres-Rios E, Torres-Torres R, Valdovinos-Fierro G, Gutiérrez-D EA. A method to determine the gate bias-dependent and gate bias-independent components of MOSFET series resistance from *S*-parameter measurements. IEEE Trans Electron Dev 2006;53(March):571–3.
[12] Hauser JR. Small signal properties of field effect devices. IEEE Trans Electron Dev 1965;ED-12(December):605–18.
[13] Taur Y, Ning TK. Fundamentals of modern VLSI devices. Cambridge University Press; 1998 [p. 94–5].