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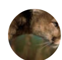
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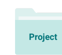
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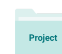
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ANALYTICAL CHARACTERIZATION AND MODELING OF SHIELDED TEST STRUCTURES FOR RF-CMOS

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A new modeling and parameter extraction methodology to represent the parasitic effects associated with shielded test structures is presented in this paper. This methodology allows to accurately account for the undesired effects introduced by the test fixture when measuring on-wafer devices at high frequencies. Since the proposed models are based on the physical effects associated with the structure, the obtained parameters allow the identification of the most important parasitic components, which lead to potential measurement uncertainty when characterizing high-frequency devices. The proposed methodology is applied to structures fabricated on different metal levels in order to point out the advantages and disadvantages in each case. The validity of the modeling and characterization methodology is verified by achieving excellent agreement between simulations and experimental data up to 50 GHz.

Keywords: Modeling; RF-CMOS; semiconductor device measurements; microwave measurements.

1. Introduction

Nowadays, the increasing demand for high data transmission rates, bandwidth, data processing and transmission frequency requires the improvement of circuits and systems at the lowest cost[1]. Therefore, many types of high frequency devices have to be modeled and characterized at microwave frequencies[2-5]. This means that accurate measurements are needed to design a high-performance radiofrequency integrated circuit (RFIC) at a reduced cost. This is the reason why on-wafer S-parameter measurements are of great importance in the semiconductor device industry. In this case, the device under test (DUT) is interconnected to the measurement probes by means of a test fixture. Since this test fixture is intended for measuring purposes (i.e. it will not be included in the actual RFIC), its effect has to be removed from the S-parameter measurement using a de-embedding technique. In this case, the de-embedding technique is considered as a two-tier calibration that moves the measurement reference plane from the probe tips to the DUT to be characterized[6]. In order to remove the effect of the test structure from the experimental S-parameter measurements, several methods have been developed[7-10]. These methods, however, do not allow the identification of the impact of the test fixture parasitic components on the DUT experimental data. This is due to the fact that a de-embedding algorithm is formulated to remove the undesired effects, but the physical

origin of these effects is usually ignored, complicating the identification of the dominant parasitics and the possible optimization of the test fixture.

Due to the considerable high parasitic effects introduced by test fixtures at the frequencies at which the characterization of the devices is currently required, the optimization of the test fixtures has recently become an important topic. In fact, alternative test structures have been specifically designed to reduce the parasitic effects associated with the undesired pad coupling through the substrate[6]. These are called "ground-shielded test fixtures"[11-12]. This type of structures, however, introduces a high capacitance that may be comparable to the input impedance of the DUT within the GHz range[10]. In consequence, an optimization process —supported by a physically based modeling and characterization methodology— is also required.

Hereafter, a physical model for the parasitic effects associated with RF shielded test structures fabricated on 90 nm CMOS technology is presented. The proposed model is applied to an improved shielded test structure, where the pad design for measuring probes is two metal levels above the ground plane. For the parasitic components parameter extraction a de-embedding procedure which uses only two standards to reduce the space needed for this type of structures is used. The results obtained from shielded test structures are compared with the improved layout design. The extracted parameter values are validated with experimental data up to 50 GHz.

2. Description of fabricated test structures

On-wafer measurement of S-parameters is the preferred choice to carry out the characterization of semiconductor devices at high-frequencies. In our case, ground-signal-ground (GSG) configured probes were used due to their good confinement of the electric field. In fact, the distribution of the electric field in a GSG-configured test structure is similar to that of a coplanar waveguide. In Fig. 1a, the conventional test structure to probe a DUT with a GSG probe configuration is shown. As can be seen in this figure, the pads are formed in the first metal level (the closest to the substrate). In the cross sectional view of the structure shown in Fig. 1b, it is observed that there is a coupling between the signal and the ground pads through the substrate. Hence, a parasitic capacitance appears due to the distribution of the electric field lines in the pad corners, and a lossy network is introduced by the low resistivity substrate. The model for a conventional test structure is presented in Fig. 1c, where the shunt admittances (Y_i and Y_o) represent the coupling of the signal and ground pads. In order to overcome the problem associated with this parasitic substrate path, ground shielded structures have been proposed. In this case, as shown in Fig. 2a, the first metal layer above the substrate is used as a ground plane to prevent the coupling of the signal and ground pads through the substrate. As can be observed, a solid metal ground plane is extended in every direction under the signal pad to prevent the capacitive coupling between the pads and the substrate. Therefore, the electric field is confined between the ground plane and the probe pads, as shown in Fig. 2b. A window at the centre of the ground plane is designed

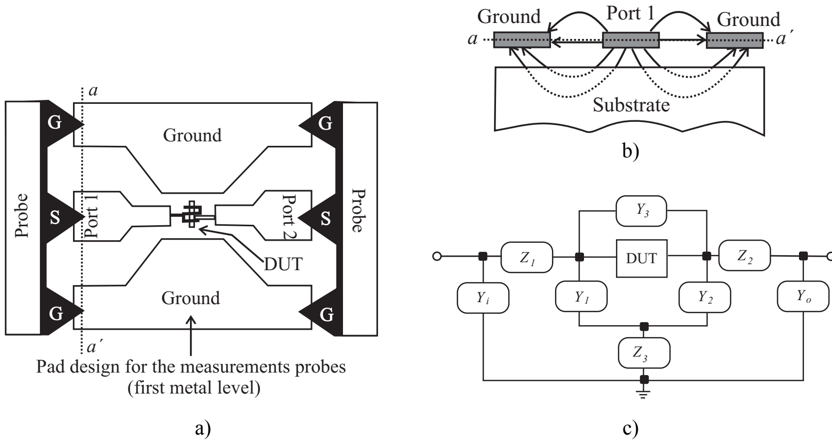

Fig. 1. a) Layout for the pads of a conventional test structure, used to connect the measuring probes with the DUT. b) Cross sectional view (from *a* to *a′*) showing the distribution of the electric field. c) Parasitic effects associated with the conventional test structure.

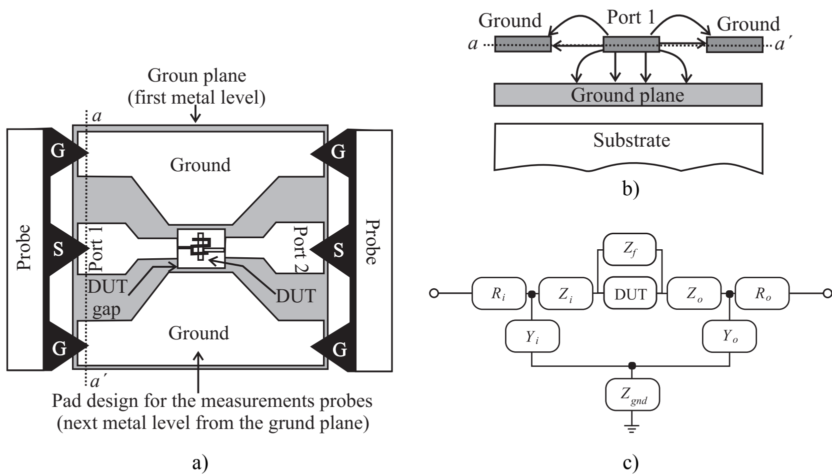

Fig. 2. a) Layout for the pads of a shielded test structure, used to connect the measuring probes with the DUT. b) Cross sectional view (from *a* to *a′*) showing the distribution of the electric field. c) Parasitic effects associated with the shielded test structure.

(DUT gap) to allow the interconnection of the pads with the DUT[11,12]. A model for a shielded test structure is presented in Fig. 2c. Notice that in this model the shunt admittances Y_i and Y_o represent the capacitance between the pads and the ground shield since the pad-to-substrate coupling effect is negligible. This capacitance, however, may present a considerable higher value when compared with that associated with a conventional test structure[6].

A simple solution to reduce the effect of the pad capacitance in shielded test structures is the design of the probe measurements pads on the second metal level above the ground plane. As shown in Fig. 3, the use of an upper metal level increases the distance between the pad and the ground plane, reducing the shunt capacitance. Nevertheless, additional parasitic effects become apparent as the distance between the pad and the DUT increases. For this reason, we analyze the impact of the pad layout on two different metal levels by means of a simple but rigorous methodology explained in the following sections.

3. General models for RF shielded test structures

Several models have been proposed to determine the effects introduced by the pads and interconnection lines surrounding the DUT in a shielded test structure. All previously proposed models are based on the model of Koolen *et al.*[6], with some simplifications in order to reduce equation complexity, considering the frequency range of interest. In order to apply the model for higher operation frequencies, more elements need to be added. Nevertheless, to make the shielded test structures a standard for on-wafer high frequency measurements, new layout techniques have to be developed to reduce the associated parasitic effects, and better models have to be proposed. In this article, a model for shielded test structures in which the pad for probe measuring is located on different metal levels, is presented and compared to that of the conventional structure. In the latter case, the pad is located on the metal layer next to the ground plane, while in the former it is located on an upper metal level.

3.1 *General model for the shielded test structure with pad probe design at the second metal level*

This is the most employed pad design because of its simplicity, as shown in Fig. 3a. The proposed model for this type of shielded test structure is that shown in Fig. 2c. As can be seen in this figure, the proposed model takes into account the ground impedance (Z_{gnd}) and the through impedance (Z_f) associated with the pad coupling through air. These parasitic elements had generally been neglected in previous models, since they only become important at frequencies above 20 GHz[12].

This type of shielded test structure pad design presents several advantages, such as simple modeling and parameter extraction, and the elimination of the pad coupling through the substrate. Nevertheless, the high pad capacitance has a considerable value in comparison with the conventional test structure without ground shield.

3.2 *General model for the shielded test structure with pad probe design at the third metal level*

In order to optimize a shielded test structure, the reduction of the shunt capacitance is necessary. A simple solution to this problem is the use of a metal layer two levels above the ground plane. As can be seen in Fig. 3b, using upper metal levels increases the distance between the pads and the ground shield, which allows reducing the pad capacitance. However, some resistive elements become apparent as a result of the vias

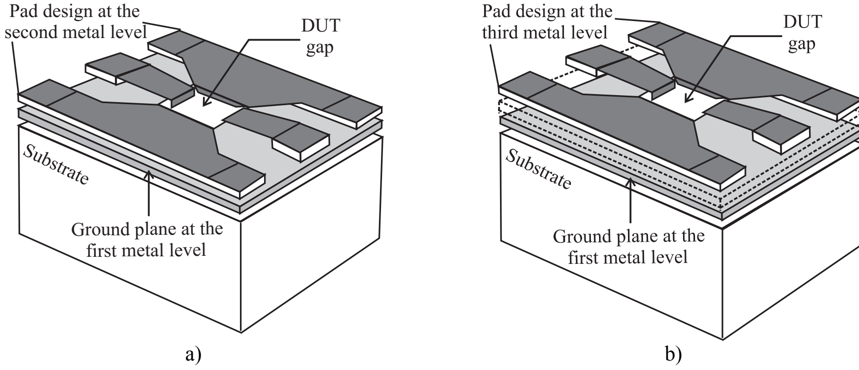

Fig. 3. a) Conventional shielded test structure pad design. b) Improved shielded test structure pad design, where an upper metal level is used.

needed to connect the higher metal level to the DUT. These elements are considered in the model of Fig. 2c by means of the series impedances Z_i and Z_o, which will be explained with more detail in the next section. Once the parasitic elements of the shielded structure have been identified, an equivalent circuit can be associated with each impedance and admittance in the model. Furthermore, we explain in the next section the determination of the model parameters from experimental data.

4. Equivalent circuit modeling

4.1 *Calculation of the model parameters*

To determine the eight parameters associated to the proposed model in Fig. 2c, the S-parameter measurements of the open and short dummy structures are used. The parasitics associated to open and short dummies are shown in Fig. 4. Then, from the short dummy, the measured S-parameters are converted in Z-parameters represented by the 2x2 matrix $\mathbf{Z}_{sh}$. Thus, the following parameters can be extracted from operations on the elements of $\mathbf{Z}_{sh}$:

$$R_i \approx \mathrm{Re}\left(Z_{11sh} - Z_{21sh}\right)\Big|_{LF} . \tag{1}$$

$$R_o \approx \mathrm{Re}\left(Z_{22sh} - Z_{21sh}\right)\Big|_{LF} . \tag{2}$$

$$Z_{gnd} = Z_{12sh} = Z_{21sh} . \tag{3}$$

where the subscript *LF* indicates that this approximation is valid at relatively low frequencies at which the reactive components associated with the elements of $\mathbf{Z}_{sh}$ are negligible. Furthermore, since passivity is assumed, the measured two-port network parameters present reciprocity as stated by means of equation (3).

This follows because the structure under analysis is symmetrical and can be transformed in a T-network. Under this condition and in accordance with the model of

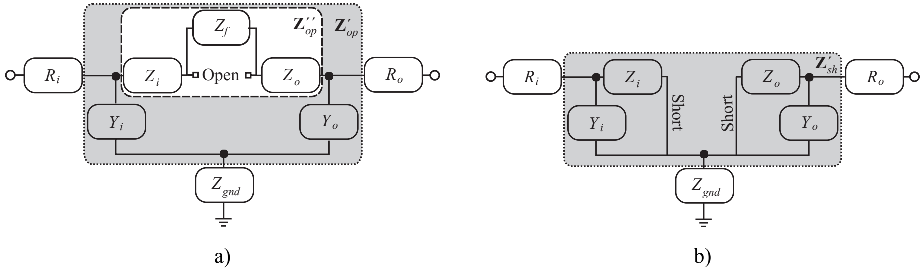

Fig. 4. Equivalent circuits associated with the a) open ($\mathbf{Z}_{op}$) and b) short ($\mathbf{Z}_{sh}$) dummy structures.

Fig. 4, Z_{gnd}, R_i and R_o can be removed from the measured data using simple algebraic operations; mathematically:

$$\mathbf{Z}'_{sh} = \mathbf{Z}_{sh} - \begin{pmatrix} R_i & Z_{gnd} \\ Z_{gnd} & R_o \end{pmatrix}. \tag{4}$$

A similar equation can be written for the model for the open dummy shown in Fig. 4a; this is:

$$\mathbf{Z}'_{op} = \mathbf{Z}_{op} - \begin{pmatrix} R_i & Z_{gnd} \\ Z_{gnd} & R_o \end{pmatrix}. \tag{5}$$

Upon transforming (5) to Y-parameters and inspecting Fig. 4a, the input and output port admittances are determined as:

$$Y_i = Y'_{11op} + Y'_{21op}. \tag{6}$$

$$Y_o = Y'_{22op} + Y'_{21op}. \tag{7}$$

Once Y_i and Y_o are known, their effect is removed from $\mathbf{Y}'_{op}$ using:

$$\mathbf{Y}''_{op} = \begin{pmatrix} Y'_{11op} & Y'_{12op} \\ Y'_{21op} & Y'_{22op} \end{pmatrix} - \begin{pmatrix} Y_i & 0 \\ 0 & Y_o \end{pmatrix}. \tag{8}$$

Then, Z_i and Z_o can be extracted from the measurements using:

$$Z'_i = \frac{1}{\dfrac{1}{Z'_{11sh}} - Y_i}. \tag{9}$$

$$Z'_o = \frac{1}{\dfrac{1}{Z'_{22sh}} - Y_o}. \tag{10}$$

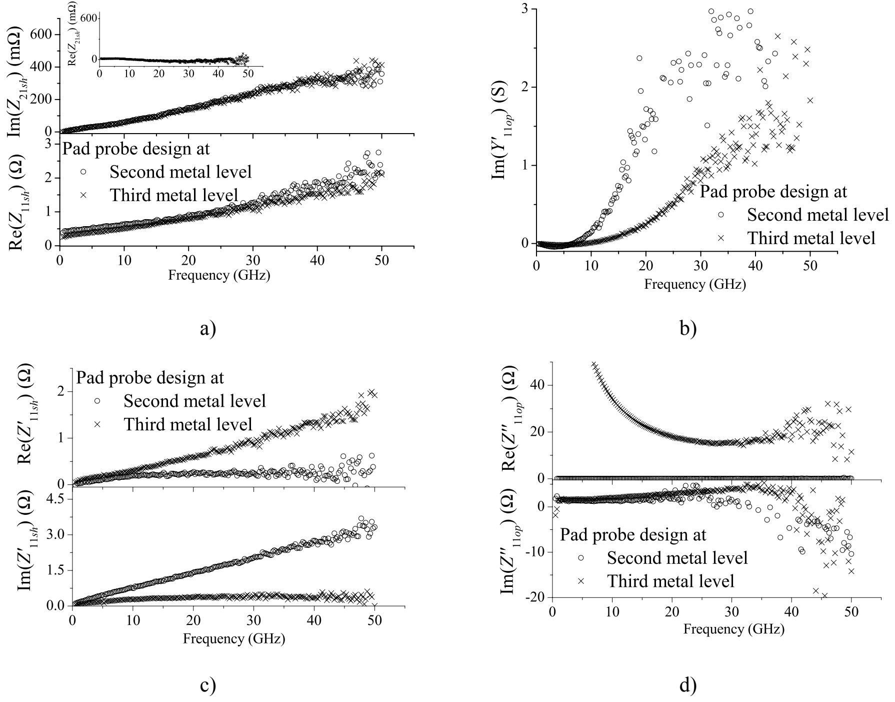

Fig. 5. In these figures the frequency behavior of the parasitic elements of shielded test structure, where the probe pad is designed in the second and third metal layer, are presented.

Finally, Z_f is calculated from:

$$Z_f = \frac{1}{Y''_{21op}} - Z_i - Z_o \,. \tag{11}$$

4.2 *Analytical parameter extraction*

In the model for a shielded test structure R_i and R_o represent purely resistive elements since they are inherent to the sheet resistance of the pad metal layer and contact resistance. This is the reason why these resistances are determined from the Re(Z_{11sh}) and Re(Z_{22sh}) versus frequency curves accordingly to the expressions (1) and (2). As shown in Fig. 5a, there exist considerable differences between the extracted values for R_i and R_o according to which metal layer is used to form the pads. Fig. 5a also shows the data corresponding to Z_{21sh}; as can be seen, this parameter is associated with a pure inductance. Thus, Z_{gnd} can be modeled by means of a lumped inductor. Furthermore, this figure shows that Z_{21sh} presents the same trend for the two different shielded structures; this is because the same metal level is used for the ground shield. Therefore, the value of the ground inductance can be determined from:

$$L_{gnd} = \frac{\text{Im}(Z_{21sh})}{\omega}. \quad (12)$$

Also notice from Fig 5b, that the trend of Y_i and Y_o indicates that these parameters are not purely capacitive. An appropriate equivalent circuit for these parasitic elements is a capacitor (C_p) in series with a resistance (R_p). Their values can be extracted from Re($Y_{i,o}$) (which indicates that the procedure is applicable to Y_i and Y_o) by using:

$$\frac{1}{\text{Re}(Y_{i,o})} = \frac{1}{\omega^2 C_p{}^2 R_p} + R_p. \quad (13)$$

Hence, from the linear regression of 1/Re($Y_{i,o}$) versus $1/\omega^2$, R_p can be determined from the intercept with the abscises (b), and C_p can then be determined from the slope (m):

$$C_p = \sqrt{\frac{1}{mR_p{}^2}}. \quad (14)$$

At this point, it is necessary to point out the fact that C_p and R_p present different values depending on the parameter they are associated with, either Y_i or Y_o.

For Z_i and Z_o two solutions are possible. The first one is when the pad metal layer is located on the metal level immediately above the ground plane. In this case, a pure inductive effect is observed, as is shown in Fig. 5c. It then follows that the inductance value can be determined from:

$$L_i = \frac{\text{Im}(Z_{i,o})}{\omega}. \quad (15)$$

When an upper metal level is used, $Z_{i,o}$ are no longer purely inductive elements, as can be seen in Fig. 5c. A better model is that of an inductor (L_i) in parallel with a resistor (R_z)[10]. The values for these elements can be calculated from:

$$\frac{\omega}{\text{Im}(Z_{i,o})} = \frac{\omega^2 L_i}{R_z} + \frac{1}{L_i}. \quad (16)$$

In this case, a linear regression of ω/Im($Z_{i,o}$) versus ω^2 is employed to find the intercept with the abscises (b) and the slope (m). Therefore, $1/L_i$ is determined from b while R_z is determined from m using:

$$R_z = \frac{L_i}{m}. \quad (17)$$

Finally, likewise in the case for $Z_{i,o}$, Z_f has a different trend when plotted versus frequency when an upper metal level for the pad design is used, as shown in Fig. 5d. As can be seen, when the probe pad is at the metal level next to the ground plane, a pure LC

effect is observed. When a higher metal level is used, however, the contribution of a series resistance is needed to model the curves. The values for L_f and C_f in both cases are obtained from the linear regression of:

$$\omega \operatorname{Im}(Z_f) = -\frac{1}{C_f} + \omega^2 L_f . \tag{18}$$

Then, $-1/C_f$ is obtained from the intercept with abscises, whereas L_f is obtained from the corresponding slope. In the case of R_f for the structure that uses a higher metal level, the extraction is performed from the value of $\operatorname{Re}(Z_f)$ at low frequencies, where the effect of L_f is negligible.

5. Results and discussion

The complete equivalent circuit model for the shielded test structure is presented in Fig. 6a. To validate the values obtained using the proposed analytical extraction methodology, in Fig. 6b we show a comparison between the simulated and experimental data of the real and imaginary parts of Z_{11} of the open dummy up to 50 GHz. As can be observed in Fig. 6b, the proposed model agrees very well with the experimental data. The advantages of using higher metal levels to reduce the input/output shunt capacitance is corroborated, but with the cost of introducing new resistive elements in the equivalent circuit model. The new resistive elements are caused by metal thickness differences in each layer, and the use of deep vias to connect the DUT to the pad. Moreover, even though one would expect Z_f be the same for both cases, experimental data show that this is not the case. As explained above, the metal characteristics of upper levels are not the same (mainly the metal thickness), and thus the pad coupling through air varies according to which layer is used.

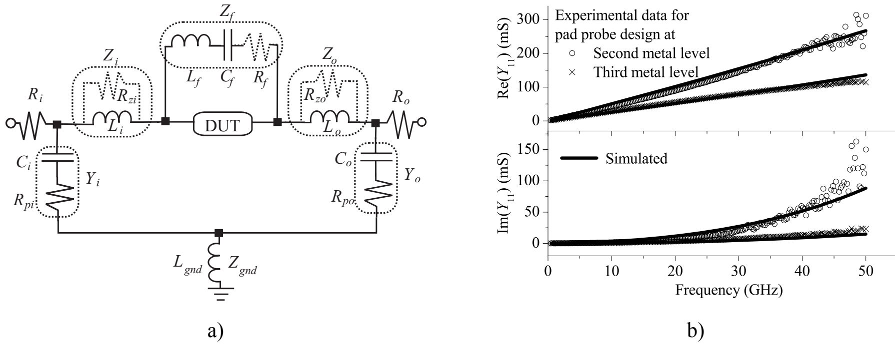

Fig. 6. a) Complete equivalent circuit model for the shielded pad design. The solid lines represent the model for conventional structures, and the dotted lines the elements that have to be added to improve the model for the test structure. b) Comparison between the simulated and experimental data of the real and imaginary parts of parameter Z_{11} for the open dummy, up to 50 GHz.

The results presented in this experiment show a trade off between the reduction of the input/output shunt capacitance and the parasitic resistive elements. It is clear that more experiments are needed in order to determine the best metal level for pad design, where the optimum shunt capacitance and parasitic resistance values are obtained. Work is ongoing in order to determine the best compromise.

6. Conclusions

An accurate model and an analytical parameter extraction methodology for the parasitics associated with a RF shielded test structure fabricated in a CMOS technology have been presented and demonstrated up to 50 GHz. The pad parasitics distribution is proposed, and a simple de-embedding method is based on the use of only two dummy structures is employed. The experimental results show a compromise in the reduction of the shunt input/output capacitance and the appearance of parasitic resistances, when using different metal levels for the pad design.

The proposed equivalent circuit model is shown to be accurate within the measuring range, allowing the proper representation of the parallel and series parasitic components. All of these can be assigned to the physical aspects of the structure, giving the designer insight into the structure, needed to optimize layout techniques in order to reduce undesirable effects on the DUT.

7. Acknowledgments

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