Built-In Sensor for Signal Integrity Faults in Digital Interconnect Signals

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***Abstract*—Testing of signal integrity (SI) in current high-speed ICs, requires automatic test equipment test resources at the multigigahertz range, normally not available. Furthermore, for most internal nets of state-of-the-art ICs, external speed testing is not possible for the newest technologies. In this paper, on-chip testing for SI faults in digital interconnect signals, using built-in high speed monitors, is proposed. A coherent sampling scheme is used to capture the signal information. Two monitors to test SI violations are proposed: one for undershoots at the high logic level and the other for overshoots at the low logic level. The monitors are capable of detecting small noise pulses and have been extended to test sequentially more than one signal. The cost of the proposed strategy is analyzed in terms of area, delay penalization, and test time. The effects of clock jitter and process variations are analyzed. Experimental results obtained in designed and fabricated circuits show the feasibility of the proposed testing strategy. A good agreement appears between the theoretical analysis, simulation results, and the experimental measurements.**

***Index Terms*—High speed, noise pulses, overshoots, signal integrity (SI) faults, testing, undershoots.**

I. Introduction

SCALING of semiconductor technologies has made it possible to integrate circuits with increasing functionality, speed, and interconnect density [1], [2]. However, at the same time, it has become a critical issue to assure proper quality of interconnect signals.

The interconnect architectures play an important role in signal integrity (SI). The waveform of the interconnects is influenced by the signal activity in neighboring lines. Noise appears as a consequence of the electric and magnetic field perturbations on internal electrical nodes [3], [4]. Lateral capacitance has a significant impact in actual CMOS semiconductor technologies. This coupling capacitance can exceed 70% of the total capacitance [5]. High-performance circuits also present significant inductive coupling [6], [7] that needs be taken into account in some ICs. Signal current variations in an interconnection generate variable magnetic fields. This variable flux creates an electric field E in near loops, inducing noise voltages. The noise levels depend on the resistance/capacitance/inductance characteristics of the interconnect under analysis, the surrounding interconnect topology, and the interconnect drivers. Substrate noise, power supply voltage, and ground bouncing are other sources affecting SI [8]–[11].

SI is normally understood as the ability of a signal to generate assured correct responses in a circuit. For designers, good levels of SI means clean data, free of ringing, and not sensitive to interference. However, high-performance systems, for example, system on chips (SoCs), made in nanometer semiconductor technologies, have signals with unavoidable noise levels. SI degradation may lead to unreliable performance of the system causing hard-to-detect transient system failures. Preserving SI in complex designs is a current challenge in nanometer technologies [12], [13]. To ensure SI compliance, designers need to consider circuit layout design, placement and routing, and circuit simulation [3], [4]. Present tools could help the designer in all these tasks. However, all possible operational conditions are unlikely to be taken into account by the present state-of-the-art computer-aided design (CAD) tools. Consequently, chips fail although they passed standard test procedures [14].

External at-speed testing may not be possible for the newest technologies, and the automatic test equipment (ATE) requirements to validate certain I/O signals in the multigigahertz range become prohibitive. As a consequence, built-in testing using on-chip monitors appears as a good alternative for present and future nanometric ICs. This strategy also allows testing of some internal nodes that are difficult to control or observe through the I/O pins.

Cells to detect noise and skew violations on interconnects are presented in [15]. The sensing cell is based in a cross-coupled pMOS amplifier. The authors in [16] present a test pattern generation algorithm aimed at SI faults on long interconnects. In this approach, it is possible to detect intermittent failures due to integrity loss on long interconnects. An online testing technique that captures noise-induced logic errors using a double sampling data checking is presented in [17]. In [18], the authors present an on-chip mechanism for testing SoC interconnects for SI using an enhanced JTAG architecture. Test-wrapper designs for the detection of signal-SI faults on core-external interconnect of SoCs is presented in [19]. Test monitors to test skew and SI faults at the high and low level of the signals are presented in [20].

In this paper, an on-chip testing strategy for SI violations (SIVs) in digital interconnect signals is proposed. Two novel monitors for testing these critical signals have proper voltage levels are proposed. One of them is used to test undershoots below V_{DD} and the other is used to test overshoots above G_{ND}.

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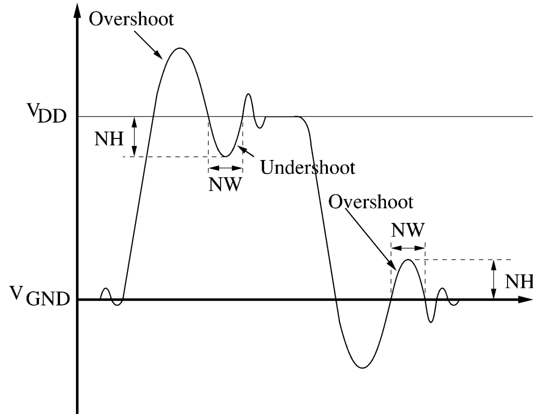

Fig. 1. Signal having undershoots and overshoots. NH and NW are the voltage noise magnitude and the noise width, respectively.

Each of the proposed monitors can be used to test several critical signals. The information of the critical signals is read by the monitors using coherent sampling.

The rest of the paper is organized as follows. Section II presents different issues affecting the SI quality. Section III presents the test methodology and the novel monitors to test SIVs. Section IV outlines the main principles of coherent sampling. Section V analyzes the effects of clock jitter and process/power supply variations on the proposed testing methodology. The cost of the proposed monitors is given in Section VI. Section VII presents the experimental results obtained from designed and fabricated circuits, and our proposal is compared with previous work. Finally, in Section VIII, the conclusions are presented.

II. Signal Integrity Quality

A signal with good integrity characteristics is defined as a signal arriving at the receiver location during the desired time window and with adequate voltage levels [16], [21]. Some important SI issues are shown in Fig. 1 [15].

1) A signal at a stable high logic state can drop below a certain level.
2) A signal at a stable low logic state can go above a certain level.
3) Overshoots/undershoots above/below V_{DD}/V_{DD}.
4) Skews, not shown in Fig. 1, larger than those allowed may appear.

These anomalous behaviors affect the performance of the ICs. A logic system failure may occur when a signal at a stable low (high) logic state presents an overshoot (undershoot) that is sufficiently large for the driven gate(s) to switch. Overshoots/undershoots above/below V_{DD}/V_{DD} that occur repeatedly may produce injection of high-energy carriers into the gate oxide, degrading its characteristics. This represents a reliability issue. Proposals to test overshoots representing a reliability issue can be found in [19] and [22]. Signals must also satisfy an allowed skew region [15]. Excessive delays can lead to system failures.

This paper is focused to test SI undershoots below V_{DD} and undershoots above G_{ND} with sufficient duration to impact the logic response of a gate. The unacceptable level of noise (i.e., SI degradation) requires further discussion. In practice, logic circuits can tolerate certain noise levels. A CMOS gate interprets as logic 0 (1) input voltages below (above) the low (high) noise margin level [23]. In this way, the maximum (minimum) input voltage guaranteed to be interpreted as a logic 0 (1) is defined. Beyond these margin voltages, both transistors of a CMOS complementary gate will turn-ON and enter the high-gain transition region where small noise perturbations may cause a faulty response. Furthermore, as noise is an ac pulse, the height (NH), width (NW), and shape of a noise pulse (see Fig. 1) all determine the actual behavior of a CMOS gate [24].

Due to the high number of interconnects in nanometer technologies, it is important to select which interconnects may suffer SI loss. Global interconnects (length usually $> 300\ \mu$m) are candidated for SI loss [25]. Among the global interconnects, we have SOC's interconnects. Their lengths can even extend to the chip-edge size and can compromise SI, especially in nanometer designs. Signals in data/address buses and in clock distribution are also susceptible to SI loss. Furthermore, an important criterion in the selection of interconnects is that built-in monitors for SI testing may also allow probing of the signals that are otherwise difficult to observe due to the large number of metal layers and high metal density [14]. This particularly occurs in nanometer CMOS ICs.

III. SI Testing

A. Test Methodology

The proposed test methodology is shown in Fig. 2. The signals arriving at the second logic block are considered as susceptible to noise. Two novel built-in high-speed monitors are used to verify noise compliance of these critical signals. One monitor is used to test SIVs at a stable high logic level and the other at a stable low logic level. The signals arriving at the second block are monitored using coherent sampling [26]. The sampling signal can be obtained from an internal clock. A programmable block divider sets the required frequency relations for coherent sampling. More information about coherent sampling is given in Section IV. Periodical signals are applied to the primary inputs of the logic blocks. Test patterns causing worst-case SI loss can be used [15], [16]. Pseudorandom patterns have also been investigated [15], [27]. Recently, it has been suggested to use pseudo-exhaustive testing of SI for high-speed SoC interconnects [28].

Well-defined rectangular shapes for the noise pulses have been considered for analysis purposes and electrical simulations unless otherwise stated. A signal degradation is considered unacceptable when it has an NH and NW that produce a faulty response at the receiver gate. This is illustrated in Fig. 3(a) where the receiving gate (circled inverter) receives the signal under test (SUT). A hypothetical noise margin curve of the receiving gate is shown in Fig. 3(b). Let us assume that the SUT should be at logic 0. All noise voltages into the unacceptable noise region will cause false switching in that gate (inverter B in Fig. 3). Hence, in our test strategy, the proposed monitor(s)

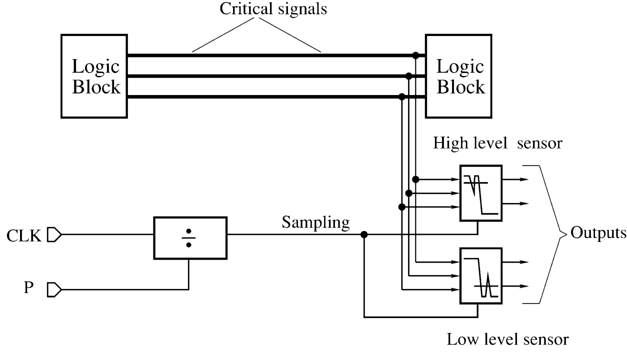

Fig. 2. Block diagram of the test methodology.

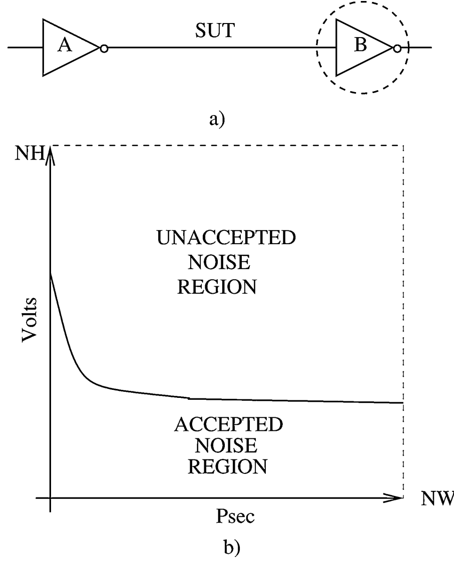

Fig. 3. Acceptable/unacceptable regions of a receiving gate.

are designed to detect noise voltage violations located in the unacceptable region of the receiving circuit.

B. Testing Noise Violations

Let us focus on the high-level monitor. This monitor is composed of a differential pair with a latch as load (see Fig. 4) [29]. The latch is built with two cross-coupled pMOS transistors. It helps to switch the nodes X and XN to complementary logic levels. The input transistors $N1$ and $N2$ and the pMOS latch transistors determine the acceptable/unacceptable noise levels. Nodes X and XN are both precharged to V_{DD} by transistors $P3$ and $P4$. Transistor $P_{\rm eq}$ equalizes nodes X and XN.

Testing of selected critical signal is made in two steps. In the first step, when CLK is low, a precharge operation takes place. Transistors P3 and P4 are turned ON and nodes X and XN go to V_{DD}. Transistor $P_{\rm eq}$ equalizes nodes X and XN, and transistor N_b is OFF. In the second step, when CLK goes high, the precharge transistors P3, P4 and the equalization transistor $P_{\rm eq}$ are turned OFF. In this step, the SUT is evaluated. The right input transistor (see Fig. 4) has a reference voltage (V_{DD}) at its input. The other input transistor N1 receives the SUT. For a noise-free signal, the SUT has a value of V_{DD}. Hence, the final state of node $X(XN)$ is 0 (1) logic. This behavior is because the aspect ratio (W/L) of N1 is designed to be larger than the aspect ratio of N2. If the height and duration of the noise pulse is sufficiently large, the final state of node $X(XN)$ is 1 (0) logic. Therefore, an SIV is detected. The aspect ratios of the input transistors and the latch establish the threshold detection conditions of the monitor.

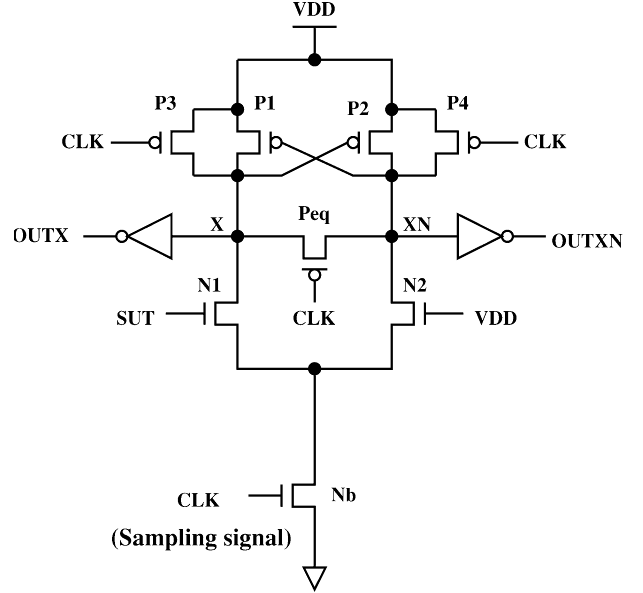

Fig. 4. High-level SI monitor.

Insights into the behavior of the monitor can be obtained using phase plane analysis techniques [30]. To perform this analysis, a simplified schematic circuit of the monitor is used (see Fig. 5). The voltage at the sources of the input transistors has only slight variations during the monitor operation. Hence, a constant voltage is placed at the sources of the input transistors as a first-order model approximation. The circuit analysis of the simplified monitor circuitry gives two differential equations applying Kirchoff's current law at nodes X and XN

$$C_X \frac{dV_X}{dt} = I_{DP1} - I_{DN1} \quad (1)$$

$$C_{XN} \frac{dV_{XN}}{dt} = I_{DP2} - I_{DN2}. \quad (2)$$

For the current expressions, we use the low-power transregional model's saturation drain current [31], [32]. Neglecting the small weak inversion region and performing a three-term binomial expansion of the bulk charge, the saturation current can be expressed as

$$I_D^{\rm SAT} \approx \frac{W}{L} C_{\rm OX} \mu_{\rm eff} V_{DS}^{\rm SAT} \left[V_{GS} - V_T - \left(\frac{\eta}{2}\right) V_{DS}^{\rm SAT} \right] \quad (3)$$

where W/L is the channel width-to-length ratio, $C_{\rm OX}$ is the gate oxide capacitance per unit area, $\mu_{\rm eff}$ is the effective mobility including vertical and lateral high field degradation effects [31], [32], and V_T is the transistor threshold voltage.

The saturation voltage is given by

$$V_{DS}^{\rm SAT} = E_C L \sqrt{1 + \frac{2}{E_C L} \left(\frac{V_{GS} - V_T}{\eta} \right)} - 1 \quad (4)$$

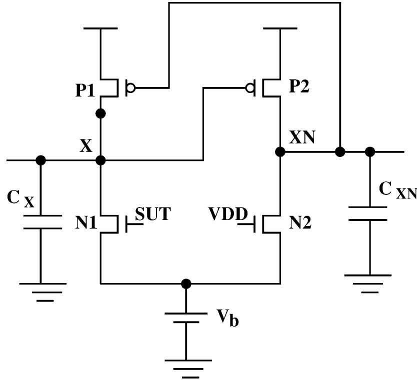

Fig. 5. Simplified schematic of the high-level monitor.

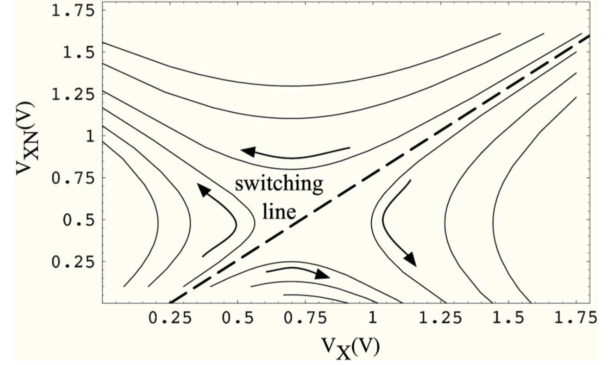

Fig. 6. Noise-free input/output characteristics.

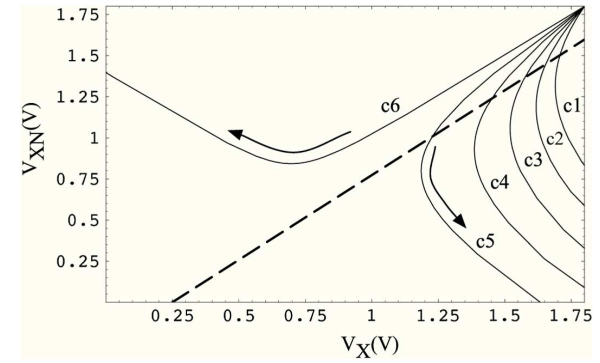

Fig. 7. Input/output characteristics with noise. **c1**: $\mathrm{NH} = 1.3$ V; **c2**: $\mathrm{NH} = 1.1$ V; **c3**: $\mathrm{NH} = 0.9$ V; **c4**: $\mathrm{NH} = 0.7$ V; **c5**: $\mathrm{NH} = 0.5$ V; **c6**: $\mathrm{NH} = 0.3$ V.

where E_C is the critical field for velocity saturation and η is a parameter related to the body effect [31].

The drain current expression has been linearized obtaining the first two terms of the Taylor series expansion. The current expression is linearized at $V_{GS} = (V_{DD} + V_T)/2$. The error of the linearized analytical expressions with the simulations carried out using Hspice level 49 for TSMC 0.18 μm is less than 10%.

Assuming that the transistors work mainly in saturation, the previous equations are replaced in (1) and (2). Analytical solutions for $V_X(t)$ and $V_{XN}(t)$ have been obtained using Mathematica [33]. These expressions are not shown because they are lengthy and present several exponential terms.

The input/output characteristics of the monitor under a noise-free SUT have been obtained by plotting the obtained equations by Mathematica [33] and using different initial conditions at the nodes X, XN (see Fig. 6). Each point of the input/output characteristic is obtained by plotting the resulting V_X, V_{XN} voltage pairs from the equations $V_X(t)$ and $V_{XN}(t)$ for the same time **t** (PHASE PLANE Trajectory). The noise-free case corresponds to $V_{\mathrm{SUT}} = V_{DD} = 1.8$ V. In this example, $W_{N1}/L_{N1} = 5/0.6, W_{N2}/L_{N2} = 3/0.6, W_{P1}/L_{P1} = 15/0.18$, and $W_{P2}/L_{P2} = 15/0.18$ are used. A *switching line* divides the phase plane in two regions depending on the final state of the Monitor circuit (see Fig. 6). This line defines two semiplane regions. The monitor evolves to $V_X(V_{XN})$ low (high) for all those initial conditions located on the left of the *switching line*. The monitor evolves to $V_X(V_{XN})$ high (low) for all those initial conditions located on the right of the *switching line* (see Fig. 6). Output signals $OUTX$ and $OUTXN$ are set to proper voltage values by the output inverters (see Fig. 4).

The input/output characteristics of the monitor for signals in the presence of noise are drawn in Fig. 7. Different noise magnitudes have been considered. Curve c1 is for the highest noise magnitude and the curve c6 is for the lowest noise magnitude. These curves are obtained using $V_{\mathrm{SUT}} = V_{DD} - \mathrm{NH}$ in the previous equations where NH models the magnitude of the noise pulse. Only those curves for the initial condition $V_X(0) = V_{XN}(0) = 1.8$ V are considered. This is because this condition is forced during the precharge and equalization step under the testing strategy.

The behavior of the high-level monitor in the presence of a noise pulse (with NH and NW values) is explained as follows. While the SUT is below V_{DD}, the monitor evolves according to curves c1–c6 (see Fig. 7). The voltage value below V_{DD} defines NH, and the time duration at this value defines NW. Once the undershoot disappears the monitor evolves according to the noise-free input/output characteristics (see Fig. 6). The dashed line in Fig. 7 corresponds to the switching line of the noise-free input/output characteristics of the monitor (see Fig. 7). The final state of the monitor defined by $V_X(V_{XN})$ is high (low) if the monitor has evolved on the right side of the *switching line* during the time that the signal was below V_{DD}. Hence, a noise violation is detected. Otherwise, the monitor does not detect a noise violation. Curves c1–c5 may evolve on the right or left of the *switching line* depending on the time that the undershoot (NW) is present. NW must be sufficiently wide to allow the curve to cross the switching line. Furthermore, curve c6 never evolves on the right side of the *switching line*. This is because of the low magnitude (NH) of the noise pulse.

The crossing points of curves c1–c5 with the switching line are plotted in Fig. 8. Hence, a noise pulse is detected as a violation when for a given noise magnitude (NH) its width (NW) is sufficiently large to allow the input/output curve under noise to cross on the right side of the noise-free switching line. Two well-defined regions can be identified in Fig. 8. Those noise pulses with NH, NW above (below) the curve are detectable (undetectable).

The schematic of the low-level monitor is shown in Fig. 9. The low-level monitor is composed of a pMOS input differential pair with a latch made with nMOS transistors. Its behavior is

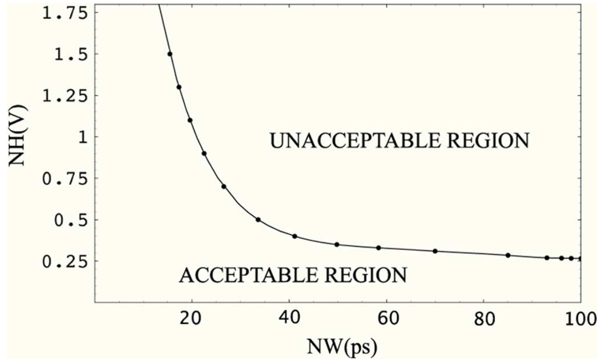

Fig. 8. Dependency of the monitor behavior on the magnitude and width of the noise pulse.

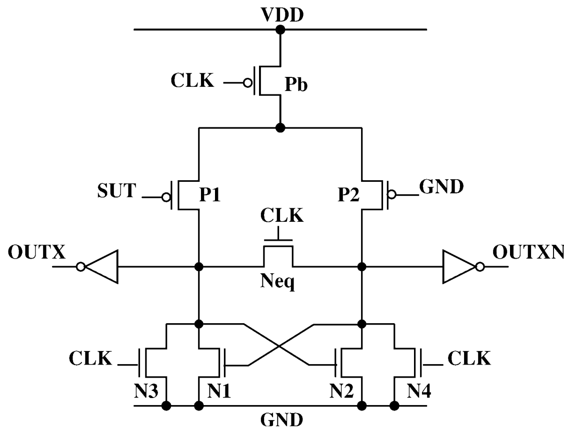

Fig. 9. Low-level signal integrity monitor.

TABLE I
TRANSISTOR SIZES FOR THE HIGH-LEVEL MONITOR

Transistors	W/L (μm / μm)
P1, P2	15/0.18
P3, P4	2/0.18
Peq	10/0.18
N1	5/0.18
N2	3/0.18
Nb	10/0.18

complementary to the high-level monitor. In this case, the monitor detects nonallowed overshoots that occur at the low logic level of the SUT.

C. Monitor Performance Evaluation

The performance of the high (low) level monitor is characterized by the width, NW, and height, NH, of a rectangular noise pulse. Without loss of generality, it has been considered to be a monitor with only one input signal to test. The monitor has been designed for reliable detection of minimal noise pulse duration. Monitor transistors are sized in order to achieve this goal. TSMC 0.18 μm CMOS technology is used. The channel widths and lengths of the transistors are indicated in Table I.

The integrity high logic state is verified by the high-level monitor. Fig. 10 shows the case when a SIV does not occur. The upper panel shows the SUT. The next panel is the CLK

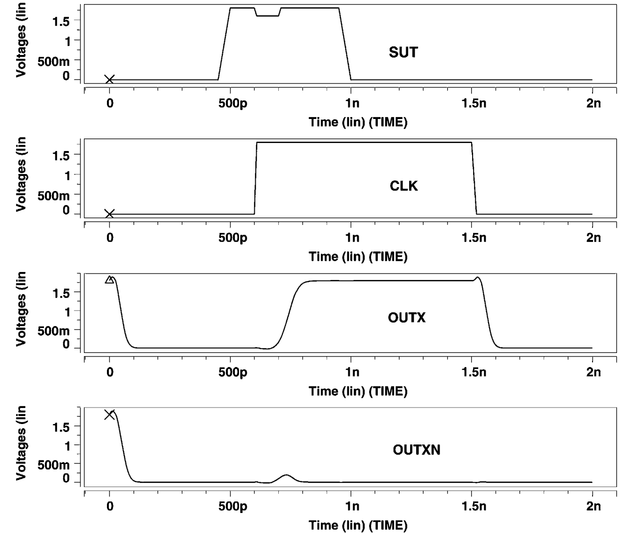

Fig. 10. Output response of the high-level monitor when a SIV does not occur.

signal. The third panel shows the signal at node $OUTX$, which corresponds to the buffered signal of the voltage at node X. The signal at node $OUTXN$ is shown in the lower panel. This signal is complementary to signal $OUTX$ only when CLK is high. The cross-coupled pMOS transistors maintain proper voltage levels at $OUTX$ and $OUTXN$ while the CLK is high. Because the noise pulse is small (height and width), node X is discharged through the transistors N1 and Nb. Buffered signal $OUTX$ goes high (see Fig. 10).

Fig. 11 shows the case when an SIV occurs. In this case, a noise pulse of sufficient energy (height and width) is present at the input transistor receiving the SUT. Because of this N1 (see Fig. 4) does not have enough current drive capability to discharge node X. Node $OUTX$ becomes logic 0. Node XN is discharged by N2, which is on due to the constant reference voltage (VDD) at its gate. Node $OUTXN$ becomes logic 1.

The height and width of the noise pulse determine the detectability regions for the high-level monitor (see Fig. 12). This agrees with the previous analytical results. For the high-level monitor, those undershoots below V_{DD} with NW and NH values located above the curve are detected. Those located below the curve are not detected. Undershoots of small duration require a higher NH in order to be detectable. The detectable NH of the undershoot lowers as the NW increases. For a sufficiently large undershoot duration, the required NH does not increase for larger NW. For the designed monitor, the minimum detectable NW is 10 ps.

The detectability regions for the low-level monitor can be similarly obtained.

D. Monitor Sizing

The acceptable (nonacceptable) regions shown in Fig. 12 can be modified to meet the noise margin requirements of the receiving gate. This can be achieved by adjusting the channel width ratios of the input transistors and the transistor sizes of the latch load. Fig. 13 shows the acceptable (nonacceptable) regions of the high-level monitor for different channel width ratios of transistors $N1$ and $N2$. The detection curve moves up as the

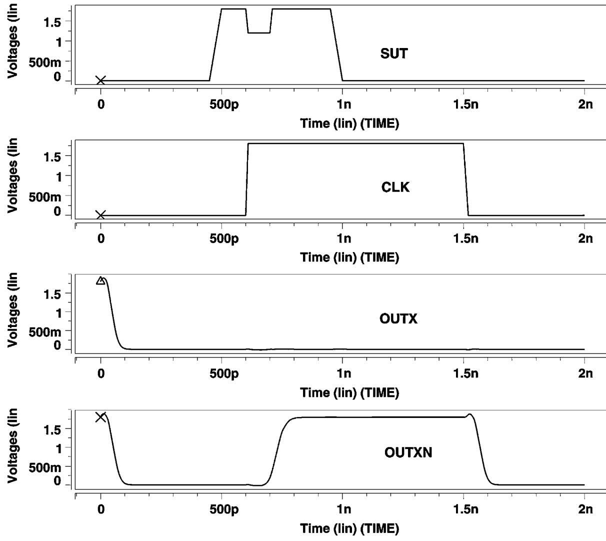

Fig. 11. Output response of the high-level monitor when a SIV occurs.

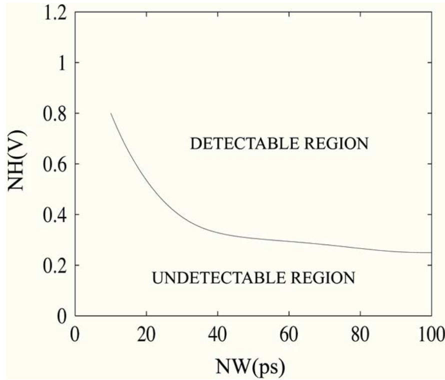

Fig. 12. Detectable regions for the high-level monitor.

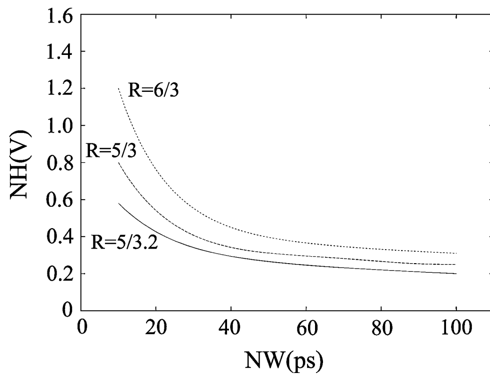

Fig. 13. Pulsewidth of the noise versus voltage noise for different ratios of the inputs transistor widths for high-level SIV monitor, $R = W_{N1}/W_{N2}$.

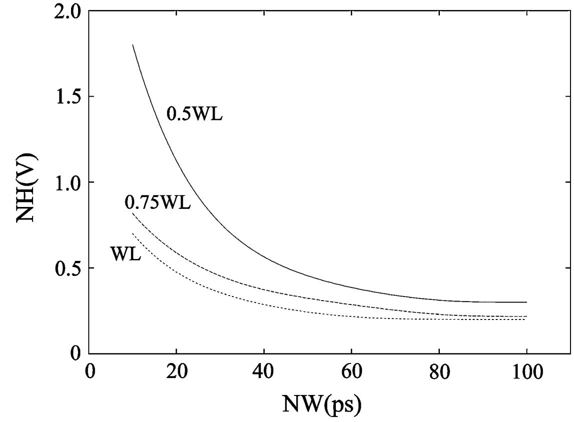

Fig. 14. Dependence of the performance of the high-level monitor on transistor sizing of the latch load.

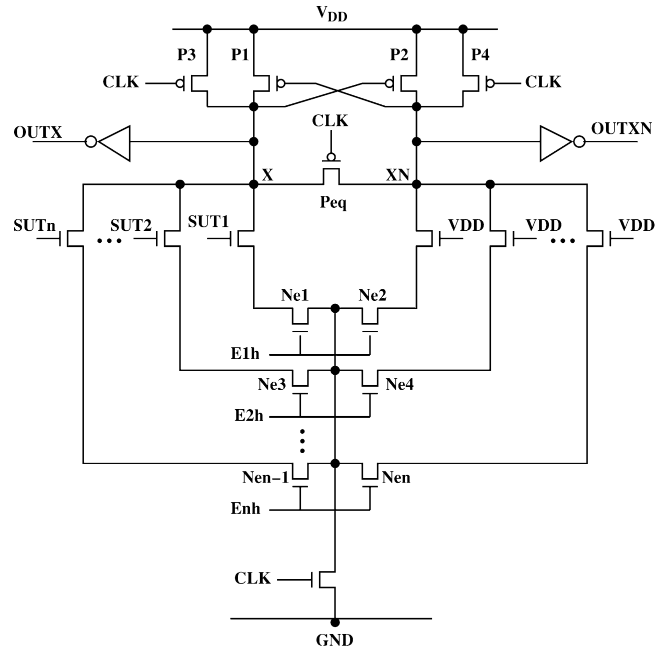

Fig. 15. High-level signal integrity monitor with multi-input signals.

ratio W_{N2}/W_{N1} increases. The dependence of the high-level monitor on transistor sizing of the latch load is shown in Fig. 14. The detection curve moves up as the transistor sizes of the latch load decrease. The sizes of the precharge transistors do not require to be designed large because the precharge takes several clock cycles.

E. Multisignal Monitor

The monitors mentioned before have been adapted in order to test multiple signals (see Fig. 15). Let us define n as the number of SUT. By adding equal n number of transistors in both input sides of the monitor (input and reference signals) and pairs of enable transistors (controlled by signals E_n), it is possible to test n signals. One signal at a time is tested enabling the control signal E_n that corresponds to the SUT. Equal numbers of input and reference transistors are required to have the same load at nodes X and XN. In a similar way, the low-level signal integrity monitor is modified to test multiple signals. Signals in the multisignal monitor are tested sequentially. The enable transistor of the signal to be monitored is activated followed by the activation of the CLK control signal. Using this sequencing of signals and sizing, the transistor controlled by CLK properly reduces interference due to nonideal switch behavior of the enable transistors.

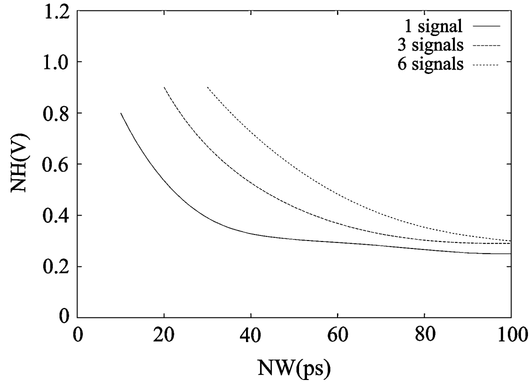

Fig. 16. Dependence of the monitor behavior on the number of monitored signals.

The dependence of the behavior of the multisignal monitor on the number of sensing signals has been analyzed. The designed one signal monitor is used as reference. Transistors with sizes similar to the one signal monitor are added for the multisignal monitors. As a monitor tests more signals the performance curve moves up (see Fig. 16), which means that the ability of the monitor to test noise pulses with lower NH and NW decreases. In other words, for the same pulsewidth (height), the minimum detectable noise magnitude (width) is higher (larger) as the number of sensing signals increases. Let us assume that the receiver gates have similar noise margin curves. The performance of the multisignal monitor should match the noise margin curves of the receiver gates. The behavior of the multisignal monitor is also influenced by the gate–drain coupling capacitances and drain–source charge distribution of the nonenabled input transistors (see Fig. 15). Worst-case perturbation at nodes X and XN have been simulated. For a multisignal monitor that handles three signals, the noise voltage perturbation added by each monitor at the nodes X and XN is less than 10 mV.

The testing strategy allows to test a signal in the high and low logic level in one unit test period (UTP), which is formally defined in Section IV, without loss of information. The control logic uses a flag (ER) to indicate the stable state of the SUT. The period of the ER signal is equal to 1 UTP. When ER is high, the enable signal of the high-level monitor for signal S2 is activated. At the same time, the enable signal corresponding to the test of the low logic level of the next signal (S3) is also asserted. At this state of ER, the stable high logic level of S2 is under test and the output information of S3 is discarded. When ER goes low, the enable signal for the low-logic-level monitor for S3 continues to be asserted, and the enable signal of the high-logic-level monitor for signal S3 is asserted. At this state of ER, the stable low logic level of S3 is under test and the output information of high logic level of S3 is discarded. This process repeats in order to test the stable high and low logic levels of the other signals.

The choice of using single or multisignal monitor needs to be evaluated for each application. The natural choice is to use a single monitor that has less complex implementation and a more controllable performance curve (see Fig. 16). To use a multiple signal monitor instead of a single monitor(s) requires the evaluation of the following aspects:

1) required NH and NW of a noise pulse to be detected (see Fig. 16);
2) nearness of the signals to be tested (near signals save routing area);
3) control circuit complexity due to enable and control CLK signals;
4) routing overhead due to the enable signals (this cost is minimized having the control circuit close to the SUTs);
5) test time overhead for multisignal monitor due to sequential access of the signals to test.

F. Test Architecture

The test architecture to read out the information stored at the output monitor cells depends significantly on the testing objective and cost considerations [15]. The proposed test architecture has been adapted from [15] and [27]. Let us assume that the identification of an SIV event is required. In this case, an n-bit bus requires $2n$ single monitors. Each output of the monitors goes to a flip-flop. The flip-flop outputs are inputs to an AND function. Inverter gates can be added to assure a 0 logic state at the AND output when there is no SIV. A violation is identified when the AND output goes to 1 logic. For diagnosis purposes, the test architecture proposed in [15] and [27] can be used. When a multisignal monitor is used, the number of required flip-flops is reduced. In this case, the data from the monitors are time-multiplexed.

IV. Coherent Sampling

Coherent sampling is used to read the information of the SUT. Coherent sampling guarantees that the sample set contains a complete, periodic waveform representation [26]. Using coherent sampling, a relatively low actual sampling rate is used to achieve a highly effective sampling rate.

The relationship that creates a coherent sample set is [26]

$$\frac{F_t}{F_s} = \frac{M}{N} \tag{5}$$

where F_t is the frequency of the SUT, F_s is the sample frequency, and M is the total number (integer) of cycles of the SUT over which samples are taken. This forms a UTP. N is the total number (integer) of samples taken in one UTP.

The sampled signal is the SUT that is a periodic waveform. Our approach is mainly oriented to those signal integrity perturbations related with the internal behavior of the circuit such as crosstalk, and ground/VDD bouncing. It is not oriented to cover perturbations linked with the external environment of the circuit. The sampled signal repeats M times into one UTP, and N samples are taken (see Fig. 17). In one UTP, all the information of the sampled signal is obtained. Into this UTP, the high and low logic levels of the SUT are verified.

To avoid duplicate samples in different signal periods, M and N are chosen mutually prime [26]. In other words, this condition ensures that each cycle contributes unique and independent information. Mutually prime numbers means that M and N have no common factors other than 1. Coherent sampling makes it possible to obtain all information of the signal in one UTP; the

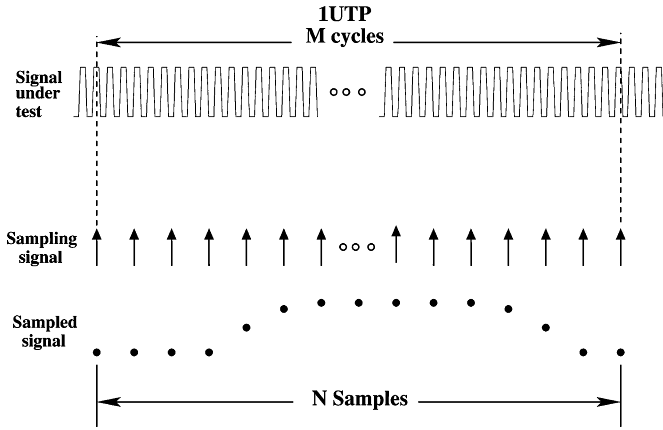

Fig. 17. Basic scheme of coherent sampling where the SUT is sampled N times. The signal repeats M times.

number of samples N in a periodic waveform should be sufficient to capture the total signal information. The effective sampling rate F_s' is given by [26]

$$F_s' = F_t N \qquad \text{or} \qquad F_s' = F_s M. \tag{6}$$

In coherent sampling, the effective spacing $\Delta T_P (1/F_s')$ is important rather than the actual sample spacing. ΔT_P can be expressed in degrees as

$$\Delta T_P^o = \frac{360}{N}. \tag{7}$$

In units of time, ΔT_P is equal to

$$\Delta T_P^t = \frac{1}{F_s \times M}. \tag{8}$$

V. Implementation Considerations

A. Effect of Clock Jitter

Under coherent sampling, the SUT is sampled several times depending on the effective sampling rate. For an effective sampling rate, K samples can be taken in the detectable part of a given noise pulse. The detectable part is defined by graphical representation of the high-level monitor performance (see Fig. 12). The required effective spacing for having at least K detections of the sampled signal can be estimated by

$$\Delta T_P^t = \frac{\text{NW}'}{K} \tag{9}$$

where NW$'$ is the time duration of the desired detectable region of the noise pulse noise.

Clock jitter can cause a time variation of the trigger sampling points at the SUT that may affect the detection of the noise pulse. Because of this, the total amount of allowed jitter in order to assure the detection of a desired minimum pulse noise needs to be estimated. The influence of the clock jitter in the SUT is represented in Fig. 18. t1, t2, t3 and t4 correspond to the samples without jitter. t1$'$, t2$'$, t3$'$, and t4$'$ are assumed trigger sampling points due to clock jitter. Let us analyze the third sample illustrated in Fig. 18. This sample should normally be taken in the detectable part of the undershoot. However, because of clock

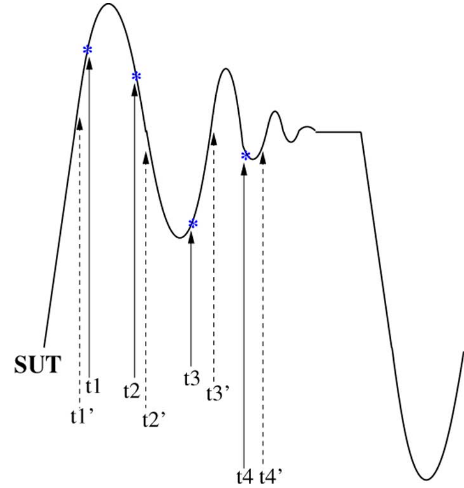

Fig. 18. Jitter influence on signal integrity testing.

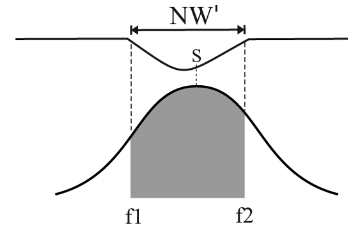

Fig. 19. Probability of detection of one sample.

jitter, the sampling may occur at a different point of the SUT as shown in Fig. 18. Hence, a signal violation is not identified by this sample.

Let us assume that the clock (PLL) jitter is a Gaussian distribution random variable. The probability of one sample (P_D) being taken in the noise pulse region (NW$'$) in the presence of clock jitter can be expressed as

$$P_D = \frac{1}{\sigma\sqrt{2\pi}} \int_{f1}^{f2} e^{-(x-\mu)^2/2\sigma^2} dx \tag{10}$$

where σ is the standard deviation of the clock jitter, μ is the mean value of the trigger sample, and $f1$ and $f2$ define the integration region of interest of the noise pulse.

The probability of detection of one sample is illustrated graphically in Fig. 19. For the sample "S," the probability of detection of the noise pulse (P_D) for a given clock jitter is obtained by integrating the area of the curve in the region that the noise pulse is present.

The probability of detection for K samples (P_D^K) taken in the noise pulse region is given by

$$P_D^K = 1 - P(S_1')P(S_2')\cdots P(S_K') \tag{11}$$

where S_1', S_2', and S_K' are the complement of the detection probabilities of each sample taken in the noise pulse.

The probabilities of detection for K samples taken in the detectable region of a noise pulse are given in Table II. A detectable region of a noise pulse of 40 ps and an effective spacing of 10 ps are considered. Because the first sample at the noise pulse can occur at different times, P_D^K was obtained for different

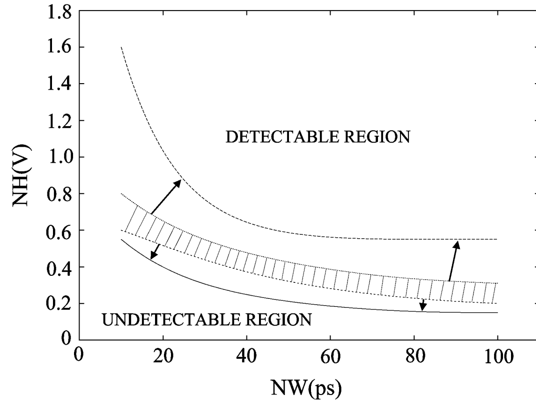

Fig. 20. Process and power supply variations impact on the performance of the high-level monitor. Shaded area is the "uncertain region."

TABLE II
DETECTION PROBABILITIES FOR DIFFERENT STARTING SAMPLING TRIGGERS

σ	5ps	10ps	20ps	30ps	40ps
$P_D^K(S_1)$	0.9999	0.9994	0.9773	0.9176	0.8405
$P_D^K(S_5)$	0.9999	0.9994	0.978	0.919	0.842
$P_D^K(S_8)$	0.9999	0.9993	0.9762	0.9151	0.8367

TABLE III
DETECTION PROBABILITY DEPENDENCE ON THE EFFECTIVE SPACING

σ	5ps	10ps	20ps	30ps	40ps
$P_D^K(\Delta T_P^t = 20ps)$	0.9988	0.9774	0.8528	0.7158	0.6025
$P_D^K(\Delta T_P^t = 10ps)$	0.9999	0.9994	0.978	0.919	0.842

initial sampling triggers at the noise pulse: S_1 for the first sample to occur at 1 ps after the beginning of the detectable region of the noise pulse, S_5 at 5 ps and S_8 at 8 ps.

It has been found that the detection probability decreases as the standard deviation of the clock jitter (σ) increases. Also, it can be observed that the probability of detection just changes slightly with the location of the first sampling trigger on the noise pulse. The dependence of the probability of detection on the effective spacing is shown in Table III. Two cases have been considered. The first has an effective spacing of 20 ps. In this case, the samples are taken at 5 and 25 ps. The second has an effective spacing of 10 ps. In this second case, the samples are taken at 5, 15, 25, and 35 ps. In Table III, it can be observed that the probability of detection increases for a lower effective spacing.

Using Table III, the required effective spacing is determined according to the desired probability of detection for a given standard deviation of the clock jitter. Using this, the other coherence parameters can be obtained according to (5) and (8).

B. Effect of Process and V_{DD} Variations

Process parameter variations in the manufacturing process may cause deviation of the monitor behavior from the nominal values. Variation in channel length has the greatest effect on circuit performance [34]. Other important parameters are effective gate oxide thickness variation [34] and random doping fluctuations [35].

TABLE IV
AREA USED BY THE FLIP-FLOP OF THE DIVIDERS

Relation M/N	Area (μm^2)
25/6	590.5
41/10	732.2
67/16	791.2

A Monte Carlo analysis has been carried out for the monitor. According to the information supplied by the foundry a uniform distribution is used with the following tolerances: 3.18% for the gate oxide thickness, 22.46% for the nMOS transistor threshold voltage, 15.3% for the pMOS transistor threshold voltage, 4.4% for the channel width, and 7.3% for the channel length. All the parameters subject to process variations are randomly varied during each run of the Monte Carlo simulation. The simulation results, obtained with 35 Monte Carlo runs, are shown in Fig. 20. The dashed area shows the effect only due to process variations. The upper (lower) curve of the dashed area corresponds to the lower (upper) limit of the detectable (undetectable) region. As a consequence, only those noise pulses, characterized by NH, NW, located above (below) the lower (upper) limit of the detectable (undetectable) region can be assured as detectable (undetectable). The behavior is uncertain for those noise pulses located in the shaded region. In other words, detection/nondetection for noise pulses located in this region cannot be assured.

Interconnect is also subject to process variations. In our case the interconnect length from the accessed point of the line under test to the monitor location is especially important. Because of process variations the information arriving at the monitors may suffer changes with respect to the accessed point. This can be minimized by locating the monitors close to the lines under test.

Fluctuations of the power supply influence the performance of the monitor. V_{DD} variations move the performance curve defining the accepted/nonaccepted regions (see Fig. 3). The effect of power supply fluctuations (variation of 10%) is to shift upward (downward) the lower (upper) limit of the detectable (undetectable) region. This is also shown in Fig. 20. The monitor is designed to assure that noise pulses (NH and NW) not affecting the logic response of the receiving circuit, i.e., corresponding to the accepted noise region (see Fig. 3), fall in the undetectable region (see Fig. 20) in the presence of process and power supply variations.

VI. COST

The cost of the proposed testing strategy has been estimated in terms of area, delay penalization, and test time.

Two monitors are required. Using TSMC 0.18 μm technology, the estimated area for one high-level monitor with three signals to be verified is 274 μm^2. The cost is shared between the three signals to test. Flip-flops to divide the clock signal are required. Their area depends on the chosen coherent relation M/N. The area used to implement some coherent relations M/N are given in Table IV. A typical flip-flop from TSMC 0.18 μm technology with an area of 70.85 μm^2 is used. In addition, routing of the clock signals to the monitors is also required. This area depends on the particular design and the number of monitors used.

TABLE V
DELAY IMPACT DUE TO THE PROPOSED TESTING METHODOLOGY

l(mm)	Delay penalty
1	2.3%
2	2.1%
4	1.9%
6	1.65%
8	1.55%
10	1.4%

For each sensing line, the added capacitance due to the gate capacitance of the monitor sensing transistor is about 4.4 fF. Let us assume a 1-mm-long interconnect line driven by a buffer inverter. A similar inverter is placed at the end of the line. Moderate-sized inverters are used ($W_N = 10$ μm, $W_P = 30$ μm). The delay penalization due to monitor loading for different interconnect lengths is given in Table V. The delay penalization decreases for longer interconnect lines.

Selection of the coherence parameters determines the test time that has a high economic impact on the overall cost. The time to test "*n*" signals (T_{test}) can be estimated by

$$T_{\text{test}} = MT_{\text{SUT}}n \tag{12}$$

where T_{SUT} is the period of the SUT.

The desired narrowest noise pulse to be detected, obtained from the noise margin curve of the receiver, determines the required effective spacing. However, test engineers also need to consider the test time. From (8) and (12), it can be observed that there is a tradeoff between effective spacing and test time. Decreasing (increasing) M reduces (enlarges) the test time and enlarges (reduces) the effective spacing.

VII. Silicon Validation and Comparison With Previous Work

In this section, measurements taken in designed and fabricated circuits are presented. Finally, our proposal is compared with previous work.

The circuits have been fabricated in AMI 0.35 μm CMOS technology. Using this technology, the feasibility of the performance of the proposed monitors is shown. The block diagram of the designed circuit is shown in Fig. 21, and a photograph picture is shown in Fig. 22.

High- and low-level monitors have been implemented in this module. Both monitors have been designed for sensing three signals. The SUT is internally generated by a voltage-controlled oscillator (VCO, see Fig. 21). A free-running three-stage ring oscillator is used. The maximum working frequency of this oscillator is 1.2 GHz. However, the noise injector circuitry limits the useful maximum frequency to 917 MHz. At this frequency, well-controlled overshoots and undershoots can still be injected into the generated signal of the VCO. Working at these frequencies allows us to have a well-controlled experiment. The signal generated by this module can be indirectly observed at an external pin. A frequency divider ($\div 32$) is used to divide the frequency of the signal generated by the VCO. The output of the frequency divider is sent out to an output pin.

Noise injector circuitry has been designed to inject undershoots and overshoots to the SUT (see Fig. 21). The basic noise

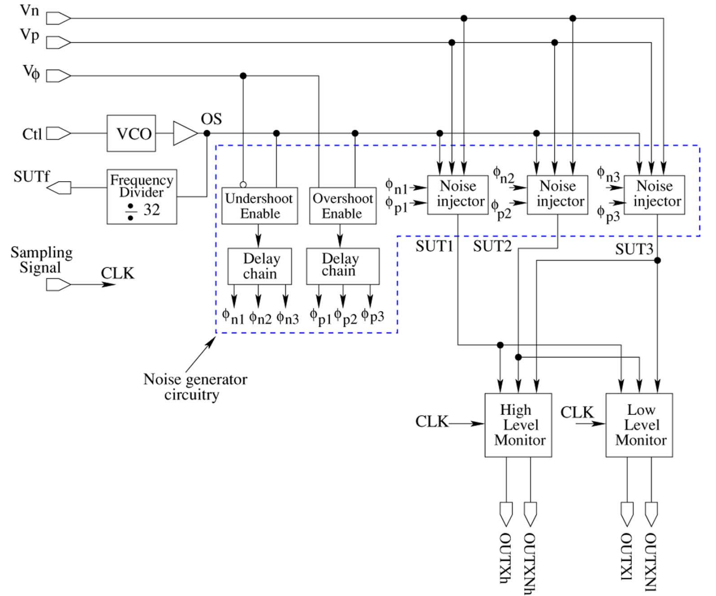

Fig. 21. Block diagram of the designed circuit.

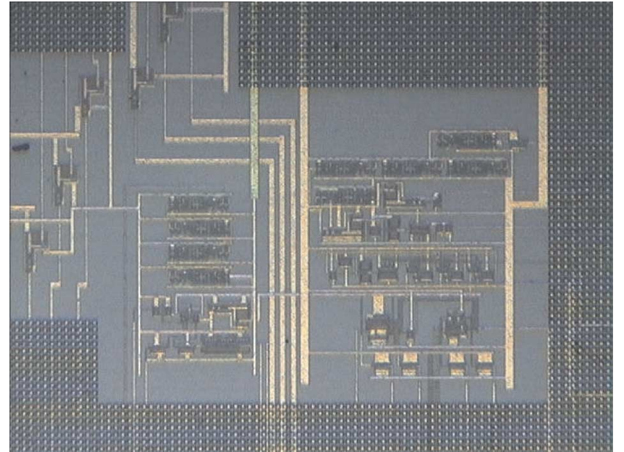
Fig. 22. Picture of the designed circuit.

injector circuitry is shown in Fig. 23. The circuit generates overshoots (undershoots) if the transistor M1 (M2) is activated by the pulse $\phi_p(\phi_n)$. A delay chain is used to generate signals ϕ_p and ϕ_n for each monitor. The characteristics of the noise pulses are controlled externally by the dc voltages V_n and V_p. Control signal $V\phi$ (see Fig. 21) selects the noise injection for either the undershoot or the overshoot.

A. Measurements for the High-Level Monitor

The measurements for the high-level monitor are presented in this section. The dynamic performance of the monitor for the noise-free and noise-present cases has been obtained. The transistor channel widths and lengths for the high-level monitor (see Fig. 4) implemented in the modules are shown in Table VI. Ne1–Ne6 are the enable transistors (see Fig. 15).

The following measurements are presented:

1) Noise-free SUT at coherent sampling 1, fclk $=$ 6.8 MHz;
2) SUT with a noise pulse at coherent sampling 1, fclk $=$ 6.8 MHz;

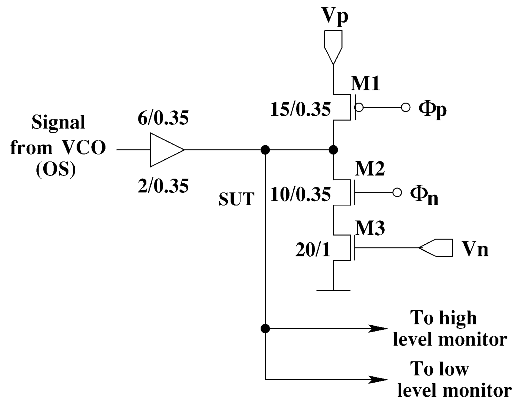

Fig. 23. Schematic of the basic noise injector circuitry.

TABLE VI
TRANSISTOR SIZES FOR THE FABRICATED HIGH-LEVEL MONITOR

Transistors	W/L (μm / μm)
P1, P2	25/0.35
P3, P4	10/0.35
Peq	10/0.35
N1	10/1
N2	5/1
Ne1 to Ne6	8/0.35
Nb	15/0.35

3) SUT with a noise pulse at coherent sampling 2, fclk = 13.6 MHz.

The characteristics of the experimental noise pulse, used for the high-level monitor, have been estimated from electrical simulations. The signal generator and the noise pulse generator circuitry have been simulated with the dc voltages values of V_p and V_n, which define the noise characteristics, used during the experimental measurements. The estimated noise pulse has a height (NH) of 1 V and a width (NW) of 198 ps. Let us explain the expected results before showing the measurements. When the SUT does not have integrity violation, the output of the high-level monitor (see Fig. 4) behaves as follows. For one sample of the SUT in a low logic level, the node $OUTX$ remains low and $OUTXN$ presents a pulse when the SUT does not have SIV. For one sample of the SUT in a high logic level, the node $OUTX$ presents a pulse and $OUTXN$ remains low when the SUT does not have SIV. For one sample of the SUT in a high logic level, $OUTX$ remains in a low logic level and $OUTXN$ presents a pulse when the noise is sufficiently large.

Fig. 24 shows the measurements for the high-level monitor when the SUT is noise-free; eight samples are taken. The frequency of the SUT is 917 MHz. The observed SUT was internally generated by a VCO and then divided by 32 (see Fig. 21). The SUT frequency before the division is 917 MHz. The sampling signal (CLK) is also shown in Fig. 24. The sampling frequency is 6.8 MHz. Due to the chosen coherent relation, eight samples of the SUT are taken in one UTP. From left to right, during the first four samples, $OUTX$ presents pulses indicating that the SUT is sampled in the high logic state. For the last four samples, this node remains at logic 0, indicating that the SUT is sampled in the low logic state. Because the SUT is noise-free, $OUTX$ commutes four times for the first four samples. $OUTXN$ is also shown in Fig. 24.

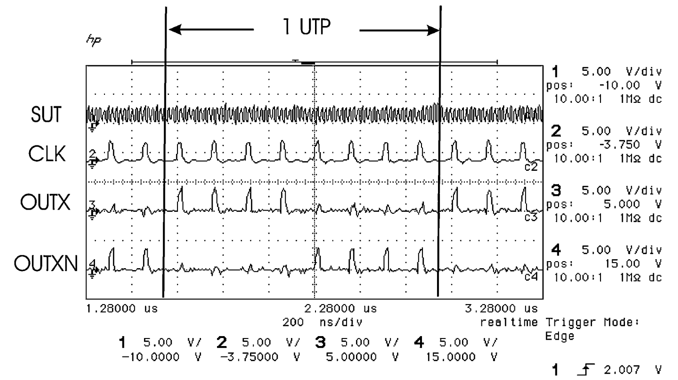

Fig. 24. Measurement of the high-level monitor response in the case of the noise-free SUT. Eight samples are taken into the UTP at rate of $f_{\rm SUT} = 917$ MHz, $f_{\rm CLK} = 6.8$ MHz.

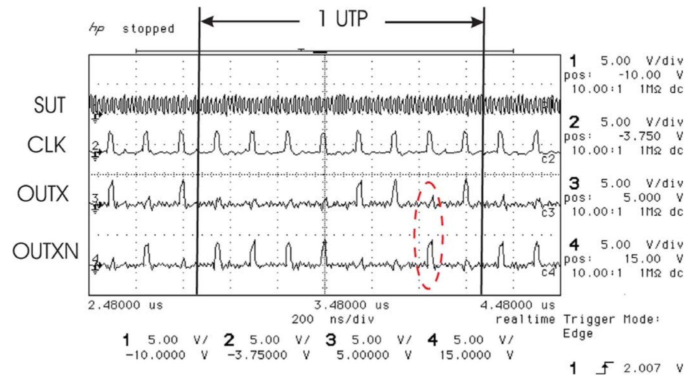

Fig. 25. Measurement of the high-level monitor response in the case of the SUT with signal integrity degradation. Eight samples are taken into the UTP, $f_{\rm SUT} = 917$ MHz, $f_{\rm CLK} = 6.8$ MHz, $\rm NH = 1$ V, $\rm NW = 198$ ps.

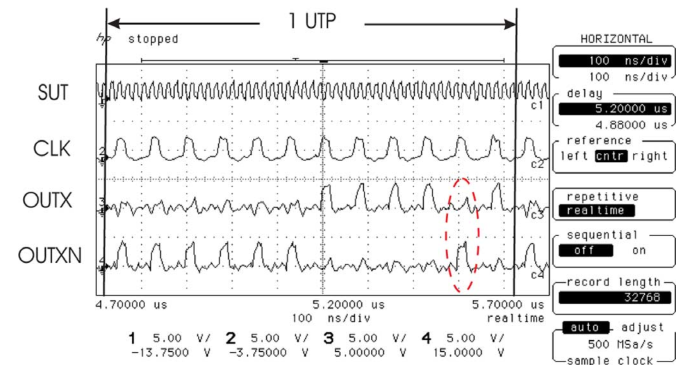

Fig. 26. Measurement of the high-level monitor response in the case of SUT with signal integrity degradation. Twelve samples are taken into the UTP, $f_{\rm SUT} = 917$ MHz, $f_{\rm CLK} = 13.6$ MHz, $\rm NH = 1$ V, $\rm NW = 198$ ps.

The monitor performance for the case of the SUT with an SIV is shown in Figs. 25 and 26. An undershoot is injected by the noise generator circuitry in the high logic level of the SUT.

Fig. 25 shows the measurements for the case of a sampling signal with frequency of 6.8 MHz. Using this, eight samples are taken into one UTP. From left to right, the first four samples are taken in the low logic level of the SUT. As a result, $OUTX$ remains at low logic level and $OUTXN$ presents pulses. In the

TABLE VII
TRANSISTOR SIZES FOR THE FABRICATED LOW-LEVEL MONITOR

Transistors	W/L (μm / μm)
N1, N2	10/0.35
N3, N4	10/0.35
Neq	10/0.35
P1	10/1
P2	5/1
Pe1 to Pe6	10/0.35
Pb	25/0.35

last four samples, the SUT is sampled at its high logic level. In the seventh sample, into the UTP, the high-level monitor detects an integrity violation. Node $OUTX$ is a logic 0 and node $OUTXN$ presents a pulse.

Fig. 26 shows the measurements for the case of a sampling signal with frequency of 13.6 MHz. Because of this, 12 samples are taken into one UTP. From left to right, in the first six samples, the SUT is sampled in the low logic level. $OUTX$ remains at logic 0 and $OUTXN$ presents pulses. In the next six samples, the SUT is sampled in the high logic level. In the eleventh sample, the undershoot is detected. $OUTX$ is logic 0 and $OUTXN$ presents a pulse.

B. Measurements for the Low-Level Monitor

Measurements for the low-level monitor are presented. The transistor channel widths and lengths for the designed and fabricated low-level monitor (see Fig. 9) are shown in Table VII. In a similar way to the high-level monitor, Pe1–Pe6 are the enable transistors (not shown in Fig. 9). The frequency of the SUT is 917 MHz. In this case, overshoots above the logic 0 level (G_{ND}) are injected by the noise generator circuitry. The used noise pulse has a height (NH) of 1.3 V and a width (NW) of 198 ps.

The following measurements are presented:

1) noise-free at coherent sampling 1, $\text{fclk} = 6.8$ MHz;
2) SUT with a noise pulse at coherent sampling 1, $\text{fclk} = 6.8$ MHz.

The measurements for the noise-free case are shown in Fig. 27. For the sampling signal with $\text{fclk} = 6.8$ MHz, eight samples are taken into one UTP. In the first four samples from left to right, the SUT is sampled at the low logic level, and because the SUT is noise-free, $OUTX$ presents pulses on each CLK period and $OUTXN$ remains at logic 1. In the last four samples, the SUT is sampled at the high logic level. Because of this, $OUTX$ is logic 1, and $OUTXN$ presents pulses.

The performance of the low-level monitor for the case of the SUT with an SIV is shown in Fig. 28. In this case, an overshoot has been injected by the noise pulse generator circuitry in the low logic level of the SUT. For the sampling signal with $\text{fclk} = 6.8$ MHz, eight samples are taken into one UTP. From left to right, the first four samples are taken in the high level of the SUT. Because of this $OUTX$ remains at logic 1 and $OUTXN$ presents pulses. In the last four samples, the SUT is sampled at the low logic level. In the sixth and seventh samples of the UTP the low-level monitor detects an integrity violation.

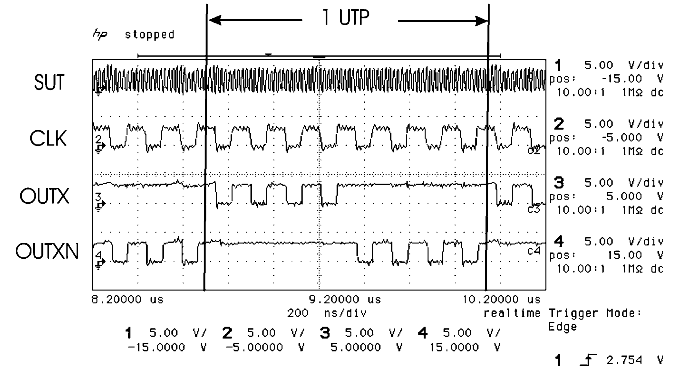

Fig. 27. Measurement of the low-level monitor response in the case of the noise-free SUT. Eight samples are taken into the UTP at rate of $f_{\text{SUT}} = 917$ MHz, $f_{\text{CLK}} = 6.8$ MHz.

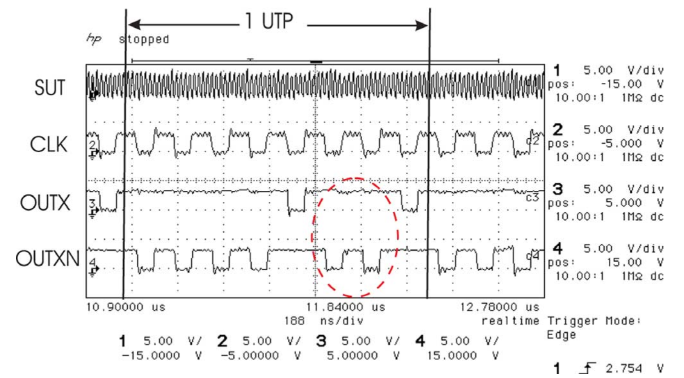

Fig. 28. Measurement of the low-level monitor response in the case of the SUT with signal integrity degradation. Eight samples are taken into the UTP, $f_{\text{SUT}} = 917$ MHz, $f_{\text{CLK}} = 6.8$ MHz, $\text{NH} = 1.3$ V, $\text{NW} = 198$ ps.

$OUTX$ is logic 1 and the node $OUTXN$ presents a pulse in these samples.

C. Comparison With Previous Work

The sensor cell proposed by Attarha and Nourani[15] is composed of a cross-coupled differential amplifier and a discriminating inverter. This sensor has hysteresis. This property allows the testing of noise violations above and below the stable values (V_{DD} or V_{GND}) with the same cell. On the other hand, once an event is detected, it cannot detect another violation for the same stable state. This issue is addressed by Xu *et al.* [19]. They introduce an extra transistor working as a Reset. Whenever a signal integrity error is captured, a "shift" signal resets the detector back to the error-free state. They also modified the amplifier to be self-biased. Their sensor is intended for detecting overshoots above (V_{DD}). However, this topology is also able to detect noise violations below (V_{DD}) with minor modifications. Our proposed sensor is also based on a cross-coupled differential amplifier. Discriminating inverters are used. We have added two precharge transistors and the tail transistor is controlled by a sampling clock signal (coherent sampling). This strategy allows testing more than one violation event at the stable logic values. This is because precharge takes place each time that the signal is sampled (tested) at different

locations. The detection can be made for short separations between the noise violations. Our sensor also uses an equalization transistor to assure well-established voltage values at the comparison nodes. Furthermore, our sensor has been adapted to test more than one signal. In this paper, a coherent sampling strategy is proposed. A level detection approach [15], [19] can also be used to test SI faults. This approach may serve the test requirements for given SI test specifications at a lower test time penalization.

VIII. Conclusion

Testing of signal integrity undershoots and overshoots using novel built-in high-speed monitors has been proposed. Coherent sampling is used to read the information of the SUT(s). Two monitors have been proposed. The high- (low-) level monitor is used to test undershoots (overshoots) for high (low) logic levels. The capability of the proposed monitors to detect noise violations depends on the width and height of the noise pulses. For each monitor, two well-defined regions appear: the detectable and the undetectable regions. The detectable and undetectable regions can be modified by proper sizing of the transistors of the monitor circuits. For a monitor designed to test one input signal, using TSMC 0.18 μm technology, the minimum detectable NW is 10 ps. The monitor has been extended to test more than one signal. The minimum detectable noise pulsewidth increases for a higher number of SUTs by the same monitor. The implementation considerations of the proposed testing strategy have been analyzed. Both the effect of clock jitter and process variations have been considered. The cost of the proposed testing strategy has been analyzed. The delay and area penalization is small. Furthermore, for the multisignal monitor, the area cost is distributed among the signals to test. Experimental measurements carried out on specially designed and fabricated circuits have been obtained. High- and low-level monitors have been considered. The monitor responses for the noise-free case and under the presence of noise have been obtained at different coherent frequencies. A good agreement appears between the theoretical analysis, simulation results, and the experimental measurements.

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