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Optimized reduction of spur tones in fractional frequency synthesizers

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Abstract In this article the contribution of the digital ΣΔ modulator in fractional frequency synthesizers is explored. Due to the circuit's non linear behavior, the spur tones generated by the digital ΣΔ modulation degrade the synthesizer's phase noise even in regions where the charge pump noise is dominant. A new method to dither digital MASH ΣΔ modulators for fractional frequency synthesizers is proposed. The method barely increases the circuit complexity and has the same performance as more cumbersome architectures. Also, a new design consideration to linearize the voltage control oscillator is proposed. Experimental results are obtained in an on-chip fractional synthesizer manufactured in CMOS technology.

Keywords Fractional · Frequency synthesizers · Digital-sigma-delta · Phase noise · Spur tones

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1 Introduction

Mixed signal circuits are essential in many integrated circuit applications and problems regarding to coexistence of analog and digital blocks should always be controlled. In particular, the Fractional Frequency Synthesizers [1] used in many communication and clock recovery circuits, are mixed circuits which may suffer from this problem. The periodicity in the digital ΣΔ modulator degrades the phase noise figure.

The fractional frequency synthesizer shown in Fig. 1 generates an output signal whose frequency is an integer L plus a fractional multiple $\frac{K}{2^m}$ of a reference frequency (that is: $F_{out} = (L + \frac{K}{2^m})F_{ref}$). In order to obtain the fractional division, the division modulus of a programable divider is changed pseudo-randomly by a digital ΣΔ modulator. In this way, the average total division value is $L + \frac{K}{2^m}$. Each block in the synthesizer of Fig. 1 introduces perturbations that degrade the total phase noise figure. Figure 2 shows a theoretical phase noise characteristic which can be obtained with the approximations made in [2].

From Fig. 2 it is evident that for high frequencies offset from the carrier the digital ΣΔ modulator increases the phase noise. If the ΣΔ order is augmented, the shaped quantization noise is not well filtered by the low pass network in the frequency synthesizer. One solution could be a low order ΣΔ that has a smoother noise shaping. Nevertheless, the low order topologies suffer the periodic characteristic which is reflected as spur tones that degrade the phase noise figure even more. The practical solution is therefore a sufficiently complex digital ΣΔ architecture to increase the sequence length that controls the programable divider. However, the drawback is the increase of resources for the digital modulator.

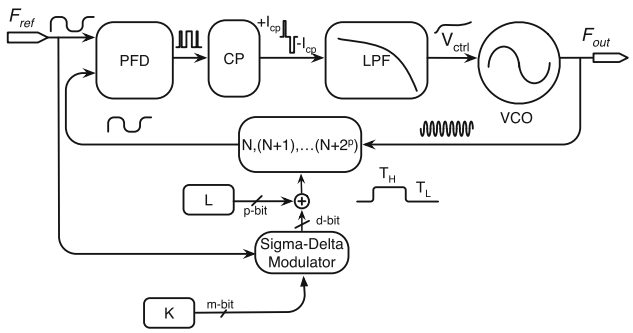

Fig. 1 PLL-based fractional frequency synthesizer

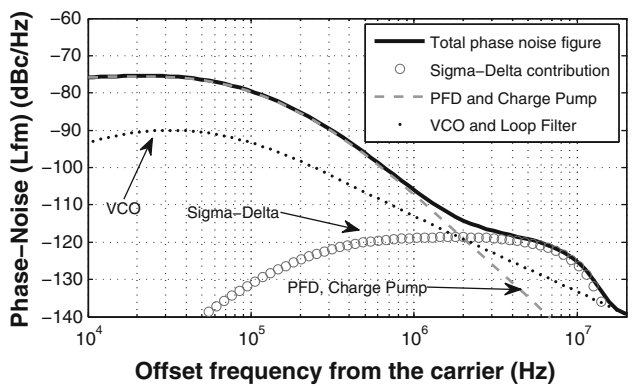

Fig. 2 Theoretical synthesizer phase noise

Multi-stAge-noise-SHaping (MASH) modulators can be constructed only with adders and registers and they are inherently stable. These characteristics make them suitable for fractional synthesizers. Their periodicity can be reduced with Modified Error Feedback MASH modulators [3, 4] but this architecture increases the circuit cost.

This paper presents a more simple solution to extend the periodicity in digital MASH ΣΔ modulators. It is based in a low complexity Linear Feedback Shift Register (*LFSR*) which adds the dither signal in an efficient manner. Section 2 presents the theory which leads to the proposed solution to cancel the ΣΔ MASH periodicity. Section 3 discusses some design considerations for the blocks in a fractional synthesizer. Section 4 presents experimental results of a complete fractional synthesizer with the efficiently dithered ΣΔ MASH to demonstrate that this simple architecture reduces the spur tones.

2 Efficient dither for digital MASH ΣΔ modulators

For an nth order digital MASH modulator the output signal is:

$$Y(z) = X(z) + \left(1 - z^{-1}\right)^n E_n(z) \tag{1}$$

where n is the modulator order and $E_n(z)$ is the quantization error of the last stage. In the digital MASH ΣΔ modulator, the quantization errors are deterministic and all of them are cancelled but the one in the last stage. This property makes the periodicity of the quantization error to depend on the input signal X and the quantization level $M = 2^m$ (where m is the number of bits in the modulator) [3]. One of the most commonly used methods to break the periodicity of a digital ΣΔ modulator is to add a pseudo random signal as a least significant bit in the MASH modulator [5, 6]. For those previous solutions it was proposed to add the dither signal at the input signal or within the MASH middle stages. In general, a very large LFSR was used but this increases the hardware complexity. In this paper we demonstrate that a small LFSR can be as effective as a very large one if it is added in a proper way.

If a dithered signal is added to the carry input of the third stage of a MASH 1-1-1, in order to obtain a shaped dither as is shown in Fig. 3, the quantization error ($e_3[n]$) of the last stage yields the condition:

$$\left(\frac{N(N+1)(N+2)}{3 \cdot 2} X + \frac{1}{M}\sum_{k=1}^{N} d[k]\right) \bmod M = 0 \tag{2}$$

where N is the $e_3[n]$ quantization error period, X is the constant input signal, $M = 2^m$ is the resolution for the m-bit modulator and $d[k]$ is the pseudo random sequence. Actually, at any point in a 1-bit pseudo random sequence, the occurrences of a one or a zero are equal [7] so $\sum_{k=1}^{N} d[k] = N/2$ and therefore Eq. 2 is satisfied for several values of X and M. Under these conditions, even a very long LFSR will not disable the digital modulator's periodicity. In conclusion, no matter how much the size of the LFSR size is increased, it will not reduce the spur tones. This will be experimentally demonstrated in Sect. 4.

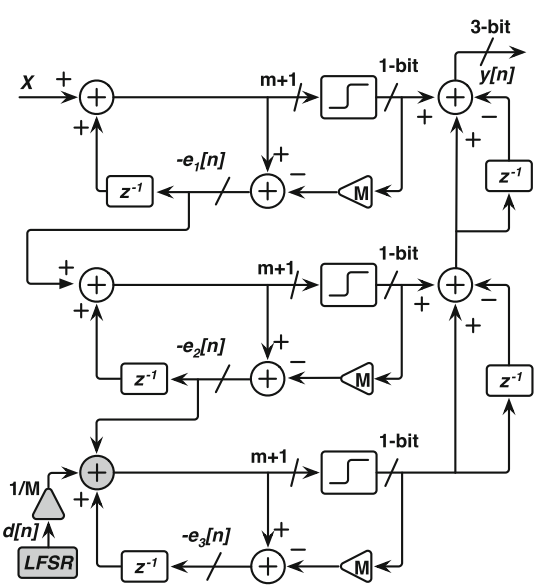

Fig. 3 MASH 1-1-1 digital ΣΔ modulator with dither in the last stage

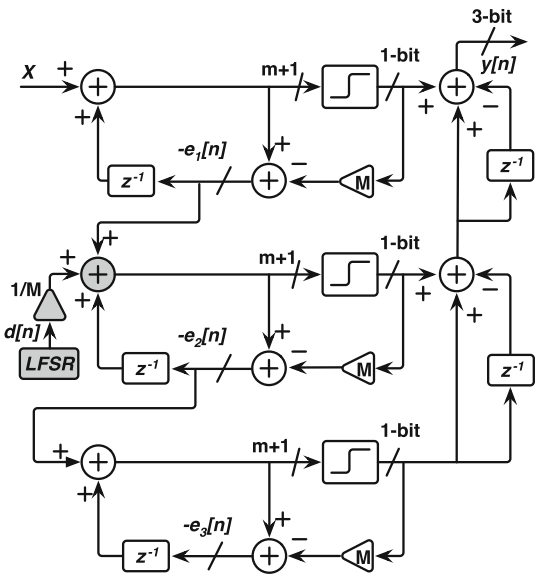

Fig. 4 Proposed solution to disable the periodicity in a MASH 1-1-1 architecture

By contrast, if the pseudo random sequence is added to the least significant bit at the second stage's input, the condition for the $e_3[n]$ quantization error becomes:

$$\left[\frac{N(N+1)(N+2)}{3\cdot 2}X+\frac{1}{M}\sum_{k=1}^{N}\sum_{j=1}^{k}d[j]\right]\bmod M=0 \qquad (3)$$

If the quantization error $e_3[n]$ is to be periodic, the last equation must be satisfied. Differently from Eq. 2, in Eq. 3 the pseudo random expression $\sum_{k=1}^{N}\sum_{j=1}^{k}d[j]$ does not result in a closed form expression. This is because in a pseudo random sequence the ones and zeroes occurrence have the same probability but they are not uniformly distributed within time.

The operation can be realized by a very simple m-bit LFSR which replaces the carry input of the second stage in an m-bit MASH 1-1-1 architecture, as is shown in Fig. 4. The technique can be extended to higher order architectures by dithering the $(n-1)$st. stage carry input. In this way, the dither signal is shaped to $(n-1)$st. order for a nth order MASH ΣΔ modulator, the periodicity is broken and the input X is not affected. The veracity of Eqs. 2 and 3 will be demonstrated in a integrated digital ΣΔ modulator in Sect. 4.

3 Implementation of the architecture in a fractional synthesizer

The proposed solution to eliminate spur tones in a MASH ΣΔ modulator was implemented for a fractional frequency synthesizer in a 0.35 μm CMOS process. This section presents the design considerations used for the constituent blocks of the synthesizer.

3.1 Charge pump and loop filter

To minimize the non linearities in the charge pump, a suitable delay is selected in order to reduce the dead zone of the phase to frequency detector. In addition, a dummy charge pump is used and non-overlapping clocks reduce the charge injection noise [8]. An on-chip current source with low sensitivity to temperature [9] is used to reduce the variations in the charge injection. This current source needs a start-up circuit that it is made with the transistors M_{ps1}, M_{ps2}, M_{ns1} shown in Fig. 5.

Moreover, an active implementation of the first stage in the loop filter helps to set the DC level at the charge pump output. It is achieved by fixing the virtual ground V_x which is the charge pump output in Fig. 6. This dramatically reduces the injected noise from the switches in the charge pump because the switches charge is a strong function of the value V_x. If this value is fixed around a value V_{ref} then the switches can be designed to inject the minimum noise. Otherwise, if the voltage V_x is varying within time, the switches will inject different quantities of noise depending on the bias conditions.

3.2 Voltage controlled oscillator (VCO)

The VCO uses a LC-tank topology as this has the best phase noise performance of all VCOs. The tuning range for

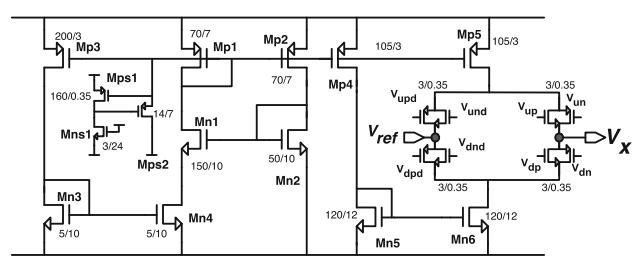

Fig. 5 Charge pump transistor level schematic, it uses a current source with low sensitivity to temperature

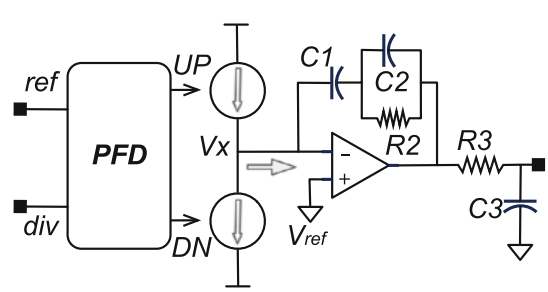

Fig. 6 Fixed voltage in the charge pump output

these architectures is rather non linear due to the non linearity in the varactors. Usually, the varactors can be implemented with minimum length transistors to obtain high Q. In this work, the VCO is designed as shown in Fig. 7 where a high compliance current source was used to give the necessary current for the circuit. The DC value of the output nodes and the control voltage V_{ctrl} determine the region where the transistors (M_7, M_8) used as varactors work. If the voltage ($V_{ctrl} - V_{out}$) is high enough to make the transistors operate in the deep inversion region, the reverse biased diodes (in the source and the drain) behave as the varactors. When the voltage V_{ctrl} is closer to the V_{out} value, the channel to bulk capacitance is a series combination of the gate to oxide capacitance and the depletion capacitance. Thus when the channel is not deeply inverted the varactors are less dependent on the reverse biased diodes of the drain and source. This results in a non desired reduced linearity in the VCO transfer function.

On the other hand, the proposed scheme improves the linearity of the VCO tuning characteristic by setting the DC value of the output nodes closer to the most negative rail for the PMOS cross-coupled pair. Similarly, the DC output value could be set closer to the most positive rail for an NMOS pair. A current source transistor (M_3 in Fig. 7) with a very low value of V_{ds} yields the desired result. In addition, with this scheme, the V_{gs} in the cross-coupled differential pair is increased, allowing a smaller size for these transistors and reducing the parasitic capacitance. Table 1 shows the sizes of the transistors in the VCO. Figure 8 illustrates how the linear range can be improved with this strategy. The varactors remain in the triode condition over a wider range when the output DC value (V_{dsM3}) is close to the most negative rail. Figure 9 shows a photo of the fabricated VCO in a 0.35 μm CMOS process. The experimental result for the improved tuning range of the PMOS cross-coupled VCO is shown in Fig. 10 and is compared with a simulation result when the DC value is at half rail. The low DC output not only improves the linear range but also increases the output frequency as the PMOS cross-coupled pair is smaller and has smaller parasitics. The linearized tuning range can be increased if bigger varactors are used but at the expense of a reduced output frequency. This technique can be used for digitally programable VCOs for multi user communication protocols.

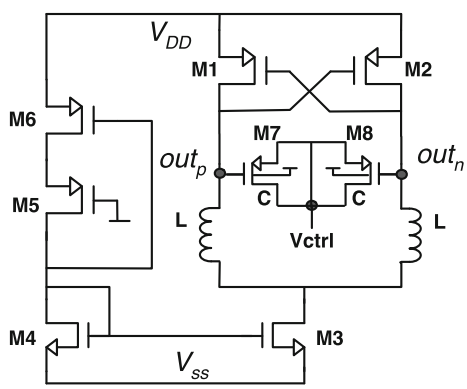

Fig. 7 Schematic of the LC-tank VCO

Table 1 Sizes of the transistors in the VCO

Transistor	W/L (μm/μm)	Transistor	W/L (μm /μm)
M1, M2	150/0.35	M3	2000/2
M4	200/2	M5, M6	500/2
M7, M8	120/0.35	V_{dd}	3.3V

4 Fractional synthesizer experimental results

A microphotograph of the entire fractional frequency synthesizer fabricated in a 0.35 μm CMOS process is

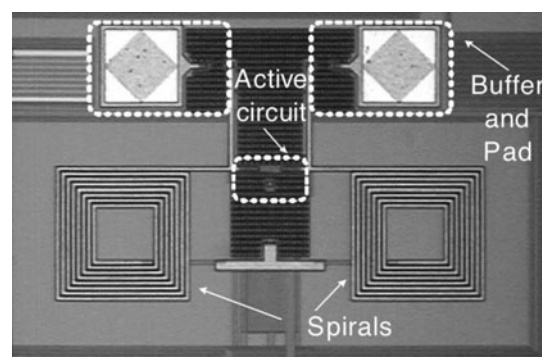

Fig. 9 VCO microphotograph

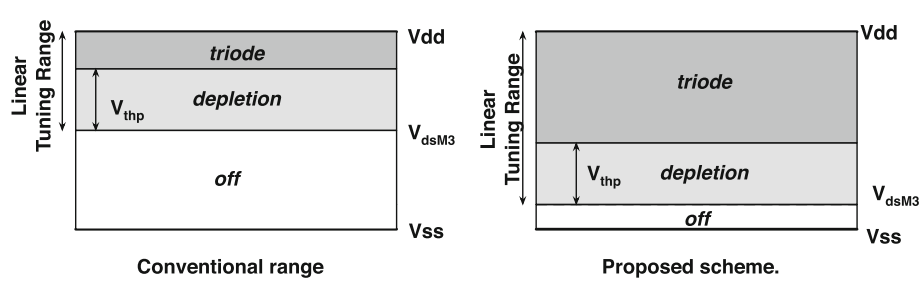

Fig. 8 Increasing the linear operation for varactors in a LC-tank VCO

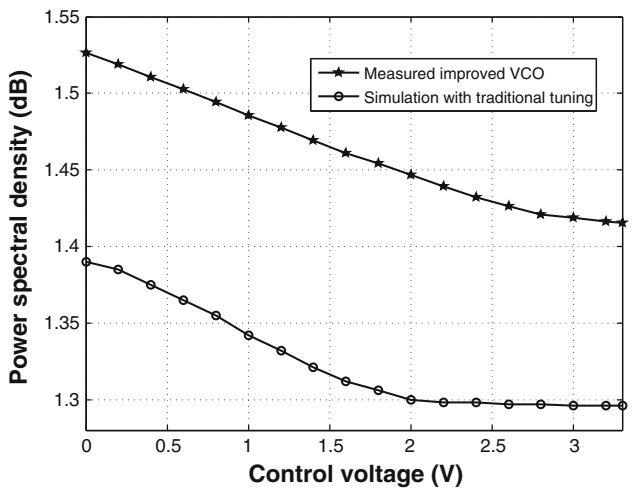

Fig. 10 Experimental result showing the improved tuning range

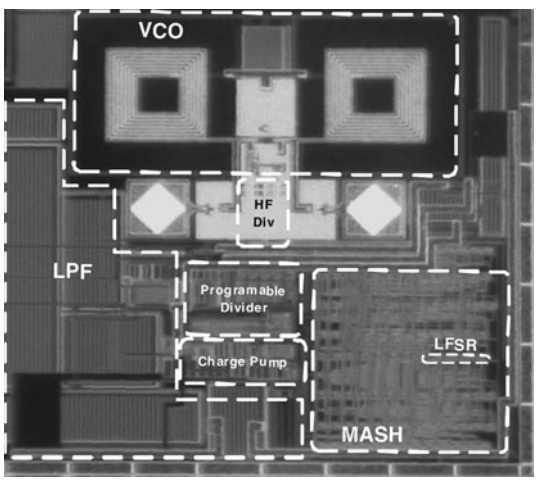

Fig. 11 Microphotograph of the complete fractional synthesizer

shown in Fig. 11. It uses an 8-bit digital ΣΔ modulator whose periodicity is broken with an 8-bit LFSR as is proposed in Sect. 2. The VCO was designed to drive an analog buffer in order to make on-die measurements of the fractional synthesizer. The area labeled low pass filter in the chip includes the OTA, the passive elements and 2–20 pF decoupling capacitors for the analog an digital bias sources, respectively. The charge pump current is generated on-chip with the architecture described in Sect. 3.1.

The experimental results for the digital MASH 1-1-1 ΣΔ modulator are shown in Fig. 12. The measure was done with a constant input value of $X = 128$ to test the digital ΣΔ under the critical conditions for the periodicity according to Eqs. 2 and 3. The proposed dither technique is compared with behavioral simulations of the MEFM architecture [4], when the dither is added in the last stage of the MASH (as in Fig. 3) and with the expected theoretical noise shaping of Eq. 1. The results show that when the

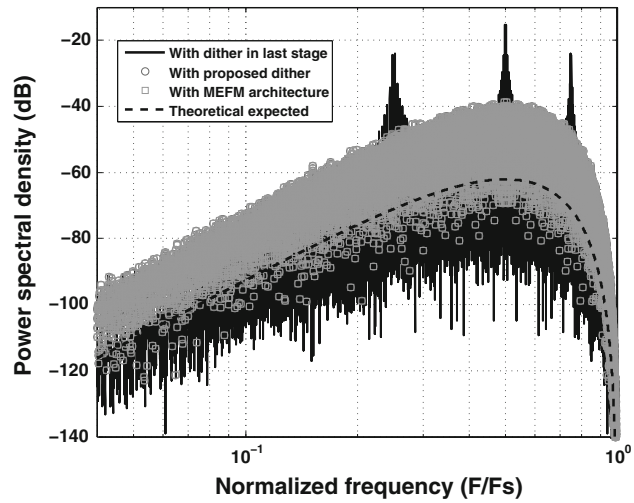

Fig. 12 Experimental result of the MASH 1-1-1 with the proposed dither addition

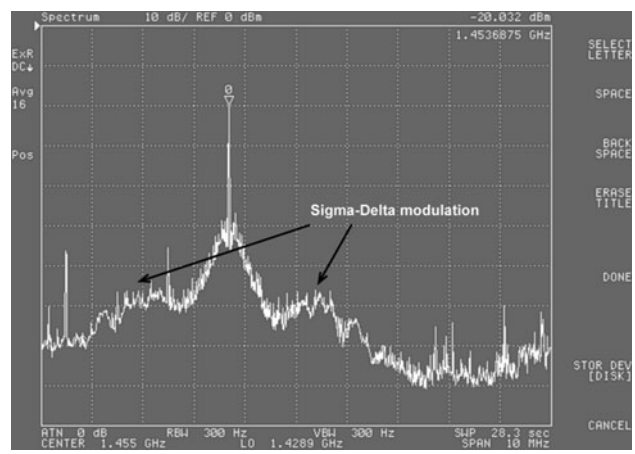

Fig. 13 Measured spectrum of the fractional synthesizer at $f_{out} = 1.453696875$ GHz

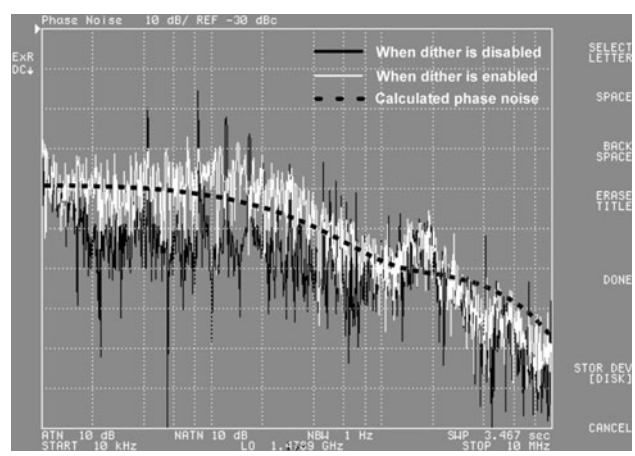

Fig. 14 Measured phase noise characteristic when the dither is not enabled

Table 2 ΣΔ Fractional frequency synthesizer architectures comparison

ΣΔ	ΣΔ Order	Synt. order and (f_c/f_{ref})	Dither	Phase noise spurs
Single-loop [11]	3	4 (0.0037)	2^{24} LFSR	−80dB@60 KHz
Multi-loop [12]	4	5 (0.0190)	No dither	−70dB@300 KHz
Error-feedback [13]	3	4 (0.0153)	2^{10} Off-Chip LFSR	−85dB@13 MHz
Hybrid [1]	≥4	5 (0.0200)	No Dither	−70dB@10 MHz
Hybrid [10]	≥6	3 (0.0015)	No Dither	No
Chebyshev [14]	3	5 (0.0106)	No Dither	N. A.
MASH [8]	3	4 (0.0013)	Off-Chip Dither	−50dB@200 KHz
MASH this work	3	4 (0.0016)	Eff. 8-bit	No

dither is added as in Fig. 3 the LFSR does not break the periodicity, thus verifying Eq. 2. In the Fig. 12 the performance of the proposed technique is very similar to the MEFM but without increasing the hardware significantly as the MEFM requires an additional 8-bit adder for each stage and a post filter stage to cancel the input filtering. The proposed technique only requires an 8-bit LFSR that substitutes the carry-in in the second stage which proves Eq. 3.

The spectrum of the fractional synthesizer when programmed for a fractional division of $67 + \frac{77}{256}$ with a reference frequency of 21.6 MHz is shown in Fig. 13. An output frequency of 1.453696875 GHz is expected and from the Fig. 13 it is observed that the circuit works as expected. The value of $X = 77$ is chosen to show that, even for this non prime input, the spur tones degrade the phase noise but can be corrected with the proposed solution.

The test setup allows to enable and disable the 8-bit LFSR which adds the dither to the 8-bit MASH 1-1-1 digital ΣΔ modulator, as proposed in Sect. 2. Figure 14 shows the measured phase noise of the fractional synthesizer for both cases and compared to the calculated phase noise with a frequency domain model [2]. The measured results were obtained without a time average in the analyzer to avoid the spurs cancellation by averaging. It can be noticed that the spur tones affect the phase noise even in a lower frequency range where the charge pump noise dominates. This is due to the inherently non linearities in the charge pump that become more evident as a result of the digital ΣΔ 's periodicity.

Table 2 presents a comparison of the method with state of the art architectures. The fractional synthesizer's order, the ΣΔ order and the normalized loop filter's cut-off frequency (f_c/f_{ref}) are detailed. For traditional solutions, the use of a cumbersome ΣΔ as the hybrid topology [10] or a high synthesizer's order are needed. For some cases the latter is not sufficient to cancel the spurs [1] . In this work a third order synthesizer with the proposed efficiently dithered MASH are sufficient to reduce the spur tones in the phase noise, demonstrating the effectiveness of the proposed method.

5 Conclusion

It was demonstrated that the periodicity in a digital m-bit MASH ΣΔ modulator can be broken only with a m-bit LFSR. The mathematical analysis used in this work allowed us to show that if the signal from a simple LFSR is added at the input of the $(n-1)$st. stage of an nth order MASH modulator, the periodicity is well broken. The theoretical results were validated by a fully integrated fractional frequency synthesizer.

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