Using S-parameter measurements to determine the threshold voltage, gain factor, and mobility degradation factor for microwave bulk-MOSFETs

Germán Álvarez-Botero *, Reydezel Torres-Torres, Roberto Murphy-Arteaga

Department of Electronics, Instituto Nacional de Astrofísica, Óptica y Electrónica (INAOE), Tonantzintla, Puebla, Mexico

ARTICLE INFO

ABSTRACT

In this paper, we present an extraction and characterization methodology which allows for the determination, from S-parameter measurements, of the threshold voltage, the gain factor, and the mobility degradation factor, neither requiring data regressions involving multiple devices nor DC measurements. This methodology takes into account the substrate effects occurring in MOSFETs built in bulk technology so that physically meaningful parameters can be obtained. Furthermore, an analysis of the substrate impedance is presented, showing that this parasitic component not only degrades the performance of a microwave MOSFET, but may also lead to determining unrealistic values for the model parameters when not considered during a high-frequency characterization process. Measurements were made on transistors of different lengths, the shortest being 80 nm, in the 10 MHz to 40 GHz frequency range.

© 2010 Elsevier Ltd. All rights reserved.

1. Introduction

Nowadays, integrated circuits (IC's) fabricated on CMOS technology are widely used for RF applications. Therefore, a precise characterization of these devices, both in the DC and high-frequency regimes, is fundamental for the successful design and simulation of circuits for these applications. The extraction of device parameters from DC (i.e. static measurements) has been an ongoing research topic for the last decades; many new techniques have been proposed and published in the specialized literature [1–9]. As it is well known, however, all these techniques give slightly different values for fundamental parameters such as threshold voltage, mobility degradation factor, and gain. Furthermore, in order to fully characterize the device, many of these techniques require arrays of transistors with different geometries [10], even when using small-signal data [11,12], which is inconvenient due to the variation of the MOSFET parameters for different dimensions.

On the other hand, it is important to remark that some previously reported methods may give accurate results, even for sub-100 nm devices [9,13]. Unfortunately, these methods are only suitable for single-fingered MOSFETs, which are rarely used for high-frequency applications. In fact, using a multi-fingered gate electrode is the common practice for these applications, and directly characterizing devices with this geometry is desirable to avoid discrepancies when employing separate test structures for performing parameter extractions based on additional measurements.

Thus, CMOS parameter extraction for simulating high-frequency device performance generally requires both DC and high-frequency characterization routines [14,15]. If these routines are not carefully designed, errors in one can affect the results of the other, and the simulation will not render satisfactory results once confronted with experimental data. In order to reduce these possible variations, in this article we propose an extraction technique based solely on S-parameter measurements. With this technique, important DC quantities such as threshold voltage, gain factor, and mobility degradation factor, can be obtained from measurements performed on individual devices in the high-frequency regime, hence representing a truer operation of the device, and avoiding the need of a separate DC characterization routine. Device effects, especially present in RF transistors, such as the finite substrate impedance, effects of multi-fingered structures, and the dependence of the device characteristics with geometry are taken into account by the method, which is based on the small-signal determination of the channel resistance.

As such, with this method the different parameters needed to carry out high-frequency response simulations can all be obtained from S-parameter measurements directly performed to the MOSFET to be modeled and characterized, independently on the layout used to interconnect the corresponding terminals. The values obtained with this method show a very good agreement with those derived from static routines.

2. Theory

As it is well known, the basic model to represent a MOSFET considers that the current flowing between the source and the

* Corresponding author. Tel.: +52 222 2663100; fax: +52 222 2470517.
 E-mail addresses: galvarez@inaoep.mx (G. Álvarez-Botero), reydezel@inaoep.mx (R. Torres-Torres), rmurphy@inaoep.mx (R. Murphy-Arteaga).

drain terminals is controlled by adjusting the voltage applied to the gate terminal. However, when developing a small-signal model for an actual MOSFET, it is necessary to consider several effects that yield undesirable and not-controllable currents through the substrate [16–19]. These parasitic effects are inherent to RF-CMOS technologies [20,21]. One can thus consider that the MOSFET presents two possible paths for the current flowing between the intrinsic drain and source regions: (i) the channel and (ii) the substrate. This is illustrated in Fig. 1.

In order to start with the analysis, the equivalent circuit model of a two-fingered common source/bulk nMOSFET including the substrate effects is presented in Fig. 2a. Notice that this figure shows the corresponding equivalent circuit elements distributed within the different sections of the device, whereas Fig. 2b shows the equivalent circuit of the device considering single lumped elements for every effect occurring in the structure. The reason for showing Fig. 2a and b is to illustrate that a multi-fingered device can be treated as an equivalent MOSFET whose elements are obtained considering the parallel connection of multiple MOSFETs. Thus, the equivalent circuit shown in Fig. 2b can be divided into two parts; the extrinsic parasitic elements (C_{JS}, C_{JD}, R_{BKS}, R_{BKD}, and R_G) and the intrinsic elements (C_{GS}, C_{GD}, C_{DS}, and R_{ch}).

In an ideal case, it is desirable that all the drain-to-source current flows within the channel region. If this is the case, the total current (I_{tot}) flowing between the drain and source/bulk terminals is approximately equal to I_{ds}. Under high-frequency operation, however, there exists an additional current flowing through the substrate (I_{bulk}) (not to be confused with the DC substrate current), which means that, in accordance to Fig. 2b, the following expression can be written

$$I_{tot} = I_{ds} + I_{bulk} \qquad (1)$$

Notice in Fig. 2b that the magnitude of I_{bulk} strongly depends on the operating frequency, since the impedance associated with the substrate includes capacitive effects (the capacitive reactance varies with frequency). In consequence, in (1), the contribution of I_{ds} and I_{bulk} to the total current flowing from the drain terminal to the source terminal is dependent on the frequency of the applied signals. For this reason, it is desirable to separately determine the impedances associated with the two branches in the circuit of Fig. 2b. This allows for the assessment of their corresponding contribution to the output impedance of a MOSFET as shown herein.

All the parameters of interest for this article can be obtained from two-port S-parameter measurements, using a typical two-port network representation for a common source/bulk MOSFET. In this case, the gate and drain terminals are associated with Port 1 and Port 2 respectively, whereas the source/bulk terminal is considered as the reference, as it is shown in Fig. 3.

In order to study the characteristics of the MOSFETs under investigation, S-parameter data is converted to Z-parameters, since Z_{22} can be used to analyze the device's output impedance. Y_{22} could also be used to analyze the output characteristics of a MOSFET as in [21]. However, for the calculation of the Y-parameters, short-circuit conditions are required. This means that, for instance, the determination of Y_{22} requires that Port-1 is brought to ground, which introduces a new branch in the analysis connecting R_G from the MOSFET's intrinsic gate to ground. In contrast, Z_{22} requires that Port-1 is left open and R_G is not involved in the analysis, which simplifies the interpretation of the resulting data.

The equivalent circuit for the calculation of Z_{22} at $V_{ds} = 0$ is presented in Fig. 4. Notice that in this circuit the source-to-bulk resistance (R_{BKS}) was neglected since the source region is implanted next to the bulk contact in the common source/bulk MOSFETs analyzed here, as illustrated in Fig. 2a. Furthermore, the source and bulk regions are connected using a metal layer. This considerably reduces the effect of R_{BKS}. Moreover, C_{JS} can also be neglected, since typically $R_S \ll 1/\omega C_{JS}$ for the frequency range in consideration. In order to simplify the analysis, a new parameter is defined. This is C_x, which represents the equivalent capacitance that includes the effect of C_{GD}, C_{GS} (including the corresponding parasitic components), and C_{DS}, and is expressed as $C_x = C_{DS} + C_{GS}C_{GD}/(C_{GS} + C_{GD})$.

Notice in Fig. 4 that at relatively low frequencies, the current flow through C_{JD} can be considered as negligible and the output impedance (in this case represented by Z_{22}) can be represented solely by means of $Z_{channel-path}$. However, as the frequency increases,
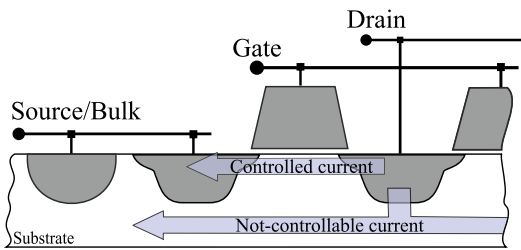

Fig. 1. Simplified cross section of a common source/bulk MOSFET showing the possible paths of the current flowing between drain and source.
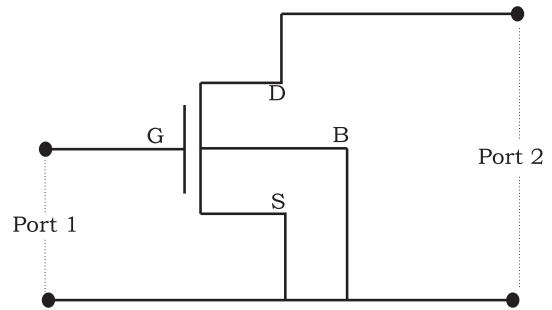

Fig. 3. Typical two-port measurement configuration for a common source/bulk RF-MOSFET.
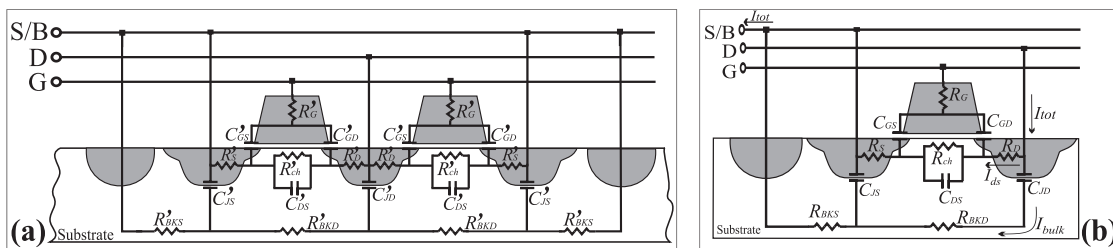

Fig. 2. (a) Cross-sectional view of a two-fingered common source/bulk MOSFET including the corresponding distributed circuit model. (b) Simplified model using lumped elements for representing the effective values of the device distributed effects.
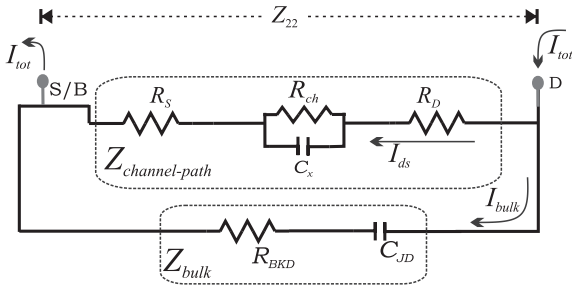
Fig. 4. Simplified equivalent circuit associated with the calculation of Z_{22} at $V_{ds} = 0$.

the reactance associated with C_{JD} decreases, which causes Z_{bulk} to become comparable to $Z_{channel-path}$, and the contribution of I_{bulk} to I_{tot} may be substantial. Clearly, this bulk effect is frequency dependent and is one of the aspects studied in this paper.

A second important aspect to be taken into account is that the impedance $Z_{channel-path}$ is bias dependent, whereas Z_{bulk} can be approximately considered as bias independent. Thus, at a given frequency, as V_{gs} increases $Z_{channel-path}$ is reduced since R_{ch} becomes smaller. In this case, the impact of the current flowing through the substrate path is reduced since $Z_{bulk} \gg Z_{channel-path}$, yielding $I_{bulk} \ll I_{ds}$. Furthermore, when $V_{gs} \gg V_t$ the impact of the substrate current in the small-signal characteristics of the MOSFET can even be negligible. This bias dependent impact of the substrate losses on the MOSFET's output characteristics is also quantitatively analyzed here.

3. Experiment

The devices under test (DUTs) were four common source/bulk nMOSFETs fabricated on a p-type Si substrate with finger width $W_f = 3$ μm, number of gate fingers $NF = 64$, and channel mask lengths $L_m = 80$ nm, 0.25 μm, 0.5 μm, and 1 μm. Fig. 5 shows a cross section view of the structure of these devices. Notice that the substrate contact is performed outside of the multi-fingered structure and is externally short-circuited with the source terminal through a metal interconnection. This connection is made so that the effect of the source-to-bulk device impedance is reduced and the high-frequency model can be simplified. In addition, the gate contact is performed at both sides of the gate electrodes to reduce the corresponding parasitic resistance.

In order to analyze the characteristics of the DUTs, on-wafer two-port S-parameter measurements were performed up to 40 GHz using a vector network analyzer (VNA) and ground-signal-ground (GSG) coplanar RF probes. The equipment was previously calibrated up to the probe tips, as shown in Fig. 6, using an LRM (line-reflect-match) procedure [22]. Afterwards, the measurements were performed at different bias conditions (according to the requirements of the methods described in subsequent sections) applying a power of −20 dBm at each port. Notice also in Fig. 6 that
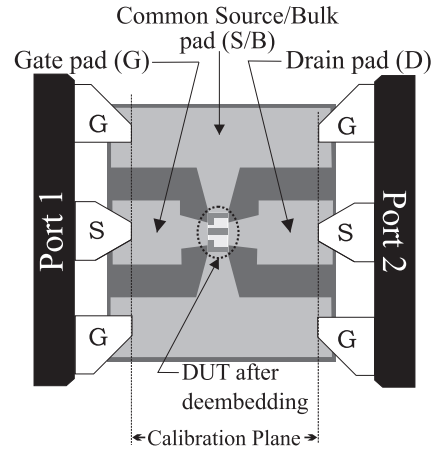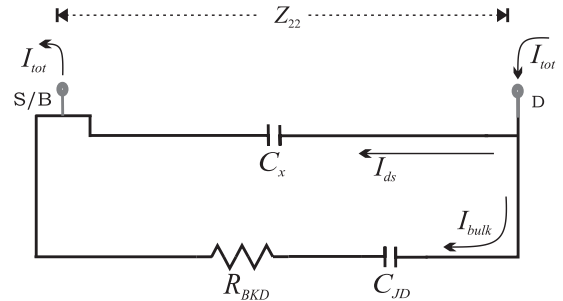

Fig. 6. Test structure pad configuration.

Fig. 7. Equivalent circuit for a MOSFET biased at $V_{gs} = V_{ds} = 0$.

every DUT is embedded between pads and other interconnects to allow for the corresponding probing. In order to minimize the undesired effects associated with these interconnects, the pads are isolated from the substrate by using ground shielding techniques [23]. This allows to reduce the uncertainty introduced by the de-embedding of the pad parasitic effects, which is performed by using short and open dummy structures and the procedure outlined in [24]. In what follows, the experimental data used to verify the validity of the procedures proposed in this paper are based on the S-parameter measurements described in this section.

4. Proposed Method and Results

4.1. Determination of the substrate impedance elements

The first step for the implementation of the model shown in Fig. 4 is obtaining the substrate elements. At $V_{gs} = V_{ds} = 0$ there is no inversion channel, yielding $R_{ch}\|1/j\omega C_x \approx 1/j\omega C_x$ since R_{ch} becomes very large and its effect can be neglected [25]. Moreover,
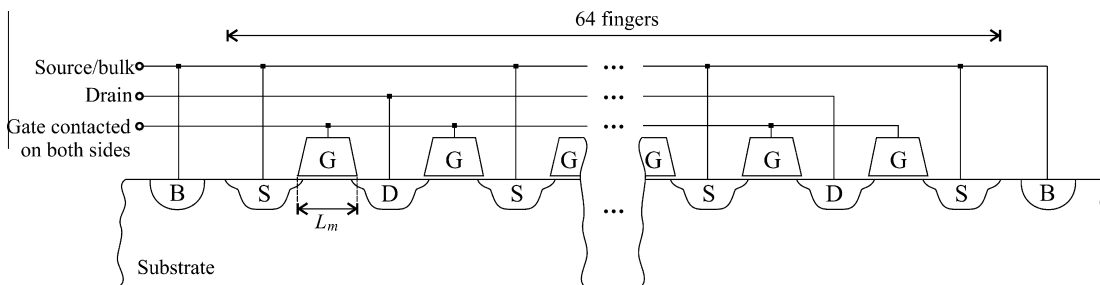

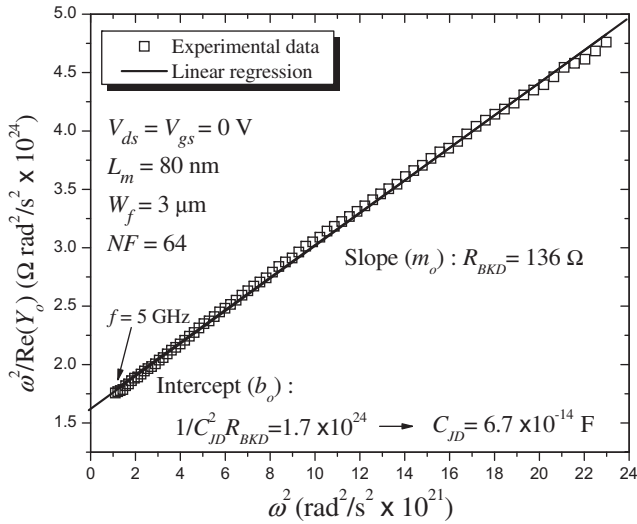Fig. 5. Simplified sketch showing the cross section view of the measured devices.

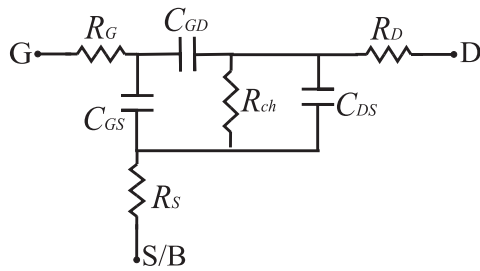**Fig. 8.** Linear regression used to determine R_{BKD} and C_{JD}.

Fig. 9. Equivalent circuit for a MOSFET biased at $V_{ds} = 0$ and $V_{gs} > V_t$ after removing the substrate effects.

under this condition, the series resistances R_S and R_D are much smaller than $1/(j \omega C_x)$, which allows to assume $R_S + 1/j\omega C_x + R_D \approx 1/j\omega C_x$. In this case, the simplified equivalent circuit shown in Fig. 7 can be used to represent a zero-biased MOSFET. In accordance with this circuit, the MOSFET's output admittance (Y_o) can be defined as the inverse of Z_{22}; thus, at $V_{gs} = V_{ds} = 0$, the following equation can be written [19]:

$$\frac{\omega^2}{\text{Re}(Y_o)} = \omega^2 R_{BKD} + \frac{1}{C_{JD}^2 R_{BKD}} \tag{2}$$

Consequently, R_{BKD} and C_{JD} can be determined after performing a linear regression of the experimental $\omega^2/\text{Re}(Y_o)$ versus ω^2 data. Hence, R_{BKD} and C_{JD} are respectively obtained from the slope and the intercept of this data regression as shown in Fig. 8. This regression is performed at a frequency sufficiently high so that the noisy experimental data associated with Y_o at low frequencies is avoided. The noisy data is obtained due to the fact that at $V_{ds} = V_{gs} = 0$ the admittance Y_o becomes very small since there is no channel formed, which is accentuated at relatively low frequencies. Nevertheless, notice the excellent linear trend observed in Fig. 8, beyond approximately 5 GHz. Thus, before determining these parameters, plotting $1/\text{Re}(Y_0)$ versus frequency is recommended to observe the range at which the noise in the corresponding experimental data is not at a level that hinders parameter extraction.

4.2. Determination of the elements in the channel path

After R_{BKD} and C_{JD} have been determined, the substrate effects can be removed from the experimental data by applying a simple matrix operation [19]. This data processing allows to obtain $\mathbf{Y}^*$,

which is the Y-parameter matrix under a given bias condition after removing the substrate effects.

Once that the substrate effects have been removed from the experimental data, and assuming $V_{gs} > V_t$, the equivalent circuit associated with the MOSFET is that shown in Fig. 9, where the device's output impedance under these conditions can be represented by means of the model illustrated in Fig. 10. Notice in Fig. 10 that Z_{22}^* is determined after converting $\mathbf{Y}^*$ to the corresponding Z-parameter matrix ($\mathbf{Z}^*$).

From Fig. 10, the following expression can be obtained:

$$-\frac{\omega^2}{\text{Im}(Z_{22}^*)} = \omega^2 C_x + \frac{1}{R_{ch}^2 C_x} \tag{3}$$

Thus, after performing a linear regression of the experimental $-\omega^2/\text{Im}(Z_{22}^*)$ versus ω^2 data, C_x and R_{ch} can be respectively obtained from the corresponding slope and the intercept with the abscises as shown in Fig. 11. Similarly to the regression illustrated in Fig. 8, the frequency range used to obtain C_x and R_{ch} can be determined by observing the range at which the experimental $-1/\text{Im}(Z_{22}^*)$ versus frequency data presents relatively low noise.

In order to obtain the series resistances in the model of Fig. 10, the real part of the Z_{12} and Z_{22} parameters associated with the circuit shown in Fig. 9 are expressed as:

$$\text{Re}(Z_{12}) = \text{Re}(Z_{21}) = R_S + \frac{A}{2} \tag{4}$$

$$\text{Re}(Z_{22}) = R_D + R_S + A \tag{5}$$

where $A = R_{ch}/(1 + \omega^2 C_x^2 R_{ch}^2)$.

Thus, once that R_{ch} and C_x have been determined R_S and R_D can be calculated by respectively solving (4) and (5), which yield [26]:
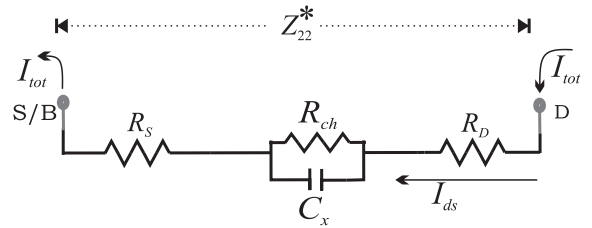

Fig. 10. Simplification of the circuit shown in Fig. 9 to represent the output impedance, $C_x = C_{DS} + C_{GS}C_{GD}/(C_{GS} + C_{GD})$.
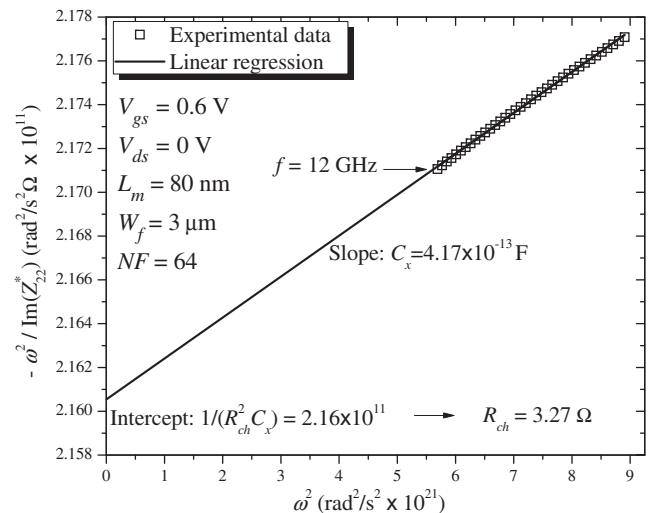

Fig. 11. Linear regression used to determine R_{ch} and C_x at $V_{gs} = 0.6$ V.

$$R_S = \text{Re}(Z_{12}^*) - \frac{1}{2} \cdot \frac{R_{ch}}{1 + (\omega C_x R_{ch})^2} \qquad (6)$$

$$R_D = \text{Re}(Z_{22}^*) - R_S - \frac{R_{ch}}{1 + (\omega C_x R_{ch})^2} \qquad (7)$$

Using this procedure, R_D, R_{ch}, R_S, and C_x were determined at a given V_{gs}. However, in order to study the variation of the impact of these parameters on the MOSFET's output characteristics at different bias conditions, several gate-to-source voltages are considered in the analysis: $V_{gs} = 0.5$ V to $V_{gs} = 0.7$ V in steps of 20 mV. Hence, from the obtained bias dependent R_{ch}, a physically-based parameter extraction of MOSFET parameters can be proposed as explained below.

4.3. Physically-based extraction of MOSFET parameters

The intrinsic small-signal conductance between source and drain (g_{ch}) at $V_{ds} = 0$ can be expressed as [11]

$$g_{ch} = \frac{1}{R_{ch}} = \frac{\mu_{eff} C_{ox} W_{eff}}{L_{eff}} (V_{gs} - V_t) \qquad (8)$$

where C_{ox} is the gate oxide capacitance per unit area, μ_{eff} is the effective inversion layer mobility, and W_{eff} and L_{eff} are the effective channel width and length, respectively. Then, considering that

$$\beta = \frac{\mu_{eff} C_{ox} W_{eff}}{L_{eff}} \qquad (9)$$

it is possible to express (8) as

$$g_{ch} = \beta V_{gs} - \beta V_t \qquad (10)$$

In order to obtain V_t from experimental data using (10) the well known concept that states that small variations on V_{gs} introduce small variations in β can be applied [27]. Thus, β can be obtained from the slope of the linear regression of the g_{ch} versus V_{gs} data, allowing for the determination of V_t from the corresponding intercept with the abscisses. In Fig. 12, the extraction of V_t at $V_{gs} = 0.6$ V is shown for an 80 nm MOSFET. Notice that three points were considered to carry out the linear regression: $V_{gs} = 0.6$ V, which is the central point, and $V_{gs} = 0.6\text{V} \pm \Delta V_{gs}$ with $\Delta V_{gs} = 20$ mV. In this case, the small-signal S-parameters measured on a single MOSFET can be used to obtain V_t in a simple and direct way without having to know the precise effective dimensions of the transistor or the oxide capacitance, as it is done, for instance, in [11].
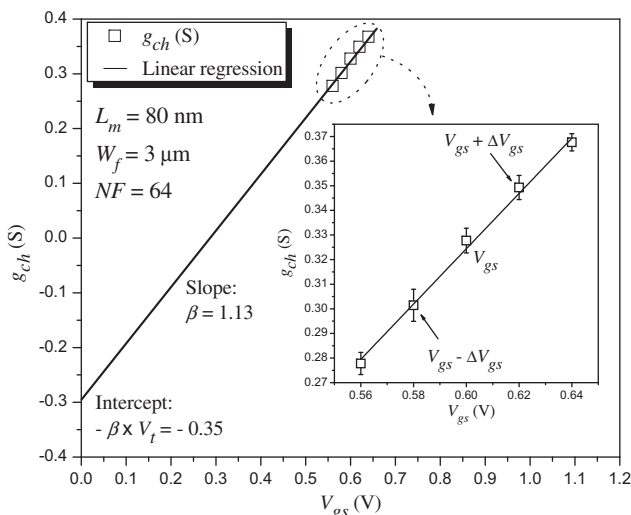
Fig. 13 shows the extracted V_t for the MOSFET with $L_m = 80$ nm as a function of V_{gs}. As expected, there is no significant variation in the extracted V_t since V_{ds} is kept constant at zero volts over all the range of V_{gs}, thus guaranteeing that the inversion layer is uniform along the channel. Moreover, the frequency independence of the extracted data observed in Fig. 13 is an indicative of the correctness of the applied procedure.

Fig. 14 shows the extracted V_t using the proposed method and the DC measurement-based method in [7] for MOSFETS with channel mask lengths of 80 nm, 0.25 μm, 0.5 μm, and 1 μm. The method reported in [7] uses an extrapolation that involves the square root of the transconductance at a low V_{ds}, eliminating the effect of the gate-bias-dependent mobility on the extrapolated V_t, which is crucial to obtain realistic results when characterizing short channel length devices. Moreover, the model assumed in [7] for the mobility degradation with V_{gs} is the same one used later in this paper when modeling the corresponding impact on R_{ch}. Notice in Fig. 14 that excellent agreement between the RF and DC determined V_t is obtained even for the shortest characterized device.

Once the threshold voltage has been determined, the mobility reduction factor due to the vertical electric field in the channel
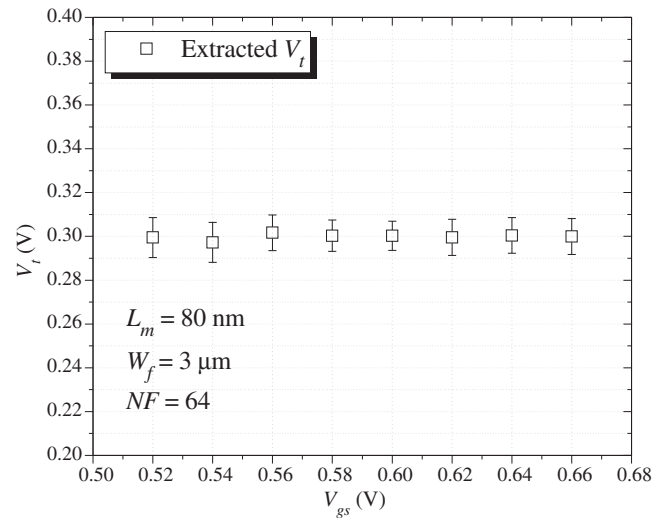
Fig. 13. Extracted V_t for a 80 nm channel length MOSFET.

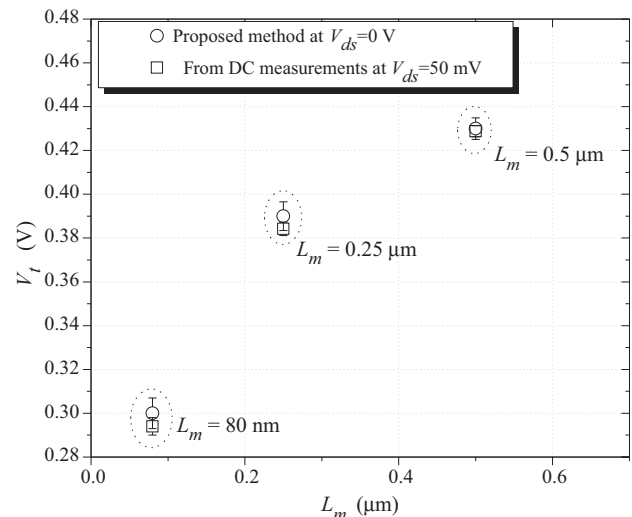**Fig. 12.** Linear regression used to determine V_t.

Fig. 14. Comparison between the threshold voltage extracted using the proposed method and the static method in [7].

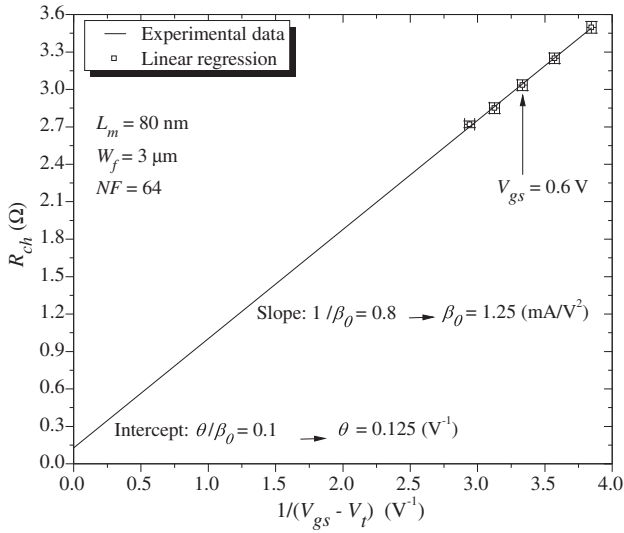Fig. 15. Linear regression used to determine θ and β_0.

(θ) and the gain factor (β_0) can be obtained. In order to do this, (8) is rewritten as

$$R_{ch} = \frac{L_{eff}}{\mu_{eff} C_{ox} W_{eff}(V_{gs} - V_t)} \quad (11)$$

The effective inversion layer mobility (μ_{eff}) can be modeled to first order by [11]:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta(V_{gs} - V_t)} \quad (12)$$

where μ_0 is the low-gate-field mobility. Thus, when substituting (12) into (11), the channel resistance can be expressed as

$$R_{ch} = \frac{1}{\beta_0(V_{gs} - V_t)} + \frac{\theta}{\beta_0} \quad (13)$$

with β_0 given by

$$\beta_0 = \frac{\mu_0 C_{ox} W_{eff}}{L_{eff}} \quad (14)$$

From (13) and again considering that small variations in V_{gs} yield negligible variations on the effective length and width of the device [27], it is possible to obtain θ and β_0 by means of a linear regression within a suitable gate voltage range, as illustrated in Fig. 15.

4.4. Experimental verification

In order to verify the validity of the proposed extraction method, once that all the model parameters associated with the circuit of Fig. 4 were determined, equivalent circuit simulations were carried out to reproduce the MOSFET output admittance (Y_o) at several gate-to-source voltages. When performing these simulations, Eq. (13) was used to represent the channel resistance. Notice in Fig. 16 the excellent simulation-experiment correlation up to 40 GHz when considering the substrate losses. In contrast, the model that neglects the substrate effects yields a considerable deviation from the experimental data beyond a frequency that is gate-bias-dependent, as explained below.

An interesting point to remark when observing the results in Fig. 16 is the following. Even though the model that neglects the substrate impedance accurately reproduces the experimental Y_o up to 10–20 GHz (depending on V_{gs}), the model is not physically-based since some effects may be either underestimated or
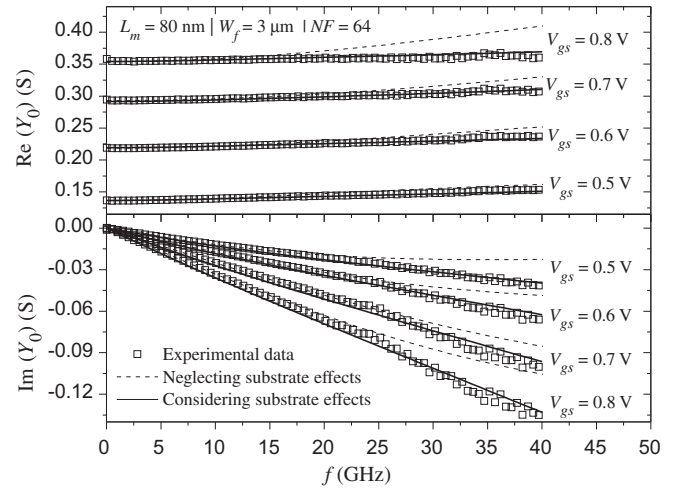
overestimated. This may result in misinterpretation of the results and an incorrect extraction of MOSFET parameters.

5. Impact of the Parasitic Substrate Impedance

In order to quantify the influence of the substrate elements in the total output characteristics, we define a new parameter X_{bk} as,

$$X_{bk} = \frac{|Y_{bulk}|}{|Y_{bulk}| + |Y_{channel-path}|} \times 100 \quad (15)$$

where Y_{bulk} and $Y_{channel-path}$ are admittances obtained from Z_{bulk} and $Z_{channel-path}$ respectively, once that the parameters in the model of Fig. 4 have been experimentally determined using the abovementioned procedures.

As can be observed in Eq. (15), X_{bk} represents the contribution in percentage of the substrate admittance to the MOSFET's total admittance. This means that the current flowing through the substrate is proportional to X_{bk}. Thus, from Eq. (15), a quantification of the parasitic-substrate losses as a function of frequency can be obtained, as shown in Fig. 17. Notice that the substrate current can contribute as much as 60% of the total output current when

Fig. 16. Comparison between simulated and experimental output admittances showing the impact of neglecting the substrate losses.
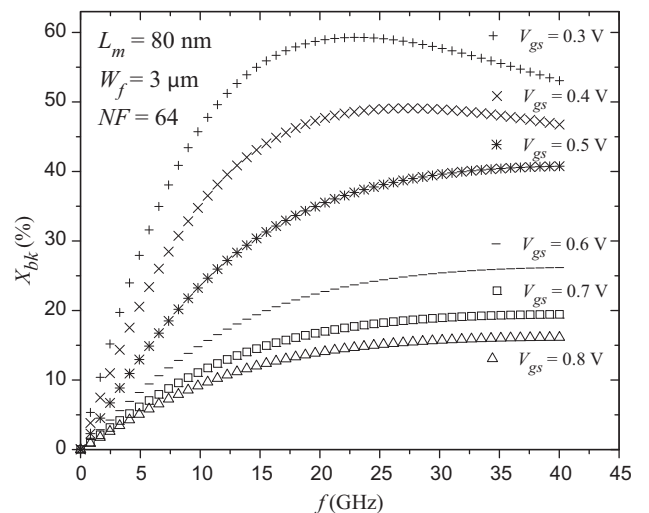

Fig. 17. Contribution of the substrate admittance to the total MOSFET admittance for different gate-to-source bias conditions.
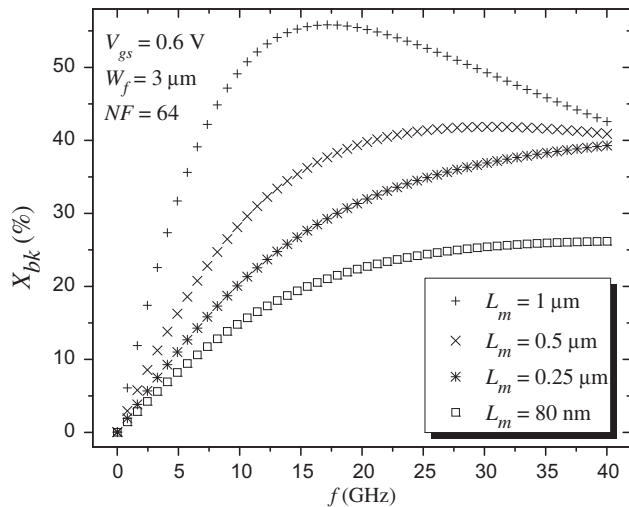
Fig. 18. Contribution of the substrate admittance to the total MOSFET admittance for different gate-mask lengths.

operating the device close to the threshold voltage. In low-power applications, transistors are operated in the moderate-inversion region. Hence, if this effect is not taken into account, simulations will be overly optimistic. On the other hand, as the bias voltage is increased, the substrate AC current is reduced; this behavior is attributed to the reduction of the channel resistance as the bias voltage is increased, thus the current flowing through Z_{bulk} decreases according to expectations. It is important to notice, however, that even at high gate biases, this current can represent as much as 15% of the total current flowing through the device.

For completeness of the present analysis, the parasitic-substrate losses as a function of the frequency for devices with different channel lengths, at a given V_{gs}, are shown. In reference to Fig. 18, the substrate losses are more considerable as the channel length is increased; this corroborates the fact that the influence of the substrate parasitic effects on the output characteristics are reduced when the channel resistance decreases, in this case due to the channel length variation.

As a final remark, notice in Figs. 17 and 18 that even at relatively low frequencies (e.g. below 10 GHz) the contribution of the substrate losses may be significant and cannot be neglected when carrying out a physically-based modeling. Moreover, as can be seen in these figures, the curves are not monotonic but present a maximum within the studied range. This is due to the fact that, above a given frequency, $Z_{channel-path}$ decreases at a higher rate that Z_{bulk}. Analytical formulas that model this frequency behavior have been developed, but are too cumbersome to include in this article. It is, however, worthy to note that the position of the maximum of the X_{bk} versus frequency curve is a complicated function of all the model elements.

6. Conclusions

A methodology, based solely on S-parameters measurements, for the extraction and characterization of the basic parameters for a bulk MOSFET has been presented. One of the main advantages of this methodology is that measurements performed on each device reflect the true values for that particular device, avoiding the dependence on the variation of the electrical characteristics with device geometry. The effects of the AC substrate current were also quantified, based on the intrinsic and extrinsic components of the transistor. This parasitic current can constitute a large part of the total current flowing through the device, and it has to be consid-

ered when simulating CMOS circuits for RF applications, since it can represent as much as 60% of the total. If this is not taken into consideration, simulations will be overly optimistic due to the assumption that the total drain current is controlled by V_{gs}, using then an unrealistically high transconductance. Furthermore, the obtained model includes a physically-based representation of the channel resistance, which allows for an accurate representation of the MOSFET at high frequencies. An excellent simulation-experiment correlation was obtained up to 40 GHz.

References

[1] Liou J, Ortiz-Conde A, Garcia-Sanchez F. Analysis and design of MOSFETs. Kluwer Academic Publishers.; 1998.
[2] Zhou X, Lim K, Qian W. Threshold voltage definition and extraction for deep-submicron MOSFETs. Solid-State Electron 2001;45:507–10.
[3] Terada K, Nishiyama K, Hatanaka K-I. Comparison of MOSFET-threshold-voltage extraction methods. Solid-State Electron 2001;45:35–40.
[4] Hamer M. First-order parameter extraction on enhancement silicon MOS transistors. IEE Proc Solid-State Electron Dev 1986;133(3):49–54.
[5] D. Fleury, A. Cros, H. Brut, G. Ghibaudo, New Y-function-based methodology for accurate extraction of electrical parameters on nano-scaled MOSFETs. In: IEEE proccedings of international conference on microelectronic test structures, Edinburgh: IEEE; 2008. p. 160–5.
[6] Romanjek K, Andrieu F, Ernst T, Ghibaudo G. Improved Split C–V method for effective mobility extraction in sub-0.1-um Si MOSFETs. IEEE Electron Dev Lett 2004;25(8):583–5.
[7] Ghibaudo G. New method for the extraction of MOSFET parameters. Electron Lett 1988;2(9):543–5.
[8] Ortiz-Conde A, García-Sanchez F, Liou J, Cerdeira A, Estrada M, Yue Y. A review of recent MOSFET threshold voltage extraction methods. Microelectron Reliab 2002;42:583–96.
[9] Chaisantikulwat W, Mouis M, Ghibaudo G, Gallon C, Fenouilletberanger C, Maude D, et al. Differential magnetoresistance technique for mobility extraction in ultra-short channel FDSOI transistors. Solid-State Electron 2006;50(4):637–43.
[10] van Meer H, Henson K, Lyu J-H, Rosmeulen M, Kubicek S, Collaert N, et al. Limitations of shift-and-ratio based L_{eff} extraction techniques for MOS transistors with halo or pocket implants. IEEE Electron Dev Lett 2000;21(3):133–6.
[11] Kong FCJ, Yeow YT, Yao ZQ. Extraction of MOSFET threshold voltage, series resistance, effective channel lenght and inversion layer mobility from small-signal channel conductance measurement. IEEE Trans Electron Dev 2001;48(12):2870–4.
[12] Lee S, Yu HK. A new technique to extract channel mobility in submicron MOSFETs using inversion charge slope obtained from measured S-parameters. IEEE Trans Electron Dev 2001;48(4):784–8.
[13] Sites J, Wieder H. Magnetoresistance mobility profiling of MESFET channels. IEEE Trans Electron Dev 1980;27(12):2277–81.
[14] Torres-Torres R, Murphy-Arteaga R, Decoutere S. MOSFET bias dependent series resistance extraction from RF measurements. Electron Lett 2003;39(20):1476–8.
[15] Siu S-L, Wong H, Tam W-S, Kakusima K, Iwai H. Subthreshold parameters of radio-frequency multi-finger nanometer MOS transistors. Microelectron Reliab 2009;49(4):387–91.
[16] Jen SH-M, Enz CC, Pehlke DR, Schroter M, Sheu BJ. Accurate modeling and parameter extraction for MOS transistors valid up to 10 GHz. IEEE Trans Electron Dev 1999;46(11):2217–27.
[17] Cheng Y, Matloubian M. On the high-frequency characteristics of substrate resistance in RF MOSFETs. IEEE Electron Dev Lett 2000;21(12):604–6.
[18] Chang RT, Yang M-T, Ho PPC, Wang Y-J, Chia Y-T, Liew B-K. Modeling and optimization of substrate resistance for RF-CMOS. IEEE Trans Electron Dev 2004;51(3):421–6.
[19] Torres-Torres R, Murphy-Arteaga R. Straightforward determination of small-signal model parameters for bulk RF-MOSFETs. In: Proceedings of the fifth IEEE international caracas conference on devices, circuits and systems, 2004. p. 14–8.
[20] Cheng Y, Deen MJ, Chen C-H. MOSFET modeling for RF circuit design. IEEE Trans Electron Dev 2005;52(7):1286–303.
[21] Mahalingam U, Rustagi SC, Samudra GS. Direct extraction of substrate network parameters for RF MOSFET modeling using a simple test structure. IEEE Electron Dev Lett 2006;27(2):130–2.

[22] Reynoso-Hernandez J. On-wafer LRM calibration technique using a non-reflecting lossy line of arbitrary length. In: 63rd ARFTG conference digest, IEEE, 2004. p. 205-10.

[23] Torres-Rios E, Torres-Torres R, Murphy-Arteaga R. Analytical characterization and modeling of shielded test structures for RF-CMOS. Int J High Speed Electron Syst 2008;18(4):793–803.

[24] Torres-Torres R, Murphy-Arteaga R, Reynoso-Hernandez JA. Analytical model and parameter extraction to account for the pad parasitics in RF-CMOS. IEEE Trans Electron Dev 2005;52(7):1335–42.

[25] Kwon I, Je M, Lee K, Shin H. A simple and analytical parameter-extraction method of a microwave MOSFET. IEEE Trans Microw Theory Tech 2002;50(6):1503–9.

[26] Torres-Rios E, Torres-Torres R, Valdovinos-Fierro G, Gutiérrez-D EA. A method to determine the gate bias-dependent and gate bias-independent components of MOSFET series resistance from S-parameters. IEEE Trans Electron Dev 2006;53(3):571–3.

[27] Hu GJ, Chia CCY-T. Gate-voltage-dependent effective channel length and series resistance of LDD MOSFET's. IEEE Trans Electron Dev 1987;34(12):2469–75.