# Systematic Modeling and Characterization of a Via-to-SIW Transition

Miguel A. Tlaxcalteco-Matus and Reydezel Torres-Torres, Member, IEEE

Abstract—A model and parameter extraction method for a via-to-SIW transition is presented. The model is derived from an analysis of experimental data and full-wave simulations, allowing to obtain the equivalent circuit parameters for the via including its interaction with the SIW. It is demonstrated through a careful model-experiment correlation that the application of this method allows the correct representation of the via-to-SIW transitions implemented on printed circuit board technology even when changing the structure of the SIW environment.

*Index Terms*—Interconnection, printed circuit board (PCB), substrate integrated waveguide (SIW), transition, via.

#### I. INTRODUCTION

UBSTRATE integrated waveguides (SIWs) are good candidates for implementing interconnects in high-speed systems [1]. Thus, several approaches have been reported to study these structures on printed circuit boards (PCBs). Whereas characterizing homogeneous SIWs is carried out in a simple way using TRL-like methods [2], modeling the transitional structures is a challenge due to the presence of evanescent fields in the surrounds of the region where a waveguide is excited [3], [4]. For the case of a via-to-SIW (v-SIW) transition, which is one of the preferred interfaces for an SIW due to its simplicity [1], some modeling approaches have been proposed. However, these approaches either require a priori knowledge of the material properties and effective dimensions of the structures or fully rely on the correlation of electromagnetic models with experimental data [3]. An alternative approach, the  $Z_{\rm pp}$  formulation, uses an infinite summation to represent the impedance of the via embedded within the waveguide [5]. Unfortunately, this impedance also requires previous knowledge of the material properties and effective dimensions of the structure, which can even be frequency dependent in an SIW environment.

In order to obtain the physically-based parameters that represent the behavior of an SIW fed by means of vias, an approach for systematically extracting the equivalent circuit parameters of a v-SIW transition is presented in this letter. The proposal allows to obtain the parasitics associated to the via, and the impedance related to the excitation of the SIW once that the cutoff frequency ( $f_c$ ) of the fundamental propagation mode is reached. Excellent agreement between the equivalent circuit

The authors are with the Department of Electronics, Instituto Nacional de Astrofísica, Óptica y Electrónica (INAOE), Tonantzintla, Puebla 72840, Mexico (e-mail: mtlaxcalteco@inaoep.mx).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LMWC.2010.2073694

Perimeter ground vias Off-line ground vias (only in some test structures) v-SIW transition  $V_{L_{g}=1}$  $L_{t}$  $L_{g}$  $L_{$ 

Fig. 1. Top view of the SIWs fabricated for illustrating the formulation and verification of the proposal (the dimensions are given in millimeters).

model and S-parameter measurements is observed within the useful bandwidth of the SIW, even when modifying the structure of the waveguide.

# II. DESCRIPTION OF THE INVESTIGATED STRUCTURES

SIWs with different lengths  $(L_{\rm max})$  were fabricated on a PCB made of Rogers RT/Duroid 5880 material with a thickness of 0.79 mm. The nominal relative permittivity and loss tangent for this material at 50 GHz are  $\varepsilon_r = 2.2$  and  $\tan \delta = 0.0017$  respectively. The layout of the fabricated structures is shown in Fig. 1. Notice that two types of structures were fabricated: a) regular SIWs formed using perimeter ground vias (GVs), and b) SIWs including two additional rows of vias referred to as off-line GVs [6]. The latter structures behave as narrow-band filters and are only used here for verifying the validity of the proposal. The SIWs present a via as a launch structure and are terminated with ground-signal-ground (GSG) configured pads so that coplanar RF-probes with a pitch of 150  $\mu$ m can be used for measuring *S*-parameters.

To prevent signal degradation, it is desired that the power of a signal traveling along an SIW is transmitted in a single (i.e., the dominant  $TE_{10}$ ) mode. Thus, the v-SIW transitions shown in Fig. 1 were designed to excite this mode. For that matter, the v-SIW transitions were symmetrically placed in such a way that even modes, such as  $TE_{20}$ , cannot be excited. This allows to extend the usable transmission bandwidth from the cutoff frequency of the  $TE_{10}$  (i.e.,  $f_c$ ) to the cutoff frequency of the  $TE_{30}$ , which is the next higher order odd mode.

As the starting point, a 3D-model was implemented for the regular SIWs in the CST Microwave Studio full-wave simulator. This model was calibrated with experimental data so that the equivalent circuit parameters of the implemented transitions can be obtained as shown hereafter.

## **III. PARAMETER DETERMINATION METHOD**

Fig. 2 shows the equivalent circuit of the v-SIW transition. In addition to the inductive and capacitive elements in the typical  $\pi$ -model of a via, the parameter  $Z_{eq}$  considers the inter-

Manuscript received July 27, 2010; accepted August 25, 2010. Date of current version December 03, 2010. This work was supported in part by Intel Co. and CONACyT-Mexico under Grants 227913 and 118818.



Fig. 2. Equivalent circuit model for a v-SIW transition.

action of the via with the SIW environment. In practice, when the signal frequency f is below  $f_c Z_{eq}$  only includes the effect of the evanescent fields present at the transition. In this case,  $Z_{eq}$  is purely imaginary and can be represented by means of a lumped inductance. For simplicity, this effect is included in the inductance of the via  $(L_{via})$ . Thus, by defining a dummy port at the bottom of the v-SIW transition in the 3D-model, the via-to-ground capacitances  $C_1$  and  $C_2$ , and  $L_{via}$  can be obtained from the simulated Y-parameters associated with the circuit shown in Fig. 2. In this case, the values for  $C_1, C_2$ , and  $L_{via}$ shown in Fig. 2 were obtained from a fit of the  $Im(Y_{11}-Y_{12})/\omega$ ,  $IM(Y_{22} - Y_{12})/\omega$ , and  $1/\omega Im(Y_{12})$  versus  $\omega$  curves respectively for  $f < f_c$ , where  $\omega = 2\pi f$ .

Now consider the SIW shown in Fig. 3(a), where the v-SIW transition is located at the middle along the length of this structure. The full-wave simulation of this structure was carried out for  $f > f_c$  to obtain the Y-parameters between the port-1 and the dummy port located at the bottom of the v-SIW transition. Fig. 3(b) shows the corresponding equivalent circuit, including the parasitics of the via, a transformer that accounts for the impedance change at the transition, and the impedance  $Z_t$  related to the evanescent fields occurring at the v-SIW transition (i.e., within the distance  $L_t$ ). Notice that  $Z_t$  is not dependent on the structure that surrounds the transition provided that the boundaries are found at a distance bigger than  $L_t$  (L in Fig. 3(a) is arbitrarily selected considering this). In addition, two uniform SIW sections associated with both propagation directions are considered by using the propagation constant ( $\gamma$ ) and the wave impedance of the  $TE_{10}$  mode  $(Z_0)$  [2]. Thus, when these uniform sections are terminated with perfect matched boundaries (PMBs),  $Z_{x1} = Z_{x2} = Z_0$ . This allows to reduce  $Z_{in}$  to  $Z_0/2$ in the equivalent circuit model. For reference,  $Z_0 \approx 80 \ \Omega$  at f = 50 GHz. The resulting equivalent circuit under these assumptions is shown in Fig. 4(a). As can be seen in this simplified model, the transformer is not present since the ratio n equals 1 when the v-SIW transition is located at the middle along the width of the SIW [7], which is the case of the fabricated structures. Thus, since Lvia is already known, after obtaining the simulated Y-parameters for the implemented 3D model for  $f > f_c$ ,  $Z_{\rm eq}$  can be determined as

$$Z_{\rm eq} = -\frac{1}{Y_{21}} - j\omega L_{\rm via}.$$
 (1)

Notice in Fig. 4(a) that  $Z_t = Z_{eq} - Z_0/2$  can be now obtained. Moreover,  $Z_t$  can be represented by means of an equivalent circuit that involves negative elements [7], which are shown in Fig. 4(b). To obtain the negative  $L_z$  and  $C_z$  elements, the regression shown in Fig. 5(a) is performed. As can be seen in Fig. 5(b), when using these parameters in the equivalent circuit for  $Z_t$ , accurate modeling of  $Z_{eq}$  is achieved up to 85 GHz.



Fig. 3. (a) Sketch showing the 3D model of a v-SIW transition embedded between two perfectly-matched waveguide terminations and (b) the corresponding equivalent circuit for  $f > f_c$ .



Fig. 4. (a) Simplified model for the v-SIW transition assuming PMBs in the radiation directions. (b) Model for  $Z_t$ .



Fig. 5. (a) Determination of the model parameters for  $Z_t$ . (b) Comparison between the equivalent circuit model and full-wave simulations for  $Z_{eq}$ .

To verify that the extracted parameters allow to represent the v-SIW transition within different environments, the model of Fig. 3(b) is implemented but now considering electric-wall (i.e., short-circuit) terminations instead of PMBs. In this case,  $Z_{x1} = Z_{x2} = 0$ , and  $Z_{in}$  now represents the input impedance of two identical short-circuit terminated transmission lines in parallel; mathematically

$$Z_{\rm in} = \frac{Z_0}{2} \tanh(\gamma(L - L_t)) \tag{2}$$

where L is shown in Fig. 3(a), and  $L_t$  is left as a fitting parameter that decreases from 1 mm to 0.2 mm for f varying from 27 to 85 GHz. Hence, the impedance of the v-SIW transition assuming electric-wall terminations is given by

$$Z_{\rm eq} = Z_t + Z_{\rm in} \tag{3}$$

where  $Z_t$  has been previously determined. Fig. 6 shows the  $Z_{eq}$  versus f curves obtained using (3) and full-wave simulations. Since in this case  $Z_{eq}$  corresponds to the input impedance of a via surrounded by rectangular-shaped electric walls, this parameter can also be determined using the  $Z_{pp}$  formulation [5], which is also shown in Fig. 6. As can be seen, there is a good agreement between the extraction using the proposed method and full-wave simulations for the entire useful bandwidth. This means that the proposed method can be used to implement



Fig. 6. Equivalent impedance for the transition obtained from full-wave simulations, using the proposed method, and the  $Z_{\rm pp}$  formulation.



Fig. 7. Equivalent circuit for an SIW fed by means of a v-SIW transition.



Fig. 8. Comparison between the measured and simulated return and insertion losses for the fabricated SIW structures: (a) without off-line GVs ( $L_{\text{max}} = 10.9 \text{ mm}$ ), and (b) with off-line GVs ( $L_{\text{max}} = 94 \text{ mm}$ ).

models for signal vias embedded within rectangular waveguide-like structures. For the case of the  $Z_{\rm pp}$  formulation, also good model-experiment correlation is achieved but requiring previous knowledge of the effective dimensions and material parameters of the structure. Bear in mind, however, that in the studied structures this formulation failed to reproduce  $Z_{\rm eq}$ above approximately 54 GHz (see Fig. 6). This is due to the fact that  $Z_{\rm pp}$  considers all the modes supported by the structure even though some modes are intentionally omitted, as the  $TE_{20}$  in the SIWs studied here.

## IV. EXPERIMENTAL VERIFICATION AND DISCUSSION

Fig. 7 shows the model implementation for the structures depicted in Fig. 1. This model includes the equivalent circuits for the v-SIW transitions at each port of the structure. In addition, the homogeneous section of SIW is represented by means of  $L_{\text{SIW}} = L_{\text{max}} - L_t$ ,  $\gamma$ , and  $Z_0$  for the regular SIWs [2], and using the ABCD-matrix formulation given in [8] for the SIWs including off-line GVs. The small electric wall-terminated sections of SIW located at the outer sides of the structure are represented by means of the impedance  $Z_W = Z_0 \tanh(\gamma(L_s - L_t))$ . Fig. 8 shows the comparison between the measured S-parameters and the simulations using the proposed equivalent circuit for the fabricated SIWs. As can be seen, excellent simulation-experiment correlation is achieved from the cutoff frequency of the  $TE_{10}$  mode to that corresponding to the  $TE_{30}$  mode, which is the useful bandwidth of these SIWs. In spite of previous approaches [1], [3], [4], excellent correlation was obtained for  $|S_{11}|$  in a relatively wide frequency range. This is not only due to the use of probes instead of coaxial test fixtures for minimizing the insertion losses, but also due to the reliable extraction of the f-dependent  $Z_t$  for modeling the v-SIW transition. Moreover, even though the SIW that includes off-line GVs was not used during the parameter determination process, the proposed equivalent circuit accurately reproduces the corresponding data as shown in Fig. 8(b).

#### V. CONCLUSION

A methodology for modeling v-SIW transitions using only capacitive and inductive elements has been presented and demonstrated. In addition to the via parasitics, the model for the equivalent impedance of the transition was obtained and validated using full-wave simulations. Excellent agreement between simulated and experimental data was achieved for both transmission and reflection parameters within the entire useful bandwidth of SIWs with different structures.

#### REFERENCES

- J. Simpson, A. Taflove, J. Mix, and H. Heck, "Substrate integrated waveguides optimized for ultrahigh-speed digital interconnects," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 5, pp. 1983–1990, May 2006.
- [2] R. Torres-Torres, G. Romo, B. Horine, A. Sachez, and H. Heck, "Full characterization of substrate integrated waveguides from S-parameter measurements," in *Proc. IEEE EPEPS Conf.*, 2006, pp. 277–280.
- [3] A. Suntives and R. Abhari, "Transition structures for 3-D integration of substrate integrated waveguide interconnects," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 10, pp. 697–699, Oct. 2007.
- [4] C. Yau, T. Huang, T. Shen, H. Chien, and R. Wu, "Design of 30 GHz transition between microstrip line and substrate integrated waveguide," in *Proc. APMC*, Dec. 2007, pp. 1–4.
- [5] W. Chen *et al.*, "An efficient approach for power delivery network design with closed-form expressions for parasitic interconnect inductances," *IEEE Trans. Adv. Packag.*, vol. 29, no. 2, pp. 320–334, May 2006.
- [6] G. Romo and A. Ciccomancini, "Substrate integrated waveguide (SIW) filter: Design methodology and performance study," in *Proc. IEEE MTT-S IMW Symp.*, Feb. 2009, pp. 23–23.
- [7] L. Lewin, "A contribution to the theory of probes in waveguides," in *IEE Monograph*, Oct. 1957, pp. 109–116.
- [8] J. D. Schwartz *et al.*, "Design and analysis of 1-D uniform and chirped electromagnetic bandgap structures in substrate-integrated waveguides," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 7, pp. 1858–1866, Jul. 2010.