Characterization and modeling of passive components and interconnects using microwave techniques

By

Svetlana Carsof Sejas García

A thesis
Submitted to the Program in Electronics Science,
Electronic Department,
in partial fulfillment of the requirements for the degree
of
Doctor in Electronics

from the
National Institute for Astrophysics, Optics and Electronics
June 2014
Tonantzintla, Puebla

Advisor
Reydezel Torres Torres, Ph.D.

Abstract

This thesis is dedicated to characterizing, modeling, and analyzing passive components and interconnects to help solving signal integrity problems occurring in advanced microwave circuits and systems. This type of systems require ultra-wide bandwidth, low dispersion, and low attenuation in the signal transmission to allow high-speed data processing and transmission. In an actual system, however, the transmission of signals from source to destiny suffers attenuation, dispersion and distortion, in addition to high-order effects like resonances, crosstalk, reflection, mismatch, etc., which reduce the bandwidth and the quality of the signals. In this regard, much of the signal power is lost in interconnects, passive devices, and the corresponding interaction with the propagation media as well as with other devices. For this reason, it is very important to understand and properly modeling this type of components in an electronic circuit.

The passive elements characterized in this thesis are found at different integration levels. Moreover, different functions are performed by these devices depending on the level at which they are fabricated: interconnection between elements, implementation of matching networks, filters, oscillators, etc. Thus, in order to provide valuable information for circuit designers, the characterization process used in this project was based on the processing of *S*-parameters measurements, which includes effects corresponding to the intrinsic nature of the passive device, plus the interaction with the surrounding materials. This information allows to represent the performance of passive devices and interconnects by using simple circuits that physically represent their behavior. Bear in mind that using the *S*-parameters for characterization purposes requires to take into consideration the parasitic effects of the text fixtures necessary to reach the devices under test. In this regard, the impact of these fixtures was also studied in detail in this work.

In addition, the potential of *S*-parameter measurements for characterizing and modeling the properties of the materials used in microwave devices is also explored. This points out the fact that these data is of great value when developing and optimizing circuit and devices since it is possible to analyze the properties even at the level of the fabrication materials.

Contents

Preface

This project started in 2010 after I obtained my M.Sc. degree working on high-frequency characterization of interconnects on packaging technologies. At that time, I realized the importance of microwave electronics not only in the development of new devices and systems, but also to understand the effects present in the structures as the operation frequencies increase. In fact, it is now evident that little details such as small changes in the structures and using different materials may considerably impact the performance of devices working in this condition. Thus, now more than ever before, accurate characterization is fundamental in microwave electronics. This is the reason behind the motivation of this Ph.D. project, which contains the result of employing microwave techniques in the characterization of passive devices and interconnects.

Regarding this document, it is organized in five chapters where the analysis performed at different passive devices and interconnects is presented. **CHAPTER 2** is dedicated to transmission lines on different levels of integration: on PCB boards and on silicon. As a result, it is proposed a method for determining the parameters of the frequency-dependent attenuation model for transmission lines on PCB board. The method allows separate the conductor and dielectric losses even when the conductor losses present a non-ideal frequency variation. Furthermore, the modeling of uniform transmission lines on silicon permitted implementation of equivalent circuit model in both the frequency and time domains. **CHAPTER 3** presents an analysis of experimental data of on-wafer structures to verify the differences between the one and two-step de-embedding algorithms. This analysis allows the identification of the potential errors introduced by one-step de-embedding in low and high impedances structures at RF measuring. Additionally, a systematic methodology for characterizing and modeling on-chip inductor over a lossy substrate is presented, using only S-parameters measurements. **CHAPTER 4** describes a high frequency technique to characterize advance dielectric material employing RF measurements. The extraction method allows the determination of frequency dependent parameters through the RF measurements performed to a simple Metal-Insulator-Metal structure. **CHAPTER 5** presents a summary of the obtained results and the most important conclusions of the work.

Svetlana Carsof Sejas García

June, 2014.

CHAPTER 1
Introduction

MICROWAVE ELECTRONICS is currently one of the most important fields studied at academic and industry levels with the purpose of contributing in science and technology aspects. This is due to the fact that microwaves, ranging in frequency from 0.3 GHz to 300 GHz (i.e., 1 m > λ > 1 mm in free space), provide enough power to radiate energy with communication purposes, but also because the processing of information is reaching frequencies within this range [1, 2].

This vast discipline encompasses the generation, absorption, radiation, processing, and guiding of microwaves using electronic devices, but also the desired and undesired interaction of microwaves with these devices through free space and within different media. In this regard, it is understandable why many research groups working on microwave electronics are dedicated to particular research with apparent no relation with each other. For instance, heat generation in dielectrics exposed to microwaves can be used with either cooking or medical purposes [3-6], but it can also be considered as an undesired effect when occurring within a computer motherboard where it degrades the integrity of the information carried by the waves [7-9].

From a perspective of electronic circuits and systems, microwaves interact with different materials and devices. Thus, the corresponding characterization and modeling is required to carry out systematic designs. It is therefore imperative to know the properties of the active and passive devices included in these circuits and systems. In this context, during the past decades must of the research was dedicated to understand and predict the behavior of active components (e.g., transistors and other amplifiers) since the operation of the circuits and systems was mainly determined by these devices [10, 11]. As the operation frequency has increased, however, the delay and power loss related to other components and even to interconnects have taken importance, considerably influencing the performance of electronic systems [12, 13]. Moreover, a better understanding of signal propagation within the systems is needed, requiring the precise knowledge of the properties of the structures and materials used to implement electronic systems for prototyping and production purposes [14-16].

In order to contribute within the aspects discussed in the previous paragraph, in this thesis, the microwave characterization and modeling of passive devices is studied from a theoretical-experimental point of view. The study covers Transmission Lines (TL), as well as inductors and capacitors used in integrated circuits. Thus, the project focuses in the application of measurement-based techniques to develop and implement

models and parameter extraction algorithms that allow to represent these devices in circuit simulators. This is performed with the intention of exposing the feasibility of carrying out physically based analyses in circuit design stages when microwave measurement equipment is available.

1.1 Interconnects, passives and system levels in electronic systems

As already mentioned, the continuous increase of the operation frequency and circuit density is a result of the demand for improved performance of electronic equipment as well as the requirements for low power consumption and high portability [17]. In fact, the development of smaller and faster transistors in combination with materials with improved characteristics is the reason why high system integration has been achieved. However, the transistors only represent about 10% of the ICs area, whereas the interconnections (e.g., transmission lines, vias, pads, etc.) and passive devices (e.g., inductors, capacitors, filters, etc.) occupy near 90% of the area left [18], which is depicted in Fig. 1.1. Moreover, the global performance of a chip and even of a complete system is determined to a high extent by interconnects and passive devices. This is due to the fact that the circuit's bandwidth, center frequency, and impedance matching greatly rely on the performance of passives. Therefore, many problems related to power consumption, signal integrity, thermal dissipation, wideband, and delay can be solved and even prevented when paying care to the design and optimization of passive components and interconnects [19, 20]. For this reason, it is necessary to characterize and model these components, particularly when the

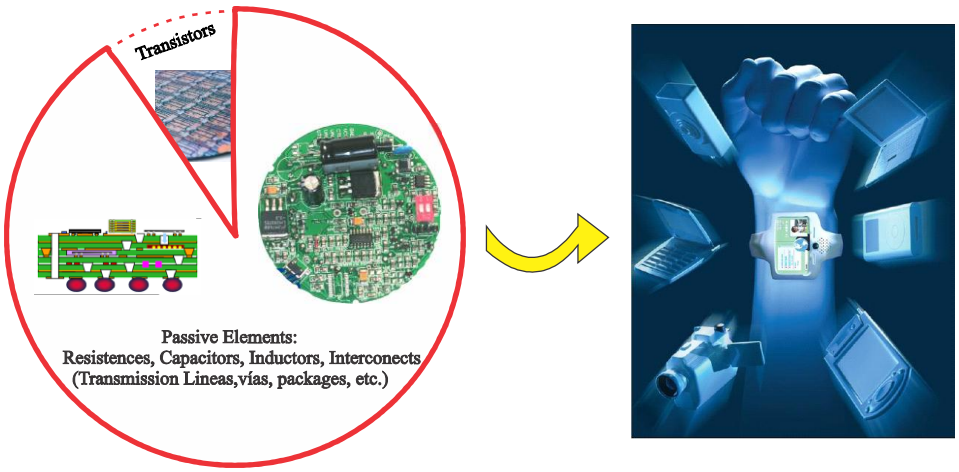


Fig. 1.1 Sketch of the integration in high-tech gadgets [18].

corresponding impact takes more importance such as in the case of high-frequency operation. In order to do so, a correct understanding of the devices behavior is necessary, which allows to develop physically based useful representations to be employed during the different design stages.

1.1.1 On-chip interconnects

Interconnects exist at every level of electronic systems. For the case of on-chip interconnects, they can be classified into different integration levels [21- 24]. The integration levels allow the identification of the corresponding requirements, as well as the physical effects influencing their operation performance. In current integrated circuits, there are three basic levels of integration:

1. **LOCAL**: The local interconnects are those in the lowest levels, usually connect gates, source, drains, meaning transistor-transistor connection. This type of interconnects present high resistance as a result of the small transversal cross section of the traces.

2. **SEMIGLOBAL**: This type of interconnects are used to connect functional blocks. For instance inverters, signal boosters, etc.

3. **GLOBAL**: The global interconnects are long and run all around the circuit, as those used for power distribution, clocking, and to serve as return pad. These interconnects present relatively low resistance but necessary have to be treated as transmission lines at high frequency due to their long length.

Fig. 1.2 shows different interconnection levels within an IC. The interconnect level is an important parameter to take into account in modeling because interconnects at different levels experience effects in a different manner: losses, delay, interference, etc.

1.1.2 PCB interconnects

PCB interconnects are those outside the semiconductor IC. In fact, sometimes global IC interconnects are taken outside the semiconductor substrate and implemented at this level within a PCB or a small version of it called package. In this regard, packages typically contain one or several ICs belonging to the same or to different semiconductor technologies. Moreover, packages may even contain other packages, ICs and components such as passives. In fact, the design and analysis of the

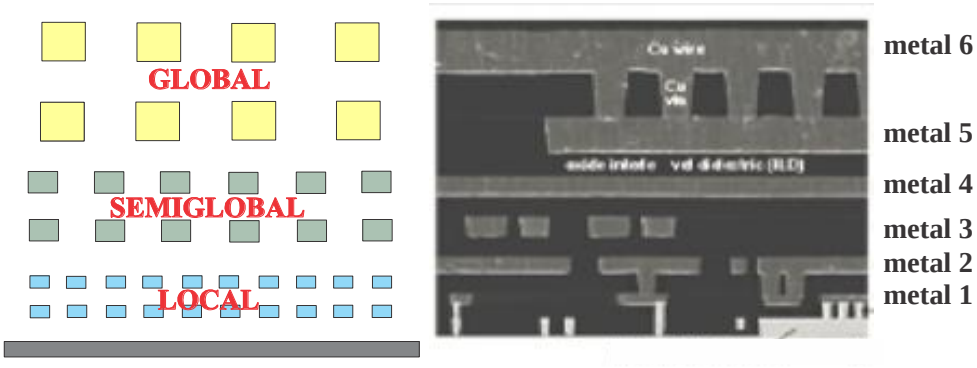


Fig. 1.2 Sketch (left) and micrograph (right) illustrating the stack-up and simplified description of the different levels within an IC [22].

corresponding interconnects necessarily require to consider thermal, mechanical, electromagnetic, and fabrication aspects, which is covered in a technology commonly referred to as Packaging [18, 20, 25]. PCB interconnects in current technologies present much larger dimensions than those used in ICs. This is owing to the fact that they are mostly used to connect functional blocks, like packages and even to serve as board to board interfaces. Thus, as for the case of any other off-chip interconnect, the main issue that affect their performance is the signal delay due to their relative long length and high inductance [2]. Fig. 1.3 shows the interconnect delay time relative to that associated with interconnects fabricated on 250-μm technology. Notice that as technology evolves, local interconnects become faster (i.e., the delay time is smaller to that corresponding to the 250-μm technology) since the inter-device distance becomes shorter. In contrast, longer interconnects such as those on package or on PCB present substantially larger RC delays. Therefore, in order to maintain the signal integrity within the margins established to warrant proper operation, additional circuits are necessary, which increments the power consumption and the cost of the final product.

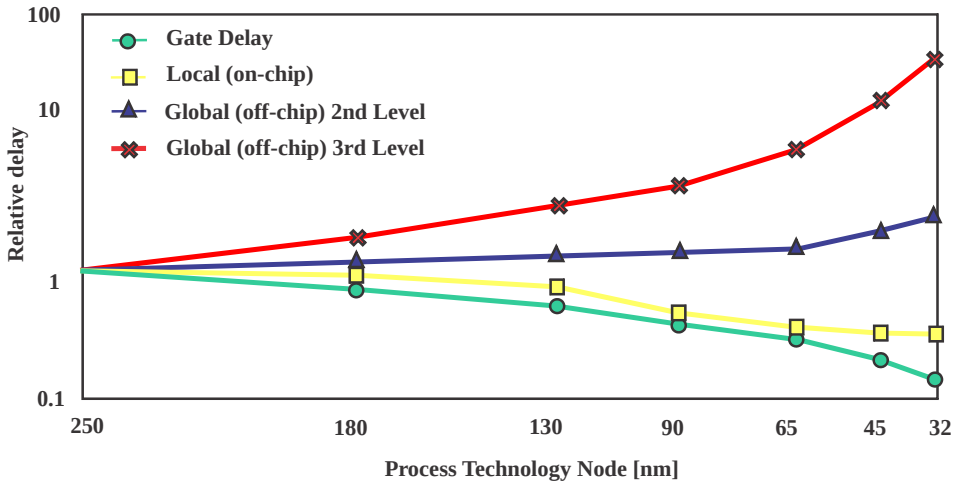


Fig. 1.3 Curves showing the interconnect delay time for interconnects at different system levels relative to that associated with the technology node [12].

Technology evolution also yields that electronic systems become more complicated and reduced in size. Thus, heterogeneous solutions are currently used to combine the advantages of different semiconductor and packaging technologies [26-28]. These solutions are usually referred to as convergent systems. Fig. 1.4 depicts some of the most used. Hence, when considering integration involving PCB and package levels, different approaches have been proposed to achieve better performance. Similarly to the case discussed previously for on chip interconnects, a classification of these approaches involving packaging technologies can also be made; in this regard, proposals currently used for practical applications include:

- **2D INTEGRATION**:
  - System on Chip (SoC). This is an IC that contains all the components of an electronic system into a single semiconductor die.
  - Multi-Chip Module (MCM): Specialized package where RF subsystems, multiple ICs, and other types of modules are packaged. In this case, several chips working independently are unified within a single packaging substrate so that the final discrete component (i.e., the module) performs a given function. This is the simplest approach to incorporate multiple unpackaged chips as a single piece.

- **3D INTEGRATION**:
  - System in Package (SiP). In this case, the system is composed of several ICs and other semiconductor components enclosed into a single module known as package (i.e., a small PCB). This is a generalization of a MCM, since a SiP performs all the system functions. In addition, the chips can be vertically stacked.
  - Package on Package (PoP). In this case, the system is implemented by vertically stacking individually packaged ICs. Thus, each IC is mounted within a package and then the different packages are interconnected usually through ball-grid-arrays. This allows for a higher integration density, which is useful particularly for mobile and compact devices such as cell phones.
  - System on Package (SoP). This approach combines the advantages of SoC and SiP by moving the global interconnects required within an IC to the package. This represents a tremendous advantage due to the fact that the losses associated with the package interconnects (with considerably larger cross section) are substantially lower than those occurring within an IC. Furthermore, passive components such as capacitors, inductors, and

antennas, are more cost-effective on a package than on a semiconductor substrate.

Regarding the electrical part, signal propagation through interconnects is a key theme to be considered when developing all these systems.

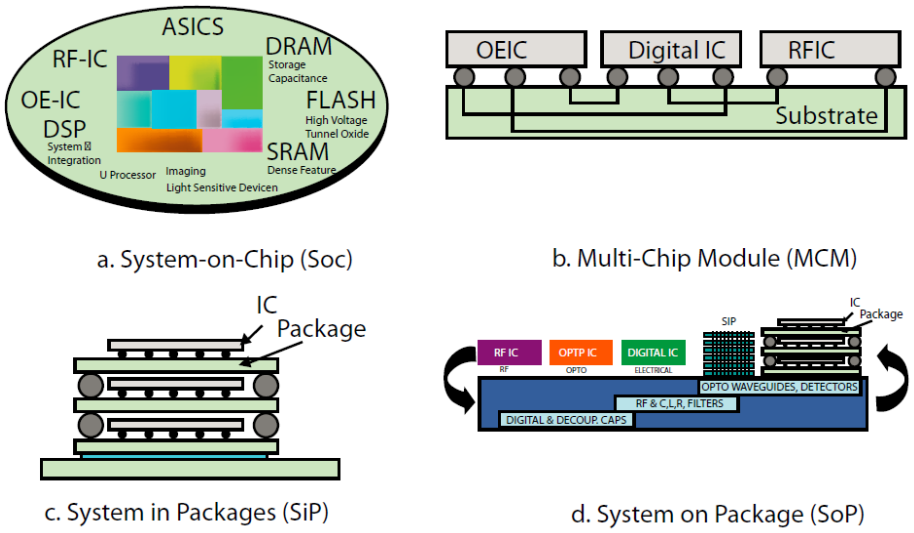


Fig. 1.4 Depiction of some convergent systems [26].

1.1.3 Passive components

A key part of any electronic system is that related to passive components. These elements allow to generate, adapt and preserve signals throughout a circuit. In this regard, passives do not require any source of energy to perform their function. Inductors, capacitors, resistances, and many matching networks fall into this category. In current technologies, the integration of many different functions into smaller areas is required. Unfortunately, in contrast to what happens to most active components, the performance of passives typically decreases with size. Thus reducing their size without compromise the performance is a tradeoff to be taken into account by designers. In this regard, since passive devices are chosen to present given characteristics under tight design specifications, the corresponding accurate modeling and characterization is one of the most important topics studied by engineers and scientist working in the development of systems operating at microwave frequencies.

To improve the performance of passive components, different geometries and integration methods have been proposed not only in a planar way [29]. In fact, 3D integration [30] has been explored to improve their performance, reducing their dimensions. However, the effects like substrate loss, leakage currents, electromagnetic coupling, conductor losses, degrade their behavior at high frequency.

Thus, the figures of merit to evaluate the passive performance is the quality factor (*Q*), bandwidth, frequency of resonance, all have a frequency dependent behavior, for that reason is complicated accurate model a passive device, in CHAPTER 3 is modeled a inductor fabricated on semiconductor substrate.

1.2 Signal integrity

Electronics technology manipulates electrical currents in a controlled way to transport and process information. Thus, the quality in the transmission of the signals from a source to a destination should be carefully analyzed in a systematic manner. This is the field of study of Signal Integrity (SI). In this regard, the integrity of transmitted signals is influenced by many effects including impedance mismatch (e.g., undesired signal reflections), crosstalk, EM coupling, attenuation (i.e., signal losses), and jitter [31]. Moreover, the continuous reduction of the signal rise time substantially worsen SI problems since many previously neglected effects are accentuated in this case. Hence, SI is of great importance for scientists and engineers working on electronics; they all work with electronic signals. It is thus mandatory, to solve SI problems as early as possible during the design process. For this purpose, accurate modeling and simulation of components is required, paying particular attention to passive devices and interconnects. This takes even more importance when the circuits are operated at microwave frequencies, where the distributed nature of these devices become apparent [1, 32].

For designing and developing accurate models to represent the transmission channel that defines the signal path, understanding the principles of Electromagnetic Theory, such as wave propagation, boundary conditions, as well as the reflection and transmission of waves is extremely important. Furthermore, to properly represent the distributed nature of interconnects and devices, concepts belonging to Transmission Line Theory like the telegraph's equations, transmission line's propagation constant and characteristic impedance need to be clearly understood and applied. In addition, the properties of materials and structures like dispersion and absorption need to be taken into consideration through the quantification of fundamental parameters such as the conductivity and permittivity, which are frequency dependent [32-34]. All this allows obtaining realistic results and to predict the performance of a circuit in a useful way.

Properly addressing SI problems at the different stages for the design of electronics systems results in a considerably reduction of possible fails on the system. This fails may be difficult to identify and even yield catastrophic results when occurring after a product has been launched to the market. Thus, since interconnects

and passive devices are carrying and processing high frequency signals in current applications, much of the noise and signal degradation occurring in electronics systems can be avoided when carefully designing this devices. This also allows to establish the guidelines used for designs, as well as layout, material, and fabrication specifications. Thus, notice the importance of the appropriate modeling and characterization of devices based on the understanding of the associated physical phenomena.

1.2.1 Simulation tools

This type of model is one the most important tools used in PCB, IC interconnect, and passive device design. Thus, the simulation allows predicting the performance of a device or system before prototyping the hardware. Thus, when properly used, it is a valuable tool for assessing the impact of the parasitics on the performance of an actual circuit. In this case, basically there are two ways for simulating a device, one is carrying out an analysis by transforming the structure into an equivalent circuit where the simulator can be used to predict the voltages an currents in any node using the Kirchhoff's equations. Among the advantages of this type of simulations is the short time required to get the results. Thus, iterative simulations changing one or several conditions might be performed when improving a design. In this category of simulation tools, the circuit simulators HSPICE and Agilent's ADS have been the most popular choices both in academy and industry environments for many years [34, 35].

Alternatively, electromagnetic (EM) simulators employ 2D or 3D geometries involving and the material properties to define the boundary conditions to calculate the electric and magnetic fields using Maxwell's equations. In this case, a behavioral model of the structure is used to carry out a representation that allows to obtain the corresponding characteristics under different stimuli (e.g., different frequencies). EM simulators are employed for the analysis of complex structure so that key features can be optimized [33]. Since the time to solve the simulations is substantially longer than when using circuit simulators, the use of these tools is restricted to detail study of single structures, such as when developing a model for a device, to learn the origin of a problem occurring in the structure, or for device optimization.

Among the most commonly used tools belonging to this category highlight Ansys's HFSS, Agilent's EM Solver, and CST's Microwave Studio. In this thesis, results obtained using this type of software allowed to identify some important effects that lead to the development of equivalent circuit models that are more suitable for

device and circuit design simulations. More details about this type of models are given in the following section.

1.2.2 Equivalent circuit modeling

A popular alternative to model interconnects and passive devices at high frequencies is using equivalent circuits. This is because equivalent circuits represent the device's characteristics by describing its topology, which provides intuitive details about the corresponding operation. In this case, each effect influencing the device's behavior is represented by means of lumped elements that can be extracted directly or indirectly from simulations or measurements. The main advantage of this type of models is their simple implementation and accuracy. In addition, when a model is properly implemented, the value for the lumped elements is associated with a physical effect.

One of the most important characteristics of these models is the necessity of determining the value of the intrinsic elements at the desired conditions (e.g., frequency and geometry). Moreover, when a passive structure's electrical behavior is represented at high frequency, some requirements must be fulfilled by the applied models in order to make them feasible for simulations. Among the most important demands for a good high frequency model are [31, 35]:

1. Scalability: Many passive devices with different layouts and dimensions are used to implement RF circuits. Thus, the model must be adequate to represent the characteristics of a given device as a function of its geometry. In addition, can be portable to move easily from one domain to another (e.g., frequency to time). This last point is important since, for instance, whereas frequency dependent elements are easily represented when performing simulations in this domain, time domain simulations cannot be directly performed. One contribution in this direction was developed in this thesis (detailed in Chapter 2).

2. Accuracy within the gigahertz range: For high frequency applications, the operation frequency is within the gigahertz range. Currently, models should be accurate up to at least 30 GHz. Because, the frequency sweep issues are related to the Fourier transform, to changes between the frequency domain to the time domain, and without enough information from the frequency domain, will get incorrect results in the time domain.

3. Causality: A causal model is a that in which the simulated output depends only on the current and previous input values. In this regard, the model describes the causal mechanisms of a system since good model-experiment correlation

does not necessarily imply causation. The importance of keeping a model causal is to warranty the realistic system representation in both frequency and time domains.

Although, an ideal high frequency model should be scalable and accurate, it is very difficult to reach that goal. Nevertheless, the good agreement between simulations and measurements obtained at high frequency justifying the use of circuit modeling for RF and microwave applications. However, very good approaches can be obtained by performing a systematic modeling strategy as is explained in the following chapters.

1.2.3 Equipment characterization

Measurements play one of the most important and critical roles when developing models and assessing the performance of circuits and devices [36]. Good measured data provide relevant information that may lead to the reduction of fails, which is the reason why the validation of finished products necessarily involve experimental analyses. For measuring passive devices and interconnects, the instrument applies signals to the Device Under Test (DUT) and measures the response to allow the determination of the corresponding electrical characteristics. Particularly, at high frequencies, the proper consideration of the test fixture parasitics is extremely important due to their influence on the resulting data. In this regard, calibration and deembedding techniques have to be carefully applied to get realistic results. This thesis also shows contributions in this direction as detailed in Chapter 3.

At microwave frequencies, three basic instruments are used to perform measurements of passive devices and interconnects:

1. Impedance analyzer: A four terminal instrument that works in the frequency domain. Two of the terminals inject a constant sine-wave current to the DUT, while the last two terminals measure the sine-wave voltage through the DUT. The radio between the measure voltage and applied current is the impedance obtained the phase and magnitude in the range of 100Hz to about 40MHz.

2. Vector network analyzer (VNA): Operates in frequency domain in the ranges of low KHz to hundreds of GHz. Commercially, two and four port VNAs are the most popular today. In this case each port emits a sine-waves swept in frequency to obtain the transfer function of the device. This is the basic tool used in current microwave laboratories.

3. Time domain reflectometer (TDR): similar to the VNA but operated in the time domain, it emits a signal with a rise time step in the range of 35 psec to 150 psec, and measures the reflected transient amplitude. A TDR basically measures the instantaneous impedance of the DUT, or in other words the time domain representation of the reflection coefficient.

As the work frequency is continuously increasing, the measurement plays an important role in the passive device design, related in reducing the errors and enhancing the accuracy of the device. Measurements allow the design improvement by:

1. Verify the accuracy of the design-modeling-simulation process.
2. Verify if the device meets the performance spec.
3. Create an equivalent electrical model for a component at any stage of the design.
4. Emulate system performance of a component as quick way of determining expected performance without building an electrical model.

In this thesis, experimental data collected using a VNA were used showing that this tool by itself can be used to obtain most of the data required to carry out model development and SI analysis in today's applications.

1.3 Purpose of this Thesis

The purpose of this work is to contribute to the study and modeling of devices at high frequency applying physically based analyzes and using the tools available in a microwave laboratory. The aspects studied during the development of this work include modeling, characterization and parameter extraction at high frequency of state-of-the-art interconnects and passive devices. The models are developed for devices at different system levels and allow to show the feasibility of obtaining circuit design oriented representations using microwave measurement techniques.

CHAPTER 2
Modeling Interconnect at Different System Levels

THE REASON for dedicating part of this project to interconnects is because, as mentioned in Chapter I, interconnects represent the bottle neck limiting the global performance of electronic systems. In this regard, the complexity of the architectures, the high density of interconnects, the continuous system size shrinking, the large areas occupied by interconnects [18], as well as the higher operation frequencies are some of the aspects to be considered when designing interconnects. In fact, there are a wide variety of interconnects to add versatility to a given design: planar transmission lines, wires, waveguides, vias, ballgrid arrays, clippers, flip chip contacts, etc. For instance, to illustrate some of the interconnects used within an IC, Fig. 2.1 shows the cross section of a multi-level IC stack-up; for each metal level, different features are presented by the interconnects, and the corresponding behavior is influenced by physical effects in a different fashion.

In order to understand the context in which this proyect contributes to the study of interconnects, an overview of the different system levels is necessary. As the electronic systems become more complicated and reduced in size, heterogeneous solutions are used to combine the advantages of different semiconductor and

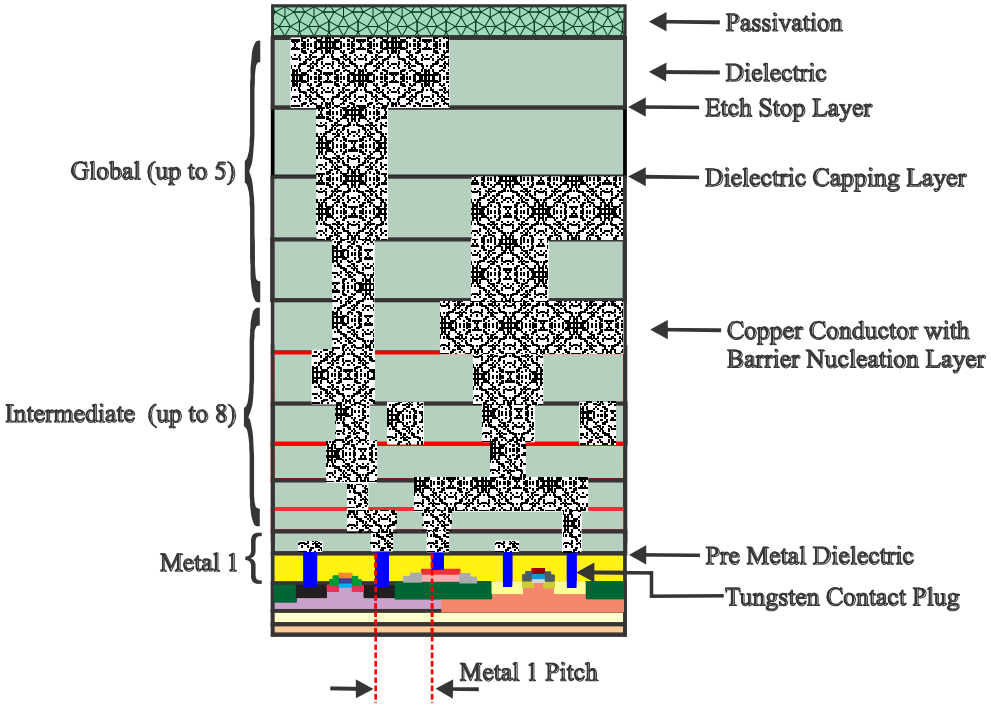


Fig. 2.1 Sketch of the cross-section of an Integrated Circuit showing multi-layer metal interconnects on top of a device layer [12].

packaging technologies [26]. These solutions are usually referred to as "convergent systems" (see Fig. 2.2), and include: SoC, SiP, PoP, SoP structures.

Signal propagation through interconnects is a key theme to be considered when developing these systems. For this reason, the electrical path followed by the signals has to be carefully designed taken into account the main effects associated with the interconnects present at each level of the system: from on-chip (e.g., between transistors) to off-PCB (e.g., between boards within a computer). Therefore, in this chapter two of the most important planar interconnects used in these systems are studied from an experimental-theoretical point of view: PCB and on-chip planar interconnects.

What follows in this chapter was written to point out the differences between two of the most important types of interconnects. Moreover, within this context, new models and analytical parameter extraction techniques are presented to allow circuit designers the appropriate representation of the interconnects present either on-chip or at a PCB level.

2.1 Modeling interconnects using transmission line theory

In general terms, a planar interconnect is that formed at a single metal layer within an electronic circuit. At frequencies at which the wavelength of the propagated signals is comparable to the physical length of the interconnect, Transmission Line Theory concepts have to be used to perform the corresponding analysis [34]. Particularly, for

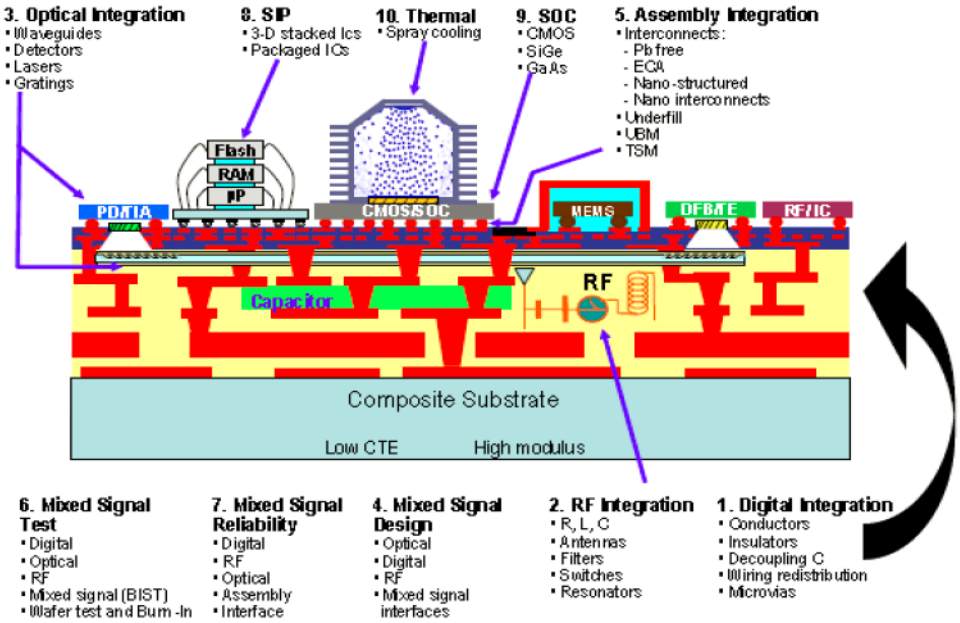


Fig. 2.2 Convergent systems [37].

the case of planar interconnects, the most common approach for studying the propagation and matching features is partitioning the line into sections that can be represented assuming homogeneity. This is discussed hereafter.

A TL presenting the exact cross section along its length is considered homogeneous and can fully represented from its propagation constant ($\gamma = \alpha + j\beta$) and characteristic impedance (Z_0). Even though in practice it is not possible to find a perfectly homogeneous TL, appropriate representations of actual lines can be achieved when obtaining effective values for γ and Z_0. On the other hand, in spite of the fact that the term 'transmission line' can be applied to a wide variety of structures that allow guiding electromagnetic signals, it is typically understood that a transmission line is that that supports propagation in either transversal electromagnetic (TEM) or quasi-TEM mode. Striplines and microstrips are planar interconnects that fall into this category and by far are the most common interconnects within current electronic circuits. For these lines, the resistance-inductance-capacitance-resistance (*RLGC*) model associated with the telegrapher's equations can be used to model the corresponding distributed nature at high operation frequencies. Therefore, if γ and Z_0 are known, the per-unit-length resistance (R), inductance (L), conductance (G), and capacitance (C) can be obtained. Bear in mind that the *RLGC* parameters are dependent on frequency. Moreover, these parameters also vary with the materials employed to fabricate the lines as well as with the integration level at which the interconnects were implemented, because this defines the corresponding dimensions and process-related parameters such as metal-dielectric roughness.

In practice, the performance of TLs is basically limited by the corresponding loss and dispersion, which are respectively quantified through the attenuation constant (α) and the phase delay (β). It is important to mention that Z_0 is mainly used to assess the matching properties of the line. For the case of the attenuation, which is considered as one of the most important figures of merit for interconnects used at the different levels of high-speed electronic systems [38, 39], the following contributions are typically taken into account:

1. The attenuation associated with the conductor losses (α_c).
2. The attenuation associated with the dielectric losses (α_d).
3. The attenuation associated with electromagnetic radiation from the line, which is much less than the other two contributions for typical lines operating at microwave frequencies.

Whereas the dielectric losses are in general independent of the line's geometry provided that the dielectric is not so thin to introduce leakage currents between the signal and ground paths, the conductor losses are a strong function of the cross section where the current is flowing. Therefore, as the circuits are made smaller, the effect of the metal losses substantially degrade the performance of interconnects. This is the reason why on-chip interconnects present higher loss when compared with on-PCB lines.

Since the series elements associated with the TL are related to the metal traces carrying the signals, it is also necessary to point out the fact that the skin effect considerably impacts the performance of interconnects [40, 41]. For this reason, the analyses presented hereafter consider this fact and point out the differences between the most important effects in two of the most widely used interconnection technologies: PCB and on-chip. Thus, the first part of this chapter is dedicated to TLs on PCB technology, whereas the second part covers TLs on semiconductor substrate.

2.2 Modeling the attenuation constant

For the case of a two-conductor TL fabricated on PCB technology operating at microwave frequencies (f), the widely used attenuation model dictates that α_c and α_d are approximately proportional to $f^{0.5}$ and f, respectively [34]. Actually, techniques for separating the conductor and dielectric losses in PCB TLs considering this fact are available [42]. However, the ideal f-dependent model for α_c fails to reproduce experimental data above a certain frequency and poor agreement between simulated and experimental data is obtained beyond this limit. For this reason, a modified model for α_c has been applied to TLs on semiconductor [38] as well as on PCB substrates [39], in which the typical dependence on $f^{0.5}$ is substituted by a dependence on f^{n}. This modified model allows the proper correlation of simulated with experimental data within a wide frequency range. Even though the physical significance of n is still subject of discussion in both academy and industry research groups, its use allows to avoid the application of fitting models that require the determination of several parameters (e.g., Hammerstad & Jensen's [43]). The following explains an approach derived from the research carried out in this project for determining the model parameters for α including the exponent n that allows for the modeling of the conductor losses at microwave frequencies; which is of particular importance when the surface roughness increases the losses associated with the metal trace on PCB technology.

2.2.1 Text structures on PCB technology

Fig. 2.3 shows the layout of the TLs used for illustrating the development and verification of a method for implementing a full model for a transmission line considering the dependence of α_c on f^n. These lines were fabricated on a PCB made of a low-loss Rogers RT/Duroid 5880 material, with a thickness of 127 μm, and nominal relative permittivity (ε_r) and loss tangent ($\tan\delta$) of 2.2 and 0.0017, respectively. The lines were made of copper with a thickness of 36 μm, and the substrate—metal interface presents a nominal root mean square roughness (h_{rms}) of 1.8 μm. Fig. 2.3 shows that the lines have a width of 350 μm, different lengths (l), and are terminated with ground-signal-ground (GSG) pads so that coplanar RF-probes with a pitch of 150 μm can be used to perform *S*-parameter measurements. These measurements were carried out using a VNA which was calibrated up to the probe tips by using a line-reflect-match (LRM) algorithm and an impedance-standard-substrate (ISS) provided by the probe manufacturer. Afterwards, γ (per meter) was determined from the experimental data of two lines with l = 12.7 mm and 25.4 mm by applying a line-line procedure that removes the effect of the parasitics associated with the pads shown in Fig. 2.3 [44]. These measurements were taken at the Intel's Guadalajara Design Center.

2.2.2 Model implementation

A detailed *f*-dependent model for the attenuation occurring in TLs is described in [34]. Assuming $\tan\theta \ll 1$, such as in the case of typical PCB substrates, the model is reduced to [42]:

$$\alpha = k_1 f^{0.5} + k_2 f \tag{2.1}$$

where k_1 and k_2 are constants. Thus, in accordance to (2.1), these constants can be respectively obtained from the intercept with the ordinates and the slope of the linear

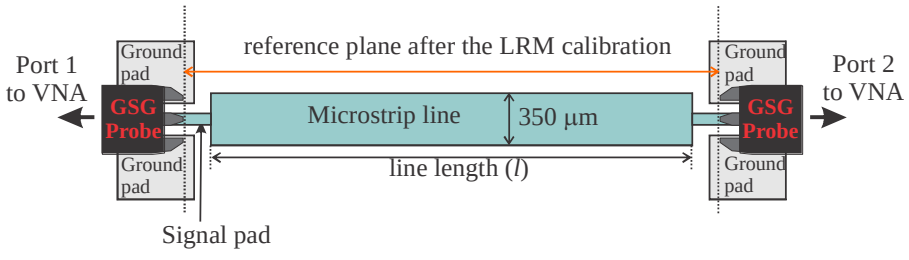


Fig. 2.3 Sketch illustrating the layout of the fabricated microstrip lines. Notice also the configuration of the probing pads for measuring *S*-parameters.

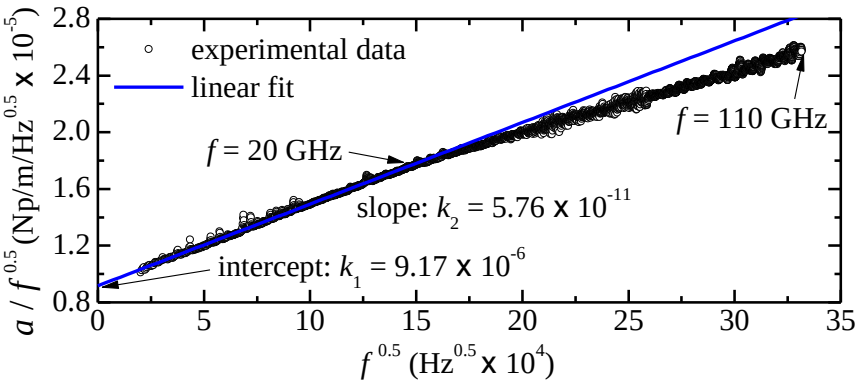


Fig. 2.4 Determination of the parameters in (2.1). A single linear regression fails for representing the data for the measured frequency range (up to 110 GHz).

regression of the experimental $\alpha/f^{0.5}$ versus $f^{0.5}$ curve.

Fig. 2.4 shows the extraction of k_1 and k_2 for the fabricated lines. Notice that the linear regression allows to represent the experimental data up to about 20 GHz. For higher frequencies, however, (2.1) is no longer valid and the regression deviates from the data. Here finds application the model where α_c is assumed to be proportional to f^n , where n is a positive real number. In this case, α can be written as:

$$\alpha = K_1 f^n + K_2 f \tag{2.2}$$

Even though K_1 and K_2 are constants, the introduction of the third unknown parameter n increases the difficulty of the parameter extraction since (2.2) cannot be written so that a simple linear fit of experimental data is performed. However, this problem can be solved as described as follows. Equation (2.2) can be rewritten as:

$$g = K_1 f^N + K_2 \tag{2.3}$$

where $g = {}^{\alpha}/_{f}$ and $N = n - 1$. The derivative of g is given by:

$$\frac{dg}{df} = NK_1 f^{N-1} \tag{2.4}$$

which allows to reduce the number of unknown parameters to two. Then, multiplying by –1 and applying the logarithm (with base 10) to both sides of (2.4) yields:

$$\log\left(-\frac{dg}{df}\right) = \log(-NK_1 f^{N-1}) \tag{2.5}$$

In accordance to (2.3), since $0 < n < 1$ then $N < 0$, and g is a monotonically decreasing function of f. In consequence, dg/df is negative, which makes necessary the use of the minus sign in (2.5) for the logarithms to be real number. Using logarithm identities, (2.5) can be expanded as:

$$\log\left(-\frac{dg}{df}\right) = \log(-NK_1) + (N-1)\log(f) \tag{2.6}$$

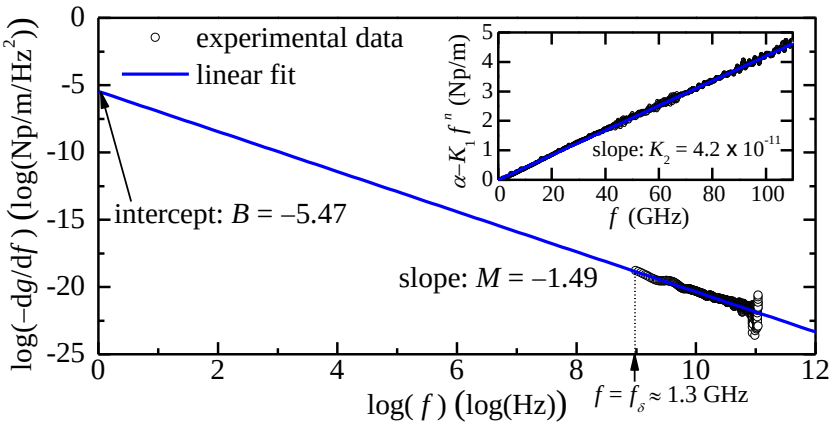


Fig. 2.5 Regressions used to determine the attenuation model parameters using the new method for the fabricated lines from 1 to 110 GHz.

which allows to respectively determine $\log(-NK_1)$ and $(N-1)$ from the intercept with the ordinates, *B*, and the slope, *M*, of the linear regression of the experimental $\log\left(-\frac{dg}{df}\right)$ versus $\log(f)$ curve. Thus, K_1 and *n* in (2.2) can be obtained using:

$$K_1 = -\frac{10^B}{(M+1)} \tag{2.7}$$

$$n = M + 2 \tag{2.8}$$

Once K_1 and n are known, (2.2) can be solved for $\alpha_d = K_2 f$, which allows to determine K_2 from the slope of the linear regression of the $(\alpha - K_1 f^n)$ versus *f* data. This regression, as well as that associated with (2.6) is shown in Fig. 2.5. In order to apply the linear regression defined by means of (2.6), the experimental dg/df has to be obtained. In this regard, it is well known that differentiating using finite-difference approaches greatly amplifies the noise associated with experimental data. Due to this, we applied an alternative differentiation algorithm described in [45] to accurately obtain dg/df. In this case, an excellent linear trend of the experimentally determined data is observed in Fig. 2.5, which allows to easily obtain the following values for the fabricated lines: $K_1 = 7 \times 10^{-6}$, $K_2 = 4.2 \times 10^{-11}$, and $n = 0.52$.

In [34], obtaining $n > 0.5$ is attributed to the effect of the roughness of the substrate—metal interface, which starts becoming apparent when f increases to around f_δ, defined as the frequency at which the skin depth of the metal (δ) equals h_{rms}. For considering this effect, k_1 in (2.1) can be modeled including an *f*-dependent term, as predicted by the Hammerstad & Jensen's model. When $f \gg f_\delta$, however, this term becomes weakly dependent on *f* [43]. Thus, since the fabricated lines present $f_\delta \approx 1.3$ GHz, it is expected that the dependence of k_1 with *f* is relatively weak at

20 GHz. Notice, however, in Fig. 2.4 the accentuated variation in α around this frequency, which indicates the combined influence of the roughness with another effect. This effect is the variation in the distribution of the current within the cross section of the metal lines, which is dependent on f and is accentuated when t is comparable to w in microstrip lines [46]. Full-wave simulations of the current distribution in the cross-section of the studied TLs indicate that, around 20 GHz, most of the current in the signal trace flows at the bottom and at the sidewalls, increasing the value of k_1 as compared to that seen at relatively low frequencies (i.e., when considerable part of the current also flows at the top of the line, as can be seen in Fig. 2.6). The combined impact of these effects on R is quantified in the following section.

2.2.3 Model implementation considering the f^n model

This section focuses on implementing a model for the *RLGC* parameters of a TL assuming quasi-TEM mode propagation and using the extracted n. Neglecting the low-frequency resistance (R_0) and conductance is valid for PCB TLs since $\delta \ll t$ the skin depth is much smaller than the trace thickness at microwave frequencies and the dielectric leakage currents are very small. In fact, this is one of the main differences between PCB and on-chip interconnects, since R_0 is not negligible for on-chip lines and therefore the approach presented in this section cannot be directly applied.

Assuming $R_0 \approx 0$ and α_c proportional to f^n, the *RLGC* parameters can be represented by using a causal model as [47]

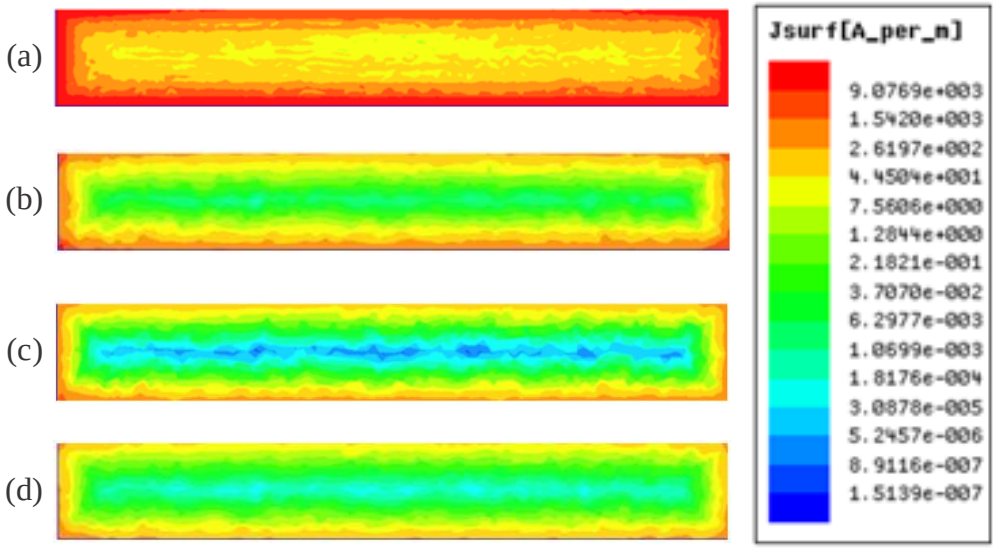


Fig. 2.6 Simulated current distribution for the signal trace of a microstrip line obtained through full-wave simulations using Ansoft's HFSS. The images show the results for the following frequencies: (a) 1 GHz, (b) 5 GHz, (c) 15 GHz, and (d) 20 GHz.

$$R = K_R \omega^n \tag{2.9}$$

$$L = L_0 + K_R \omega^{n-1} \tag{2.10}$$

$$G = \omega C \tan\theta_{eff} \tag{2.11}$$

where K_R and L_0 are constants, whereas C and the effective loss tangent $(\tan\theta_{eff})$ are dependent on f for the model to be causal. For simplicity, we used here $\omega = 2\pi f$. To obtain the parameters in (2.9)–(2.11), γ is expressed as:

$$\gamma = \alpha + j\beta = \sqrt{ZY} \tag{2.12}$$

where $Z = R + j\omega L$, $Y = G + j\omega C$ and $j^2 = -1$. Thus, substituting (2.9)–(2.11) into (2.12) and assuming $\tan\theta_{eff} \ll 1$ yields:

$$X = \frac{\mathrm{Im}(\gamma^2) - \mathrm{Re}(\gamma^2)}{\omega^{n+1}} = 2CK_R + CL_0\omega^{1-n} \tag{2.13}$$

Hence, the term CL_0 can be determined from the slope of the linear regression of the experimental X versus ω^{1-n} curve. However, since C depends on f, the regression has to be performed at intervals at which the variation of this parameter is small, which is achievable due to the weak dependence of C with f for PCB TLs [48]. Fig. 2.7 shows the extraction of CL_0 at two different frequencies showing good linearity considering a frequency interval of 1 GHz; notice also that $2CK_R$ is obtained from the intercept with the ordinates. Afterwards, K_R can be determined at low frequencies from $2CK_R/2C_0$, where C_0 is the DC capacitance of the line [48]; L_0 is found in a similar way, whereas C is obtained from CL_0/L_0.

To complete the extraction, $\tan\theta_{eff}$ is obtained from:

$$\tan\theta_{eff} = \frac{\mathrm{Im}(\gamma^2) - CK_R\omega^{n+1}}{CL_0\omega^2 + CK_R\omega^{n+1}} \tag{2.14}$$

Fig. 2.8 shows the extracted parameters, which allow to accurately representing γ as shown in Fig. 2.9. This figure also shows the curves for $\alpha_c = K_1 f^n$ and $\alpha_d = K_2 f$, as well as the crossover frequency f_θ, which is the frequency at which $\alpha_c = \alpha_d$. As is well known, f_θ is dependent not only on the material properties but also on the structure and dimensions of the TLs. Analytically, f_θ can be calculated as:

$$f_\theta = \left(\frac{K_1}{K_2}\right)^{1/(1-n)} \tag{2.15}$$

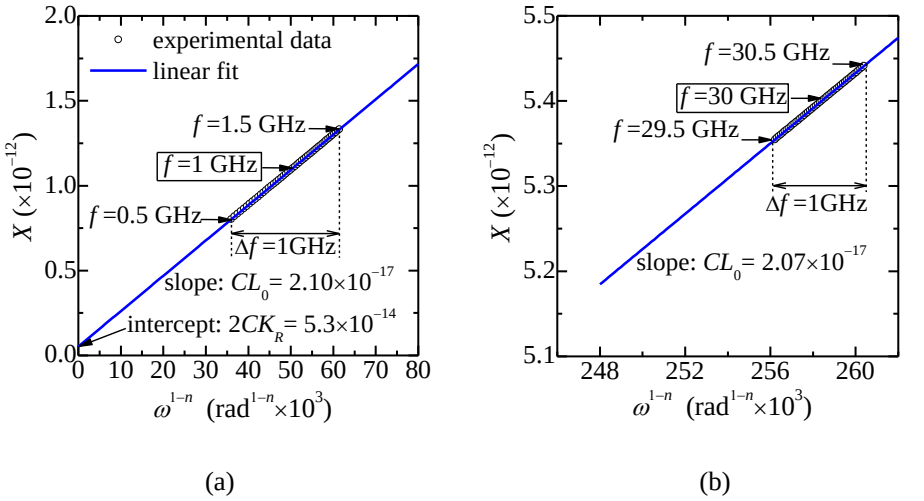


Fig. 2.7 Determination of CL_0 at: (a) f = 1 GHz, and (b) f = 30 GHz.

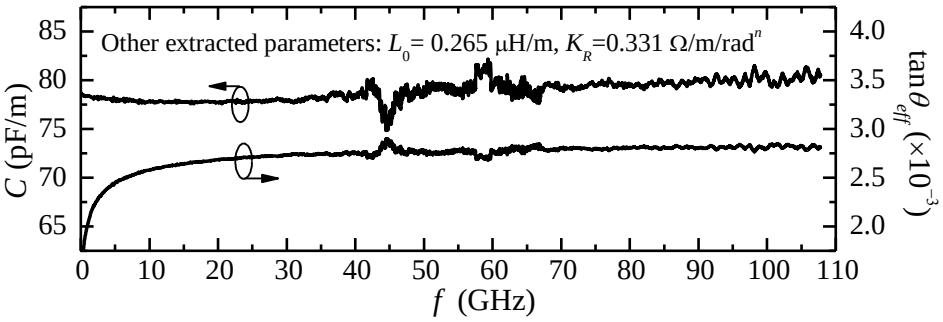


Fig. 2.8 Extracted parameters for implementing the *RLCG* model.

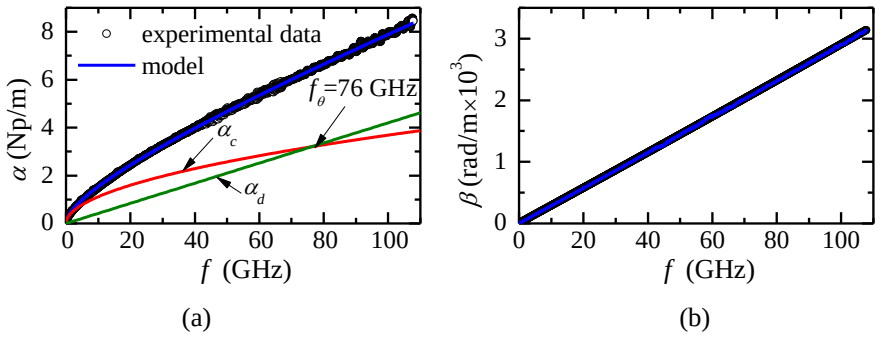


Fig. 2.9 Simulation-experiment comparison for: (a) α, and (b) β.

Notice that other than the experimental γ, no additional data is required for applying the proposed method. This is convenient because the accurate determination of Z_0 at high-frequencies represents a challenge [49]. Hence, we propose obtaining $Z_0 = \sqrt{Z/Y}$ using (2.9)–(2.11) and the extracted parameters. Fig. 2.10 shows the corresponding result, where the fluctuations introduced by the effect of the pad parasitics are not observed. Finally, R is plotted versus f in Fig. 2.11 using (2.9) and $n = 0.52$. As can be seen, R is about 10% higher when compared with the model obtained assuming $n = 0.5$ and carrying out the parameter extraction using data up to

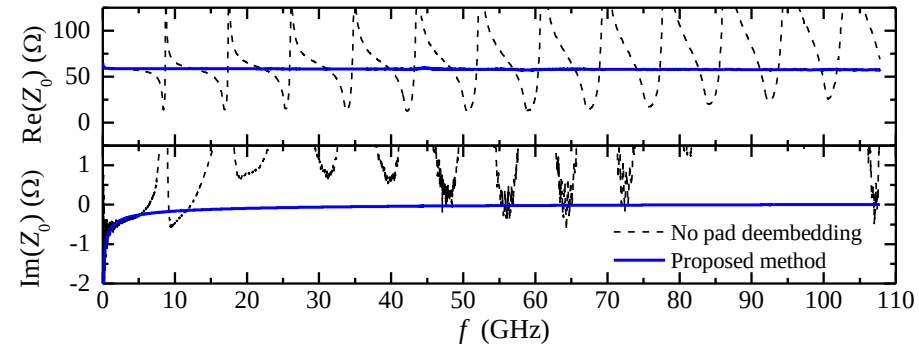


Fig. 2.10 Comparison between Z_0 obtained using the extracted parameters and directly obtained using the data of the fabricated line with l=12.7μm [49].

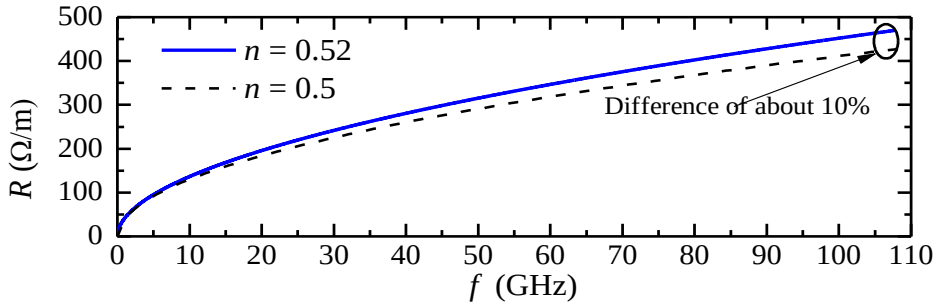


Fig. 2.11 Simulated R curves assuming n = 0.5 and n = 0.52 in the model for α.

20 GHz. This result points out the importance of considering additional effects in α_c when implementing wideband TL models [50].

To finalize this section, it is necessary to summarize that PCB interconnects are so large to allow neglecting R_0. Therefore, for PCB TLs the series resistance is only considerable at frequencies so high that the skin effect reduces the area of the cross section of the metal line where the current is flowing. This can be seen as an advantage since the model is simplified. Nevertheless, it was also mentioned and demonstrated that the roughness presented by PCB lines may be comparable to the skin depth at microwave frequencies, requiring to represent the losses with modified expressions that differ from the typical $\alpha_c \propto f^{0.5}$ representation.

2.3 On-chip interconnects

This part of the chapter is dedicated to the TLs on semiconductor substrates. In contrast to PCB lines, on-chip planar interconnects do require to consider R_0, which is due to the high resistance associated with the small cross section of the metal traces. This complicates the modeling to some extent; furthermore, substrate losses may also considerable impact the series elements of the lines. Conversely, an important simplification is also observable for on-chip TLs, which is that the metal traces are smooth for all practical purposes within the microwave frequency range. This allows for the application of the $\alpha_c \propto f^{0.5}$ representation without adding any other term. Based

on this physically justified assumptions, the following presents a methodology to implement a model for on-chip TLs.

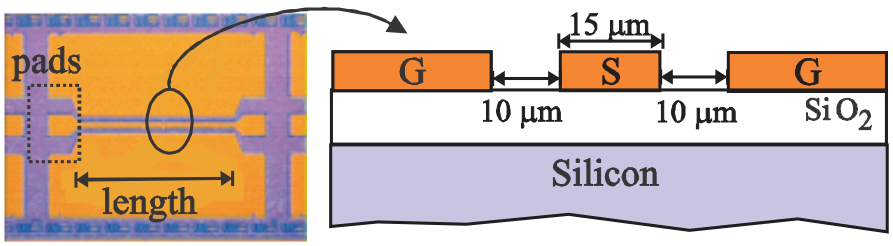
As mentioned in the previous paragraph, the losses occurring at the substrate impact the integrity of signals propagating through IC interconnects. For this reason, research focused on analyzing interconnects as TLs on lossy semiconductor substrates have been presented using data in the frequency domain [47, 51-52]. However, these proposals either require precise knowledge of the TL geometry and material properties [51] or involve curve fitting at frequencies where the experimental data typically present considerable noise [52]. Moreover, the *f*-dependent model parameters used in these proposals complicate time (*t*)-domain simulations in SPICE-like tools.

Although there are approaches for modeling TLs in the *t*-domain, these use Fourier analysis that requires special considerations to be implemented in circuit simulators [47], are limited in bandwidth [53], or require optimization routines to determine the model parameters [54]. In order to overcome the drawbacks of previous approaches, this project also contributes developing a method to characterize and model TLs on silicon, which is based on processing per-unit-length γ and Z_0 data. Once the TLs are fully characterized in the frequency domain, *f*-dependent effects are modeled using a combination of *f*-independent circuit elements that allow for the performance of simulations in the *t* domain in a simple and direct way. The proposed modeling and parameter extraction strategy are verified up to 30 GHz, causal results are obtained in the time domain for a rise time (t_r) as small as 12 ps.

2.3.1 On-wafer prototypes

In order to show the development and verification of the proposal, CPWs of several lengths (from 250 to 6400 μm) were fabricated on an RFCMOS process. These TLs were formed with aluminum on field oxide grown on a p-type silicon substrate with a 20-Ω·cm resistivity. The dimensions of the structures and an equivalent circuit model for a section with length Δl are depicted in Fig. 2.12(a) and (b), respectively. Notice that similarly to the PCB case, pads are included to measure *S*-parameters using GSG probes. In this case, however, the probes present a 150-μm pitch. A VNA setup at INAOE's Microwave Laboratory was calibrated by applying an off-wafer LRM algorithm and an ISS. Once the CPWs were measured, γ and Z_0 were obtained as in [54] to remove the pad parasitics from the measurements. Subsequently, the experimental data for the per-unit-length *RLGC* elements in the conventional model of

(a)



(b)

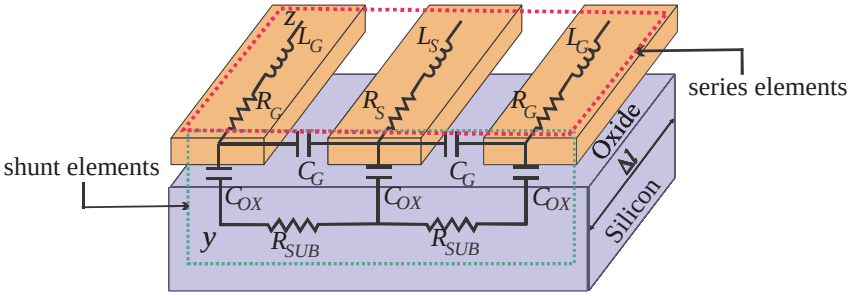
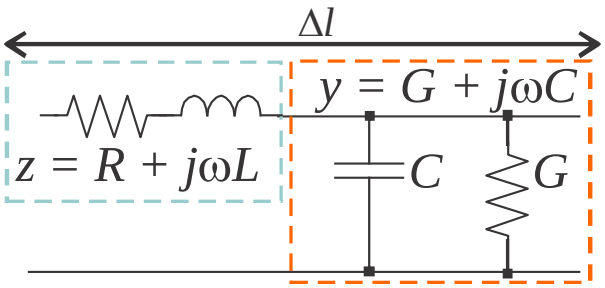


Fig. 2.12 Sketch of the fabricated CPWs: (a) micrograph and cross section detailing dimensions, and (b) equivalent circuit model for a homogeneous section of a line with length Δ*l*.

(a)



(b)

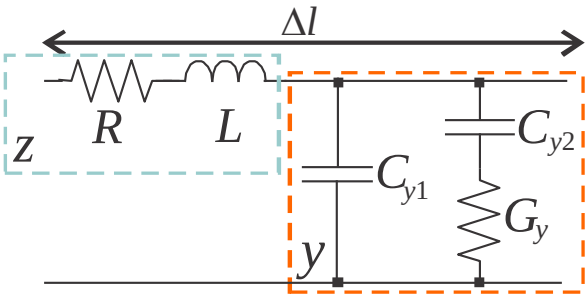


Fig. 2.13 Models for representing a CPW: (a) conventional model, and (b) alternative representation where *y* is modeled with elements independent.

a TL in Fig. 2.13(a) were calculated as $R = \mathrm{Re}(\gamma Z0)$, $L = \mathrm{Im}(\gamma Z0)/2\pi f$, $G = \mathrm{Re}(\gamma/Z0)$, and $C = \mathrm{Im}(\gamma/Z0)/2\pi f$.

2.3.2 Model development

In Fig. 2.12(b), several capacitances and conductances represent the shunt elements in a CPW on silicon. However, assuming symmetry with respect to the signal trace, this model can be simplified to the alternative form shown in Fig. 2.13(b), which is similar to that used for GSG probing pads [55]. The advantage of this model,

when compared with the model in Fig. 2.13(a), is the fact that C_{y1}, C_{y2}, and G_y are independent of f at microwave frequencies [52], simplifying the analysis as shown hereafter. The series elements R and L are strongly impacted by the f-dependent distribution of the current on the cross section of the metal lines, which is associated with the skin effect. In this case, an appropriate representation is achieved using [47].

$$R = R_0 + K_R\sqrt{f} \tag{2.16}$$

$$L = L_0 + \frac{K_R}{2\pi\sqrt{f}} \tag{2.17}$$

Since R_0, K_R, and L_0 are constant in f, simple data regressions can be used to implement (2.16) and (2.17) for the fabricated CPWs. For the case of the shunt elements, G_y, C_{y1}, and C_{y2} are related to G and C in the conventional model through

$$G = AG_yC_{y2}^2(2\pi f)^2 \tag{2.18}$$

$$C = C_{y1} + A \tag{2.19}$$

with $A = 1/(G_y^2 + C_{y2}^2(2\pi f)^2)$. In this case, the f-independent C_{y1}, C_{y2}, and G_y are obtained as for GSG probing pads [54].

Even though (2.16)–(2.19) allow to accurately reproduce the experimental *RLGC* parameters, the terms including K_R in (2.16) and (2.17) do not present a circuit equivalence using f-independent elements, which complicates the corresponding implementation in SPICE-like tools for performing t-domain simulations. Hence, several approaches to approximately represent the dependence of R and L on f using equivalent circuits [53-54] are available but require optimization techniques to obtain the corresponding parameters. Thus, the parameter-extraction method proposed here is based on a systematic procedure that involves simple data regressions, which allows a circuit-model implementation in a direct and simple way.

The selected model to represent R and L is shown in Fig. 2.14, where the f-dependent terms in (2.16) and (2.17) are approximated through the series connection of several blocks of resistors (R_i) and inductors (L_i) in parallel. In this case, the number of required blocks increases as the range of frequencies to be considered becomes wider. For the fabricated CPWs, three blocks were used, achieving good accuracy up to 30 GHz. More details on the determination of the number of blocks

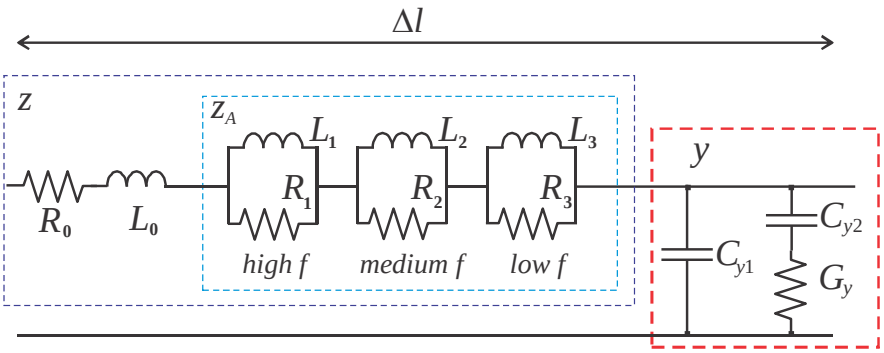


Fig. 2.14 TL model representing *R* and *L* using *f*-independent elements.

needed for higher frequencies are given hereafter. The parameter extraction starts removing the *f*-independent terms R_0 and L_0 from the series impedance of the CPW (i.e. *z*), resulting in the following impedance:

$$z_A = z - (R_0 + j\omega L_0) = (R - R_0) + j\omega(L + L_0) \tag{2.20}$$

which includes only the *f*-dependent terms in (2.16) and (2.17). In this case, each one of the blocks in Fig. 2.14 allows to represent z_A in different *f* ranges. The following step consists of determining the resistance and inductance associated with each block, starting with R_1 and L_1. Hence, assuming that the parallel connection of these elements approximately represents z_A at high frequencies, the following approximation can be used:

$$\frac{1}{z_A} \approx \frac{1}{R_1} - \frac{j}{2\pi f L_1} \quad \text{for } f \gg 0 \tag{2.21}$$

In practice, the experimental $\mathrm{Re}(1/z_A)$ approaches a constant value at high frequencies, which allows to determine $1/R_1$, as shown in Fig. 2.15. Likewise, this figure shows the value determined for L_1 when plotting $-1/\,2\pi\, f\, \mathrm{Im}(1/z_A)$ versus *f*. Afterward, the effect of R_1 and L_1 is removed from z_A, resulting in the following impedance:

$$z_B = z_A - (R_1 + j2\pi f L_1) \tag{2.22}$$

which represents the *f*-dependent terms in (2.16) and (2.17) at medium and low frequencies. Thus, when plotting $1/\mathrm{Re}(z_B)$ versus *f*, a constant value is observed at medium frequencies, which correspond to those just below the range where the effect of R_1 and L_1 is dominant in the total *f*-dependent series impedance. From this constant value, $1/R_2$ is determined. Similarly, L_2 is obtained when plotting $-1/2\pi f\mathrm{Im}(1/z_B)$ versus *f* at these frequencies.

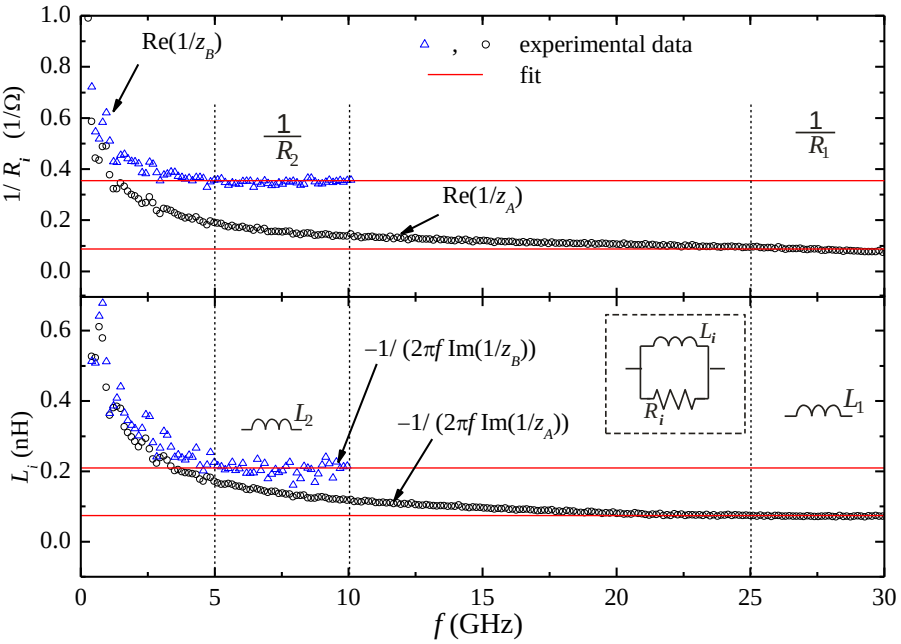


Fig. 2.15 Extraction of the inductances and resistances for the blocks representing the *f*-dependent terms of *z* at medium and high frequencies.

These extractions are shown in Fig. 2.15. A third impedance z_C can be defined to represent the *f*-dependent terms of the series impedance at low frequencies. In fact, subsequent impedances can be defined to extract the parameters of additional blocks until the whole *f* range of interest is covered. Fig. 2.16 shows a model–experiment confrontation in the *f* domain when applying (2.16)–(2.19) and when using the circuit in Fig. 2.14 in HSPICE after obtaining the corresponding parameters with the proposed method.

For assessing the accuracy of these models, the feature selective validation (FSV) can be applied [56-57]. In this case, the total amplitude difference measure (ADMt) can be computed, which is a figure that provides the goodness of fit between two data sets. In fact, when ADMt < 0.1, a model is considered as excellent [56]. Regarding the models in Fig. 2.16 for *R*, for the one that directly uses (2.16)–(2.17), ADMt = 0.034, whereas for the *f*-independent model in Fig. 2.14, ADM = 0.081. Thus, both of them are considered as excellent, and similar results are obtained for *L*. Notice also that Fig. 2.16 includes the curve corresponding to a simulation after including a fourth block. Even though more accuracy (e.g., ADM = 0.035 for *R*) is obtained, considering a tradeoff between accuracy and simulation time might be necessary for implementing the model, particularly for circuits including many interconnects.

2.3.3 Model implementation

A common practice for analyzing the response of a TL in the *t* domain is obtaining the corresponding transfer function from *f*-domain data using an inverse fast

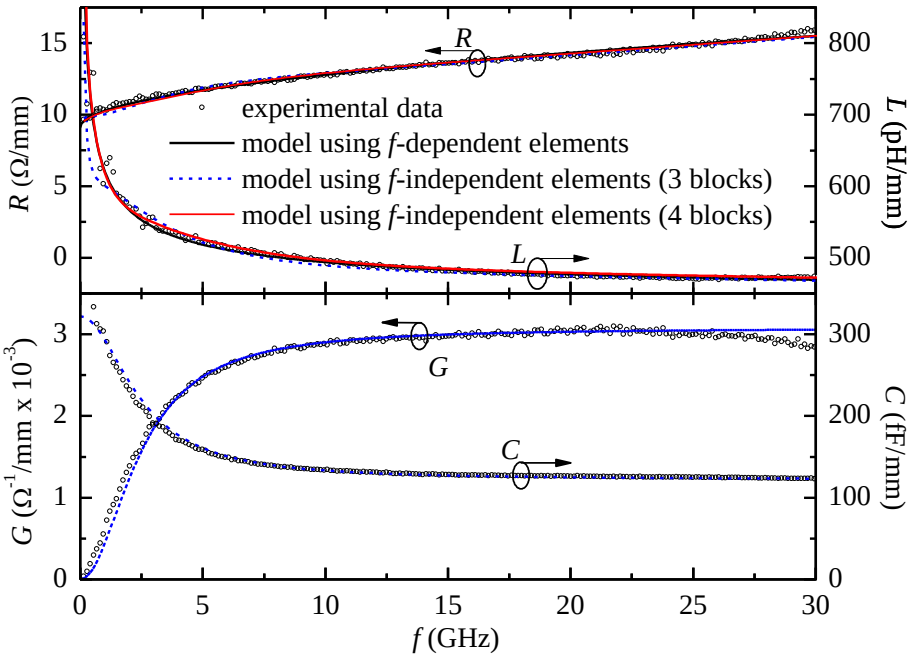


Fig. 2.16 Curves showing the model–experiment correlation for *R*, *L*, *C*, and *G*.

Fourier transform (iFFT). For the TLs analyzed here, these *f*-domain data can be defined using either of the following:

1) Experimental *S*-parameters

2) The circuit shown in Fig. 2.13(b).

For the latter case, basic TL-theory concepts are used to obtain the minimum number of *RLGC* blocks in cascade for representing a line of a given length. In accordance to [58], it can be demonstrated that using data up to 30 GHz presenting *f* steps of 150 MHz allows for the representation of signals with t_r as small as 12 ps propagating in lines with a delay time as long as 6.6 ns. Following these guidelines, a model to perform *t*-domain simulations was implemented in Agilent's ADS simulator directly using the experimental *S*-parameters of the CPWs and *f*-domain data generated using the model in Fig. 2.13(b). It is important to point out that this simulator applies a causality enforcement algorithm to obtain realistic results. Even though the previously described simulations allow us to obtain causal results, a model to directly perform *t*-domain simulations using a circuit containing only *f*-independent elements is desirable. This is because this type of circuit is compatible with SPICE-like tools. Thus, a model based on the circuit shown in Fig. 2.14 was implemented in HSPICE to perform simulations that can be compared to the ones obtained using iFFT.

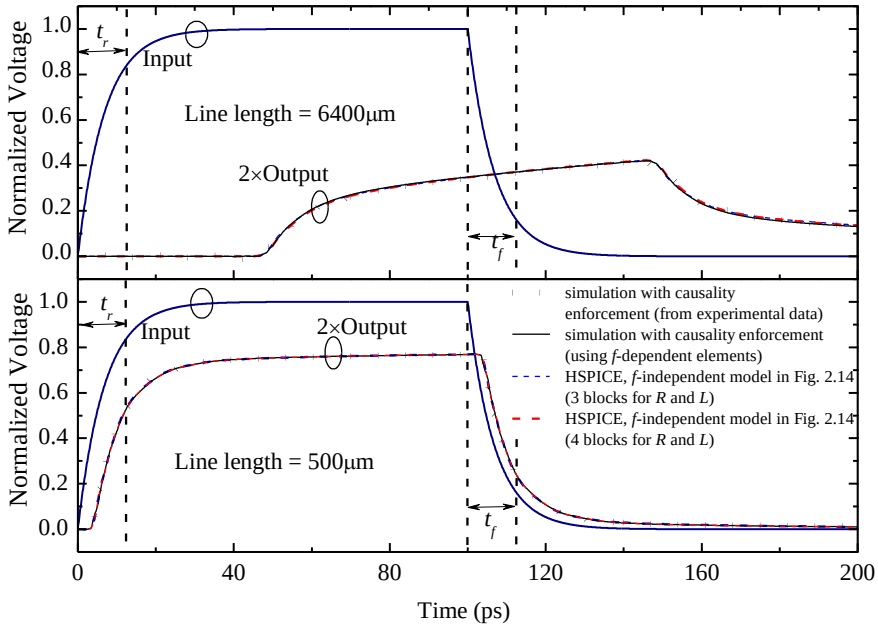


Fig. 2.17 Waveforms in the *t* domain obtained using the model in Fig. 2.14 and using commercial simulators applying iFFT and a causality correction.

As noticed in Fig. 2.17, the waveforms at the output of two lines presenting different lengths were obtained when a pulse voltage with t_r = 12 ps was applied at the input terminals. After performing an FSV analysis, it is observed that excellent agreement between the obtained waveforms with the model in Fig. 2.14 and when using the simulations involving iFFT of *f*-domain data is achieved (i.e., ADMt < 0.1 in all cases). The agreement is due to the accurate modeling of the *RLGC* elements implementing the model in Fig. 2.14 using the proposed extraction method up to 30 GHz [59].

2.4 Chapter conclusions

This chapter focused in analyzing planar interconnects on-PCB and on-chip. The main differences in the modeling, as well as the physically-based simplifications required to keep the model implementation straightforward were also discussed. For the case of PCB interconnects, a method to obtain the attenuation model parameters for PCB transmission lines has been presented and demonstrated up to 110 GHz. The method allowed the implementation of a model for the fundamental parameters of a transmission line.

For the case of on-chip interconnects a model was developed to perform simulations in SPICE-like programs. The accuracy achieved in this case is in part due to a simple extraction methodology that allows to obtain the model parameters in a simple and direct way. Moreover, the model bandwidth can be extended to higher

frequencies when including more elements in the equivalent circuit and performing subsequent extractions using the proposed methodology. It has been verified that this model also allows to obtain waveforms in the time domain that accurately reproduce those obtained with commercial software that applies frequency-to-time-domain transform techniques. Moreover, since this methodology uses experimental data involving γ and Z_0, all the physical effects influencing the electrical characteristics of the TLs are adequately taken into consideration, including the substrate losses occurring in CMOS technologies.

CHAPTER 3
Measurement-Based Modeling of On-Chip Devices

IN SPITE THAT all the integrated circuits start with just sand, prototyping ICs is extremely expensive, the cost reaches thousands of dollars per wafer in current technologies. For that reason, circuit designers must optimize the wafer space. Thus, considering that characterizing and modeling circuits and devices is a crucial part in the development of electronic products, test chips must be carefully designed, where the IC is disassembled into components like a Leggo puzzle; this is required to verify the proper operation of each part of the IC. In this case, a chip test is divided into different sections that typically include: transistors, transmission lines, passive devices, sub-circuits, and the actual design. Unfortunately, much die space may be taken by test structures, which is represent an important concern when carrying out RF characterizations where requires deembedding and calibration dummies for correcting the experimental data from the text fixture parasitics. Hence, a usual way to optimize the die space by the circuit designers is to reduce the number of deembedding structures, many times at the cost of reducing the accuracy of the measured data. Therefore, analytically determining the accuracy and validity of the experimental data collected to on-chip devices is necessary to be able to determine the minimum set of structures required to carry out an appropriate modeling and characterization.

In this chapter, the description of the necessary procedures to characterize on-chip DUTs from S-parameter measurements is revised by pointing out the purpose of each one of the structures required to consider the test-fixture parasitics. This is necessary because removing all the external effects negatively impacting the experimental data is mandatory to carry out a realistic and useful analysis of passive and active devices. For this reason, several aspects regarding the concepts of calibration techniques, the systematic errors associated with the measurement equipment are qualitatively and quantitatively revised here. In addition, concepts to bear in mind in the design of the deembedding structures are revised as well as the way the results are affected when not appropriately accounting for the test fixture effects.

In order to show a practical example of the application of a measurement-based characterization and modeling technique using RF measurements appropriately deembeded, this chapter includes the full analysis of an on-chip inductor using a model proposed here. The corresponding parameter determination is also shown demonstrating that an accurate representation of this type of devices can be carried out

in a simple and straightforward way when carefully collecting, correcting, and processing experimental RF data.

3.1 Calibration

As pointed out before in this thesis, modeling and characterizing the high-frequency behavior of semiconductor devices on-wafer require reliable experimental data, which is achieved by measuring S-parameters using a VNA. When using this equipment, it is necessary to bear in mind that systematic errors are always introduced [60], which adds uncertainty to the measurements. Fig. 3.1 depicts a typical setup used for measuring S-parameters to on-wafer and on-chip devices. As can be seen, cables, connectors, and other electrical transitions are used to interconnect the equipment with the DUT. In fact, the systematic errors are related to the port mismatches and other parasitic effects occurring in the electrical path from the VNA to the DUT. In this context, the calibration technique is the characterization and elimination of systematic errors, through the measurement of several standard structures with given electrical characteristics that are at least partially known (e.g., it is necessary to know the type of termination). The calibration procedure is typically performed by using data measured off-wafer to an impedance-standard-substrate (ISS) provided by the probe manufacturer [61], among the typical standards structures are: SHORT, OPEN, LOAD, LINE and THRU. Thus, depending on the type of calibration is different the

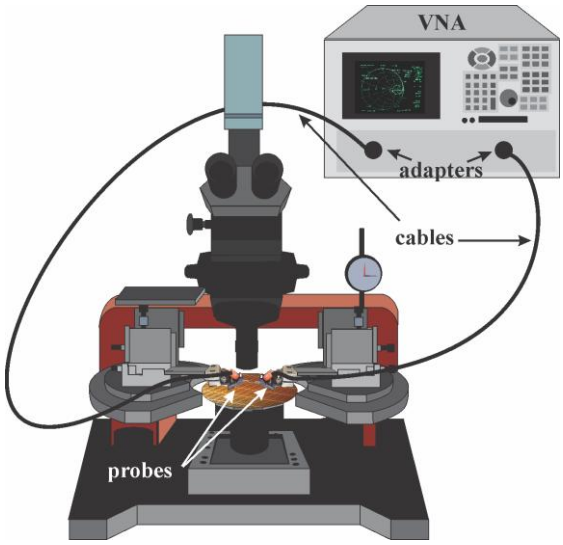


Fig. 3.1 Sketch showing a typical VNA setup for measuring on-wafer S-parameters.

set of structures that is necessary to measure. The most popular calibration technique is the so-called Short-Open-Load-Thru (SOLT) [62], whereas alternative calibration techniques are Line-Reflect-Match (LRM), and Thru-Reflect-Line (TRL) [63-64], that require LINE, REFLECT, MATCH and THRU standards. So, the selection of the most appropriate calibration technique for particular structures are dependent upon the measurement bandwidth.

At this point, it is clear that to obtain accurate and realistic S-parameters of any DUT when using a VNA, it is necessary to eliminate the systematic errors using calibration technique that shifts the measurement reference plane closer to the DUT [63]. Ideally, this reference plane must "see" only the DUT so that the experimental data contain only information about the desired device. Fig. 3.2 shows a sketch illustrating the calibration reference plane for the case of a two-port setup for measuring S-parameters using coplanar RF probes. This plane can be shifted even closer to the DUT using a deembedding technique, which is explained in the following section.

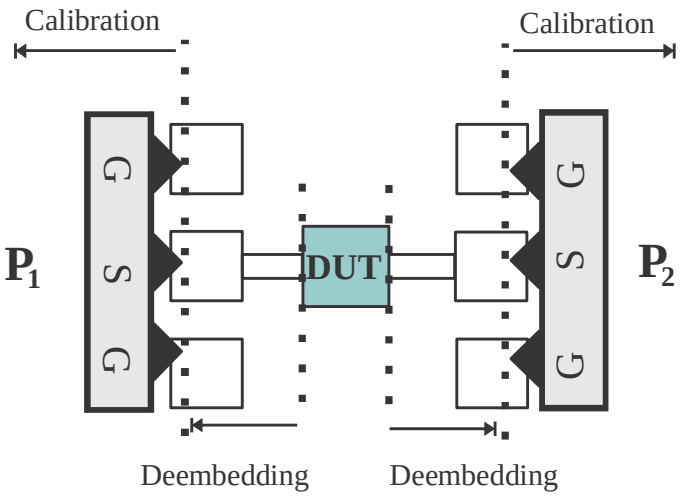


Fig. 3.2 Sketch depicting calibration and deembedding planes when measuring using coplanar probes (the arrows indicate what is removed after each one of these procedures is applied).

3.2 Deembedding

When performing on-wafer measurements, the error correction algorithms are categorized into two types: calibration and deembedding procedures. In essence, these two types of procedures are used with the same purpose. However, the term "calibration" is used to refer to the procedure that removes the systematic errors associated with the measurement equipment up to the probe tips [61, 65], as explained above. On the other hand, a "deembedding" procedure is that used to remove the effects associated to the on-wafer interconnects that serve as interface between the DUT and the probes, such as transmission lines, pads, vias, etc. For clarifying the

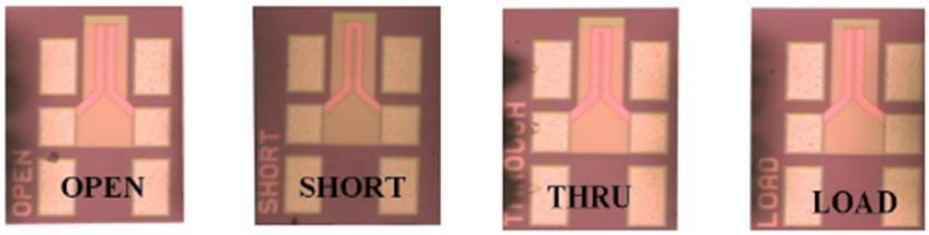
difference between these two procedures, Fig. 3.2 shows the measurement planes after performing calibration and deembedding of measured two-port network parameters.

For carrying out a deembedding of experimental data, measuring on-wafer dummy structures additional to the desired structure is needed [66, 67]. Unfortunately, these dummy structures take precious space from the die, which increases the corresponding cost and in many cases is not available. For this reason, it is desirable to use the minimum number of these structures when correcting the measurements for the pad parasitics. In fact, this is the main reason why the one-step deembedding is still very popular for removing the effect of these parasitics [68] since only a single 'open' dummy is required. However, this deembedding does not appropriately account for the effect of the series parasitics associated with the pads and other on-wafer interconnects outside the DUT, introducing errors in the collected data. For this reason, several deembedding procedures have been proposed in recent years, [66, 69-70].

Notwithstanding the advances in the development of deembedding procedures, an analysis that allows to determine the conditions at which using only one dummy structure (together with a one-step deembedding) is enough for correcting the pad parasitics in on-wafer measurements is not available. Hence, this analysis is important for designers that are limited in die space and for those measuring at relatively low frequencies.

3.2.1 Prototypes for deembedding analysis

Here, two different deembedding approaches are analyzed by processing measurements up to 30 GHz. It is thus the purpose of this analysis to allow the designer to take informed decisions about the structures strictly required in the test-chip to perform either one- or two-step (including a 'short' dummy) deembedding procedures.
In order to carry out the analysis from experimental data, test structures were fabricated on an RFCMOS process. These structures are named: 'open' (open circuit at both ports), 'short' (short circuit at both ports), 'load' (a broadband 50-Ω load interconnecting the signal pads of port-1 and port-2), and 'thru' (a line of negligible length interconnecting port-1 and port-2). The pads in these structures were formed with aluminum on field oxide (silicon dioxide SiO_2) grown on a p-type silicon substrate with 20-Ω·cm resistivity. Fig. 3.3 shows the corresponding micrographs. It is important to mention that these pads are shielded from the substrate by means of a metal layer formed at a low metal level (i.e., a ground shield). This is a common practice in modern test chips since it reduces the negative impact of the substrate losses in the measurements.



(a) (b)

Fig. 3.3 Micro-photographs of fabricated structures for analyzing the one and two-step deembedding methods: (a) dummy structures for deembedding, (b) test structures for verification.

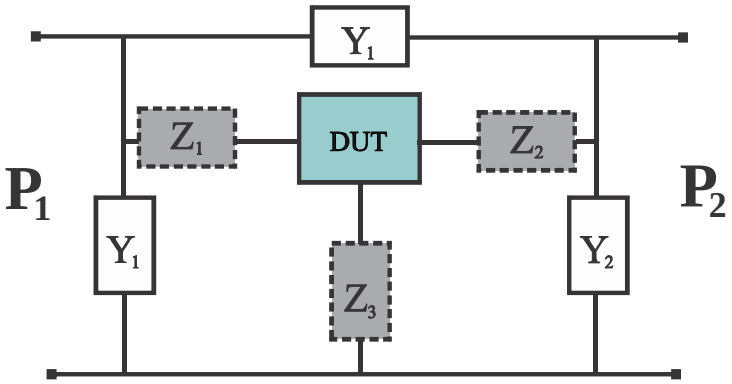


Fig. 3.4 Model representing the DUT embedded between the parasitic effects associated with the pad structures.

In addition, the pads are designed to measure *S*-parameters using GSG probes with a 150-µm pitch. To perform the measurements, a vector network analyzer setup was calibrated up to the probe tips by applying an off-wafer LRM algorithm and an ISS. These measurements are used throughout this work to analyze the differences between the one-step deembedding (1SD) that uses only an open structure and the two-step deembedding (2SD) that uses an open and a short.

3.2.2 Reviewing the 1SD and 2SD procedures

Fig. 3.4 shows the model of a DUT embedded between a test-fixture consisting of pads and other interconnects. In this case, the parasitic effects associated with the test fixture are represented by means of generic admittance and impedance blocks. The admittance blocks account for the shunt parasitics associated with the capacitors formed between the pads and the ground shield, whereas the impedance blocks take into account the series parasitics associated with the finite resistance of the pads and other interconnects. As is well known, all these parasitics must be removed from the measurements so that the experimental data correspond to the DUT. Thus, to eliminate these effects, a deembedding technique is performed as explained hereafter.

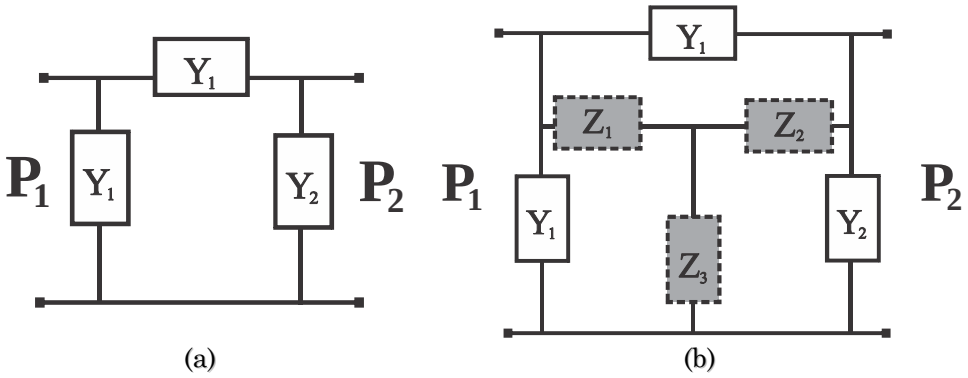


Fig. 3.5 Models that represent the: (a) 'open', and (b) 'short' structures.

The simplest deembedding procedure is 1SD. In this case, an open dummy structure is used, in which each one of the two pad-to-DUT interfaces is terminated with an open circuit, and the corresponding equivalent circuit is that shown in Fig. 3.5a. When comparing the models in Fig. 3.4 and 3.5a, it can be seen that the series impedances have no effect; thus, the *Y*-parameters associated with the DUT can be obtained by applying the following matrix operation:

$$Y_{DUT\_1SD} = Y_{RAW} - Y_{OP} \tag{3.1}$$

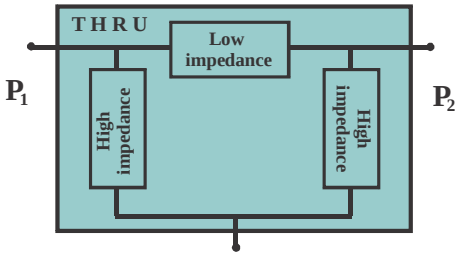
where the subscripts *RAW* and *OP* are used to distinguish the parameters associated with the raw measurements (i.e., those including the test fixture effects), and those corresponding to the open structure, respectively.

Since the series parasitics are avoided in the 1SD, some errors are still present. For this reason, the 2SD was developed. In this case, the deembedding process requires the measurement of the open and short structures. Thus, considering that the short structure can be represented using the model shown in Fig. 3.5b, the *Y*- parameters associated with the DUT are now obtained by means of:

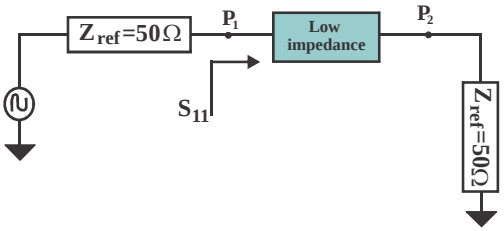
$$Y_{DUT\_2SD} = \left[[Y_{RAW} - Y_{OP}]^{-1} - \left[{Z_{SH}}^{-1} - Y_{OP} \right]^{-1} \right]^{-1} \tag{3.2}$$

where the matrix Z_{sh} represents the experimental *Z*-parameters associated with the short structure.

From (3.1) and (3.2) it is clear that the matrix operations used in both deembedding procedures are simple and can be easily implemented in any software that allows data processing. Thus, the reason why the 1SD could be preferred by microwave and device engineers is because it only uses one dummy structure. However, in this case, there is a penalty in accuracy which is discussed afterwards.

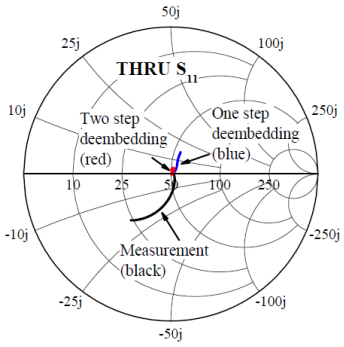


(a)

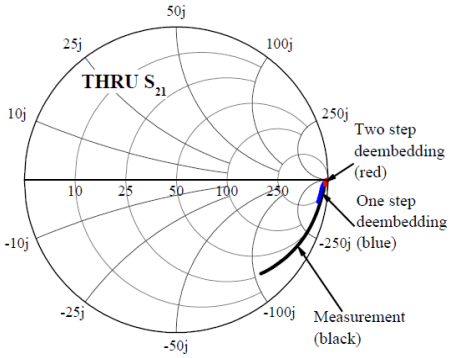


(b)

Fig. 3.6
(a) Model that represents the 'thru' structure.
(b) Model for obtaining S_{11} for the THRU.



(a)



(b)

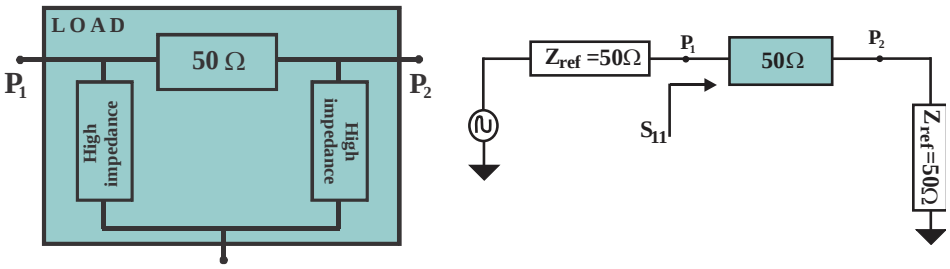
Fig. 3.7 (a) S_{11} for the THRU plotted in a Smith Chart up to 30 GHz, (b) S_{21} for the thru plotted in a Smith Chart up to 30 GHz.

3.2.3 Comparison between 1SD and 2SD using thru and load structures

For comparing the 1SD and 2SD procedures, the deembedded measurements corresponding to the THRU and LOAD structures were analyzed. Ideally, after deembedding the effect of the pads from the measurements of the THRU structure, the DUT corresponds to a very small line which ideally presents a series impedance equal to zero. A more realistic model, however, is that shown in Fig. 3.6a. Assuming that the parasitic capacitance to ground introduced by this small line is very small, the equivalent circuit model for obtaining the reflection parameter S_{11} is illustrated in Fig. 3.6b. In this case, an RF source with a reference impedance (in this case of 50 Ω) applies a signal to the port-1 and the port-2 is terminated with the same reference impedance. Since S_{11} is obtained as:

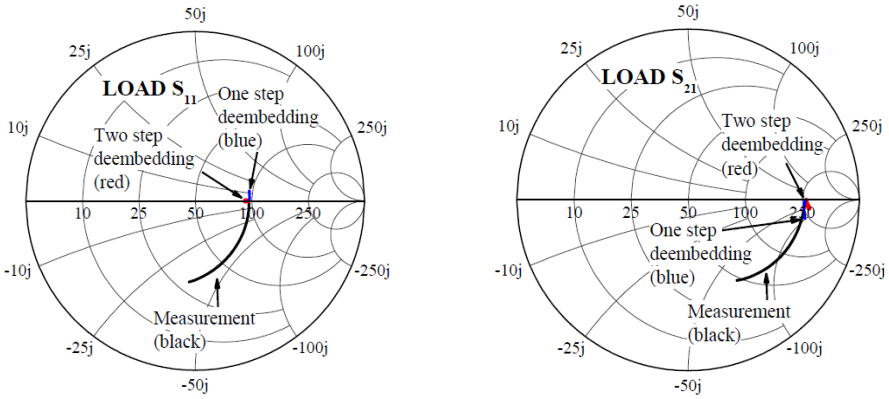
$$S_{11} = \frac{Z_L - Z_{REF}}{Z_L + Z_{REF}} \tag{3.3}$$

where Z_L is the sum of the low impedance associated with the THRU plus the reference impedance at port-2, then it is expected that the result approximately corresponds to a measurement in matched condition (corresponding to a point at the



(a) (b)

Fig. 3.8 (a) Model that represents the 'load' structures, (b) Model for obtaining S_{11} for the LOAD.



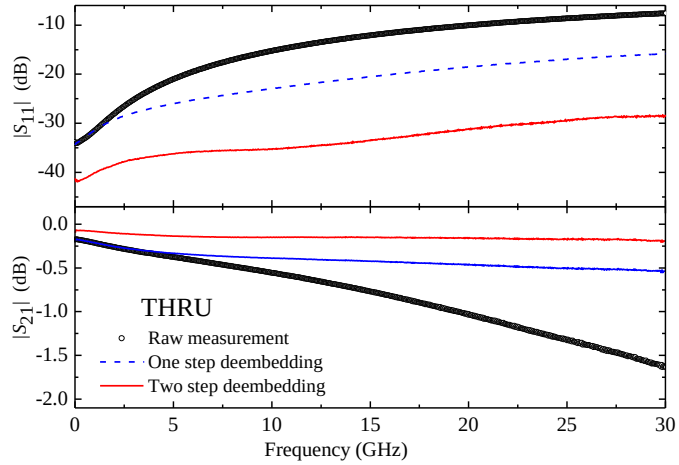
(a) (b)

Fig. 3.9 (a) S_{11} for the LOAD plotted in a Smith Chart up to 30 GHz, (b) S_{21} for the load plotted in a Smith Chart up to 30 GHz.

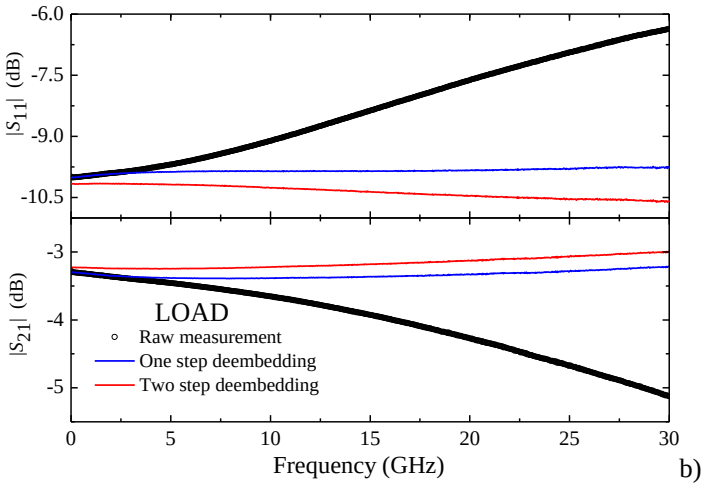
center of a Smith Chart). Fig. 3.7a shows that the raw measurements corresponding to S_{11} considerably differ from the ideal behavior of a THRU structure and these data show the considerable impact of the capacitive parasitics introduced by the pads. Once the 1SD is applied, the corrected data now presents noticeable inductive effects associated with the series parasitics, which are still not removed. In contrast, the 2SD also takes into consideration these series parasitics and the corresponding data approach the single point expected for an ideal THRU. This is not perfectly achieved due to the fact that the measured THRU still presents a finite series impedance as depicted in the model shown in Fig. 3.6a. Similar reasoning can be applied when analyzing the transmission S_{21} parameter of the THRU. In this case, it is ideally expected that the signal reaching port-2 is neither attenuated (i.e., $|S_{21}|\approx 1$) nor delayed (i.e. phase(S_{21})≈ 0) with respect to the signal applied at port-1. The data corresponding to this parameter are shown in Fig. 3.7b. Again, substantially better results are obtained using the 2SD procedure.

Now, for the case of the LOAD after removing the effect of the test fixture, the port-1 and port-2 are interconnected through a 50-Ω load. The corresponding equivalent circuit is that shown in Fig. 3.8a. Similarly to the case of the THRU, assuming that the parasitic capacitive coupling of the LOAD with the ground is

(a)



(b)



b)

Fig. 3.10 (a) Magnitude of the reflection and transmission parameters for the THRU structure up to 30 GHz, (b) Magnitude of the reflection and transmission parameters for the LOAD structure up to 30 GHz.

negligible, the equivalent circuit model for obtaining the reflection parameter S_{11} is that illustrated in Fig. 3.8b. Now, the RF source with a reference impedance applies a signal to the port-1, the signal travels through the LOAD and the port-2 is terminated with the reference impedance.

The representation of S_{11} for the LOAD in a Smith Chart is also very simple. Notice in Fig. 3.9a that the impedance seen at point P_1 by the RF source is 100 Ω, which can be mapped to the Smith Chart using (3.3) as $S_{11}\approx 1/3$. As in the case corresponding to the THRU, some inductive parasitics remain after performing the 1SD. However, in this case the difference is smaller since the impedance of the LOAD is considerably larger than that of the THRU. In other words, the error introduced in the deembedded data when applying the 1SD is lower for the LOAD than what it is for the THRU.

This will be explained with more detail in the following section. For completeness, Fig. 3.9b shows S_{21} for the LOAD, showing that the difference between

1SD and 2SD is less accentuated than that observed in Fig. 3.7b for the THRU. A final comparison is carried out in this section to point out the differences between the two studied methods when applied to DUTs with relatively low and high impedances. As mentioned before, 1SD neglects the series parasitics associated with the test fixture. These impedances are in the order of a few ohms and can be neglected when measuring the high-impedance DUTs; for instance, a MOS capacitor. Fig. 3.10 shows the magnitude of the reflection and transmission for the THRU and LOAD structures after performing 1SD and 2SD. Notice that the error is less than 0.5 dB up to 30 GHz in all cases (except for $|S_{11}|$ corresponding to the thru since the return loss is very low). However, the percentage of error is much bigger for the THRU since the insertion and return losses are considerably smaller than those associated with the LOAD. Thus, when measuring low impedance devices such as inductors or transistors, even at low frequencies it is expected to obtain erroneous data when only applying a 1SD procedure.

After, revising the de-embedding processes, it is pointed out the importance of bearing in mind the magnitude impedance presented by the DUT, as well as the frequency range at which the device is measured [71]. This may yield to optimizing die space while preserving data accuracy for developing an appropriate device model.

3.3 Applying RF-measurement techniques to modeling on-chip inductors

The concepts revised in previous sections can now be applied to a particular case of interest for microwave circuit designers: on-chip inductors. In this regard, modeling on-chip inductors at microwave frequencies is mandatory in today's IC technology; hence, an accurate deembedding process is fundamental for the development of the corresponding circuit model. This is due to the fact that current applications require accurate models for representing these devices at gigahertz frequencies [72-73]. Moreover, in addition to the challenge introduced by the high-frequency operation, the continuous shrinking of on-chip inductor's geometry tights the tolerance in the model accuracy when performing circuit simulations [74–76]. In this regard, even though alternative structures have been proposed to achieve better Q-factors in extremely compact spaces [77-78], the conventional inductor over a lossy silicon substrate is still the most cost-effective solution in CMOS technology [79]. For this reason, much research has been focused on developing methodologies for implementing high-frequency inductor models considering the undesirable substrate losses [71-80]. Unfortunately, when attempting to obtain the corresponding parameters from exact closed-form equations, the formulation becomes very complicated. Thus, some

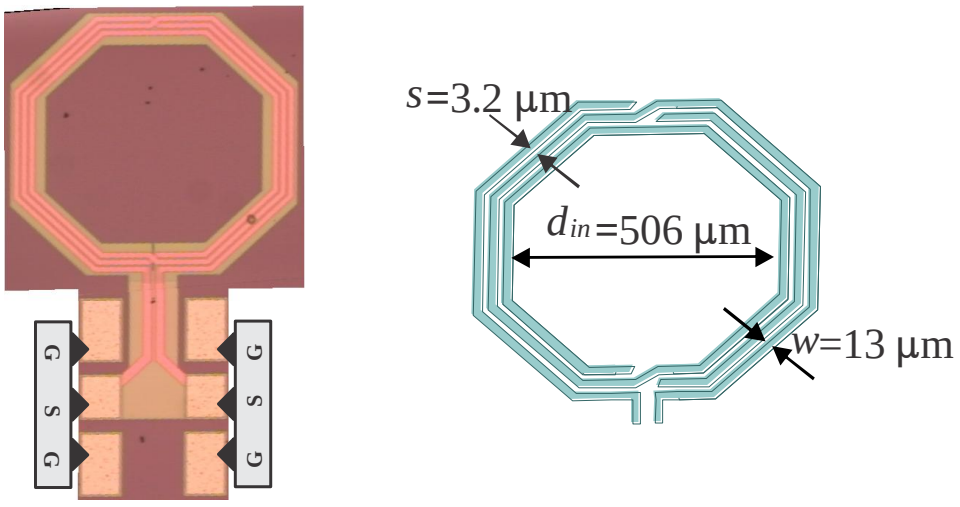
alternative simplified models and parameter extraction techniques are available. These approaches, however, either require precise knowledge of the fabrication process and geometry, or rely on optimization for determining the corresponding parameters.

Thus, in order to provide IC designers with an accurate model and parameter extraction to represent on-chip inductors while simultaneously considering the substrate losses at gigahertz frequencies, this section presents a useful strategy that allows a simple and straightforward implementation without significantly penalizing the accuracy. The approach is based on a systematic separation of the impedances that represent:

- The intrinsic device,
- The input-port substrate parasitic
- The output-port substrate parasitics.

3.3.1 Description of fabricated inductors

In order to show the development and verification of the proposal, a test chip fabricated on a RFCMOS process is available for measuring. A micrograph of an inductor used for the analysis presented here is shown in Fig 3.11a, whereas the corresponding dimensions are detailed in Fig. 3.11b. The device presents a symmetrical octagonal design with three turns, n = 3, it was formed by metal traces made of aluminum on the Metal-4 layer level (and crossing bridges at lower metal levels). The metal traces present a width w = 13 μm, and the spacing between adjacent turns is s = 3.2 μm. The inner diameter is d_{in} = 506 μm, and the outer diameter is d_{out} = 551.4 μm. Notice also in Fig. 3.11a that the inductor includes coplanar pads formed with aluminum; these pads are designed to measure *S*-parameters using GSG RF



(a) (b)

Fig. 3.11. (a) Micrograph showing the on-chip inductor, and (b) sketch detailing the corresponding dimensions.

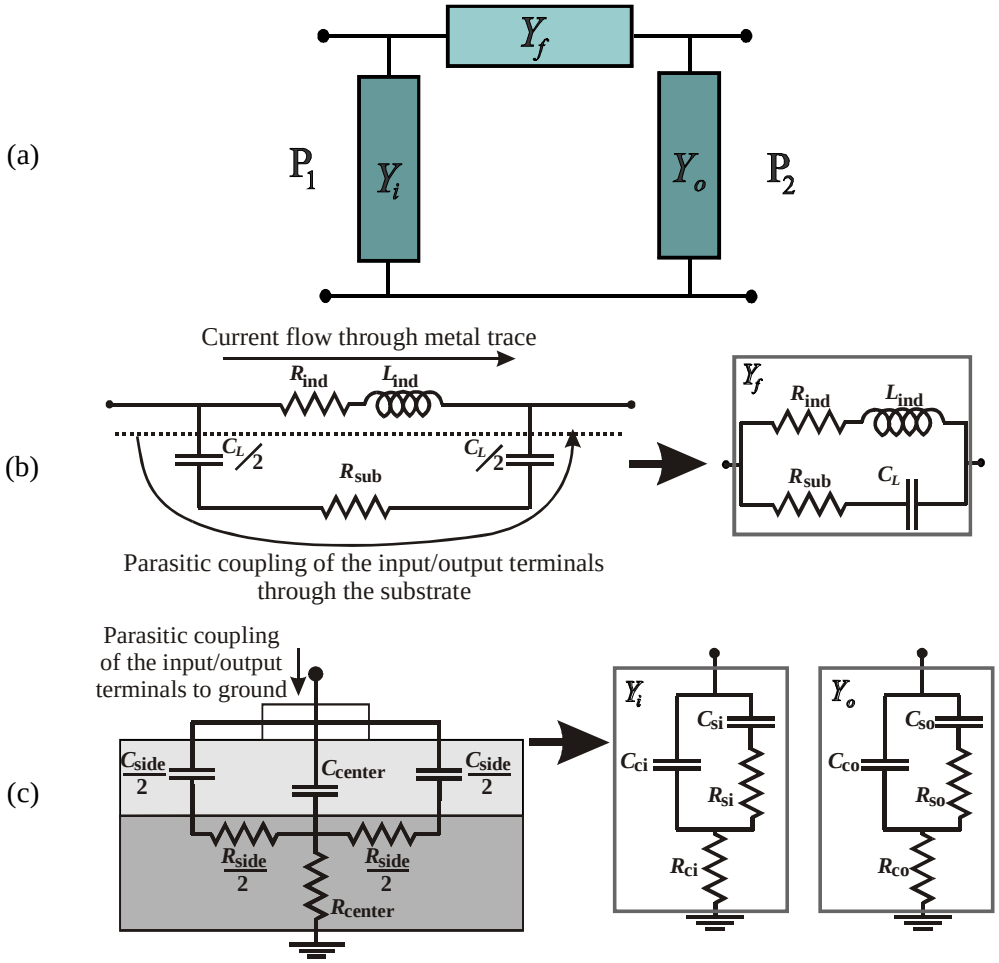


Fig. 3.12. (a) Block model representing the inductor as a two-port π-network, and equivalent circuit models for: (b) Y_f, and (c) Y_i and Y_o.

probes with a pitch of 150 μm. For this propose, a VNA setup was calibrated up to the probe tips by applying the LRM algorithm.

In addition to the inductor, two dummy structures are found within this test chip to allow the application of a 2SD, shown in Fig. 3.11a. The dummy structures were described and analyzed in the previous section of this chapter (Fig.3.3a). Using the *S*-parameters measured to the fabricated structures, it is possible to obtain the model parameters for the inductor in a systematic way as explained afterwards.

3.3.2 Formulation of the extraction method

Once the effect of the pads is removed from the measurements performed to the inductor, the device is modeled using the π-network shown in Fig. 3.12a. This model contains three admittance blocks representing the transmission between the input and output terminals Y_f, and the coupling of the input and output terminals to ground, Y_i and Y_o, respectively. The elements in the equivalent circuit for representing these admittances are explained hereafter. Fig. 3.12b shows the derivation of the circuit

model for Y_f. In this figure, the circuit at the left hand side includes the intrinsic inductance of the device (L_{ind}) and the series resis- tance (R_{ind}). In addition, this circuit presents a second branch to account for the current flowing from port-1 to port-2 through the substrate, where C_L is the effective inductor-to-substrate capacitance, and R_{sub} is the substrate resistance. Notice also that the equivalent circuit for Y_f can be simplified to that shown at the right hand side of Fig. 3.12b.

For the case of Y_i and Y_o, these admittances are associated with the direct current path from the input and output terminals to ground. Thus, an effective way to consider the corresponding effects is by means of the circuit shown at the left hand side of Fig. 3.12c, which includes distributed resistances and capacitances to represent the oxide and the finite resistance of the substrate, respectively. Since the fabricated inductor can be considered as symmetrical, it is expected that $Y_i \approx Y_o$. Nevertheless, it is reasonable to assume that some differences in these admittances occur because of variations in the layout. For this reason, even though the corresponding circuits for Y_i and Y_o are essentially the same (see Fig. 3.12c), different values for these elements might be found when carrying out the parameter extraction.

It is important to mention that the elements in the equivalent circuits in Fig. 3.12 take effective values that also include effects like the eddy currents occurring in the substrate, and the current within the metal trace [79]. Moreover, these effects influence the performance of the inductor at different frequency ranges. Thus, the methodology proposed in this thesis takes advantage of this fact to determine the values of the model parameters at different frequency ranges where the corresponding effect is accentuated.

To determine the values of the elements in the circuit model for Y_f, it is necessary to obtain the complex value of this admittance within the measured frequency range. In this case, the *S*-parameters are transformed to *Y*-parameters using basic circuit network theory and Y_f is obtained as:

$$Y_f = -Y_{12} \tag{3.4}$$

Now, observe that the circuit for Y_f shown in Fig 3.12b involves four unknown parameters, whereas (3.4) only provides two equations (i.e., those associated with the real and imaginary parts of Y_f). Hence, some considerations are necessary for obtaining these parameters. Previous research shows that the coupling of transmission line sections through the substrate is observed at relatively high frequencies [68]. Thus, the effect of R_{sub} can be ignored at low frequencies in the circuit in Fig. 3.12b. As explained later, for the studied inductor this frequency range is defined below a frequency of a few gigahertz. Therefore, at these frequencies it is possible to simplify Y_f to:

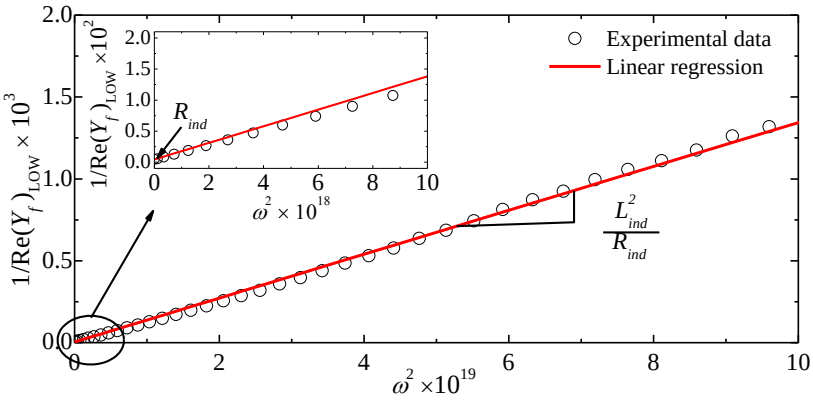


Fig. 3.13. Determination of the parameters in equation (3.7) in the frequency range: 0.2–1 GHz.

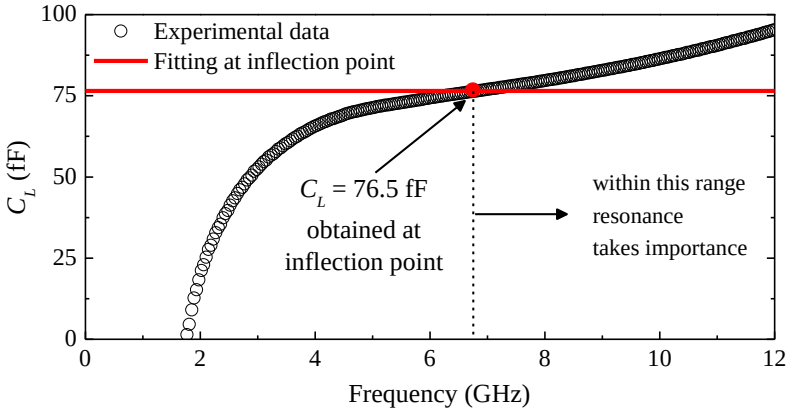


Fig. 3.14. Determination of C_L.

$$Y_f\big|_{\mathrm{LF}} \approx \frac{R_{ind}}{R_{ind}^2 + \omega^2 L_{ind}^2} + j\omega \frac{C_L R_{ind}^2 + \omega^2 C_L L_{ind}^2 - L_{ind}}{R_{ind}^2 + \omega^2 L_{ind}^2} \tag{3.5}$$

where ω is the angular frequency and $j^2 = -1$. Afterwards, (3.5) can be separated in real and imaginary parts. For the real part, the corresponding equation is:

$$\mathrm{Re}(Y_f)\big|_{\mathrm{LF}} = \frac{R_{ind}}{R_{ind}^2 + \omega^2 L_{ind}^2} \tag{3.6}$$

which can be rewritten in the form:

$$y_1 = \frac{1}{\mathrm{Re}(Y_f)\big|_{\mathrm{LF}}} = \frac{L_{ind}^2}{R_{ind}}\omega^2 + R_{ind} \tag{3.7}$$

Then, when applying a linear regression to y_1 versus ω^2 data, R_{ind} can be determined from the extrapolation to $\omega^2 = 0$, whereas L_{ind} is easily found by solving a simple equation involving the corresponding slope. The extraction of these parameters is illustrated in Fig. 3.13. Once the values for R_{ind} and L_{ind} are known, the following

step is determining the value of the effective inductor-to-substrate capacitance C_L. This capacitance is a parasitic effect that modifies the main frequency of resonance in the inductor, which implies that affects the *Q*-factor. C_L can be found by solving the imaginary part of Y_f in (3.5), which yields:

$$C_L = \frac{\mathrm{Re}(Y_f)\big|_{\mathrm{LF}}}{\omega} + \frac{L_{ind}}{R_{ind}^2 + \omega^2 L_{ind}^2} \tag{3.8}$$

Fig. 3.14 shows the experimental data associated with equation (3.8) plotted versus frequency. Notice that no constant value is observed since resonances occur at higher frequencies, which influences the trend of this curve, requiring the consideration of additional parameters and complicating the determination of C_L. Nevertheless, when obtaining the inflection point of this curve, it is possible to establish the maximum frequency at which $Y_f \approx Y_f|_{\mathrm{LF}}$ can be assumed. Thus, the constant function at this inflection frequency is C_L, which is illustrated in Fig. 3.14. At this point, the only unknown parameter to complete the extraction of the model for Y_f is R_{sub}. In this case, in accordance to the circuit in Fig. 3.12b, the imaginary part of Y_f can be expressed as:

$$\mathrm{Im}(Y_f) = \frac{\omega^2 C_L^2}{\omega^3 C_L^3 R_{sub}^2 + 1} - \frac{\omega L_{ind}}{R_{ind}^2 + \omega^2 L_{ind}^2} \tag{3.9}$$

Hence, R_{sub} can be solved from this equation, which yields:

$$R_{\mathrm{sub}} = \pm \frac{\sqrt{L_{ind}(C_L R_{ind}^2 + \omega^2 C_L L_{ind}^2 - L_{ind})}}{\omega L_{ind} C_L} \tag{3.10}$$

Since this is the solution of a second order equation, two possible values for R_{sub} are obtained. Obviously, the positive solution is the correct one for R_{sub}. Fig. 3.15 shows the positive and negative roots expressed in (3.10) for R_{sub}, clearly illustrating that this parameter is easily obtained. Fig. 3.16 summarizes through simplified circuits the assumptions made while developing the proposed methodology.

Now, in order to determine the values for the elements in the circuit model for Y_i and Y_o, it is necessary to obtain the complex value of these admittances. Likewise as for Y_f basic circuit network theory allows to calculate Y_i and Y_o from:

$$Y_i = Y_{11} + Y_{12} \tag{3.11}$$

$$Y_o = Y_{22} + Y_{12} \tag{3.12}$$

As explained before, the model proposed for Y_i and Y_o is essentially the same, and the process to obtain the corresponding equivalent circuit elements is identical for each port even though some little differences in these elements are expected. Here, the process for extracting the model parameters is focusing only in Y_i, to avoid redundancy.

Observe that the circuit for Y_i is shown in Fig 3.12c. In previous paragraphs, it was explained that the coupling of transmission line sections through the substrate is observed at relative high frequencies. Similarly, the effect of R_{ci} in the model for Y_i can be ignored at low frequencies. In this case, it is possible to simplify an expression for Y_i to:

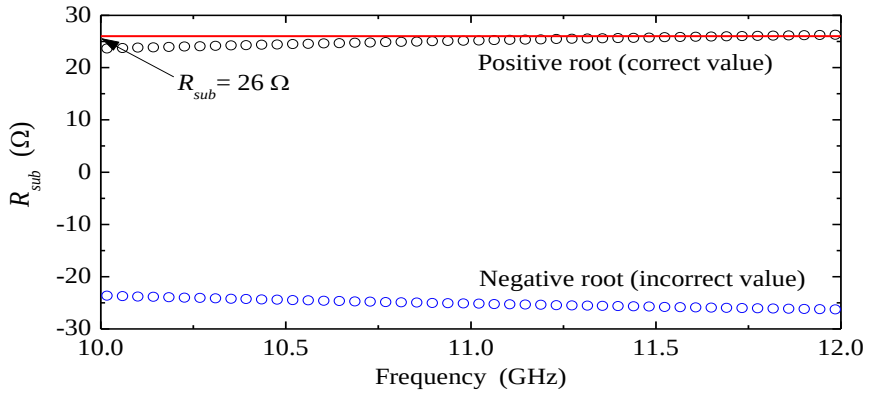


Fig. 3.15. Determination R_{sub} applying equation (3.10).

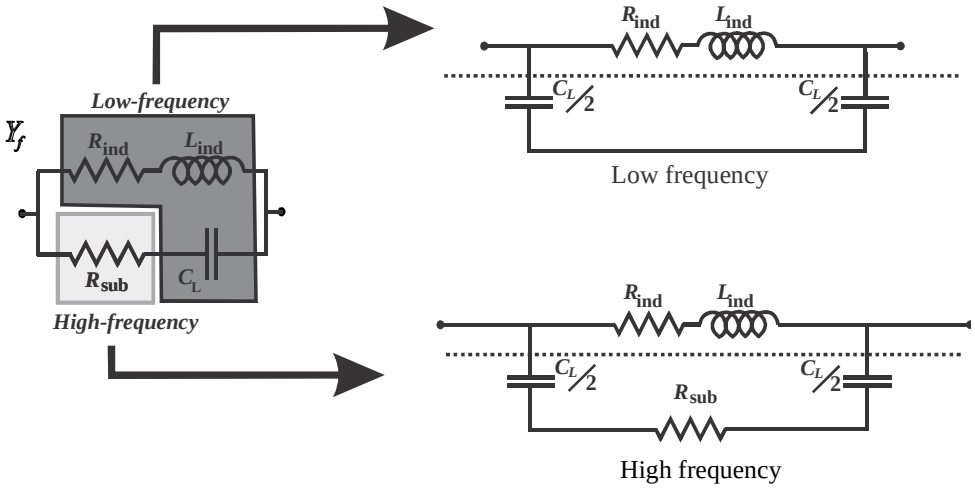


Fig. 3.16. Simplified equivalent circuits illustrating the simplifications assumed at different frequency ranges for determining the model parameters for Y_f.

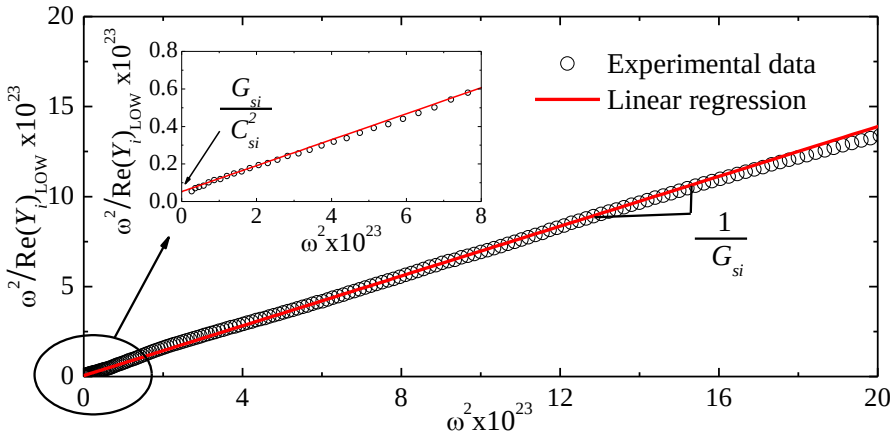


Fig. 3.17. Determination of G_{si} and C_{si} using the regression indicated in equation (4). Inset: Zoom-in showing the intercept with the ordinates.

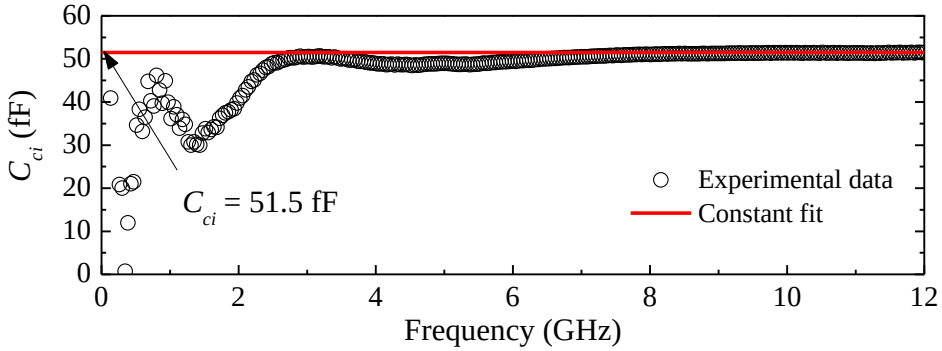


Fig. 3.18. Determination of C_{ci}.

$$Y_i|_{\mathrm{LF}} \approx \frac{\omega^2 C_{si}^2 G_{si}}{G_{si}^2 + \omega^2 C_{si}^2} + j\omega \frac{C_{si}^2 G_{si}^2}{G_{si}^2 + \omega^2 C_{si}^2} + j\omega C_{ci} \tag{3.13}$$

Afterwards, (3.13) can be separated into real and imaginary parts. For the real part, the corresponding equation (3.14) is:

$$\mathrm{Re}(Y_i)|_{\mathrm{LF}} \approx \frac{\omega^2 C_{si}^2 G_{si}}{G_{si}^2 + \omega^2 C_{si}^2} \tag{3.14}$$

which can be rewritten in the form:

$$y_2 = \frac{\omega^2}{\mathrm{Re}(Y_i)|_{\mathrm{LF}}} = \frac{\omega^2}{G_{si}} + \frac{G_{si}}{C_{si}^2} \tag{3.15}$$

Then, when applying a linear regression to y_2 versus ω^2 data, C_{si} is easily found by solving a simple equation involving an extrapolation to $\omega^2 = 0$, whereas the corresponding value for G_{si} is directly calculated as the inverse of the corresponding slope. The extraction of these parameters is shown in Fig. 3.17.

Once the values of G_{si} and C_{si} are known, the following step is determining the

value of the C_{ci} which represents one of the parasitic capacitances from the metal trace to the substrate. C_{ci} can be found after solving the imaginary part of Y_i in (3.13), this is:

$$C_{ci} = \frac{\mathrm{Im}(Y_i)|_{\mathrm{LF}}}{\omega} - \frac{C_{si}^2 G_{si}^2}{G_{si}^2 + \omega^2 C_{si}^2} \tag{3.16}$$

Fig. 3.18 shows that C_{ci} is obtained at frequencies where the experimental data obtained from (14) show a plateau. Finally, to determine R_{ci}, it is necessary to involve the following equation:

$$Y_i = Y_i|_{LOW} \parallel \frac{1}{R_{ci}} \tag{3.17}$$

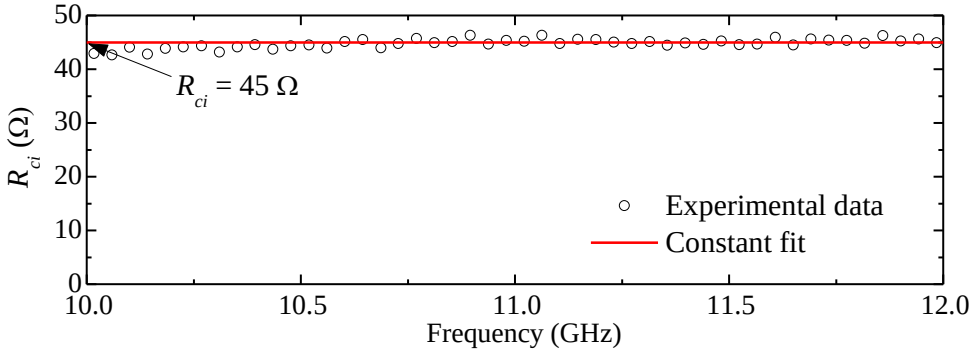


Fig. 3.19. Determination of the parameter R_{ci} from two possible equation roots.

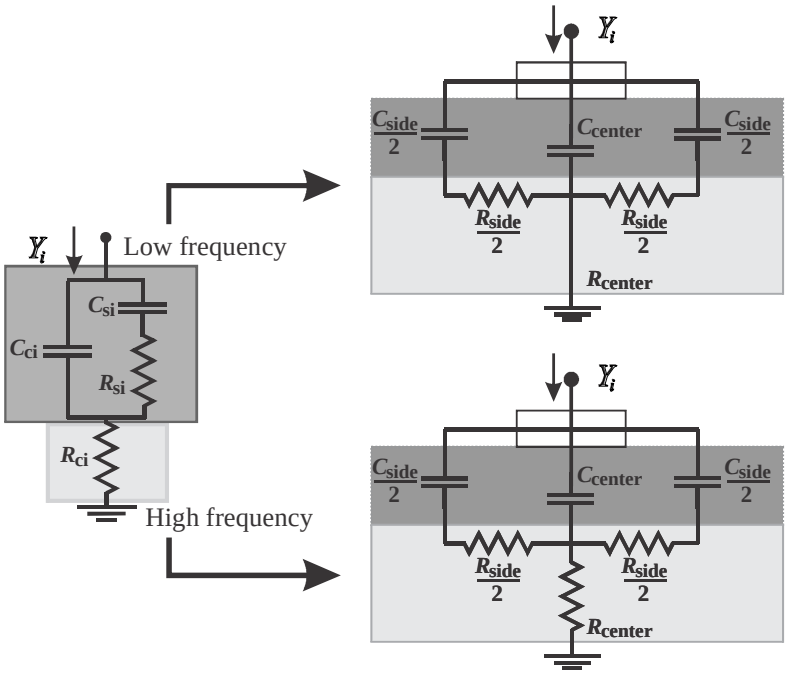


Fig. 3.20. Simplified equivalent circuits illustrating the simplifications assumed at different frequencies for determining the model parameters for Y_i and Y_o.

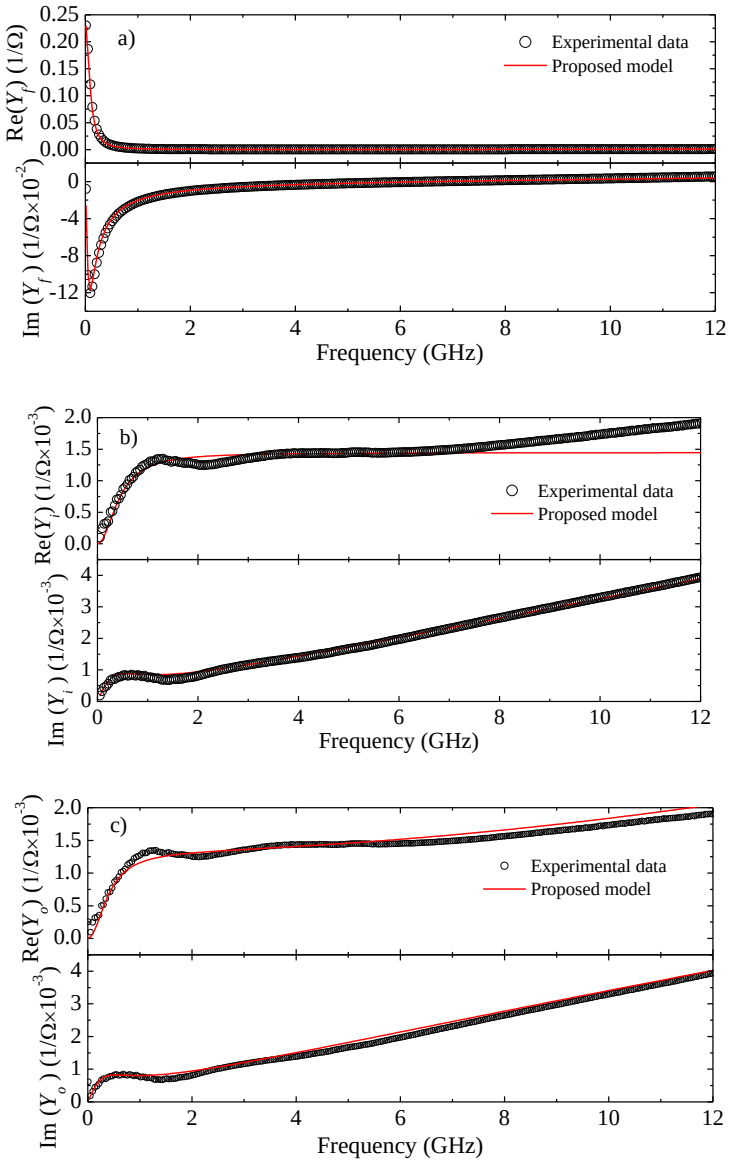


Fig. 3.21. Model–experiment correlation for the block admittances representing the inductor performance.

from which the real part is expressed as:

$$\mathrm{Re}(Y_i) = \frac{R_{ci}\mathrm{Re}(Y_i|_{LOW})^2 + R_{ci}\mathrm{Im}(Y_i|_{LOW})^2 + \mathrm{Re}(Y_i|_{LOW})}{R_{ci}^2\mathrm{Re}(Y_i|_{LOW})^2 + 2R_{ci}\mathrm{Re}(Y_i|_{LOW}) + 1 + R_{ci}^2\mathrm{Im}(Y_i|_{LOW})^2} \qquad (3.18)$$

Solving (3.18) for R_{ci} yields two roots, which present positive values. Therefore, in order to select the appropriate value, a model–experiment correlation has to be performed to find the root that allows better representation the measured data. Finally, to illustrate the assumptions considered for determining the model parameters for Y_i, Fig. 3.20 shows the equivalent circuits used to define the equations employed at different frequency ranges.

After completing the extraction process, a model–experiment confrontation can be performed to verify the obtained results. Fig. 3.21 shows that the admittances used

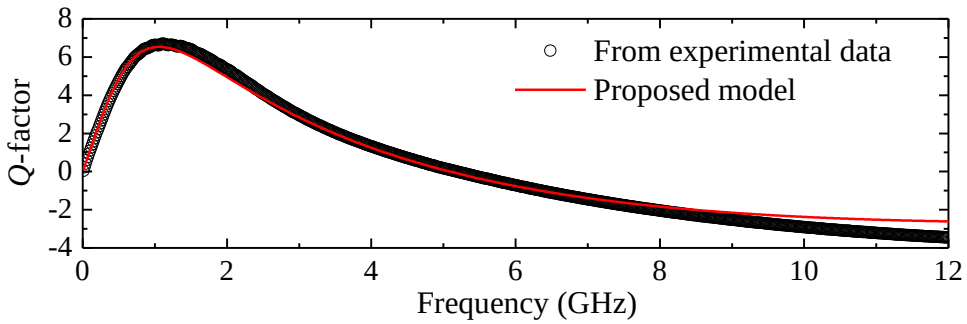


Fig. 3.22. Model–experiment correlation for the *Q*-factor.

to represent the inductor are adequately modeled when using the equivalent circuits after determining the corresponding elements with the proposed methodology. Bear in mind, that modeling this device up to 12 GHz using the very simple circuit detailed in Fig. 3.12 is desirable to speed up the model implementation as well as circuit simulations. On the other hand, observe that at high frequencies a discrepancy is noticeable in the real part of the admittance associated with the inductor's input port.

This suggests that some additional considerations are required to represent the coupling of the device terminals to the substrate at higher frequencies (i.e., a substrate network rather than a simple lumped resistance). Work in this direction is ongoing. Nevertheless, as observed in Fig. 3.22, the *Q*-factor is reproduced with accuracy within the bandwidth of peak performance but also up to at least 3 times this frequency, which covers higher order harmonics of the operation signal [81].

3.4 Chapter conclusions

An exhaustive analysis of the experimental data collected to several on-wafer structures was carried out to verify the applicability of the typically used 1-step and 2-step deembedding procedures. The results show that using only an open structure to perform deembedding may introduce severe errors in the analysis of DUTs, which becomes more serious as the corresponding impedance is comparable with the series parasitics introduced by the test fixture. In this case, using a 2-step deembedding is mandatory. However, it was also observed that the error in dB introduced by using the 1SD procedure remains approximately constant when varying the impedance of the DUT; thus, its relative value with respect to the actual data associated with the DUT becomes small when the corresponding impedance is large. In this case, the 1-step deembedding can be used even at frequencies as high as 30 GHz. Bear in mind, that this is only valid for devices with high impedance such as small capacitors or the input port of some amplifiers.

Furthermore, the work presented here contributes to the modeling of inductors fabricated on semiconductor substrates by providing a simple and accurate

representation, and parameter extraction methodology that accurately reproduces the inductor network parameters and *Q*-factor. The parameter extraction method relies on the fact that the inductor can be modeled through a simple network provided that physical effects are carefully separated in intrinsic inductor, and input/output parasitics. This eases the analysis and allows a simple model implementation using only *S*-parameter measurements. This methodology can be extended to other structures. In fact, in the next chapter, similar concepts are applied to represent a MIM capacitor for material characterization purposes.

CHAPTER 4
Using RF-Measurements to Characterize Dielectric Materials

IN PREVIOUS CHAPTERS, the analysis of particular devices was carried out within the context of RF operation. Even though understanding and representing the behavior of these devices is important, the characterization of the materials that are used for their construction is also necessary. Evidently, attempting to cover this topic including different materials, as well as modeling and characterization techniques is a challenging task that falls outside the goals of this thesis. However, in order to show the potential of RF measurements to obtain the figures of merit and to implement accurate models of advanced devices by determining the material properties is explained in this chapter. Hence, the case of study selected to present this idea involves the analysis of thin film dielectrics through the measurement and modeling of a metal-insulator-metal (MIM) capacitor. In this regard, a detailed model including the device's intrinsic properties as well as the parasitics inherent to the test-fixture required to perform the measurements is proposed here and represents one of the contributions of this thesis. The reason to choose this topic as an example is explained in the following paragraph.

It has been already mentioned that shrinking the semiconductor device's dimensions is the main strategy to increase the corresponding speed of operation, but also to reduce power consumption; however, the technology has been reached a point at which the intrinsic properties of the fabrication materials do not meet the requirements for advanced devices. One of the most important materials falling into this case is the dielectric used to isolate the gate electrode from the channel region in a MOSFET. Traditionally, the dielectric material used for this purpose is the SiO_2, due to its native nature. Nevertheless, as the thickness of the SiO_2 is made thinner to raise the gate capacitance, poorer performance as a dielectric barrier is observed, presenting considerable leakage currents. Thus, in order to alleviate this problem, materials with improved dielectric characteristics even when presenting a nanometer thickness have been developed. These dielectrics are known as high-κ dielectrics, because their relative permittivity is higher than that of the SiO_2 (i.e., $\kappa_{SiO2} = 3.9$). Therefore, the corresponding characterization and modeling has taken importance, which is the reason why in this chapter the use of RF measurements for this purpose is explored.

4.1 Relative permittivity

In this section, some basic concepts related with the properties of dielectrics will be reviewed. Ideally, the charge inside this type of materials is bounded, which implies that it cannot participate in transport current. Nonetheless, these materials can be analyzed from an electrical point of view assuming that are formed by a group of dipoles. Therefore, under the influence of an electric field, these dipoles can be polarized, which means that the particles represented by the dipoles are aligned with this field. In this case, even when the susceptibility (χ_e) is the parameter that indicates how easily the material can be polarized, the typical figure of merit widely used to characterize a dielectric material in engineering applications is the ε_r. This parameter includes the effect of the dielectric susceptibility, and indicates how easy an electric field can be formed in a given medium. In order to see the relation between these two parameters, it is necessary to remember that in a polarized dielectric material there exist the external field and the induced field due to the polarization. Thus, the electric displacement field is defined in terms of the external electric field (**E**) and the polarization vector (**P**) as:

$$\mathbf{D} = \varepsilon_0\mathbf{E} + \mathbf{P} = \varepsilon_0\mathbf{E} + \varepsilon_0\chi_e\mathbf{E} = \varepsilon_0(1+\chi_e)\mathbf{E} = \varepsilon_0\varepsilon_r\mathbf{E} = \varepsilon\mathbf{E} \tag{4.1}$$

In (4.1), $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m is the vacuum permittivity. In the case of vacuum, $\chi_e = 0$ because there is nothing to polarize, but in a medium different to vacuum $\chi_e \neq 0$ and presents a complex value, $\mathbf{P} \neq 0$, and $\varepsilon \neq \varepsilon_0$. Then ε_r is a complex number that allows to account for the effect of the field that would exist in the vacuum plus the originated by the polarized material; matemathically:

$$\varepsilon_r = 1 + \chi_e = \varepsilon' + j\varepsilon'' \tag{4.2}$$

The relative permittivity defined in (4.2) is in general a complex number, where the real part is related to the capacity of the material to store of the energy in form of an electric field, whereas the imaginary part allows to quantify the losses. In microwave electronics, the dielectric losses are typically quantified through a parameter known as the loss tangent:

$$LT = \tan\delta = \frac{\varepsilon''}{\varepsilon'} \tag{4.3}$$

which is the quotient between the imaginary and the real part of ε_r, and it is a measure of how much energy is absorbed by the material, reducing the magnitude of an applied electric field. In this regard, the modeling of ε_r for a given material is a complicated process because of the frequency dependence behavior of this parameter. In fact, there are physically based equations that predict the behavior of ε_r, such as the Debye model

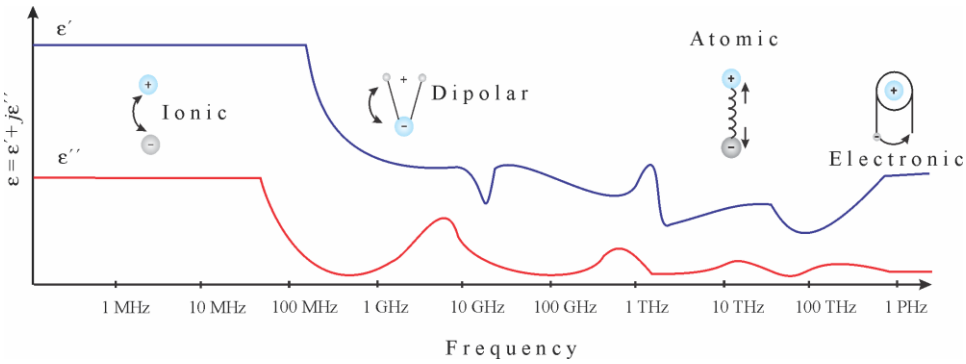


Fig. 4.1 Conceptual plot showing ε_r versus frequency for a generic dielectric material [2].

[33]; however, effects like resonances and relaxation difficult the accurate prediction of ε_r in wide frequency ranges. For this reason it is desirable to determine ε_r through experimental data performed to the dielectric under study within the frequency range at which it will be used. In order to illustrate a typical variation of ε_r with frequency, Fig. 4.1 the corresponding curve for no particular dielectric. In accordance to this plot there are ranges where ε_r: gradually falls with frequency (i.e., normal trend), abruptly either increases or decreases with frequency (i.e., anomalous trend around the frequencies of resonance), presents a very high imaginary part due to resonant absorption [2, 33].

4.2 Experimental determination of relative permittivity

As mentioned at the beginning of this chapter, the dielectric materials used for practical applications are evolving; particularly those used in IC technology, which currently present nanometer thicknesses. Thus, characterizing thin-film dielectrics is mandatory to assess the performance of advanced semiconductor devices [82]. In this regard, it is necessary to know the parameters used as figures of merit for dielectrics:

- ε_r
- tanδ

For simplicity, from this point forth it is assumed that ε_r represents only the real part of the material's relative permittivity since tanδ is used to consider the corresponding losses.

For the case of advanced devices, such as nanometric transistors, obtaining the dielectric parameters becomes a crucial task to warrant the appropriate operation within an integrated circuit. In this case, determining ε_r and tanδ from prototypes

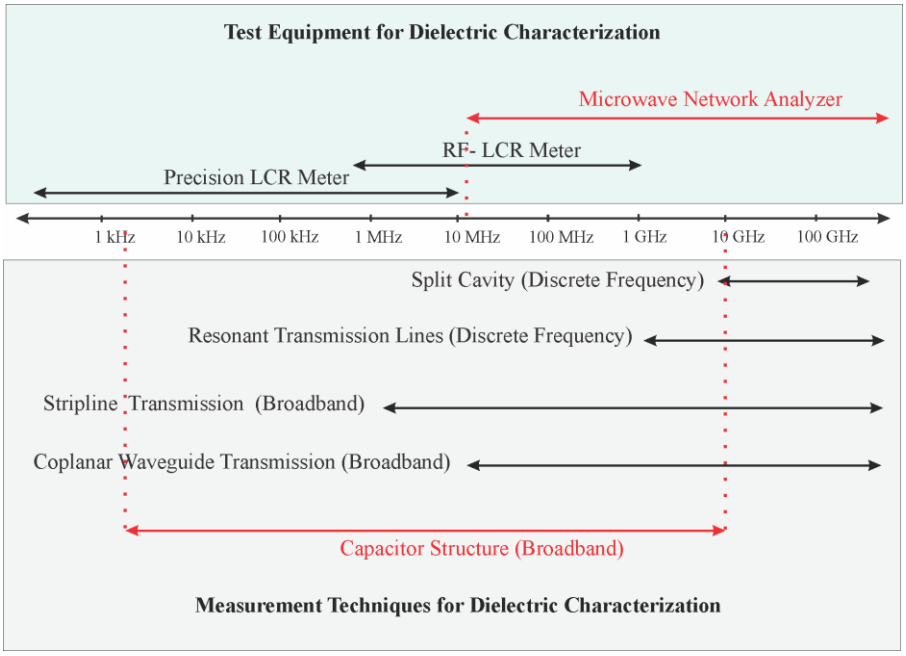


Fig. 4.2 Some equipment, structures, and techniques used to obtain ε_r at high frequencies (from Agilent and Furman [2, 33]).

presenting a thickness comparable to those used in practical applications allows to include the impact of effects such as leakage currents [83], and the frequency dependence of the dielectric material properties, resulting in a more accurate characterization of the dielectric under normal operation conditions. Typically, for thin dielectrics, ε_r is obtained from capacitance–voltage (CV) and direct-current (DC) measurements performed to MIM capacitors [83]. However, these techniques only provide information at low f and neither allow to obtain tanδ nor ε_r as a function of frequency. Alternatively, *S*-parameters can be used by employing:

- coplanar waveguides (CPW) [84],
- MIM capacitors [85].

For CPWs, obtaining ε_r and tanδ requires the determination of the propagation constant, which is difficult when the dielectric layer separating the CPW from the substrate is very thin. Comparatively, MIM capacitors are simpler, require less die space, and allow to obtain ε_r and tanδ as a function of frequency from one-port measurements [86]. Nevertheless, the parasitics inherent to the test fixture have not properly been modeled within the microwave range, which yields extracted data presenting unexpected fluctuations and even negative values [83]. Fig. 4.2 shows the different equipment, structures and techniques currently used to perform a measurement-based characterization at high frequencies.

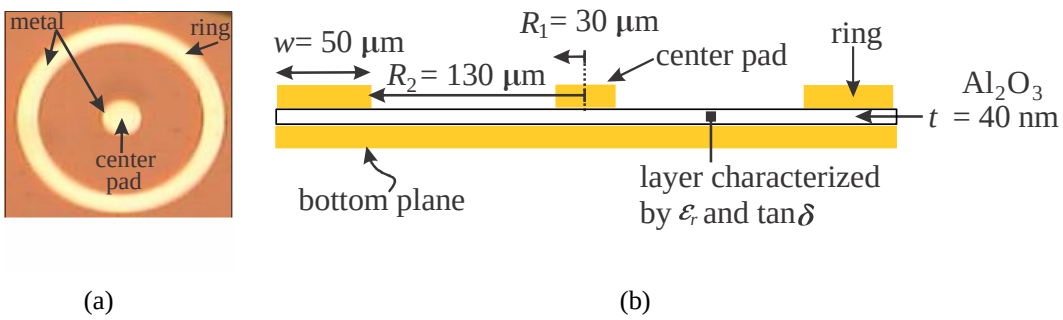


Fig. 4.3 Fabricated MIM capacitor: (a) micrograph, and (b) cross section illustrating dimensions.

4.3 Test structure

In order to illustrate the development and verification of a new technique proposed in this thesis, capacitors configured for coplanar measurements were fabricated using the process of the Microelectronics Laboratory at INAOE. These capacitors were formed with aluminum (400 nm in thickness) as both top and bottom electrodes, and an Al_2O_3 layer with a thickness t = 40 nm was used as dielectric. The aluminum electrodes were deposited using electron beam evaporation under ultra-high vacuum conditions, whereas the Al_2O_3 layer was deposited at 250°C by atomic-layer deposition using trimethylaluminum and H_2O as precursors. The top view and dimensions of the structure are detailed in Fig. 4.3. One-port *S*-parameters (i.e., the reflection coefficient Γ) were measured to this capacitor using a GSG probe with a pitch of 150 μm. And finally, the Agilent VNA setup at the INAOE's Microwave Laboratory was calibrated up to the probe tips using an impedance standard substrate. Afterwards, Γ was processed to characterize the DUT as explained hereafter.

4.4 Formulation of the method to determine the complex permittivity

The properties of a dielectric layer such as that in the prototype described in Fig. 4.3 can be represented by means of intrinsic admittances that account for the lossy capacitive coupling between the center pad and the outer ring with the bottom plane. In Fig. 4.4a, these admittances are labeled as Y_{center} and Y_{ring}. In addition, this circuit includes the resistance of the bottom metal plane (R_b), and the side capacitance (C_p) that considers the electric field between the center pad and the outer ring. Notice that the model in Fig. 4.4a is simplified to that in Fig. 4.4b by considering a total intrinsic admittance Y_{int}, which is the series connection of Y_{center} and Y_{ring}. In this model, C_p is considered lossless since the gap between the center pad and the ring is large, making the corresponding leakage currents low when compared to those of Y_{center} and Y_{ring}.

At low frequencies, the effect of the losses associated with the thin layer on the Γ are small, which allows to assume $Y_{center} \approx j\omega C_{center}$ and $Y_{ring} \approx j\omega C_{ring}$; where C_{center} and C_{ring} are lossless capacitances, ω is the angular frequency, and $j^2 = -1$. This assumption allows to consider $Y_{int} \approx j\omega C_{int}$, where $C_{int} = C_{center}C_{ring}/(C_{center} + C_{ring})$. In this case, the admittance in Fig. 4.4b can be written as:

$$Y_{DUT} = \frac{\omega^2 R_b C_{int}^2}{\omega^2 C_{int}^2 R_b^2 + 1} + j\omega\left[C_p + \frac{C_{int}}{\omega^2 C_{int}^2 R_b^2 + 1}\right] \tag{4.4}$$

where the real part of this admittance can be arranged as:

$$\frac{\omega^2}{\mathrm{Re}(Y_{DUT})} = \frac{1}{R_b C_{int}^2} + R_b\omega^2 \tag{4.5}$$

In accordance to (4.5), when obtaining Y_{DUT} from measured Γ, R_b can be determined from the intercept with the ordinates of the linear regression of the $1/\mathrm{Re}(Y_{DUT})$ versus ω^2 curve, whereas $C_{int} = (m \cdot R_b)^{1/2}$, where m is the slope of this regression. Bear in mind that this regression has to be performed at frequencies so low that the effect of $\tan\delta$ on Y_{int} is negligible and thus the experimental data present linearity. The frequency range of validity of this assumption is discussed later in this chapter.

Once R_b and C_{int} are known, C_p is obtained from (4.4) as:

$$C_p = \frac{\mathrm{Im}[Y_{DUT}]}{\omega} - \frac{C_{int}}{\omega^2 C_{int}^2 R_b^2 + 1} \tag{4.6}$$

At this point, the test fixture parasitics C_p and R_b are known. Thus, the corresponding effect can be removed from the experimental data to obtain Y_{int} even at

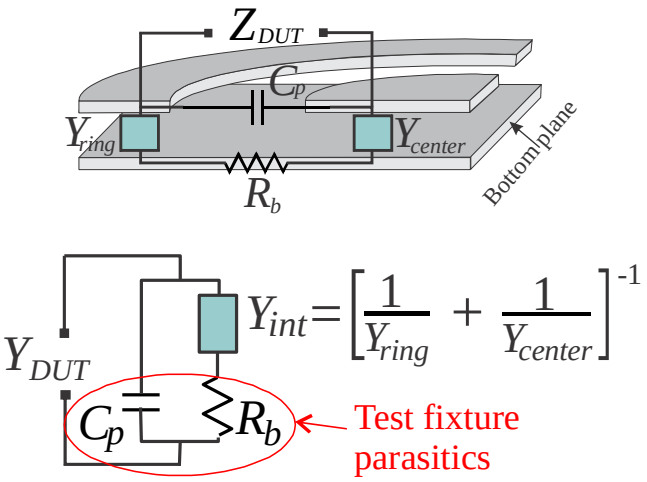
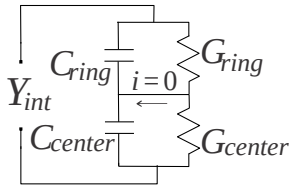


Fig. 4.4 (a) One quarter of the MIM structure showing the corresponding circuit model, and (b) simplified equivalent circuit.

(a)



(b)

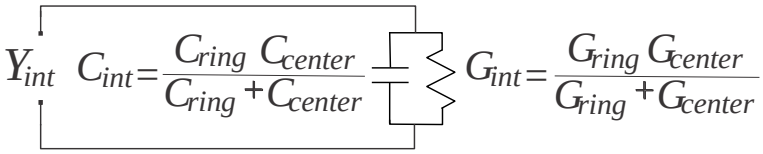


Fig. 4.5. (a) Model for the intrinsic admittance, and (b) simplified circuit.

frequencies at which the impact of tanδ on Y_{center} and Y_{ring} is considerable. In this case, from the circuit in Fig. 4.4b, Y_{int} can be obtained from:

$$Y_{int} = \left[(Y_{DUT} - j\omega C_p)^{-1} - R_b\right]^{-1} \tag{4.7}$$

In (4.7), Y_{int} is assumed to represent the MIM structure even at frequencies so high that losses impact Y_{center} and Y_{ring}. In this case, it is necessary to consider $Y_{center} = G_{center} + j\omega C_{center}$ and $Y_{ring} = G_{ring} + j\omega C_{ring}$, where $G_{center} = \omega C_{center}\tan\delta$ and $G_{ring} = \omega C_{ring}\tan\delta$ are the conductances that account for the losses in the dielectric layer [47]. Fig. 4.5a shows the equivalent circuit for Y_{int} including losses and indicating a current i. In fact, this circuit can be simplified to that in Fig. 4.5b since $i = 0$ (i.e., $C_{center}/C_{ring} = G_{center}/G_{ring}$).

Since $Y_{int} = G_{int} + j\omega C_{int}$ in Fig. 4.5b is known by applying (4.7) to experimental data, ε_r and tanδ are obtained as:

$$\varepsilon_r = \frac{t\ \mathrm{Im}[Y_{int}]}{\omega \varepsilon_0 A_{eq}} \tag{4.8}$$

$$\tan\delta = \frac{\mathrm{Re}[Y_{int}]}{\mathrm{Im}[Y_{int}]} \tag{4.9}$$

where the equivalent area of C_{int} in Fig. 4.5b considering the areas of the ring (A_{ring}) and the central pad (A_{center}) is $A_{eq} = A_{ring}\, A_{center}/(A_{ring} + A_{center})$.

Fig. 4.6 shows the extraction of R_b, C_{int}, and C_p for the MIM structure in Fig. 4.3. Notice the good linearity of the experimental data, verifying the validity of (4.5) up to f = 1.2 GHz. Thus, after obtaining Y_{int} from (4.7), ε_r and tanδ are determined as a function of frequency from (4.8) and (4.9), respectively. Fig. 4.7 shows the results,

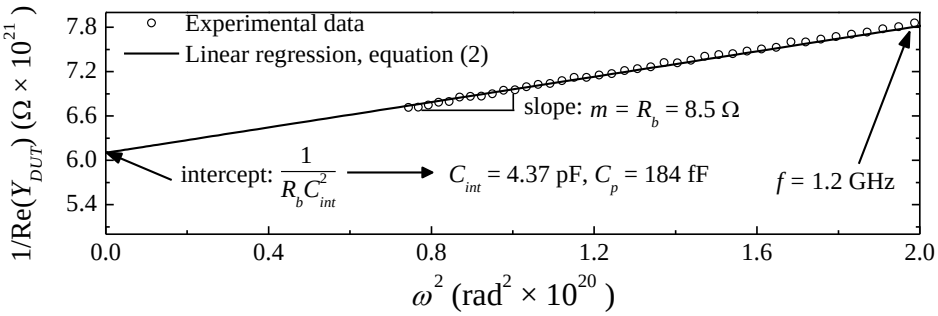


Fig. 4.6. Regression at low frequencies to determine R_b, C_{int}, and C_p.

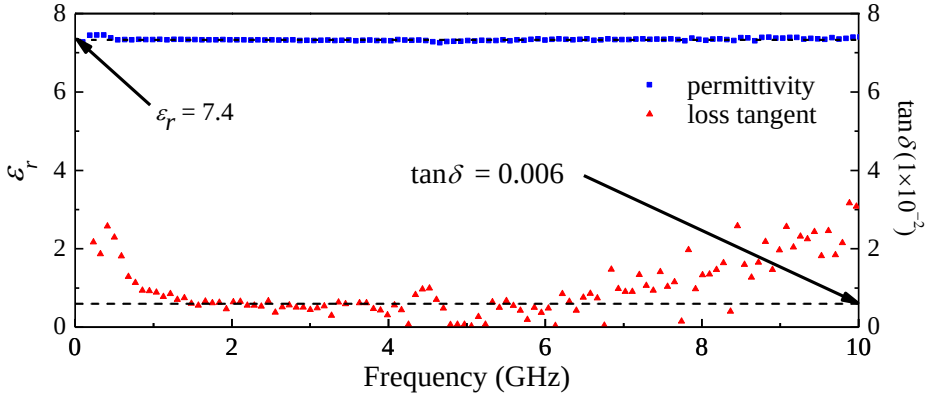


Fig. 4.7 Extracted parameters using the proposed method.

obtaining $\varepsilon_r \approx 7.4$ and $\tan\delta \approx 0.006$, which correspond to values reported for nanometric Al_2O_3 layers [87]. Observe that $\tan\delta$ starts rising with frequency at the upper end of the measured range due to the increased polarization current in the dielectric at microwave frequencies. At this point, it is important to mention that due to the relatively low value of $\tan\delta$, the correct determination of R_b in the extraction procedure is crucial since it affects the real part of Y_{int}, from which the loss tangent is obtained. Moreover, R_b requires to be minimized to reduce the uncertainty in the determination of $\tan\delta$. In fact, even though short-circuiting the central pad in the prototypes simplifies the circuit in Fig. 4.4 (i.e., Y_{center} is substituted by a series resistance), very noisy $\tan\delta$ is obtained in this case due the increase of R_b. So far, the MIM prototype considered in this section intrinsically presents two capacitors: the center pad and the outer ring capacitors. Since these capacitors are in series connection, the corresponding equivalent capacitance obtained through RF measurements is smaller than that of any of the aforementioned capacitors.

For this reason, an additional experiment was carried out here, where a MIM structure presenting the center pad shorted through a metallization to ground is measured.

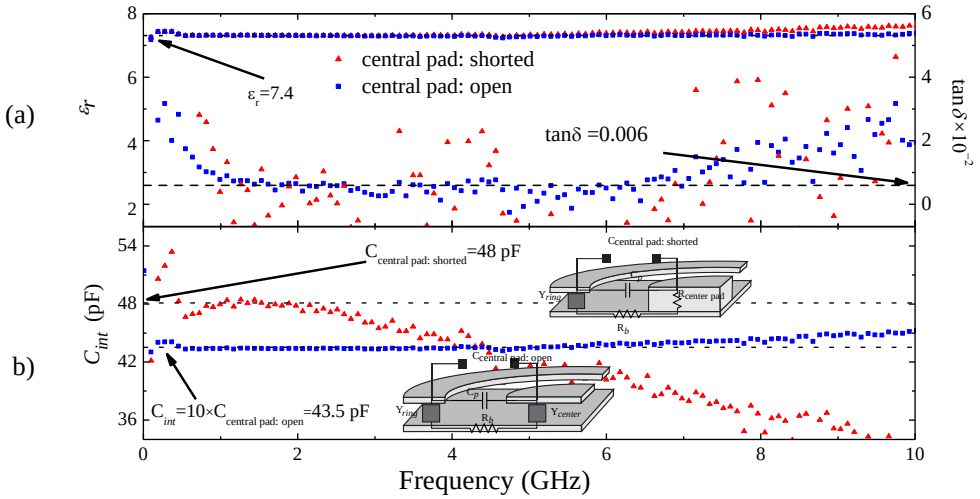


Fig. 4.8 Comparison of extracted data using structures with the central pad shorted and isolated (i.e., in open circuit condition) from the ground plane.

In this case, the experimentally obtained capacitance in Fig. 4.5 is given by $Y_{int} = G_{ring} + j\omega C_{ring}$. Unfortunately, even though the measured capacitance increases, the parasitic series resistance introduced by the metallization introduces uncertainty to the extracted data. This is critical since the resistance impacts the real part of the DUT's admittance, and due to the low value of tanδ (obtained from the real part of Y_{int}), it may yield severe errors in the corresponding extraction as illustrated in Fig. 4.8. This figure confronts the results between the short-circuited central pad and open central pad structures. Even though similar results for ε_r were obtained, Fig. 4.8a shows more noisy results for tanδ when extracted from measurements to the short-circuited MIM structure, which is due to the higher value for R_b when compared to that associated with the open structure. However, the increment in the capacitance achieved when using the short-circuited structure may give more certainty to the determination of ε_r, which is important if relatively low frequencies are of interest (Fig. 4.8b). Thus, there always are advantages and disadvantages when using either one of these structures. Here, it is pointed out that at microwave frequencies the performance of open-circuit prototype is better.

On the other hand, in order to illustrate the impact of neglecting the test fixture parasitics on the extracted parameters the results for the open structure are considered. The top of Fig. 4.9 shows ε_r when the extraction is performed neglecting C_p and R_b, and also when only neglecting C_p. Substantial differences are observed in the corresponding curves when compared with the one obtained using the proposed method. In fact, ε_r exhibits a dramatic frequency dependency when the parasitics are not taken into consideration, which is not expected within a f-range of 10 GHz. Furthermore, notice at the bottom of Fig. 4.9 that the full model employed here

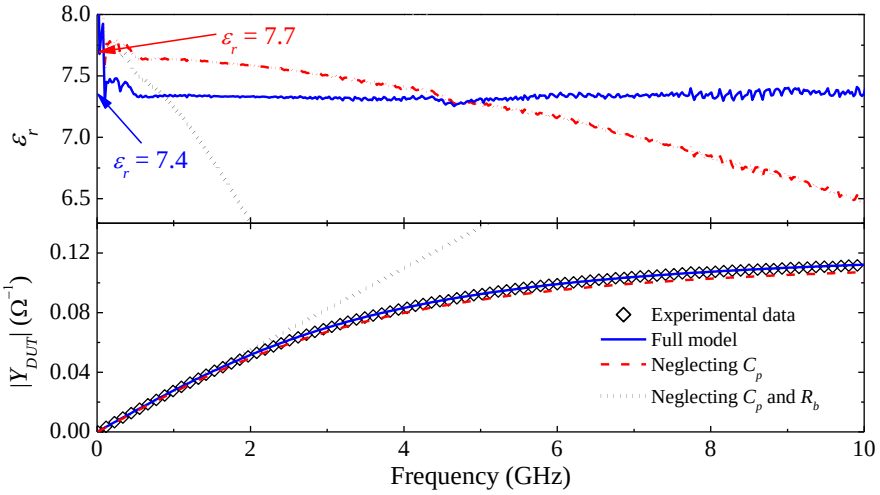


Fig. 4.9 Comparison between the proposed method and simplified approaches: extracted ε_r (top), and the MIM structure admittance (bottom).

including C_p and R_b accurately reproduces the experimental admittance of the MIM structure at least up to 10 GHz, whereas the curves ignoring the pad parasitics deviate from experimental data as frequency increases. Thus, even though it has been pointed out that the effect of C_p, and even that of R_b is negligible in structures using relatively thick dielectrics with very high permittivity [83], when characterizing films with thickness of some tens of nanometers, the effect is significant [88].

4.5 Chapter conclusions

In today's electronics, RF measurements are widely used for characterization and modeling purposes. In this context, whereas high frequency techniques for studying circuits and devices have been developed and successfully applied, the potential of these measurements for characterizing advanced materials has not been thoroughly explored. In this chapter, a contribution in this direction has been presented: the permittivity and loss tangent of a thin film dielectric layer were obtained from RF measurements performed to a single MIM structure. The extraction method allows for the consideration of the test fixture parasitics neither requiring several MIM structures nor dummy devices. The obtained results show physically expected trends and allow for an accurate representation of the MIM structure admittance. Therefore, the results presented here show that using RF measured data, the extraction of the features of advanced materials can be carried out in a simple and straightforward way, enabling microwave laboratories to analyze and develop materials for current and future applications.

CHAPTER 5
General Conclusions

THROUGHOUT this thesis, several aspects regarding the use of microwave measurements for characterization and modeling interconnects, devices, and materials have been discussed. It was the purpose of this work to make evident the potential of *S*-parameter measurements to be used in a wide variety of applications. Nevertheless, as in the case of any other tool, it requires intensive criteria from the user to carry out meaningful and helpful results. This means that by themselves, *S*-parameters are only data in the frequency domain that require a proper interpretation. Even though much work has been reported in this direction, new challenges have to be faced to enable these measurements for advanced devices evolving to occupy less space and operating at higher frequencies. In this regard, results derived from this doctoral project yield to new proposals to account for advanced effects occurring at the different levels of electronic systems. Thus, in order to summarize these contributions, the following sections are intended to conclude each one of the aspects covered in this thesis.

5.1 Transmission line characterization and modeling

Modeling interconnects is fundamental in any electrical circuit. Signals require to propagate in such a way that information is recoverable at the desired points within a system. This thesis proposed models for interconnects operating at high frequencies. In this regard, it was pointed out the importance of allowing the represent the interconnects in both frequency and time domains. Whereas frequency domain analysis allows for the identification and quantification of parasitic effects and propagation issues occurring in these structures, time domain analysis is the one preferred by engineers to verify the proper operation of the inter-device channels. Thus, both domains should be covered to carry out useful and complete modeling and characterization work.

It should also be mentioned that physical effects influencing the behavior of these structures might be substantially different when the level of integration varies. For instance, on-chip interconnects present high resistive losses whereas on-PCB lines suffer from high dispersion due to the considerably large associated inductance. Some of the aspects taken into consideration when conducting the research undertaken in this thesis include the following:

- At PCB level surface roughness and non-ideal variation of the attenuation versus frequency (it differs from the classical f^0.5 model) was considered. This allowed to develop a model and parameter extraction for PCB interconnects verified up to 110 GHz.
- At on-chip level, the finite and considerable series resistance even at frequencies near to DC was considered when implementing the corresponding model.
- In both cases, a proposal for representing interconnects using frequency independent elements incorporating all the high frequency effects was developed. This allows for interconnect model implementations in SPICE-like simulators, which is the standard tool when designing circuits in both academy and industry levels.

5.2 On-chip device modeling

For on-chip devices, moving the measurement reference plane to the DUT is extremely important since the test fixture parasitics may considerably affect the experimentally collected results. This is the reason why de-embedding is a crucial step in this case. In this thesis, this fact was studied in detail allowing to identify potential errors that may occur when not including and using the required deembedding structures in an on-chip prototype.

After de-embedding, data corresponding to the DUT can be processed in a systematic way to identify the main effects becoming apparent within the frequency range at which the device will be operating. In this regard, cascaded models allow to represent a DUT at higher frequencies that those achieved with traditional single-stage representations. One of the contributions of this thesis is the development of a technique to sectionalize a model for inductors so that every section takes into consideration the more accentuated effects at given frequencies. Excellent results were achieved demonstrating that this technique can be applied to inductors and pointing out the fact that distributed models are not limited to transmission lines. Work in this direction can be conducted to model other devices such as transformers and even capacitors.

5.3 Characterization of material properties at microwave frequencies

Understanding the behavior of a device necessarily requires the understanding of physical effects occurring within its constitutive materials. *S*-parameters may give insight about this and even allow the determination of fundamental parameters

defining the characteristics of the device. Bear in mind that the identification of particular effects from measured data, although possible, requires intensive analysis and systematic processing of data on the part of the scientist since experimental data are influenced by many phenomena. Thus, physical basis are necessary to obtain consistent and meaningful results.

In this thesis, a structure for obtaining the fundamental parameters of thin film dielectrics was used. A new parameter extraction technique allowed for the determination of the corresponding dielectric properties including the dissipation factor and leakage currents degrading its behavior. This part was carried out to point out the fact that physically meaningful results can be achieved when using an adequate test vehicle. It is necessary to point out the fact that for obtaining the results, an exhaustive analysis of the effects occurring within the test structure was carried out so that the properties of the material can be isolated from the rest of effects occurring in the structure.

5.4 Prospects of microwave measurements in characterizing and modeling advanced devices

The activities at a Microwave Laboratory are intended to electrically characterize and optimize devices and circuits used at the different levels of electronics systems, from DC behavior to high-frequency operation. Furthermore, experimental results obtained using DC and high-frequency equipment in a laboratory allow for the development of electrical models for circuits and devices.

Among the activities carried out in a microwave laboratory equipped with state-of-the-art hardware and tools highlight the measurement, characterization and modeling of devices, components, and materials. Thus, currently it is possible to experimentally study the following devices, circuits and structures:

- Passive devices on semiconductor and PCB substrates: inductors, capacitors, antennas.
- Interconnects on PCB substrates: transmission lines (single ended and differential), waveguides (e.g., SIWs), vias and other transitions.
- Basic properties of PCB materials (dissipation factor, relative permittivity, filling factor in surface interconnects)
- Advanced properties of PCB materials (resonances, lack of homogeneity)
- High-K dielectrics, thin films (e.g., dielectric losses, leakage currents , dispersion, and breakdown field).

- Interconnects on semiconductor substrates: multilevel transmission lines, vias and other transitions.
- On-chip active devices: transistors and other amplifiers, oscillators, etc.
- Extraction of model parameters and figures of merit for all the structures mentioned above for validation purposes (e.g., compliance of specifications).

Notice the wide range of research that can be performed in a microwave laboratory. Bear in mind that challenges such as those pointed out throughout this thesis need to be faced. In this regard, measurements by themselves are useless when not properly obtained or interpreted. This is the task of scientist and engineers working in this field at both academic and industry levels.

List of Figures

CHAPTER 1

CHAPTER 2

CHAPTER 3

CHAPTER 4

Bibliography

CHAPTER 1

[1] David Pozar, *Microwave Engineering.,* 4th Edition, John Wiley & Sons, Inc., USA, 2011.

[2] S. H. Hall and H. L. Heck, *Advanced Signal Integrity for High-Speed Digital Design.*, IEEE PRESS, John Wiley & Sons, USA, 2009.

[3] Pankaj Kumar, *"Recent Advancements in Microwave Technology in Pharmaceutical Industry"*, http://www.farmavita.net/content/view/1220/84/ , Aug. 09.

[4] B. S. Sekhon, "Microwave-Assisted Pharmaceutical Synthesis: An overview", *Inter. Journal of Pharmaceutical Technology Research,* vol. 2, no 1, Mar 10.

[5] M. A. Othman, P. N. M. M. M. Noor, T. S. M. Arshad, N. Y. M. Yasin, S. N. Taib, M. M. Ismail, M. H. Misram, M. A. Meor Said, H. A. Sulaiman and R. A. Ramlee, "An Analysis of Dielectric Constant of Pharmaceutical Medicines using Microwave Radiation Exposure", *3er International Conference on Instrumentation, Communications, Information Technology, and Biomedical Engineering*, Nov. 2013.

[6] F. P. Correia, M. S. Alencar, F. B. S. Carvalho, W. T. A. Lopes, and B. G. Leal. "Propagation Analysis in Precision Agriculture Environment using XBee Devices," *SBMO/IEEE MTT-S International Microwave & Optoelectronics Conference (IMOC),* Rio De Janeiro, Aug. 2013.

[7] M. Yamaguchi, K. Maruta and H. Ono, "Operating Mechanism for RF Electromagnetic Noise Suppression Sheets", *IEEE Transactions on Magnetics*, vol. 41, no. 10, pp-3565-3567, Oct. 2005.

[8] Y. Yuchen, H. Daocheng, F. C. Lee, and L. Qiang, "Analysis and Reduction of Common Mode EMI Noise for Resonant Converters", *29th Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2014.

[9] D. Boroyevich, X. Zhang, H. Bishinoi, R. Burgos, P.Mattavelli, and F. Wang, "Conducted EMI and System Integration", *18th International Conference on Integrated Power System (CIPS)*, Feb. 2014.

[10] H. Iwai, "Materials and Structures for Future Nano CMOS", *IEEE Nanotechnology Material and Devices Conference*, pp.14-18, Oct. 2011.

[11] R. Penning de Vries, "From Living Faster to Living Better", *IEEE International Symposium on Technology, Systems and Applications*, April 09.

[12] International Technology Roadmap for Semiconductors, www.itrs.net

[13] A.R. Aswatha, "Efficient Power Modeling for On-Chip Global Interconnects", *51st Midwest Symposium on Circuits and System MWSCAS*, Aug. 2008.

[14] L. Clavelier, C. Deguet, L. Di Cioccio, E. Augendre, A. Brugere, P. Gueguen, Y. Le Tiec, H. Moriceau, M. Rabarot, T. Signamarcheix, J. Widiez. O. Faynot, F. Andrieu, O.Weber, C. Le Royer, P. Batude, L. Hutin, J. Damlencourt, S. Deleonibus, and E. Defay, "Engineered Substrates for Future More Moore and More than Moore Integrated Devices", *IEEE International Electron Devices Meeting (IEDM)*, Dec. 2010.

[15] A. La Manna, T. Buisson, M. Detalle, K. J. Rebibis, D. velenis, W. Zhang, and E. Beyne, "Challenges and Improvements for 3D- IC Integration using Ultra Thin (25µm) Devices", *IEEE 62nd Electron Components and Technology Conference (ECTC)*, June 2012.

[16] H. H. Utsunomiya, "Challenge on Packaging Substrate Technologies towards Next Decade", *3rd International Microsystems, Packaging, Assembly & Circuits Technology Conference*, Oct. 2008.

[17] J. Minkyu, L. Tsung-Yang, C. Hyun-Kee, S. Bhattacharya, and K. Dim-Lee, "Future Mobile Society Beyond Moore's Law", *IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Nov. 2013.

[18] R. R. Tummala, "Packaging: Past, Present and Future", *6th International Conference on Electronic Packaging Technology*, Sept. 2005.

[19] E. Lourandakis, S. Stefanou, K. Nikellis, and S. Bantas, "RF Passives Device Modeling and Characterization in 65 nm CMOS Technology", *14th International Symposium on Quality Electronic Design (ISQED)*, Mar. 2013.

[20] P. Ramm, A. Klumpp, J. Weber, N. Lietaer, M. Taklo, W. De Raedt, T. Fritzsch and P. Couderc, "3D Integration Technology: Status and Application Development", *Proceedings of IEEE ESSCIRC*, Sept. 2010.

[21] Jisso International Council, http://jisso.ipc.org/

[22] K. C. Saraswat, "3-D ICs: Motivation, Performance Analysis, Technology and Applications", *17th IEEE International Symposium on Physical and Failure Analysis of Integrated (IPFA)*, July 2010.

[23] K. H. Koo, P. Kapur, and K. C. Saraswat, "Compact Performance Model and Comparisons for Gigascale On-Chip Global Interconnect Technologies", *IEEE Trans. Electron Devices*, vol. 56, no. 9, pp. 1787-1798, Sept. 2009.

[24] S. Borkar, "Role of Interconnects in the Future of Computing", *Journal of Lightwave Technology*, vol. 31, no. 24, pp. 3927-3933, Dec. 2013.

[25] G. Hernandez-Sosa, G. Romo, and R. Torres-Torres, "Characterization and Modeling of Electronic Packages using S-parameters", *7th International Caribbean Conference on Devices, Circuits and Systems*, April 2008.

[26] R. R. Tummala, "Moore's Law Meets Its Match (System-on-Package)", *IEEE Spectrum*, vol. 43, no. 6, pp, 44-49, June 2006.

[27] H. H. Utsunomiya, "Challenge on Packaging Substrate Technologies Towards Next Decade", *3rd International Microsystems, Packaging, Assembly & Circuits Technology Conference*, Oct. 2008.

[28] M. Swaminathan, and J.M. Pettit, "Going Vertical From More than Moore to Even Mo(o)re", *Interconnects and packaging center (IPC) and Georgia Institute of Technology*, June 2010.

[29] P. Lindner, T. Glinsner, T. Uhrmann,V. Dragoi, T. Planch, T. Matthias, E. Pabo and M. Wimplinger, "Key Enabling Processes for More-than-Moore Technologies", *IEEE International SOI Conference (SOI)*, Oct. 2012.

[30] F. Murray, F. LeCornec, S. Bardy, C. Bunel, J.F.C. Verhoeven, F.C.M. Van den Heuvel, J. H. Klootwijk, and F. Roozeboom, "Silicon Based System-in-Packages: A New Technology Platform Supported by Very High Quality Passive and System Level Design Tools", *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, Jan. 2007.

[31] S. H. Hall, G. W. Hall and McCall, *High-Speed Digital System Design A Handbook of Interconnects Theory and Design Practice*, John Wiley & Sons.

[32] H. W. Johnson, and M. Graham, *High-speed Digital Design a Handbook of Black Magic*, Pearson Education, 2nd Impression 2008.

[33] P. G. Huray, *The Foundations of Signal Integrity*, IEEE Press, A John Wiley & Sons, Inc. Publication 2010.

[34] H. Johnson, M. Graham, *High-Speed Signal Propagation Advanced Black Magic*, Prentice Hall PTR, 2003.

[35] S. Maas, "Circuit Simulation in the Dark Ages", *IEEE Microwave Magazine*, vol. 13, no. 4, pp.89-99, June 2012.

[36] E. Bogatin, *Signal and Power Integrity- SIMPLIFED*, 2nd ED. Prentice Hall, Modern Semiconductors Design Series, Signal Integrity Library, 2010.

CHAPTER 2

[37] K. Lim, M. F, Davis, M. Moonkyun, S. Pinel, W. Lixi, J. Laskar, V. Sundaram, G. White, M. Swaminathan, and R. Tunimala,"Intelligent Network Communicator: Highly Integrated System-on-Packages (SOP) Testbed for RF/Digital/Opto Applications", *Proceeding of the 53rd Electronic Components and Technology Conference*, May 2003.

[38] G. E. Ponchak, A. Margomenos, and L. P. B. Katehi, "Low-loss CPW on Low-Resistivity Si Substrates with a Micromachined Polyimide Interface Layer for RFIC Interconnects," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 5, pp. 866–870, May 2001.

[39] J. A. McCall, and D. Shykind, "Nonideal Frequency Dependent Loss in Realistic PCB Transmission Lines," in *Proceedings on 6th IEEE Workshop on Signal Propagation on Interconnects*, May 2002.

[40] J. C. Rautio, B. J. Rautio, S. Arvas, A. F. Horn, and J. W. Reynolds, "The Effect of Dielectric Anisotropy and Metal Surface Roughness", *Proceedings of Asian-Pacific Microwave Conference*, Dec. 2010,

[41] S. Pytel, P. Huray, S. Hall, R. Mellitz, G. Brist, H Meyer, and M. Garland, "Analysis of cooper Treatments and the Effects on Signal Propagation", *58th Electronic Components and Technology Conference*, May 08.

[42] R. Torres-Torres and V. H. Vega-Gonzalez, "An approach for quantifying the conductor and dielectric losses in PCB transmission lines," in *Proceedings of IEEE 18th Electrical Performance of Electronic Packaging and Systems (EPEPS)*, Nov. 2009.

[43] A. F. Horn, J. W. Reynolds, P. A. LaFrance, and J. C. Rautio, "Effect of conductor profile on the insertion loss, phase constant, and dispersion in thin high frequency transmission lines," *DesignCon*, pp. 1–22, 2010.

[44] J. A. Reynoso-Hernández, "Unified method for determining the complex propagation constant of reflecting and nonreflecting transmission lines," *IEEE Microwave and Wireless Components Letters*, vol. 13, no. 8, Aug. 2003.

[45] J. J. Stickel, "Data smoothing and numerical differentiation by a regularization method," *Computers & Chemical Engineering.*, vol. 34, pp. 467–475, Apr. 10.

[46] B. Curran, I. Ndip, S. Guttowki, and H. Reichl, "A methodology for combined modeling of skin, proximity, edge, and surface roughness effects," *IEEE Trans. Micro. Theory and Tech.*, vol. 58, no. 9, pp. 2448–2455, Sep. 2010.

[47] J. Zhang, J. L. Drewniak, D. J. Pommerenke, M. Y. Koledintseva, R. E. DuBronff, W. Cheng, Y. Zhiping, Q. B. Chen, and A. Orlandi, "Causal RLGC (*f*) models for transmission lines from measured *S*-parameters," *IEEE Transactions on Electromagnetic Compatibility*, vol. 52, no. 1, Feb. 2010.

[48] R. B. Marks, and D. F.Williams, "Characteristic impedance determination using propagation constant measurement," *IEEE Microwave and Guided Wave Letters*, vol. 1, no. 6, pp. 141–143, Jun. 1991.

[49] J. E. Post, "On determining the characteristic impedance of low-loss transmission lines," *Microwave and Optical Technology Letters*, vol. 47, pp. 176–180, Oct. 05.

[50] R. Torres-Torres, S. C. Sejas-García, , "Extraction of the Model Parameters for the Attenuation in Printed Transmission Lines," *IEEE Microwave and Wireless Components Letters*, vol.20, no.12, pp.654,656, Dec. 2010.

[51] C. Chen, R.Wang, Y. Su, and T. Hsueh, “A nanocrystalline silicon surfacepassivation layer on an HR-Si substrate for RFICs,” *IEEE Electron Device Letters*, vol. 32, no. 3, pp. 369–371, Mar. 2011.

[52] L. Tran, D. Pasquet, E. Bourdel, and S. Quintanel, “CAD-oriented model of a coplanar line on a silicon substrate including eddy-current effects and skin effect,” *IEEE Trans. Microwave Theory and Tech.*, vol. 56, no. 3, pp. 663–670, Mar. 2008.

[53] H. Kim, and Y. Eo, “High-frequency-measurement-based frequency-variant transmission line characterization and circuit modeling for accurate signal integrity verification,” in *Proceeding of the 8th International Symposium on Quality Electronic Design*, pp. 507–512, Mar. 2007.

[54] A. Schellmanns, J. Keradec, and J. Schanen, “Electrical equivalent circuit for frequency dependant impedance: Minimum lumped elements for a given precision,” in *Proc. of Industry Applications Conference*, vol. 5, pp. 3105–3115, Oct. 2000.

[55] R. Torres-Torres, R. Venegas, and S. Decoutere, “Transmission line characterization on silicon considering arbitrary distribution of the series and shunt pad parasitics,” *Solid-State Electron.*, vol. 54, no. 3, Mar. 2010.

[56] A. P. Duffy, A. J. M. Martin, A. Orlandi, G. Antonini, T. M. Benson, and M. S. Woolfson, “Feature selective validation (FSV) for validation of computational electromagnetics (CEM). Part I—The FSV method,” *IEEE Transaction on Electromagnetic Compatibility*, vol. 48, no. 3, pp. 449–459, Aug. 2006.

[57] A. Orlandi, A. P. Duffy, B. Archambeault, G. Antonini, D. E. Coleby, and S. Connor, “Feature selective validation (FSV) for validation of computational electromagnetics (CEM). Part II—Assessment of FSV performance,” *IEEE Trans. Electromagn. Compat.*, vol. 48, no. 3, pp. 460–467, Aug. 2006.

[58] D. Kaller, C. Schuster, Y. Kwark, D. Altabella, B. Truong, Z. Chen, A. Haridass, and E. Klink, “Using *S*-parameters successfully in time domain link simulations,” in *Proceeding on IEEE 14th Topical Meeting on Electrical Performance of Electronic Packaging*, pp. 95–98, Oct. 2005.

[59] S.C. Sejas-Garcia, R. Torres-Torres, R. S. Murphy-Arteaga, "Modeling Transmission Lines on Silicon in the Frequency and Time Domains from S-Parameters," *IEEE Transactions on Electron Devices*, vol.59, no.6, pp.1803-1806, June 2012.

CHAPTER 3

[60] V. Camarchia, V. Teppati, S. Corbellini, M. Pirola, "Microwave Measurements Part I Non-linear Measurements," *IEEE Instrumentation & Measurement Magazine*, vol. 10, no.3, pp.34-39, June 2007.

[61] A. Davidson, K. Jones, and E. Strid, "LRM and LRRM Calibrations with Automatic Determination of Load Inductance," *Proceedings of 36th ARFTG Conference Digest-Fall*, vol.18, pp.57-63, Nov. 1990.

[62] E. Holzman, "*Essential of RF and Microwave Grounding*", Artech House, 2006.

[63] G. F. Engen, and C.A. Hoer, "Thru-Reflect-Line: An Improve Technique for Calibrating the dual Six-Port Automatic Network Analyzer", *IEEE Transaction on Microwave Theory and Techniques*, vol. 27, no. 12, pp. 987-993, Dec. 1979.

[64] A. M. Mangan, S. P. Voinigescu, M. T. Yang, and M. Tazlauanu, "De-Embedding Transmission Lines Measurements for Accurate Modeling of IC Designs", *IEEE Transactions on Electron Devices*, vol. 53, no. 2, pp. 235-241, Feb. 2006.

[65] J. Stenarson, K. Yhland, "A Reformulation of TRL and LRM for S-Parameters," *Microwave Measurement Conference*, pp.1-4, Jun. 2009.

[66] L. Tiemeijer, R. Havens, A. Jansman, Y. Bouttement, "Comparison of the "Pad-Open-Short" and "Open-Short-Load" Deembedding Techniques for Accurate On-Wafer RF Characterization of High- Quality Passives," *IEEE Transaction on Microwave Theory and Techniques*, vol.53, no.2, pp.723-729, Feb. 2005.

[67] R. Torres-Torres, R. Murphy-Arteaga, J. Reynoso-Hernandez, "Analytical Model and Parameter Extraction to Account for the Pad Parasitics in RF-CMOS," *Transaction on Electron Devices*, vol.52, no.7, pp.1335- 1342, Jul. 2005.

[68] Y. Kuo-Liang, G. Jyh-Chyurn, "A New Method for Layout-Dependent Parasitic Capacitance Analysis and Effective Mobility Extraction in Nanoscale Multifinger MOSFETs," *Transactions on Electron Devices*, vol.58, no.9, pp.2838-2846, Sept. 2011.

[69] C. Hanjin, D. Burk, "A three-step Method for the De-Embedding of High-Frequency *S*-Parameter Measurements," *Transaction on Electron Devices*, vol.38, no.6, pp.2838-2846, Jun. 1991.

[70] M. Drakaki, A. Hatzopoulus, S. Siskos, “De-Embedding Method for On-Wafer RF CMOS Inductor Measurements,” *Microelectronics Journal*, vol. 40, pp. 958-965. Feb. 2009.

[71] S. C. Sejas-Garcia, and R. Torres-Torres, “Deembedding On-Wafer *S*-Parameters: Is a One-Step Procedure Enough?” in *Proceeding on XVII IBERCHIP*, pp. 174–178, Feb. 29–Mar. 2, 2012.

[72] C. Hwang, Y. Shim, K. Koo, M. Kim, J. S. Pak, and J. Ki “An On-Chip Electromagnetic Bandgap Structure using an On-Chip and a MOS Capacitor”, *IEEE Microwave and Wireless Components Letters*, vol. 21, pp. 439–441, Aug. 2011.

[73] T. Deng, Z. Chen and Y. Zhang, “Electromagnetic interactions of on-chip antennas and inductors” in *Proceeding of Asian-Pacific Microwave Conference (APMC)*, Dec. 2012.

[74] Yutaka Aoki and Kazuhiko Honjo, “Q-factor Definition and Evaluation for Spiral Inductors Fabricated using Wafer-Level CSP Technology”, *IEEE Transaction on Microwave Theory and Techniques*, vol. 53, pp. 3178–3184, Oct. 2005.

[75] H. L. Kao, C. S.Yeh, L. C. Chang, J. S. Fu, and H. C. Chiu, “Improvement of the Q-Factor for an Adjustable Inductor using a 90-μm Silicon Substrate on Plastic”, *International Journal Electronics*, vol. 98, pp. 1597–1607, Nov. 2011.

[76] C.H. Huang, and T.-S. Horng, “Q-Factor Behavior Study of On-Chip Inductors Using Transmission-Line Model”, *Proceeding of Asian-Pacific Microwave Conference, Dec. 2007*.

[77] G. VanAckern, R. J. Baker, A. J. Moll and V. Saxena “On-chip 3D inductors using thru-wafer vias”, *IEEE Workshop on Microelectronics and Electron Devices (WMED)*, Apr. 2012.

[78] A. Zolfaghari, A. Chan, B. Razavi, “Stacked Inductors and Transformers in CMOS Technology”, *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 620–628, Apr. 2001.

[79] Y. Aoki, S. Shimizu, and K. Honjo, "Novel Design Method for Electrically Symmetric High-Q Inductor Fabricated using Wafer-Level CSP Technology", *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 3, pp.31–39, Jan. 2013.

[80] L. N. Tran, E.Bourdel, S. Quintanel, and D. Pasquet, “New Extraction Method of an Equivalent Circuit for an Inductor in BiCMOS Technology Including Lossy Effects”, *International Journal of Microwave Wireless Technologies* , vol. 2, pp. 523–530, Mar. 2010.

[81] S. C. Sejas-Garcia, R. Torres-Torres, L. C. Moreira, "Systematic modeling and parameter extraction for on-chip inductors in CMOS technology," *SBMO/IEEE MTT-S International Microwave & Optoelectronics Conference (IMOC),* vol., no., pp.1,5, 4-7 Aug. 2013

CHAPTER 4

[82] T. M. Pan, C. H. Chen, J. H. Liu, J. L. Her, and K. Koyama, "Electrical and Reliability Characteristics of High-κ HoTiO3 α–InGaZnO Thin-Film Transistors," *IEEE Electron Device Letters*, vol. 35, no.1, Jan. 2014.

[83] W. Chen, K. McCarthy, A. Mathewson, M. Copuroglu, S. O'Brien and R. Winfield, "Capacitance and S-parameter Techniques for Dielectric Characterization with Application to High-κ PMNT Thin-Film Layers," *IEEE Transactions on Electron Devices*, vol. 59, no. 6, pp. 1723−1729, Jun. 2012.

[84] N. Orloff, J. Mateu, M. Murakami, I. Takeuchi, and J.C. Booth, "Broadband Characterization of Multilayer Dielectric Thin-Films," *IEEE/MTT-S International Microwave*, Jun. 2007.

[85] Z. Ma, A.J. Becker, P. Polakos, H. Huggins, J. Pastalan, H. Wu, K. Watts, Y.H. Wong, and P. Mankiewich, "RF Measurement Technique for Characterizing Thin Dielectric Films", *IEEE Transaction on Microwave Theory and Techniques*, vol. 45, no. 8, pp. 1811–1816, Aug. 1998.

[86] M. P. J. Tiggelman, K. Reimann, J. Liu, M. Klee, W. Keur, R. Mauczock, J. Schmitz and R.J.E. Hueting, "Identifying Dielectric and Resistive Electrode Losses in High-Density Capacitors at Radio Frequencies," *IEEE International Conference on Microelectronic Test Structures*, Mar. 2008.

[87] J. Choi, J. Kim, and T. Oh, "Dielectric Properties and Leakage Current Characteristics of Al2O3 Thin Films with Thickness Variation", in *Proc. 2001 MRS Spring Meeting*, Apr. 2001.

[88] S. Sejas-García, R. Torres-Torres, R. Valderrama-B, J. R. Molina, "Complex Permittivity Determination of Thin-Film Through RF-Measurements of a MIM Capacitor", *IEEE Microwave Wireless Components Letters*, vol. PP no. 99