ELectronics EXpress

IEICE Electronics Express, Vol.8, No.23, 1967–1971

Noise margin and short-circuit current in FGMOS logics

Luis F. Cisneros-Sinencio[1a)], **Alejandro Diaz-Sanchez**[1], **and Jaime Ramirez-Angulo**[2]

[1] *National Institute for Astrophysics, Optics and Electronics*
Tonantzintla, Puebla, Mexico

[2] *New Mexico State University*
Las Cruces, NM, USA

a) *lcisneros@inaoep.mx*

Abstract: Even when floating-gate logics are very-low-voltage circuits, as power supply is reduced, large fan-in FGMOS gates are prone to fail. Thus, determining the negative impact of noise margin and short-circuit current in this type of circuits is crucial to achieve optimal operation for a particular application. For this reason, a systematic and reliable technique for obtaining the correlation between fan-in and supply voltage, simultaneously considering noise margin and short-circuit current, is proposed.

Keywords: floating-gate logic, noise margin, FGMOS transistor
Classification: Integrated circuits

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DOI: 10.1587/elex.8.1967
Received October 05, 2011
Accepted October 26, 2011
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1 Introduction

Currently, power consumption is becoming a critical issue in modern digital circuit design due to the increasing demand of portable devices [1]. Hence, exploring new techniques for energy-efficient digital circuits is necessary. In this tendency, the use of multiple-input floating-gate MOS (FGMOS) transistors is an attractive alternative due to the fact that only passive devices are involved (i.e. a capacitive network) in the corresponding data processing, achieving virtually no power dissipation [2]. In this case, the weighted sum of the input voltages controls the channel of the FGMOS transistor. Therefore, to achieve the evaluation and give a valid digital output, a comparator is needed. In this regard, very compact low-voltage comparators using only two transistors have been proposed [3] since reduced transistor count and low-voltage is the most straightforward way to achieve low power [4].

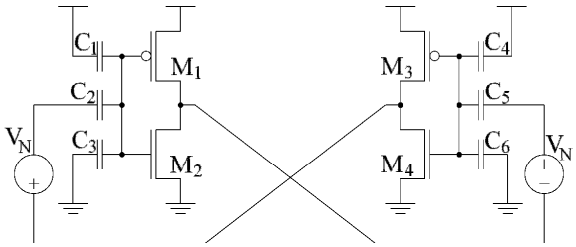
FGMOS logics have demonstrated to be very versatile circuits [5]. This versatility is because this logic style processes information in such a way that enhancing gate complexity is possible just by adding input capacitors [6]. Notwithstanding, increasing the input count introduces some problems that affect both, the stability of the gate and the most important feature of floating-gate circuits: low power. For this reason, to give a scope about how fan-in affects floating-gate logics performance, an analysis of noise margin and short-circuit current is carried out. These figures of merit will be the comparing axis while different fan-in logic gates are analysed. This analysis will set reference points to help in the design of FGMOS logic circuits.

2 Methodology

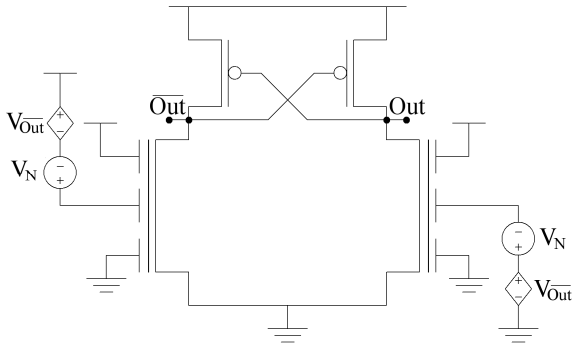
Results were obtained from SPICE simulations under an IBM 90 nm CMOS process technology for different fan-in FGMOS gates. A minimum length of 100 nm and widths of 120 nm for p-MOS and 240 nm for n-MOS transistors were used for all the simulations. The input capacitances were 0.5 fF in all the cases. To show the effect of voltage reduction over the comparison, power supply voltages (V_{dd}) of 1.2 and 0.8 volts were used. For each FGMOS gate, only one of the inputs is connected to a data source while the rest are tied to the power rails; this will show the effect of only one input over the output. In addition, to achieve realistic results, the simulation technique for FGMOS circuits discussed in [7] is used. Compensation capacitors can be

DOI: 10.1587/elex.8.1967
Received October 05, 2011
Accepted October 26, 2011
Published December 10, 2011

added to induce a dc level in the floating-gate to achieve the best performance possible, as in real FGMOS circuits. However, compensation capacitances will not count as inputs as they cannot be used for data computation. As the value of these capacitors is discrete, the induced DC level is slightly above or below the optimum point. This is reflected as a scattered shape in the graphics representing the simulation results, which is more evident as the gain of the comparator used by the logic style is made larger. In the comparison, two different FGMOS logic styles were used: Floating-Gate Complementary MOS transistor logic (FG-CMOS) [8] and Positive-Feedback Floating-Gate Logic (PFFGL) [9]. Using a single ended and a differential FGMOS logic provides information about the influence of the gate architecture on both, noise margin and short-circuit current.



(a)



(b)

Fig. 1. Flip-flop circuit to measure noise margin; for a 3-input FG-CMOS gate (a), for a 3-input PFFGL gate (b).

Regarding noise margin, it is defined as the smaller difference between the input and output low voltages (i.e., VIL-VOL) and the input and output high voltages (i.e., VIH-VOH). To measure this difference, the flip-flop method discussed in [10] is used. For FG-CMOS, two feedback gates are used as shown in Fig. 1a. The voltage sources V_N represent the noise sources and will be increased until a change at the output of any of the gates occurs. The value of V_N at which this change occurs is the noise margin of the gate. As for PFFGL, the flip-flop is already embedded in the gate; it would only be necessary to feed the outputs back to their complementary inputs. Since PFFGL shows degradation only at high output, and it is only sensitive to

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Received October 05, 2011
Accepted October 26, 2011
Published December 10, 2011

degradation in low inputs, a modification to the flip-flop method is necessary. This modification uses a unitary-gain voltage-controlled voltage source to feed the degradation of the output in high back to their inputs, as shown in Fig. 1b.

On the other hand, short-circuit current is defined as the difference between the static direct current (DC) of the gate when all of their transistors are completely on or completely off and the maximum static DC current. This difference will be obtained by subtracting the DC current while all the inputs are zero to the DC current while the input vector for the worst case noise margin is applied.

3 Simulation results

Fig. 2 shows noise margin for different fan-in gates. As PFFGL uses positive feedback to increase the comparator gain, better characteristics than FG-CMOS are achieved. However, if the input count is bigger than 9 at 1.2 V, noise margin degradation can be such that signal regeneration be required. Moreover, when V_{dd} is reduced to 0.8 V, the comparator gain is abridged, degrading noise margin. Under this voltage, if the fan-in goes above 5, noise margin reaches a minimum in such a way that it would be impossible to restore by any means. As the gain of the FG-CMOS comparator is smaller than PFFGL, noise margin degradation increases. For this logic, output regeneration is necessary even for gates with small input count. Nonetheless, if input count goes above 3, noise margin is so degraded that the output could not be regenerated with correction circuits even at 1.2 v. Furthermore, for gates with a fan-in greater than 7, no valid output is obtained at any of the voltages applied during the experiment.

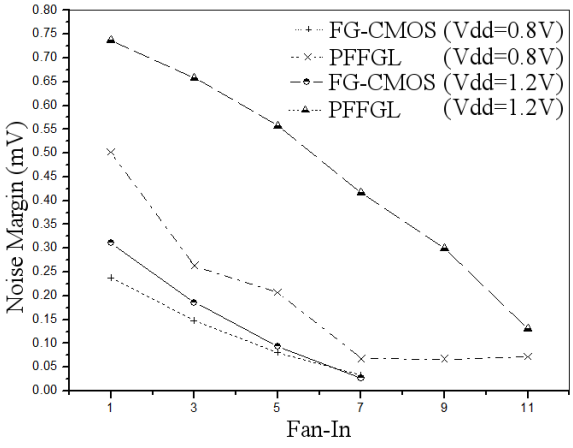

Fig. 2. FG-CMOS and PFFGL noise margin for different fan-in gates.

An increase of the input count arises the probability to have a floating-gate voltage that simultaneously turns on all the transistors in the gate, establishing a discharge path from V_{dd} to ground. This phenomenon is illustrated in the graphic in Fig. 3, which shows that increasing the input count

DOI: 10.1587/elex.8.1967
Received October 05, 2011
Accepted October 26, 2011
Published December 10, 2011

increases the short-circuit current. Furthermore, being single ended, FG-CMOS logic shows better characteristics than PFFGL at any V_{dd}; besides, differential logics have two discharge paths; these paths are bootstrapped, making more likely to have complementary transistors turned on simultaneously.

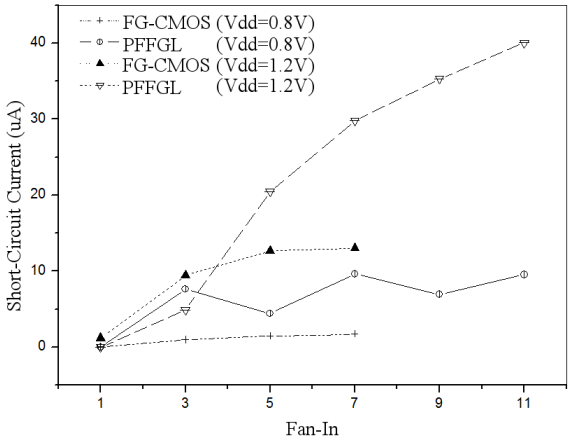

Fig. 3. Short-circuit current for different fan-in FGMOS gates.

From the previous graphic, it can be seen that increasing the input count at a given voltage will inevitably lead to a constant current flowing between the power rails, increasing total power dissipation. To diminish this unwanted phenomenon, power source voltage must be reduced as fan-in is increased. However, if V_{dd} is reduced, noise margin will be degraded. In this case, output buffers can be used in order to restore noise margin while lowering V_{dd}. Notice, however, that even though output buffers consume energy, this consumption occurs only when changing the output state, whereas short-circuit current occurs continuously as long as the conditions that simultaneously turn on the transistors exist. Nevertheless, in sub-micrometric fabrication processes, static current leakage dominates the total power dissipation, making the leakage at the output buffer transistors comparable to the short-circuit current. In either case, the designer must evaluate the advantage of adding restoring circuits.

4 Conclusions

In this paper, a study of noise margin and short-circuit current in floating-gate logics is presented. Both figures of merit show how increasing fan-in affects the performance of FGMOS logics. According to the comparison, gates with high complexity are prone to fail due to noise margin degradation if low voltage is used. This establishes a trade-off between two of the principal advantages of floating-gate logics: high-complexity and low-voltage. Alternatively, using buffers at the output restores noise margin degradation, allowing the construction of large fan-in logic gates reliable at low voltage. If that is the case, the designer must evaluate the penalty in power consumption.

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Received October 05, 2011
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