Analog Integr Circ Sig Process (2012) 70:249–263
DOI 10.1007/s10470-011-9789-0

Delay sensing for long-term variations and defects monitoring in safety–critical applications

J. C. Vazquez · V. Champac · A. M. Ziesemer Jr. · R. Reis · I. C. Teixeira · M. B. Santos · J. P. Teixeira

Received: 4 May 2010 / Revised: 17 June 2011 / Accepted: 17 September 2011 / Published online: 7 October 2011

Abstract The impact of parametric variations on digital circuit performance is increasing in nanometer Integrated Circuits (IC), namely of Process, power supply Voltage and Temperature (PVT) variations. Moreover, circuit aging also impacts circuit performance, especially due to Negative Bias Temperature Instability (NBTI) effect. A growing number of physical defects manifest themselves as delay faults (at production, or during product lifetime). On-chip, on-line delay monitoring, as a circuit failure prediction technique, can be an attractive solution to guarantee correct operation in safety–critical applications. Safe operation can be monitored, by predictive delay fault detection. A delay monitoring methodology and a novel delay sensor (to be selectively inserted in key locations in the design and to be activated according to user's requirements) is proposed, and a 65 nm design is presented. The proposed sensor is programmable, allowing delay monitoring for a wide range of delay values, and has been optimized to exhibit low sensitivity to PVT and aging-induced variations. Two MOSFET models—BPTM and ST—have been used. As abnormal delays can be monitored, regardless of their origin, both parametric variations and physical defects impact on circuit performance can be identified. Simulation results show that the sensor is effective in identifying such abnormal delays, due to NBTI-induced aging and to resistive open defects.

Keywords Delay sensors · Reliability in nanometer technologies · Failure prediction · Process variations · Predictive delay fault detection

J. C. Vazquez · A. M. Ziesemer Jr. · I. C. Teixeira · M. B. Santos · J. P. Teixeira (✉)
INESC-ID - Instituto de Engenharia de Sistemas e Computadores, Investigação e Desenvolvimento, Lisbon, Portugal
e-mail: paulo.teixeira@ist.utl.pt

J. C. Vazquez
e-mail: jcvazquez@inaoep.mx

A. M. Ziesemer Jr.
e-mail: amziesemerj@inf.ufrgs.br

I. C. Teixeira
e-mail: isabel.teixeira@ist.utl.pt

M. B. Santos
e-mail: marcelino.santos@ist.utl.pt

J. C. Vazquez · V. Champac
INAOE (Instituto Nacional de Astrofísica, Óptica y Electrónica), Tonantzintla, Puebla, Mexico
e-mail: champac@inaoep.mx

A. M. Ziesemer Jr. · R. Reis
UFRGS (Univ. Fed. Rio Grande do Sul), PGMicro – Inst. Informática, Porto Alegre, Brazil
e-mail: reis@inf.ufrgs.br

I. C. Teixeira · M. B. Santos · J. P. Teixeira
IST (Instituto Superior Técnico), UTL, Lisbon, Portugal

M. B. Santos
SiliconGate, Lisbon, Portugal

1 Introduction

For safety–critical systems (e.g., in the automotive market), digital system errors are unacceptable. Human lives are in stake. Reliable and dependable system operation is, thus, mandatory. In high-performance systems, the pace at which digital signal processing is carried out must be the fastest the physical system is able to deliver. Process variations and the majority of physical defects can be identified at production stage. Other parametric variations, namely power supply Voltage and Temperature (VT)

variations, are operation-dependent, and difficult to predict, at the design stage, namely those resulting from non-uniform IR drops in power lines, and thermal gradients. Low-power design requires lowering the power supply voltage, V_{DD}, down to the 1 V domain, or less, which leads to dramatic impact on current density across the chip. Meanwhile, minimum MOS threshold voltage (V_{th}) is limited by leakage, eroding noise margins and making circuits more sensitive to VT variations [1]. Process, power supply Voltage and Temperature (PVT) variations impact circuit performance.

Moreover, many safety–critical applications products must operate for long periods of time. For instance, in the automotive market, electronic systems must be dependable during 10 years, for cars, 15 years, for trucks. Therefore, electronic aging [2], causing long-term performance degradation, must also be considered, and should be monitored, during product lifetime. In nanometer technologies, reliability problems increase [3, 4], as well as variability [5]. Long-term circuit operation may also activate physical defects which were latent at production time. This can also be viewed as an aging effect.

On-chip, on-line delay monitoring can be used to predict catastrophic time response and, thus, to prevent harm. We refer this as *predictive delay fault detection*. In this context, a delay fault is any abnormal timing response that exceeds a given time threshold, regardless of its origin (PVT variations, aging, or activated physical defects). Hence, predictive delay fault detection allows us to identify unsafe timing behaviour *prior* a timing failure really occurs in digital system operation.

The purpose of this paper is twofold. First, a methodology for delay monitoring of safety–critical digital systems is proposed. The proposed methodology allows safe and dependable circuit operation, regardless of the abnormal delay's origin—operation-dependent VT conditions, aging or physical defects. Second, a novel programmable delay sensor, resilient to PVT and aging variations, is presented. A 65 nm sensor design is studied, using two MOSFET models—the publicly available Berkeley Predictive Transistor Model (BPTM) [6] and the one in the design kit of a commercial CMOS technology (ST [7]). The proposed sensor is programmable, and proved to be (1) more cost-effective and (2) more resilient to PVT variations than the Agarwal et al. sensor [8]. A part of an industrial design is used as Circuit Under Test (CUT) to ascertain the effectiveness of the proposed delay sensor.

The paper is organized as follows. Sect. 2 briefly reviews PVT and aging variations, and their impact on system performance. Section 3 introduces the proposed delay monitoring methodology. In Sect. 4, the delay sensor architecture is introduced and discussed. Section 5 briefly looks into the sensor's physical design. In Sect. 6, extensive simulation results are presented. Currently, a test chip is being taped out. Finally, Sect. 7 summarizes the conclusions and directions for further research.

2 PVT and aging-induced variations

Nanometer semiconductor products face many challenges [1, 5]. Power supply noise is operation-dependent, and has a direct impact on circuit performance [9]. Its effect becomes more relevant, as V_{DD} scales down. Operation-dependent power consumption creates dynamic thermal maps along the die, which also modulate system timing response [10]. Parametric variations tend to increase with device scaling down and with system complexity. As a result, the safety margins associated with worst-case (WC) PVT variations become too wide, leading to unacceptable performance degradation in high-performance applications. Moreover, electronic systems with long operation times exhibit long-term parametric variations, namely MOS threshold voltage (V_{th}) shifts, leading to performance degradation [4]. Aging creates permanent, slowly drifting footprints on system performance. Beyond a certain limit, system errors will occur. This must be avoided in safety–critical applications.

Negative Bias Temperature Instability (NBTI) has been identified as a dominant long-term effect in nanometer CMOS technologies [4]. NBTI has long been recognized as a reliability problem, and modeled by the classic Reaction Diffusion model [11] as $V_{thP} \sim t^n$, where t is time, and $n \approx 1/6$ [12]. NBTI modeling is, however, a challenging task, due to the fact that many factors contribute to the degradation process, namely temperature and/or electric field dependencies—thus, ultimately, the degradation process depends also on VT conditions. NBTI primarily affects PMOS transistors, when they are ON, increasing $|V_{thP}|$ along the time. V_{thP} degradation depends on time and on each PMOS device workload, which depends on circuit operation, difficult to predict in the design environment. Static workload (always ON PMOS) leads to increased V_{thP} degradation, while dynamic workload reduces such degradation, due to an annealing effect on thin oxide charge trapping [13]. It has been shown that NBTI can also modulate the majority carrier mobility, μ_p [14]. However, in this work we model the impact of NBTI on circuit performance by assuming that an equivalent (and uniform) V_{thP} degradation value can encapsulate all the additional relevant effects (μ_p, T, etc.). Non-uniform V_{thP} modulation can also be performed (increasing circuit simulation costs). However, this effect does not change the major conclusions of this work; hence, it is not included for the sake of simplicity. In order to accommodate possible delay variations caused by PVT variations, a time slack (τ_{slack}) is

routinely included in the clock signal period. τ_{slack} is defined as the time period exceeding the longest propagation delay time between memory elements, thus added to accommodate parametric variations. V_{thP} degradation erodes the time slack and, ultimately, will cause a delay fault.

Beyond NBTI, other aging effects, namely Hot Carrier Injection, Time Dependent Dielectric Breakdown (TDDB), Electro Migration and Stress Migration, can occur in nanometer IC technologies [15, 16]. The cumulative effect of these aging mechanisms is difficult to predict, at the design stage, especially for new node technologies. For instance, TDDB, resulting from stress due to the electric field in the thin oxide gate regions, typically induces a slow degradation, and then, over time, a sharp increase on the timing degradation, eventually the oxide breakdown [17]. As referred, in this work, NBTI is assumed to be the dominant aging effect. However, as abnormal delay monitoring is performed, other aging effects may occur and thus can also be detected by the proposed delay sensor.

Furthermore, long-term circuit operation can slowly transform latent physical defects into hard defects. In fact, defect size tends to increase with time. For instance, resistive open vias will exhibit increasing resistance value over time. Hence, *prevention* of in-field catastrophic failures due to latent defects must also be carried out. This also can be performed, by on-line delay monitoring.

The impact of NBTI on digital circuit *performance* has been under research [4, 18]. NBTI in static and dynamic operation has been modeled [13]. Recently, Agarwal et al. proposed a *circuit failure prediction* technique [8] and an aging sensor. They also presented its use on an experimental test chip [19]. Their major application was to reduce the pessimistic worst-case analysis associated with PVT variations. Nakura et al. [20] also proposed aging sensing, using what they refer as defect-prediction Flip-Flops. However, the area overhead is too large.

Recently, an aging monitoring methodology, to be used *during product lifetime*, has been proposed [21], together with a new 0.35 μm CMOS sensor design, which exhibits a much lower sensitivity to VT variations than the Agarwal et al. sensor [8]. However, the complexity of the sensor's architecture leads to a relevant area overhead, which limits the application of the sensor in real products. Moreover, its topology may be inadequate for nanometer designs. A new sensor topology, adequate for nanometer designs, has been proposed in [22, 23] and extensively discussed in this paper.

3 Delay monitoring methodology

For safety–critical applications, we propose to monitor the degrading timing response using on-line *built-in delay sensors*. In order to constrain Silicon area overhead, sensor area and sensor insertion should be as limited as possible. Sensors may be activated either on user's requirement, or at pre-defined situations (e.g., at power-up), to detect abnormal delays in critical paths, *before* they become catastrophic. Sparse sensor activation in time is effective, as sensors must monitor slowly drifting long-term effects. Occasional sensor activation has two advantages: it limits sensor aging (as it depends on the workload of their PMOS transistors) and power consumption overhead. If the timing degradation exceeds a given threshold, some preventive action is triggered, based on sensor's data, avoiding harm.

Being on-chip, the sensors must exhibit low sensitivity to operational conditions, namely to VT variations. In nanometer technologies, process variability is very large. Hence, the sensor must also exhibit low sensitivity to process (P) variations. Finally, in order to allow delay monitoring for a range of delay values, even in the presence of PVT or aging-induced variations, the sensor should be *programmable*. This allows the sensor to be able to detect a set of user's defined delay thresholds, and to trigger different actions, according to the severity of threshold violation (e.g., warning, or system driven to a safe state).

As shown in Fig. 1, the proposed delay monitoring methodology comprises two processes: (1) development of a *sensor insertion technique* and an algorithmic approach for automatic netlist reconfiguration, and (2) development of cost-effective delay sensors, accommodated in new library cells, by merging delay sensors with storage elements (FF).These delay sensors must also be resilient to PVT and aging-induced variations. This paper focuses process (2) and its effectiveness in monitoring the influence of NBTI and latent defects on circuit performance. Nevertheless, the essentials of process (1) are outlined, as follows.

A sensor insertion technique requires *sensor insertion criteria.* Limited sensor insertion must be carried out at the

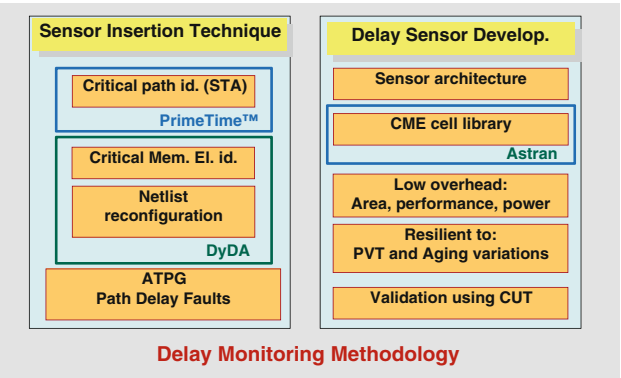

Fig. 1 Proposed delay monitoring methodology

output of each Circuit Under Test (CUT) critical path (CP). CPs are signal paths exhibiting long propagation delay times (t_{pd}). Assume that the signal path with the longest delay time has, in nominal PVT conditions, a propagation delay time, t_{pdCP}. Due to PVT or aging-induced variations, sensors must be inserted at the end of all the longest signal paths, for which $t_{pd} \geq \alpha.t_{pdCP}$. This alpha is a user defined parameter (e.g., $\alpha = 0.9$) and it allows to select the set of "critical paths" to be monitored due to the aging issue. In synchronous design, logic cones end with memory elements (FF) that capture processed data. Many critical or near-critical paths end at the same FF. Hence, the total number of sensors to be inserted is by far lower than the number of signal paths for which $t_{pd} \geq \alpha.t_{pdCP}$.

Long signal paths are identified with a Static Timing Analysis (STA) tool, like PrimeTime^{TM}. A more restrictive criterion can be used, to reduce overhead. For instance, if the primary cause of delay shifting is NBTI-driven aging, an aging-aware (NBTI-aware) STA procedure can be followed, as proposed in [19]. Nevertheless, a general STA tool has the advantage of being unbiased, as regard to the exact aging phenomena. Although bearing in mind that a trade-off must exist, unbiased STA used with reasonable α can better accommodate all aging phenomena.

The sensor insertion technique encompasses additional steps, besides STA. After STA, *critical memory elements* identification is required. *Critical memory elements* are those registers ending critical or near-critical paths, for which sensor insertion is needed. For this, a proprietary Dynamic Delay Analyser (DyDA) tool [23] generates the CUT's *delay map,* identifying the critical paths ending the logic cones of each memory element, and ranking them from the slowest to the fastest. According to user's defined α, a subset of memory elements is thus identified, where delay sensors are to be added. Typically, for low area overhead, new library cells, merging the memory cell (FF) and the delay sensor, are developed and made available.

The DyDA tool also automatically performs the third step, namely netlist reconfiguration. In fact, it reconfigures the CUT netlist, by replacing ordinary FF with these new cells. Typically, for $\alpha = 0.9$, around 10% of the CUT memory elements require a delay sensor. The exact number of sensors to be inserted is relevant, in terms of overhead; however, this is dependent on CUT topology.

Finally, for design verification, some test pattern generation must be carried out, to guarantee that, when critical or near-critical paths are activated, the sensor correctly detects the abnormal delays, according to pre-defined threshold time values (programmable sensor). If deterministic test sequences are to be derived, Automatic Test Pattern Generation (ATPG) for path delay faults associated with the identified critical (or near-critical paths) must be carried out.

The proposed methodology is a circuit failure *prediction* technique and reuses several concepts presented in [8, 19, 21]. As stated, sensors detect abnormal delays, *regardless of their origin*. Hence, they can uncover (1) PVT variations and/or aging-induced variations (namely, due to NBTI) and (2) delay faults due to physical defects activated by long circuit operation. Thus, sensor's insertion enhances the internal observability of the CUT timing degradation, before it is too late. It can be viewed as a Test Point Insertion technique. We refer it as *predictive delay detection*. Anyway, according to available data, NBTI is the dominant aging effect. Hence, on-line delay monitoring is carried out by the sensors, optimized to exhibit low sensitivity to VT variations, and to NBTI effects. The CUT will have embedded on-line delay monitors in key locations, so predictive delay fault detection can be performed, regardless of the aging mechanism (or of the combination of mechanisms) responsible for the abnormal delay.

4 Delay sensor

The delay sensor defines an *observation interval*, T_g. (referred as guardband interval in [8]) and monitors if critical path's output signal (OUT_CL) *transitions* occur during T_g. The sensor is inserted in parallel with the FF that registers OUT_CL, as shown in Fig. 2. Merging the FF (the critical memory element) with the delay sensor leads to a new library cell. The T_g period is synchronized with the clock signal, and defines the *unsafe operation region*. When an abnormal delay of OUT_CL occurs, OUT_CL transitions ($0 \rightarrow 1$ or $1 \rightarrow 0$) may occur within the unsafe region. In this case, *predictive* delay fault detection is performed by the sensor, and the sensor's output signal (OUT_AS) goes HIGH, flagging a warning signal. The unsafe operation region should be defined by different threshold delays. Hence, in order for the sensor to be *programmable*, the pulse width (i.e., the value of T_g) is programmable. In our current implementation, a three bit

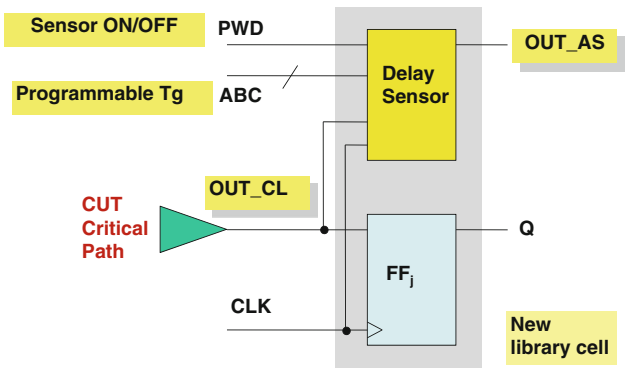

Fig. 2 CUT critical path and aging sensor interconnection

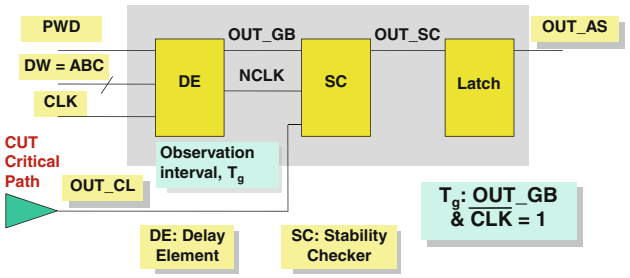

Fig. 3 Aging sensor architecture and observation interval (T_g) definition (OUT_GB = CLKN = 1)

digital word DW = ABC is used. The sensor is shut-off by PWD (power down) signal.

Figure 3 shows the sensor architecture, composed of three blocks. The *observation interval*, T_g, is generated by the *delay element (DE),* the input block of the proposed delay sensor. T_g period is defined as the time interval during which OUT_GB = 1 and $\overline{CLK}$ = CLKN = 1 (output signals of DE). The stability of OUT_CL within T_g is analyzed by the *stability checker* (*SC*), the second block. As shown below, the SC will limit the observation interval, leading to an *effective guardband interval, T_{geff},* lower than T_g. In fact, the effective observation interval depends on the setup/hold times of the SC. Anyway, as T_g is programmable, the effect of T_g degradation due to the SC can be compensated. An output latch (third block) stores the checker results. If, due to an abnormal propagation delay time, OUT_CL switches *during* the effective observation interval, OUT_SC goes HIGH, this logic value is latched and the sensor's output goes HIGH (OUT_AS = 1).

4.1 Delay element

The proposed delay sensor introduces a novel DE architecture, as compared to the sensors presented in [8, 20]. The new delay element retains the delay generation concept [21] using the charging/discharging time of a capacitor. However, a non-linear capacitor is used (MOSCAP-NP), composed of a NMOS and a PMOS transistor in parallel. This structure, referred as Complementary Gate Capacitor (CGC) in [24], exhibits low sensitivity to V_{DD} variations. Using a 2-MOSFET structure also reduces DE sensitivity to process variations. However, the current source/current mirror solution [21] is dropped, and substituted by a simple pull-down (PD) programmable network, leading to significant silicon area savings. The previous solution [21] exhibits extremely low sensitivity to VT variations, due to the use of current sources and mirrors. The new DE topology has a slightly increased sensitivity to VT variations. However, it does not compromise the sensor's correct functionality in safety–critical applications.

Figure 4 shows the novel DE circuit topology. Its main functionality is to generate the OUT_GB signal, which is synchronized by the CLK signal. The T_g period has a *rising edge*, associated with the discharging of node X, and a *falling edge*, associated with the rising edge of the clock signal—when $\overline{CLK}$ goes to LOW. By modifying the strength of the X node pull-down network, through DW = ABC, the sensor can be programmed to define variable width T_g periods.

The proposed delay sensor is a *built-in* delay sensor; hence, it is also affected by circuit aging. In order to constrain this undesired feature, two measures are taken. First, the sensor is normally OFF; in fact, it will be activated only from time to time, as the goal is to observe long-term drifts in circuit performance. In the OFF state, the sensor is designed in such a way that aging impact on T_g is minimized. Second, when the sensor is ON, the sensor design also favours low sensitivity of T_g on NBTI effects. As much as possible, NMOS transistors are used to avoid the NBTI effect [5, 13].

When the sensor is OFF (PWD = 1), M_{pnor1} (Fig. 4) will not age, and M_{pnor2} will have low aging effect, since the periodic clock signal switching will introduce the annealing effect, reducing charge traps in the thin oxide of the MOSFET. Moreover, the output of the NOR2 gate is at logic '0', the gate terminal of M_{pch} is LOW, V_X = 1 and

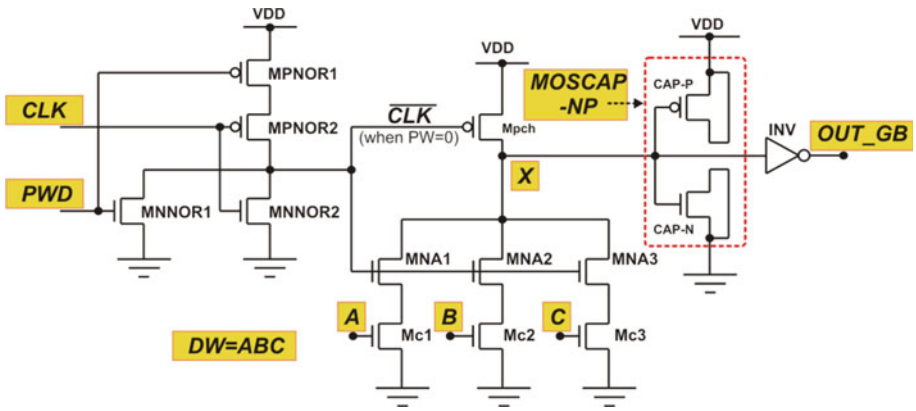

Fig. 4 Sensor's Delay Element (DE) topology

OUT_GB = 0. In these circumstances, M_{pch} ages, but MOSCAP-P transistor does not. Note that threshold voltage degradation of M_{pch} increases the pre-charge time of X node, but it does not impact the guardband interval value, T_g, which ensures the resilience of T_g to the aging effect. In fact, T_g is defined by the MOSCAP capacitance value (dominant in the X node total capacitance) and by the driving force of the pull-down network (composed of NMOS transistors, thus not affected by NBTI). For all the simulation results obtained, the increase on X node pre-charge time did not compromise the correct functionality of the sensor. Simulation results show that more than 60% ΔV_{thP} are required before M_{Pch} aging becomes problematic. The MOSCAP-NP element, together with INV input capacitance and the output capacitance of M_{Pch} and the PD network, emulate a capacitor that, in the present 65 nm CMOS design, is $C_x = 15$ fF. With MOSCAP-NP, at least one MOS transistor is in strong inversion region, showing much better capacitance linearity with V_{DD} than a Simple Gate Capacitor. The proposed DE is a 15-MOSFET solution, much more compact than the Agarwal's solution (23 MOSFET). Area savings, as compared to the aging sensor presented in [20], are even larger.

When the sensor is ON (PWD = 0), the NOR gate acts as an inverter, delivering the $\overline{CLK}$ = CLKN signal to the gate terminal of M_{pch}. For CLK = 1, $V_X = V_{DD}$ (pre-charge phase) and $V_{OUT\_GB} = 0$. However, for CLK = 0, M_{NA1}, M_{NA2} and M_{NA3} will be ON and, depending on which additional transistors in the NMOS network (M_{c1}, M_{c2} and M_{c3}) are activated too (driven by the HIGH logic value of A, B and C inputs), a pull-down network will be ON, discharging node X to ground and charging C_x capacitor to V_{DD}. As V_X goes from V_{DD} to 0, V_{OUT_GB} switches $0 \rightarrow 1$, and a guardband interval is formed ($T_g > 0$). Signals OUT_GB and $\overline{CLK}$ determine the guardband interval width, T_g, defined as the period of time in which both signals are in the HIGH state. As stated, the T_g period *rising* edge is defined by the delay introduced by DE, while its *falling* edge is defined by the CLK signal.

Therefore, with this DE architecture, *T_g is modulated by the discharging time of node X* (Fig. 4). The discharging current depends on the digital word DW = ABC. Hence, the sensor has a *programmable* T_g, by selecting DW value. The lowest valid digital number (DW = 001) (decimal 1) leads to a minimum T_g (low PD current). As DW increases, so do the discharging currents and the period width, T_g. In contrast, the DE in [8] has a hardware-fixed T_g value.

4.2 Stability checker and latch

The Stability Checker (SC) and Latch configurations are shown in Fig. 5. Two types of OUT_CL transitions can occur, HL ($1 \rightarrow 0$) and LH ($0 \rightarrow 1$). For each signal path through the combinational logic, $t_{PHL} > t_{PLH}$ or $t_{PHL} < t_{PLH}$ stands. However, PVT or aging-induced variations, or activated physical defects, may change this. Hence, SC must check that neither HL nor LH OUT_CL transition occurs within T_g. Thus, SC must be rising- and falling-edge sensitive to OUT_CL. The pull-down nets of nodes Y and Z (together with INVSC) (Fig. 5) guarantee this. When CLK = 1, OUT_SC = 0. During T_g, CLKN = OUT_GB = 1, and OUT_SC = 1 if and only if OUT_CL switches HL or LH. The presence of INVSC leads to a higher setup time for checking the HL transition, as compared to the LH transition.

The Stability Checker limits the observation interval, as defined by the Delay Element. If OUT_CL switches very close to the either rising or falling edge of the guardband, then the transition may not be detected by the Stability Checker. This occurs due incomplete discharge of the NMOS stacks. As shown in Fig. 6, two Hold Time metrics are defined to quantify the *effective* T_g interval, $T_{geff} = T_g - (T_{hold} + T_{su})$. Hold time ($T_{hold}$) is the time interval during which the Guardband must remain valid

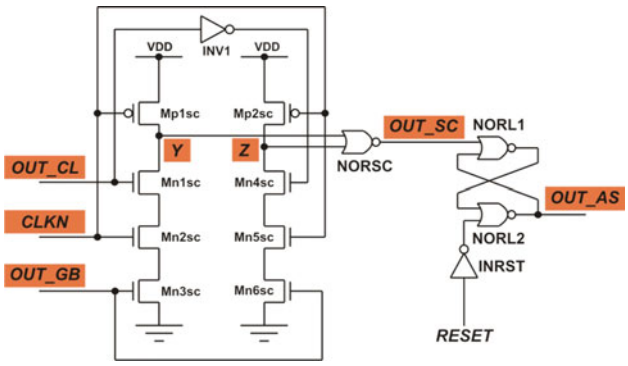

Fig. 5 Stability Checker and Latch of the proposed delay sensor

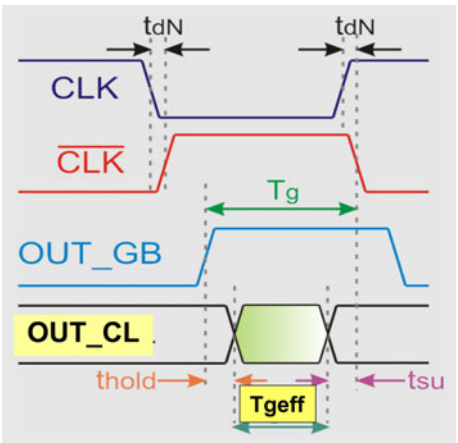

Fig. 6 Guardband degradation due to Hold time constraints of the Stability Checker

before OUT_CL makes a transition. Time setup (T_{su}) is the time interval during which the Guardband must remain valid *after* OUT_CL makes a transition (in fact, a setup time). Predictive delay fault detection is performed when the delayed OUT_CL transitions occur after of REGB + T_{hold} and before of FEGB-T_{su}, where REGB is the time when the rising edge of the Guardband (rising edge of OUT_GB) is at $V_{DD}/2$ value and FEGB is the time when the falling edge of the Guardband (falling edge of CLKN) is at $V_{DD}/2$ value. If any OUT_CL transition occurs outside of this time interval, the sensor will not detect it.

In Fig. 6, we note that CLKN is delayed with respect to CLK. This is due the inverter action of the NOR gate when PWD = 0 (this delay time is marked as t_{dN} in Fig. 6). Metastability could occur when the stability checker goes from writing phase to memory phase. Writing phase begins when OUT_GB goes HIGH. On the other hand, the writing phase ends when CLKN goes LOW (falling transition), and this is the memory phase. Hence, any transition of OUT_CL close to the falling transition of CLKN may violate the set-up time of the stability checker and a metastability problem may occur. However, t_{dN} alleviates the problem of eventual set-up time violation and metastability because in the design phase, all OUT_CL delayed transitions switch before the rising edge of the clock signal (e.g., falling edge of CLKN). Since the falling edge of CLKN appears a time t_{dN} after of the rising edge of the CLK and T_{su} metric is located before the falling edge of CLKN, the real time constraint that must be satisfied is (T_{su}-t_{dN}) instead of the original T_{su}. This issue will be revisited in Sect. 6, where additional simulation results are presented.

4.3 Sensor issues

The *loading effect* introduced by the delay sensor on the circuit to be observed depends on the input capacitance of the input node of the Stability Checker driven by $\overline{CLK}$. This loading effect, increasing the total capacitance of the OUT_CL node, tends to increase the propagation delay time of the critical path. However, this loading effect, for the proposed sensor, is almost negligible (around 1% speed degradation, according to many simulation examples using the 65 nm design).

The strength of the X node pull-down network must take this observation time degradation into account, as T_{geff} must allow the detection of OUT_CL transitions occurring in the considered unsafe region. In order to perform predictive delay fault detection, the most relevant edge of the Guardband, or observation interval, is its rising edge, occurring first in time. This defines the sensor's maximum resolution, for each DW value. If different actions are to be taken, according to the severity of the timing degradation of the CUT, different DW words can be applied to the sensor. Note that T_{hold} and T_{su} do not depend on DW; in fact, they only depend on the SC characteristics and on its sensitivity to PVT or aging-induced variations.

Low sensitivity of the delay sensor to process (P) variations is also a valued characteristic of the proposed sensor. In fact, resilience to P variations is obtained using two circuit techniques: (1) avoidance of minimum dimension transistors (L_{min}, W_{min}), and (2) use of several circuit elements in parallel (their variance is lower than an equivalent circuit element). Hence, no L_{min} MOSFETs are used, and this lead to no W_{min} transistors. Moreover, the use of MOSCAP-NP also leads to low sensitivity of C_x to P variations. The improvement of the linearity of MOSCAP-NP also helps. For the ST 65 nm CMOS technology, L_{min} = 60 nm. In our design, L_{min} = 65 nm and W_{min} = 120 nm (Fig. 4). The MOSCAP-NP is built with one NMOS and one PMOS transistors, both with W = L=745 nm.

5 Physical design: ASTRAN tool

In this work, the **Astran** academic netlist-to-layout tool [25] is used to synthesize the cells being designed. **Astran** is flexible enough to generate large cells with non-complementary logic and different number of P and N transistors, as needed in this sensor design. It generates new cells compliant to the commercial cell library. Minor hand-made optimizations are made to fix Design Rule Checking (DRC) violations and to improve layout compaction. In our flow, cells are initially described at schematic level, simulated and validated. After this, they are converted to Spice netlist to be synthesized by **Astran**.

The sensor physical design has been optimized with **Astran** for ST 65 nm technology. The library-compliant sensor layout is depicted in Fig. 7.

6 Simulation results

Simulations results are presented first, regarding the sensor design, and then using a simple CUT. In order to compare the sensitivity to VT variations of the proposed sensor and Agarwal et al.'s sensor [8], a 65 nm replica of the Agrawal sensor has also been designed. Hence, results are also presented, to compare the proposed sensor, and Agarwal et al. sensor. The reported results are for the sensor design described in Sect. 4, and Agrawal's sensor, using ST 65 nm technology [7]. In addition, some results are also shown for BPTM MOSFET models [6]. All circuit simulations are performed with HSPICE. For the ST design, Standard Vt

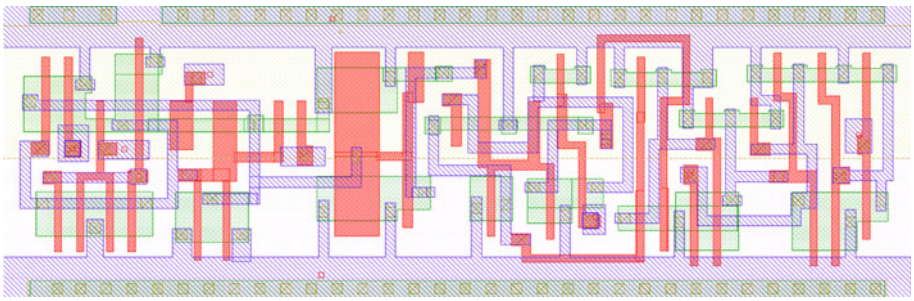

Fig. 7 Aging sensor layout (ST 65 nm) (8.4 × 2.6 μm^2)

(i.e., V_{th}) (SVT) NMOS and PMOS transistors have been used in sensor and CUT design, within the ST triple Vt available technology. The basic model parameters and VT ranges are shown in Table 1. For the BPTM model, higher Temperature has been used (T_{max} = 180°C), as for some automotive applications, high temperature electronics is used.

6.1 VT variation results

For the ST model, the V_{DD} range has been limited at 10% variation from the nominal (1.2 V) value, due to the fact that, by lowering V_{DD}, the MOS transistors easily may go from strong inversion into sub-threshold-like regime (where increasing T, the drain current increases). This is a consequence of high V_{th} values in ST technology (Table 1), probably to constrain the static power (leakage currents). In fact, we plot characteristics curves for PMOS and NMOS transistors in this technology, and the point at which the drain current switches from diffusion (sub-threshold) to drift is around V_{GS} 0.6–0.8 V. The delay sensor (with ST model) still operates at V_{DD} = 0.8 V (correct Boolean functionality). However, larger t_{PHL}(V_{DD} = 0.8 V) values occur at T = 27°C, and not at T = 180°C. The dominance of V_{th} reduction over μ_p reduction (when T increases) justifies the *reverse temperature behavior* [25, 26].

Hence, a first, relevant conclusion is that this 65 nm CMOS technology is quite sensitive to VT variations, not only on V_{DD} and T levels, but also on normal or reverse Temperature effects. Multi-Vt nanometer technologies are expected to have this problem, especially with the low-leakage (HVT) transistors. This is relevant, not only for unwanted V_{DD} variations (power supply noise), but also for planned variations, e.g., when Dynamic Voltage Scaling (DVS) techniques are used to restrict dynamic power consumption. Therefore, the Delay Sensor must be properly designed to account for these issues.

Table 1 VT ranges for the two MOSFET models used in simulation

Models	BPTM	ST	Units
V_{DDnom}	1.1	1.2	V
V_{DDmin}	0.8	1.08	V
ΔV_{DD}	27.4	10.0	%
T_{nom}	27	27	°C
T_{max}	180	150	°C
V_{thN}	0.423	0.442	V
V_{thP}	−0.365	−0.43	V

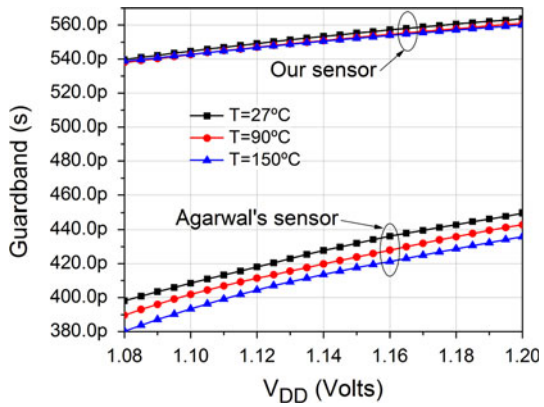

Fig. 8 T_g dependence on V_{DD} and T, for the two sensors (Agrawal et al. [8] and ours, ST model and DW = 7)

Figure 8 shows the simulation results with the proposed sensor and Agarwal et al.'s sensor [8], obtained with the ST model, of the observation interval (T_g) *variations* (as observed at the output of DE) with V_{DD} and T, for both sensors. For the proposed sensor, results are shown for DW = 7. As shown, our sensor exhibits higher T_g values than Agarwal's sensor, allowing the detection of lower propagation delay variations. As expected, higher T or lower V_{DD} values decrease T_g, due to the increase of the C_x discharging time. Moreover, it is clear that the proposed sensor, occupying less Si area, leads to lower sensitivity to VT variations than the Agarwal et al. sensor [8].

A detail of simulation results for the dependence of T_g on V_{DD} and T is depicted in Fig. 9(a), also for DW = 7. It can be observed that the curves for T = 90°C and T = 150°C intersect as V_{DD} increases. Figure 9(b) plots T_g as function of the temperature. This plot allows understanding better the sensor behaviour dependence, in ST technology, on temperature and V_{DD}. As it is well known, V_{DD} variations have a stronger impact than T variations.

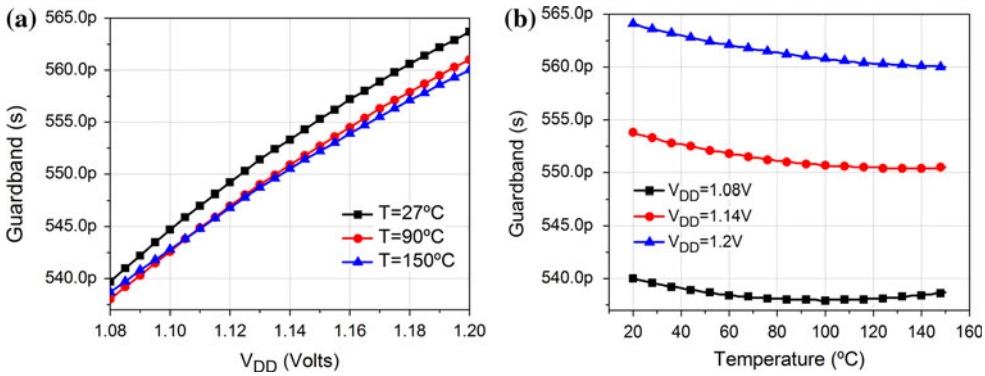

Fig. 9 Detail of T_g dependence on V_{DD} and T, for the proposed sensor, ST model and DW = 7

There are V_{DD} values for which T_g almost does not depend on T (Fig. 9(b)). The two T dependence regions become apparent: a *normal* T dependence region (for which an increase in T corresponds to a decrease in the drain current), and a *reverse temperature dependence region* (for which the opposite occurs) [27] (Fig. 9(b)). Between the two regions, it is possible to define a temperature-insensitive supply voltage value, V_{INS}, for which zero dependence occurs [26, 28]. This corresponds to the mutual compensation of channel drift mobility and threshold voltage temperature effects. Note that $V_{INS} = V_{INS}(V_{DD},T)$.

6.2 Process variation results

For safety–critical applications, the sensor must also provide reliable operation also under P (Process) variations. For the BPTM, Monte Carlo (MC) simulations results are described in [22]. For the ST model, MC simulations have been performed (100 runs, worst case VT conditions). As shown in Table 2, the proposed sensor is also more robust to process variations than the one presented in [8]. In fact, Agrawal's sensor presents a mean value of T_g of 368.92 ps and a sigma value of 66.11 ps. As shown in Table 2, the proposed sensor has a higher guardband interval (for DW = 7) and a lower standard deviation than Agrawal's sensor. Table 3 provides additional data, for the various sensor resolutions (DW from 1 to 7), as our sensor is programmable. It shows that, for all DW values, the same trend holds. Although the t_{PHL} values depend on P variations, the sensor can still be tuned (by varying DW) to identify a specific Δt_{pd} variation. As referred, the Stability Checker limits the width of the observation interval ($T_{geff} < T_g$). Table 4 provides data on the hold time metrics for the SC of the delay sensor, in ST 65 nm technology.

Figure 10 shows the CUT and its critical path used in the simulation results. The CUT is a cascade of identical combinational cones used in an industrial design—XTRAN. This circuit has been chosen to illustrate the effectiveness of one proposed delay sensor to perform predictive delay fault detection, even in the presence of PVT or aging-induced variations, or in the presence of physical defects causing performance degradation. The CUT complexity is adequate to low-cost HSPICE simulation, even Monte Carlo simulation. Circuit-level simulation makes VT variations injection trivial. Moreover, the chosen CUT avoids the problem of test pattern generation, as

Table 2 Statistical data of Monte Carlo simulation for the guardband interval, T_g (DW = 7, WC conditions)

	Our sensor	Agarwal et al.	Unit
Min T_g	510.12	44.57	ps
Max T_g	563.68	453.54	ps
Mean	537.03	368.92	ps
Variance	8.554e-23	4.371e-21	
Sigma	9.24	66.11	ps

Table 3 Statistical data of MC simulation for the guardband interval, T_g for all DW values (WC conditions)

DW	Mean	Sigma
1	333.76 ps	32.08 ps
2	371.38 ps	25.58 ps
3	469.80 ps	14.82 ps
4	478.60 ps	14.15 ps
5	512.75 ps	10.98 ps
6	517.30 ps	10.53 ps
7	537.03 ps	9.24 ps

Table 4 Hold time metrics for the Stability Checker of the proposed sensor (WC VT conditions) for the ST 65 nm technology

	OUT_CL transition	
	Rising (0 → 1)	Falling (1 → 0)
T_{hold}	49 ps	89 ps
T_{su}	140 ps	170 ps

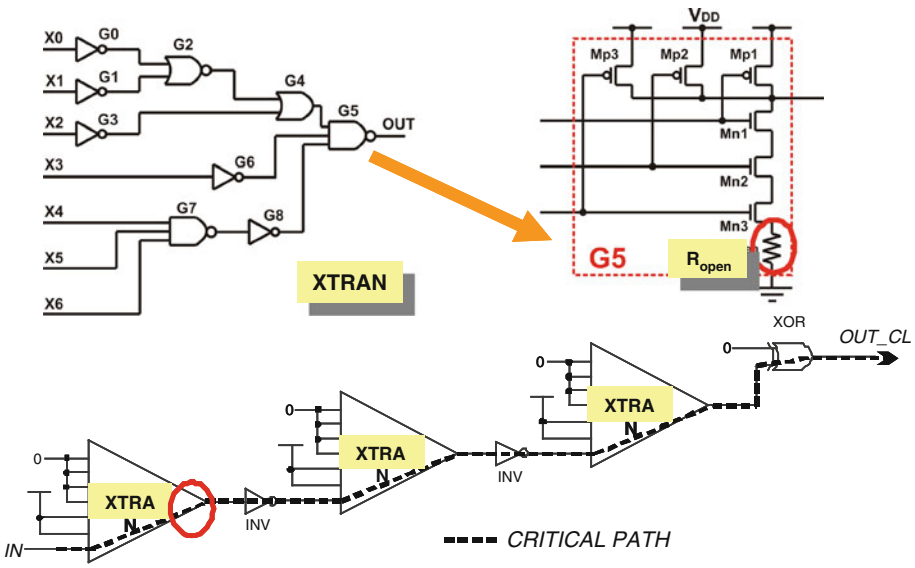

Fig. 10 CUT critical path considered in all simulations

its critical path has been identified by simulation, and all other inputs (×0 to ×5, see Fig. 10) are assigned logic values that enable critical path activation. The CUT also allows modifying OUT_CL phase as compared to the CLK phase, by changing the phase of the IN signal. The time slack can easily be modified, by modulating the clock frequency. The simulation testbench also allows injecting NBTI effects in the CUT and in the sensor, or only in the CUT (assuming that the sensor, being normally OFF, ages very little). In the simulation testbench, the delay sensor is connected in parallel with the FF that captures the CUT's response, OUT_CL (Fig. 1). Each XTRAN module has the topology shown also in Fig. 10. A resistance (R_{open}) between ground and the source terminal of the lower NMOS transistor of gate G5 (Fig. 10) is inserted (in the first XTRAN cone) only when the sensor is used for predictive fault detection of physical defects (resistive opens). Of course, other fault locations (resistive open and bridging defects) have been tried; here, a typical result is presented, for this resistive open via.

The delay sensor is analyzed under worst case (WC) VT conditions. As shown in Table 1, for the BPTM model, WC VT conditions are $V_{DD} = 0.8$ V, T = 180°C. For the ST model, WC VT conditions corresponds to $V_{DD} =$ 1.08 V, T = 150°C.

For the BPTM model, under WC VT conditions, the propagation delay time in the CUT's critical path is $t_{PLH} = 1.279$ ns. The CLK period used in the simulations is $T_{CLK} = 2.2$ ns (50% duty cycle). However, for the ST model, under different WC conditions, the longest propagation delay time in the critical path of the CUT is $t_{PHL} =$ 809 ps. Hence, this commercial IC technology leads to much better performance than predicted by the BPTM model. For the ST model, the CLK period used in the simulations is $T_{CLK} = 1.3$ ns ($f_{CLK} = 769.23$ MHz) also with a 50% duty cycle.

Simulation results to ascertain the effectiveness of the proposed delay sensor, in the presence of process variations can anticipate real experimental results on a test chip, being taped out. This can be performed, in the simulation environment, using Monte Carlo (MC) circuit simulation. Moreover, these MC results also show that, under statistical variations, OUT_CL transitions with variable delays will show up. How does the sensor cope with this reality?

Figure 11 shows typical simulation results (voltage waveforms) of Monte Carlo (MC) simulations using the CUT and the maximum sensor resolution (DW = 7), under worst case VT conditions. A Gaussian distribution with $\pm 3\sigma$ variation, corresponding to ±10% variation of the nominal parameter values, was assumed for three MOSFET parameters: L, t_{ox} and V_{TH}. For each set of MC simulations, 30 runs were performed. MC simulations were run introducing variations on the MOSFET parameters in *both* the CUT and the sensor. In these simulations, it was assumed that the sensor does not age (it will only be switched ON from time to time). All simulation results show that the proposed sensor does not trigger any warning signal (no false positives). Figure 11 shows MC simulations for $\Delta V_{thP} = 15\%$ in the CUT ($\Delta t_{PLH} = 17\%$) and the delay sensor with DW = 7. In this figure, it is shown that the T_g period is well established and, despite a large spread of OUT_CL switching transition times, the sensor is able to detect these abnormal delays (OUT_AS switching) in a significant number of cases. In fact, for $\Delta V_{thP} = 15\%$ ($\Delta t_{PLH} = 17\%$), 17 out of 30 MC runs detect the predictive timing failure. For $\Delta V_{thP} > 21\%$, the sensor is able to detect abnormal delays in *all* 30 runs in each MC analysis.

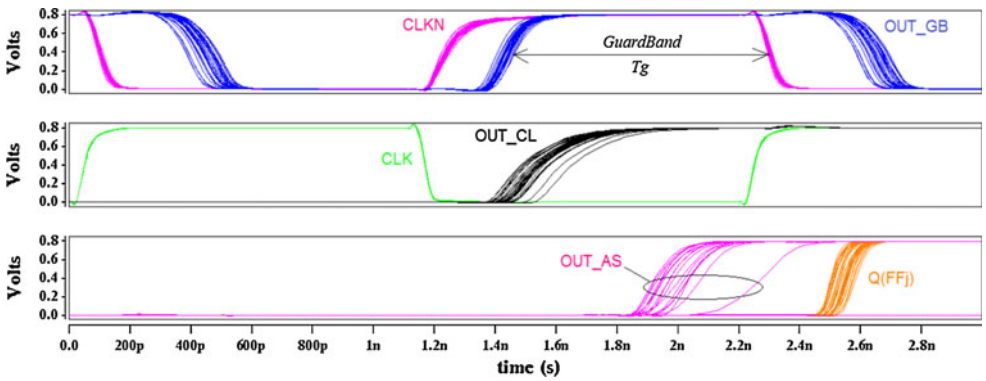

Fig. 11 CUT response under P variations and slight aging: Monte Carlo simulation under $\Delta V_{thP} = 15\%$ in the CUT (BPTM model) and worst case VT conditions ($V_{DD} = 0.8$ V, T = 180°C)

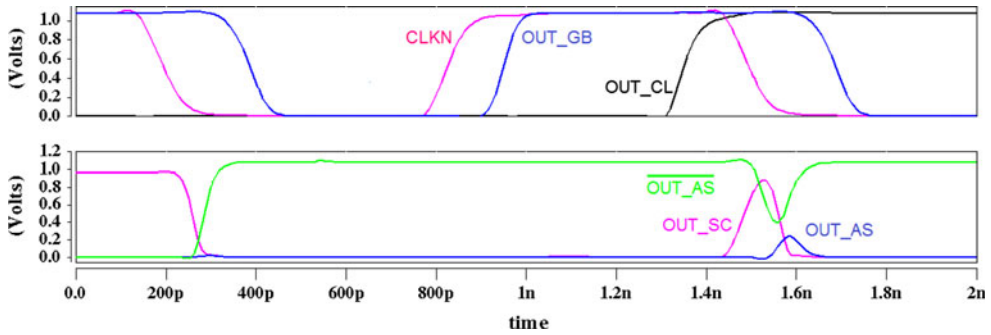

Fig. 12 Example of a set-up time violation. OUT_CL switches close to falling edge of CLKN. OUT_AS never bit-flips to complete the latch of OUT_SC

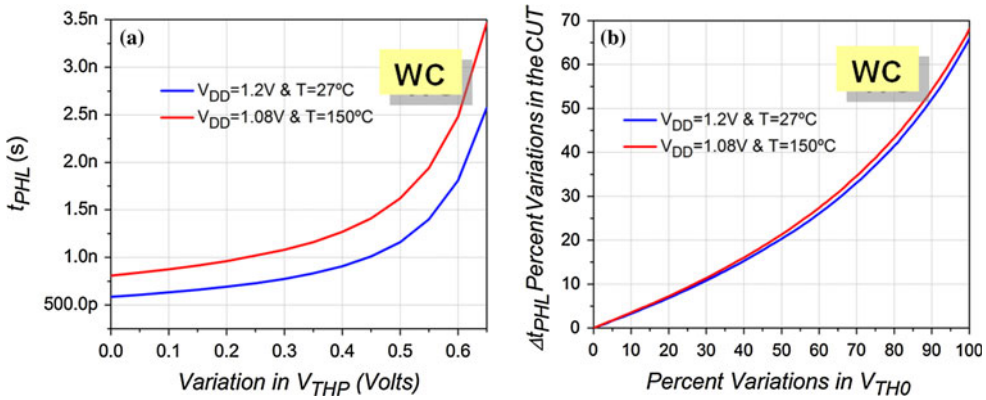

Fig. 13 *Effective* **a** t_{PHL} and **b** percentage Δt_{PHL} variations with ΔV_{thP} aging variations for the CUT under study (ST 65 nm model)

The issue of setup/hold time violations and eventual metastability problems can also be investigated, in the simulation environment. In Fig. 12, an example of a setup time violation (when OUT_CL transition occurs near the end of the T_g period) is shown. In fact, OUT_CL switches close to falling edge of CLKN. In this case, OUT_AS never flips to the opposite values to complete the latch of the OUT_SC data. The sensor does not detect this OUT_CL too delayed transition, but does not show any metastability behavior. Nevertheless, this is not a relevant issue, as basically, in order to avoid harm, the designer wants to prevent the CUT to *enter* the unsafe region (defined by the rising edge of T_g, not its falling edge), not the leave the unsafe region. Moreover, metastability refers to signals that do not assume stable 0 or 1 states for some duration of time at some point during CUT normal operation. With this Stability Checker topology, as long as CLKN goes to 0, at least one strong pull-up at nodes Y or Z occurs (logic 1), driving the NORSC gate output to 0 (see Fig. 5), thus preventing the latch to go to intermediate voltage levels for a long period of time.

6.3 Aging results

Figure 13 shows, for the ST model, the dependence of the CUT's critical path propagation delay time (t_{PHL}) (Fig. 13(a)) and delay time *variation* (Δt_{PHL}) (Fig. 13(b)) on the PMOS threshold voltage V_{thP} increment (NBTI

aging). Aging "fault" injection (by means of a V_{thP} increase) is carried out as described in [26]. A voltage source is added in series with the gate of each PMOS in the CUT, as we assume no aging for the sensor. CUT performance degradation is relevant, and significantly larger than the one observed in a similar CUT and a sensor in 0.35 μm IC technology [21]. For worst-case VT conditions, the CUT exhibits a $\Delta t_{PHL} = 100\%$ of degradation when V_{thP} of all PMOS transistors is increased 0.5 V.

However, there is not a relevant difference between WC and nominal conditions, in $\Delta t_{PHL}(\Delta V_{thP})$. As it can be seen in Fig. 13, although the real propagation delay time is significantly different for nominal and WC conditions (Fig. 13(a)), this is not the case as regards to delay *variations,* Δt_{PHL} (Fig. 13(b)). This result is significantly different than what we observed in larger technologies (0.35 μm [21]), and also predicted by the BPTM model [22].

Figure 14 shows the levels of abnormal delay detection of the proposed sensor, in WC conditions, for each digital word (DW), and for the two MOSFET models. For the BPTM model, the critical path corresponds to a LH transition of OUT_CL, while for the ST model it corresponds to a HL OUT_CL transition. As shown, for the BPTM model, our sensor allows the detection of *LH* Δt_{PLH} due to aging from 17% to 52% (for a DW = 7) and from 42% to 52% (with DW = 1). The maximum value of Δt_{PLH} (52%) depends on the time slack, which is determined by the clock period, $T_{CLK} = 2.2$ ns. For the ST model, the sensor allows the detection of *HL* Δt_{PHL} from 14.43% to 47.83% (with DW = 7) and from 44.49% to 47.83% (with DW = 1). As referred, the maximum Δt_{PHL} detection value (47.83%) depends on the time slack, which is determined by the clock period, (now, $T_{CLK} = 1.3$ ns).

Hence, both models predict similar percentage Δt_{PHL} (Δt_{PLH}) variations, and confirm the availability of a significant *range* of the predictive delay fault detection variation. Under WC VT conditions and DW = 7, the sensor in ST 65 nm technology is able to identify a 116.7 ps delay increase, in a 1.3 ns clock period (14.43% × 809 ps = 116.7 ps).

6.4 Defects detection results

The delay sensor can rewardingly be used for *predictive delay fault detection*, due to latent physical defects which may be activated by long circuit operation. Simulation results are reported for parametric (resistive) open defects. *Defect size* is modeled by a R_{open} resistance. The value of R_{open} is unknown, and may drift during product lifetime, according to workload conditions. From a user's point of view, the R_{open} value is irrelevant. What is crucial is that, if the open defect manifests itself as an additional delay Δt_{pd}, this abnormal delay should not exceed a given *safety value*, to prevent a circuit error. Hence, it is not important if the sensor can detect the open defect for the overall R_{open} range of values for which it is detectable. Instead, the goal is to make sure the proposed sensor is able to monitor the impact of the open defect *within the range of* R_{open} *values for which it can become potentially harmful*. Moreover, as on-line detection is considered, delay detection is only considered for functional testing. Hence, we do not target 100% predictive delay coverage (e.g., transition and/or path delay fault coverage), but *100% coverage of abnormal delays in functional mode*—the one for which harm must be prevented.

Defect-induced predictive fault detection is illustrated by considering a resistive open defect [29, 30]. As an illustrative example, the open fault is injected in the lower NMOS transistor of gate G5, only in the first XTRAN cone (Fig. 10). We consider the LH transition at the input ×6, which drives a HL transition at the CUT's output (OUT_CL). Results, as shown in Fig. 15, are obtained with WC VT conditions ($V_{DD} = 1.08$ V, T = 150°C) and NBTI-induced aging. As the value of the resistive open defect (R_{open}) increases, the propagation delay in the critical path increases too, allowing predictive delay detection.

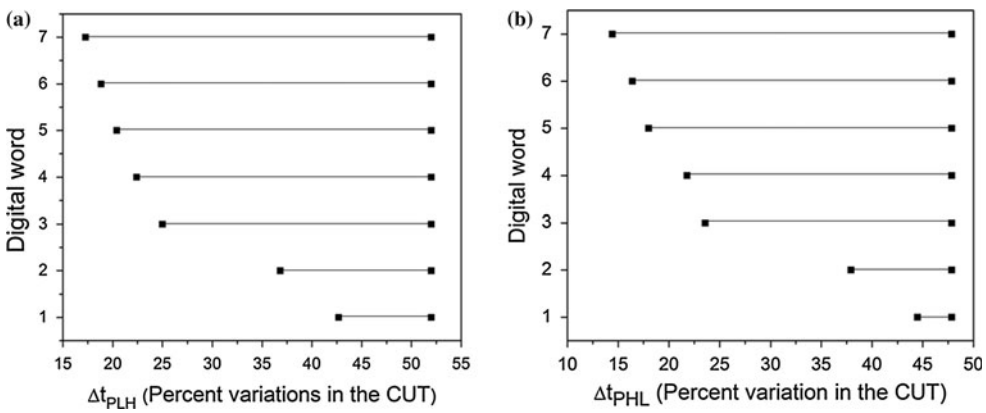

Fig. 14 Detection ranges in percent variations of Δt_{PLH} (Δt_{PHL}) of the CUT under WC conditions: **a** BTPM ($V_{DD} = 0.8$ V, T = 180°C); **b** ST ($V_{DD} = 1.08$ V, T = 150°C)

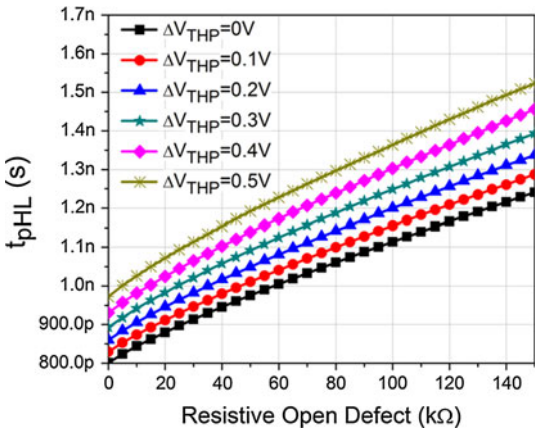

Fig. 15 Detection of a resistive open defect, causing abnormal propagation delay increase (ST model, with NBTI-induced aging)

Table 5 Detection ranges for R_{open} for various DW (ST model, no aging)

Digital word (DW)	Detection range (kΩ)
7	$35.7 < R_{open} < 137.0$
6	$41.9 < R_{open} < 137.0$
5	$43.6 < R_{open} < 137.0$
4	$56.0 < R_{open} < 137.0$
3	$60.8 < R_{open} < 137.0$
2	$101.5 < R_{open} < 137.0$
1	$120.0 < R_{open} < 137.0$

For very low R_{open} values, the additional delay is so small that OUT_CL does not switch inside the observation interval, T_g. For higher R_{open} values, the defect becomes detectable, as seen in Table 5. As expected, for high pull-down currents (high DW), T_g, is wider, and lower abnormal delays (due to R_{open}) are detectable (e.g., 35.7 kΩ for DW = 7, 120 kΩ for DW = 1). For this clock frequency, the maximum detectable value of R_{open} is 137 kΩ.

7 Conclusions

In this paper, a new methodology for delay monitoring of safety–critical digital systems, and a novel programmable delay sensor resilient to PVT and aging-induced variations have been presented.

Simulation results have shown that the sensor is cost-effective, and is able to identify abnormal delays, due to PVT variations, NBTI-induced aging, or to resistive open defects. Predictive delay testing is, hence, possible, to prevent catastrophic system errors in safety–critical applications.

In particular, the proposed research allows concluding the following. Simulations results for a given digital CMOS technology (65 nm) circuit netlist and different MOS transistor models (BPTM, ST) may provide different behaviors, even in a simple CUT and critical path, as the one used in the simulation testbench. However, despite those differences, the proposed aging sensor is able to perform the specified functionality. Being programmable, the sensors may be tuned to perform predictive delay detection for target time threshold values, even in the presence of process variations.

In these IC technologies, namely with multi-V_{th} transistors, sensitivity to VT variations may become critical, as lowering V_{DD} may easily drive the MOSFET to conduct in sub-threshold-like regions (reverse temperature behavior). This can be relevant in the presence of power supply noise, or in DVS-based designs. The normal and reverse temperature behavior is, thus, very important for 65 nm (or lower) technologies, and 1.2 V (or lower) V_{DD} values, and may have also impact on the definition of design corners for a given technology.

For this 65 nm technology, the effect of V_{thP} degradation on circuit performance is similar under nominal and WC VT conditions, as far as percentage propagation delay *variations* is concerned, although absolute values differ. This was not observed in sub-micron technologies.

On-line predictive delay fault detection can be a useful technique to uncover long-term effects in safety–critical systems, using a set of judiciously located delay sensors, seldom activated (as compared to the system's operation time). Harm prevention is carried out *regardless of the abnormal delay origin,* namely whatever aging phenomena, PVT variation or latent defects are present.

As referred, the proposed delay monitoring methodology comprises two processes. This paper dealt with sensor design. The sensor insertion technique, including selective sensor insertion criteria and an algorithmic approach for automatic netlist reconfiguration are being carried out, with large benchmark circuits and with multi-sensor insertion. Moreover, cell library development (critical memory elements) and gate-level simulation procedures, allowing PVT and aging fault injection, is under research. Work is in progress, and will be reported in the future.

Acknowledgments This work has been partially supported by ENIAC SE2A Project and by FCT—Portuguese Foundation for Science and Technology (INESC-ID multiannual funding) through the PIDDAC Program funds and by CONACYT (México) through the PhD scholarship number 207069/204311.

References

1. Itoh, K. (2009). Adaptive circuits for the 0.5-V nanoscale CMOS era. In *Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 14–20.

2. Tschanz, J., et al. (2007). Adaptive frequency and biasing techniques for tolerance to dynamic temperature-voltage variations and aging. In *Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 292–293.
3. McPherson, J. W. (2006). Reliability challenges for 45 nm and beyond. In *Proceedings of the ACM/IEEE Design Automation Conference (DAC)*, pp. 176–181.
4. Paul, B. C., et al. (2006). Temporal performance degradation under NBTI: Estimation and design for improved reliability of nanoscale circuits. In *Proceedings of the International Conference on Design Automation & Test in Europe (DATE)*, pp. 780–785.
5. Tsang, T. K., El-Gamal, M. N., Iniewski, K., Townsend, K. A., Haslett, J. W., & Wang, Y. (2007). Current status of CMOS low voltage and low power wireless IC designs. *Springer Journal on Analog Integrated Circuits and Signal Processing, 53*, 9–18.
6. Predictive Technology Model. (PTM). http://www.eas.asu.edu/~ptm/
7. http://www.st.com/stonline/products/technologies/soc/65plat.htm
8. Agarwal, M., et al. (2007). Circuit failure prediction and its application to transistor aging. In *Proceedings of the VLSI Test Symposium (VTS)*, pp. 277–286.
9. Arabi, K., Saleh, R., & Xiongfei, M. (2007). Power supply noise in SoCs: Metrics, management, and measurement. *IEEE Design & Test of Computers, 24*(3), 236–244.
10. Jaffari, J., & Anis, M. (2008). Statistical thermal profile considering process variations: Analysis and applications. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 27*(6), 1027–1040.
11. Jeppson, K. O., et al. (1977). Negative bias stress of CMOS devices at high electric fields and degradation of MOS devices. *Journal of Applied Physics, 48*(5), 2004–2014.
12. Kufluoglu, H., Alam, M. A. (2007). A generalized reaction-diffusion model with explicit H-H2 dynamics for NBTI. *IEEE Transactions on Electron Devices, 54*(5), 1101–1107.
13. Vattikonda, R., Wang, W., & Cao, Y. (2006). Modeling and minimization of PMOS NBTI effect for robust nanometer design. In *Proceedings of the ACM/IEEE Design Automation Conference (DAC)*, pp. 1047–1052.
14. Krishnan, A. T., Reddy, V., Chakravarthi, S., Rodriguez, J., John, S., & Krishnan, S. (2003). NBTI impact on transistor and circuit: models, mechanisms and scaling effects. In *Proceedings of the IEEE International Electron Devices Meeting (IEDM)*, pp. 349–352.
15. Kufluoglu, H., & Ashraful Alam, M. (2004). A computational model of NBTI and hot carrier injection time-exponents for MOSFET reliability. *Springer Journal of Computational Electronics, 3*, 165–169.
16. Keane, J., Persaud, D., & Kim, C. H. (2009). An all-in-one silicon Odometer for separately monitoring HCI, BTI, and TDDB. In *Proceedings of the IEEE Symposium on VLSI*, pp. 108–109.
17. Chen, T. W., Kim, K., Kim, Y. M., & Mitra, S. (2008). Gate oxide early life failure prediction. In *Proceedings of the IEEE VLSI Test Symposium (VTS)*, pp. 111–118.
18. Reddy, V., Wang, A. W., Yang, Sh., Bhardwaj, S., Vattikonda, R., Vrudhula, S., et al. (2007). The impact of NBTI on the performance of combinational and sequential circuits. In *Proceedings of the ACM/IEEE Design Automation Conference (DAC)*, pp. 364–369.
19. Agarwal, M., Balakrishnan, V., Bhuyan, A., Kim, K., Paul, B. C., Wang, W., et al. (2008). Optimized circuit failure prediction for aging: practicality and promise. In *Proceedings of ITC*, paper 26.1.
20. Nakura, T., Nose, K., & Mizuno, M. (2007). Fine-grain redundant logic using defect-prediction flip-flops. In *Proceedings of the IEEE International Solid State Circuits Conference (ISSCC)*, pp. 402–403.
21. Vazquez, J. C., et al. (2009). Built-in aging monitoring for safety-critical applications. In *Proceedings of International On-Line Test Symposium (IOLTS)*, pp. 9–14.
22. Vazquez, J. C., et al. (2010). Low sensitivity to process variations aging sensor for automotive safety-critical applications. In *Proceedings of the IEEE VLSI Test Symposium* (VTS), pp. 238–243.
23. Vazquez, J. C., Champac, V., Ziesemer, A. M., Jr., Reis, R., Semião, J., Teixeira, I. C., et al. (2010). Predictive error detection by on-line aging monitoring. In In *Proceedings of the IEEE International On-Line Test Symposium (IOLTS)*.
24. Shen, B., Khatri, S. P., & Zourntos, T. (2006). Implementation of MOSFET based capacitors for digital applications. In *Proceedings of the Great Lakes VLSI Symposium (GLSVLSI)*, pp. 180–185.
25. Ziesemer, A., Jr., Lazzari, C., & Reis, R. (2007). Transistor level automatic layout generator for non-complementary CMOS cells. In *Proceedings of VLSI-SOC*, pp. 116–121.
26. Wolpert, D., & Ampadu, P. (2009). A sensor to detect normal or reverse temperature dependence in nanoscale CMOS circuits. In *Proceedings of the 24th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, pp. 193–201.
27. Park, C., et al. (1995). Reversal of temperature dependence of integrated circuits operating at very low voltages. In *Proceedings of the International Electron Devices Meeting (IEDM)*, pp. 71–74, Dec.
28. Kanda, K., et al. (2001). Design impact of positive temperature dependence on drain current in sub-1 V CMOS VLSIs. *IEEE Journal of Solid-Sate Circuits, 36*(10), 1559–1564.
29. Wang, W., et al. (2007). Compact modeling and simulation of circuit reliability for 65-nm CMOS technology. *IEEE Transactions on Device and Materials Reliability, 7*(4), 509–517.
30. Rodriquez Montanés, R., Volf, P., & Pineda de Gyvez, J. (2002). Resistance characterization of interconnect weak and strong open defects. *IEEE Design & Test of Computers, 19*(5), 18–26.

J. C. Vazquez received the engineering and M.Sc. degrees from Technological Institute of Puebla and National Institute for Astrophysics, Optics and Electronics (INAOE), Mexico, in 2006 and 2009, respectively. He is working toward the Ph.D. degree in the Department of VLSI Design and Test at INAOE, in cooperation with INESC-ID, Portugal. His research interest includes design and test of Digital Systems, Circuit Reliability Degradation, particularly test of Negative Bias Thermal Instability (NBTI) effects in nanometer digital systems.

V. Champac received the Electrical Engineering Degree in 1987 from the Autonomous University of Nuevo Leon, Mexico. He received the Ph.D. degree in 1993 from the Polytechnic University of Catalonia (UPC), Spain. In 1993 he joined the National Institute for Astrophysics, Optics and Electronics (Mexico) where he is Titular Professor. Dr. Champac was cofounder of the Test Technology Technical Council-Latin America of IEEE Computer Society. He was co-General Chair of the 2nd and 9th IEEE Latin American Test Workshop held in Mexico in 2001 and 2008, respectively. He is actually member of the Board Director of the Journal of Electronic Testing: Theory and Applications. His research lines include: defect modeling in nanometer technologies, Development of new test strategies for advanced technologies, Modeling and Verification of Signal Integrity, Process Variation Tolerant VLSI Circuit Design and Noise tolerant circuit design.

A. M. Ziesemer Jr. received his B.S. degree from UFPEL in 2004 and M.S. degree from UFRGS in 2007, both in Computer Science. Currently, he is a Ph.D. candidate in Microelectronics at UFRGS, Porto Alegre, and his areas of researching interest include physical design algorithms for layout generation, placement and routing. He is also a Professor at IFRS Rio Grande since 2010 where he teaches OOP, Software Engineering and Networking.

R. Reis received the Electrical Engineering Degree from the Federal University of Rio Grande do Sul (UFRGS), Porto Alegre, Brazil, in 1978. In 1983, he received the Ph.D. degree from the Polytechnic Institute of Grenoble (INPG), France. He is currently Full Professor and the Head of the Microelectronics Graduate Program at UFRGS. His primary research interests include Physical Design Automation and Methodologies, EDA tools, Circuits Tolerant to Radiation, VLSI Design Methodologies and Microelectronics Education. He has published more than 300 papers in journals and conferences proceedings. He is also author or co-author of several books. He served as a General Chair or Program Chair of several conferences like the IFIP/IEEE VLSI-SoC, IEEE ISVLSI, IEEE LASCAS, Symposium on Integrated Circuits and Systems Design (SBCCI) and Congress of the Brazilian Microelectronics Society (SBMIcro). He is Past President of the Brazilian Computer Society and Past Vice-President of the Brazilian Microelectronics Society. He is vice president of IEEE Circuits and Systems.

I. C. Teixeira received the electrical engineering degree (telecommunications and electronics) and the Ph.D. degree and the Aggregation title, in applied electronics by Instituto Superior Técnico (IST) of the Technical University of Lisbon, Portugal. Since 1971 she has been a member of the Department o Electrical Engineering and Computer Science of IST as an Associate Professor. Her research activities are now on Design and Test of Hardware/Software Systems, mainly on the development of models, methodologies and metrics. She is now interested in the study of synchronism problems in multi clock domains systems. She is presently working on the processing electronics for medical imaging systems. Since 1985 she has joint INESC, Institute of Systems and Computers Engineering, where she is a senior researcher in the Quality, Test and Hw/Sw Co-design Group.

M. B. Santos received the M.Sc. and Ph.D. degrees in Electrical Engineering from the Instituto Superior Técnico, Technical University of Lisbon, Lisbon, Portugal, in 1994 and 2001, respectively. He has been a Professor with the Instituto Superior Técnico, Technical University of Lisbon, since 1990. His research interests include testability of digital circuits, optimization of dc–dc converters, and educational issues on microelectronics. He is cofounder of Silicongate.

J. P. Teixeira has got his Degree on Electrical Engineer (Telecommunications and Electronics) in 1971, and his Ph.D. in Applied Electronics by Instituto Superior Técnico (IST) in 1982 from the Technical University of Lisbon. He is currently a retired full Professor at IST. He carries out his research at INESC-ID (Instituto de Engenharia de Sistemas e Computadores—Investigação e Desenvolvimento, where he is responsible for the QTHS (Quality, Test and Hw/Sw co-design) R&D Group and scientific coordinator of the Embedded Electronic Systems research unit. His scientific and technical interests include the analysis, specification, design, verification, production and lifetime test and diagnosis of highly dependable hardware/software electronic systems. He has done extensive work in the area of defect-oriented test, BIST, system test and variability-aware design.