Testing of Stuck-Open Faults in Nanometer Technologies

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Editor's notes:
Failure analysis and fault modeling of integrated circuits have always been fields that require continuous revision and update as manufacturing processes evolve. This paper discusses the new face of the well-known transistor stuck-open fault model in modern nanometer technologies and proposes new detection methods that improve the robustness of tests.
—Dimitris Gizopoulos, University of Athens

Opens have become an important defect mechanism in modern technologies [1], [2] as open defects are an important contributor of test escapes [1]. Also, the introduction of copper and the damascene process have lead to a higher open defect density in copper than those found in aluminum [3].

Open defects in CMOS circuits may have different circuit defect behavioral forms [2]. Opens as a result of a narrow crack can present electron tunneling, and ICs have been known to function correctly in the hundreds of megahertz region. Opens in a single transistor gate may compromise noise margin, speed of operation, and quiescent power supply current, but the circuit will function. Interconnect opens is another important type of opens as the circuit may present malfunction, increased delay, and increased IDDQ. Opens in memory cells may present different responses. Opens in one of the parallel paths of a CMOS transmission gate will degrade signal voltages and will also slow the response rate [2], [4]. An open defect type of significant concern is called the *CMOS stuck-open fault (SOF)*. SOFs are difficult to test because they require at least a two-vector sequence. Some studies have revealed that an important number of defective chips exhibit "sequence dependent, yet timing independent" (SDTI) failures [5], [6]. These types of failures are usually detected by tests that target transition delay faults (TDFs). In a study conducted on volume production of an industrial circuit [6], 75% of the defective chips failing TDF tests, but passing exhaustive stuck-at testing, were SDTI failures. Such failures are symptomatic of SOFs. In [5], defective chips exhibiting SDTI failures were analyzed and diagnosed as SOFs. Hence, it is important to improve the detection of SOFs.

The SOF failure mode was known and discussed in the 1980s by the test community [7]. Wadsack [7] is one of the most heavily referenced papers in IC testing. In 1989 [8], Soden et al. found 125 papers in that decade about this peculiarity. However, during the 1990s, the literature on the SOF model almost

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ceased. New research on SOFs can be found from as far back as 2000, and some interesting papers have appeared in [4] and [9]–[12].

Unfortunately, test detection of this defect is made by chance: either from a lucky sequence of vectors in a functional, stuck-at fault, or delay fault voltage-based test set, or by chance in an IDDQ test. Failure analysis can experience seemingly contradictory measurements making the analysis frustrating. The presence of SOFs may make some transition faults invalid [12].

This paper shows how ICs implemented in technologies having low-signal-node capacitance that interact with transistor leakage currents can alter classic SOF behavior, which presents an even more complex detection challenge. The results show that leakage currents in SOF output nodes introduce more variables that further complicate detection. Results also show that normal IC noise may introduce a noisy output response that may or may not be correct.

First, the article presents the electronic properties of the classic SOF. Second, it presents the main leakage components in FinFET technology. Third, it investigates the influence of the SOF behavior and test on the leakage mechanisms. Fourth, it proposes new test methodologies to improve the robustness of detection of SOF in the presence of leakage currents. Fifth, it shows the influence of temperature, process variations and high-k dielectrics in SOF behavior. Finally, it presents the conclusions.

Electronic properties of the Stuck-Open Fault (SOF)

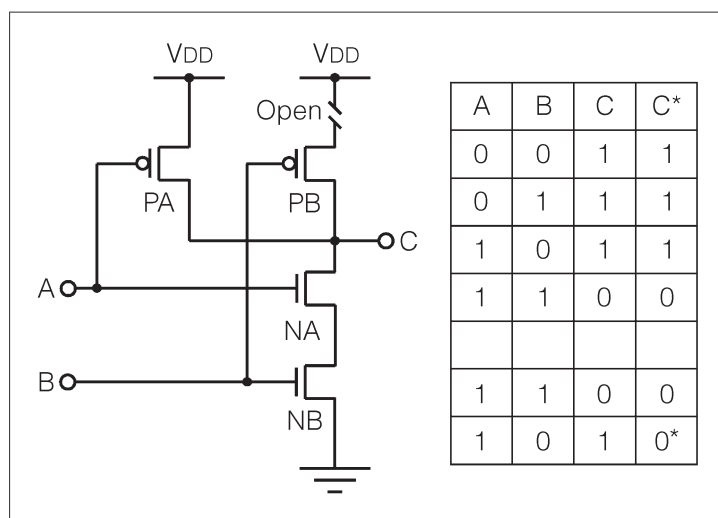
The SOF appears in combinational logic gates, particularly when a clear open circuit lies in the drain or source interconnect of parallel transistors. Figure 1 shows a 2-NAND gate accompanied by a truth table response for a good logic gate (C), and a defective logic gate (C^*) that has an open circuit defect in the source of pMOS transistor PB. For the $AB = 00$ state, both n-channel pull-down transistors are off, and the good pMOS transistor (PA) pulls the output to a correct logic value. The same result occurs for the $AB = 01$ vector. The bad pMOS transistor (PB) is off, so it doesn't affect the correct result. The third vector, $AB = 10$ is the interesting one, since the good pMOSFET (PA) is off and the bad pMOSFET (PB) is turned on, but cannot supply current to output node C. The pull down path through the two n-channel transistors is blocked, so Node-C floats in a high impedance state (high-Z) retaining the voltage of the previous state. Due to this property, the SOF is sometimes referred to as the CMOS memory fault. The previous high logic state was stored in the load capacitance C_L and at nominal tester clock rates the logic gate for vector $AB = 10$ reads a correct value of $C = C^* = 1$ in the sequence. The fourth test vector, $AB = 11$, pulls the output node C to the correct logic-0 state.

The defective gate performs correctly for a binary up count. In fact, transistor PB could be removed with the same result. However, the defective gate is sensitive to a particular sequence of test vectors. The table in Figure 1 shows that for the last two vectors the sequence $ABC = 110$ leads to an error for the next logic state $ABC = 100^*$.

SOF detection requires a specific two-vector pair that examines each transistor in the logic gate for an open defect in its drain and/or source. Older technologies had larger load capacitances and minimal transistor leakage, so that high-Z drift time constants were on the order of seconds [8].

Main leakage mechanisms in FinFET devices

This work is based on an intrinsic body symmetric device with (near midgap) metal gates MGDG. Double gate (DG) FET, particularly quasi-planar FinFET, has emerged as a feasible technology to continue scaling down to technologies with a few



A	B	C	C*
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0
1	1	0	0
1	0	1	0*

Figure 1. A CMOS stuck-open defect in a 2NAND gate with good and bad truth table response.

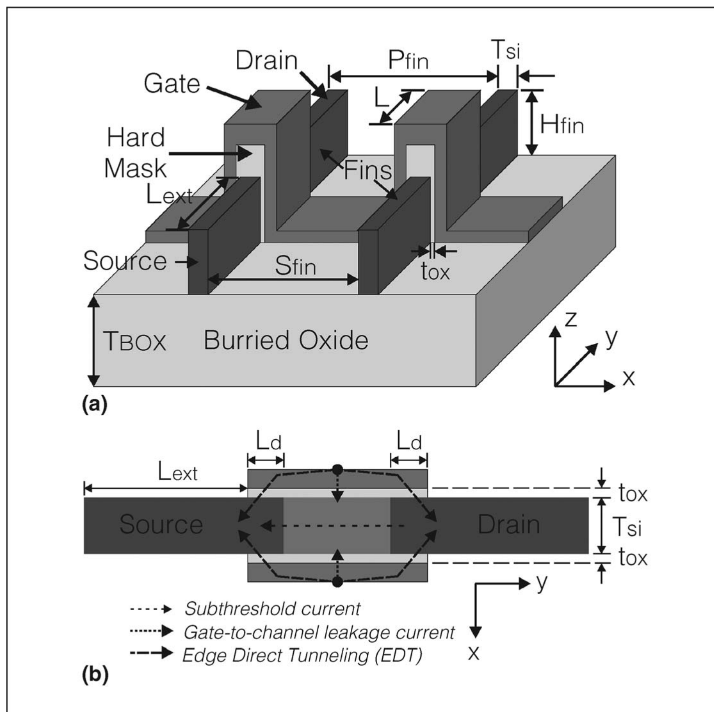


Figure 2. *Fin*FET structure and its main leakage mechanisms. (a) *Fin*FET structure. (b) Main leakage mechanisms for a *Fin*FET MGDG.

tens of nanometers. Figure 2a shows the physical structure of the FinFET device. Two parallel devices are shown. The different geometry parameters are: T_{si}: fin width, L: transistor channel length, H_{fin}: fin height, t_{ox}: gate oxide thickness, and P_{fin}: fin pitch.

The main leakage mechanism for the FinFET MGDG are (Figure 2b):

Subthreshold current

This leakage is a current between the drain and source terminals when the transistor gate voltage decreases below Vth. The subthreshold current is [13]

$$I_{\text{DS}} = \frac{2H_{\text{fin}}}{L_{\text{eff}}} \mu_0 C_g V_t^2 \times \exp\left(\frac{V_{\text{GS}} - V_{th}}{S \cdot V_t}\right) \times \left(1 - \exp\left(\frac{-V_{\text{DS}}}{V_t}\right)\right) \quad (1)$$

where C_g is the effective gate capacitance, V_t is the thermal voltage, and S is the subthreshold swing factor.

Gate-to-channel leakage current

This leakage is a current flowing into the gate of the transistor, and is due to Conduction Band Electron Tunneling (CBET) from the inverted channel in the ON state [14]. A quantum well is created in DG devices due to band bending close to the silicon-oxide interface. The tunneling current density is given by [15]

$$J_{(j,i)} = Q_{(j,i)} \cdot T_{WKB(j,i)} \cdot T_{R(j,i)} \cdot f_{(j,i)} \quad (2)$$

where $J_{(j,i)}$ is the tunneling current density due to the charge $Q_{(j,i)}$ confined in the energy levels $E_{(j,i)}.T_{WKB(j,i)}.T_{R(j,i)}$ is the transmission probability from the (j,i)th state and $f_{(j,i)}$ is the impact frequency of the electron. The total gate-to-channel tunneling current (I_{gc}) is

$$I_{gc} = L_{\text{eff}} H_{\text{fin}} \left(\sum_j \sum_i J_{(j,i)} \right). \quad (3)$$

The gate to channel leakage current is divided between the source (I_{gcs}) and the drain (I_{gcd}).

Edge direct tunneling

Edge direct tunneling (EDT) is present between the source/drain overlapping regions and the gate.

This leakage is due to CBET for nMOS transistors and VBHT (Valence Band Hole Tunneling) for pMOS transistors. To determine the tunneling current of an MGDG transistor in the ON state, the electric field through the oxide is calculated [13], [16]. Once the electric field E_{ox} is known, the charge available producing the edge direct tunneling in the ON state can be estimated. The equations to estimate the EDT current density for MGDG FinFET in the OFF state are given in [13].

SOF with leakage currents

The influence of leakage currents on the test of open defects was investigated in [17]–[20]. The slow transient response of circuits in older technologies contrasts with nm technologies. The small nanometer technology node capacitances (aF) and the increased transistor leakage mechanisms interact and produce nanoseconds drift times. The leakage scaling influence onSOF behavior is analyzed based on FinFET technology.

The results may also be applied to other CMOS technologies with low node capacitance interacting with transistor leakage currents [21], [22]. Sub-

threshold leakage have become one dominant source of leakage in nanoscale bulk CMOS technologies [21]. Due to technology scaling, the transistor threshold voltage needs to be significantly scaled to maintain a high drive current and achieve performance improvement. In addition, the gate leakage is another important source of leakage [21]. This is because the reduction of gate oxide thickness results in an increase in the field across the oxide. SOI CMOS technologies may also exhibits important leakage currents [22].

In order to simulate circuits based in FinFET technology the equations modeling the transistor, given in the previous section, were implemented using Maple [23], and the obtained transistor characteristics were implemented in Hspice electrical simulator. More details about this procedure can be found in [20]. Inputs are driven by inverters composed of an NFinFET with two fins and a P-FinFETs with four fins.

Leakage current components in a gate with an SOF

Complementary static gates having an SOF in FinFET technologies were investigated. Typical geometries were considered for the FinFETs (Figure 2): $T_{si} = 5$ nm, $L_g = 30$ nm, $L_{\text{eff}} = 18$ nm, $H_{\text{fin}} = 50$ nm, $t_{\text{ox}} = 1.75$ nm, $T_{\text{mask}} = 50$ nm, $L_d = 6$ nm, $T_{\text{poly}} = 100$ nm, $S_{\text{fin}} = 50$ nm, $L_{\text{ext}} = 14$ nm. The work-function for the $\text{N} - Fin$FET is 4.4 eV and 4.8 eV for the $\text{P} - Fin$FET. The doping levels N_a and N_d in the fins for the $\text{N} - Fin$FET and $\text{P} - Fin$FET are the same: 10^{15} cm^{-3}. The doping level for the drain and source regions is 10^{19} cm^{-3}. The threshold voltages for the N and P FinFETs gives $V_{THN} = 0.3$ V and $V_{THP} = -0.3$ V, respectively. The N-FinFETs have two fins and the P-FinFETs have four fins.

A 2NOR gate with an open in the source of transistor FNB driving one inverter was analyzed (Figure 3a). A 2-vector test pattern was applied, T1: $AB = 00$, T2: $AB = 01$. The current leakage components for the activating vector are shown in Figure 3a. I_{subNN} is the subthreshold current of transistor N, I_{gcN} is the gate-to channel leakage of transistor N, and I_{gsN} (I_{gdN}) is the gate-source (gate-drain) edge direct tunneling of transistor N. When the activating vector is applied, a gate with an SOF has three current leakage components as follows.

1) *Charging component:* It is the leakage currents entering the high impedance node [e.g., node-V_X in Figure 3a]. These current leakages raise the voltage at the high impedance node making the detection of an SOF located in the nMOS network more robust. For the 2NOR gate with an open in the source of transistor FNB (Figure 3a), the currents involved in this leakage component are indicated by arrows entering to the high impedance node.

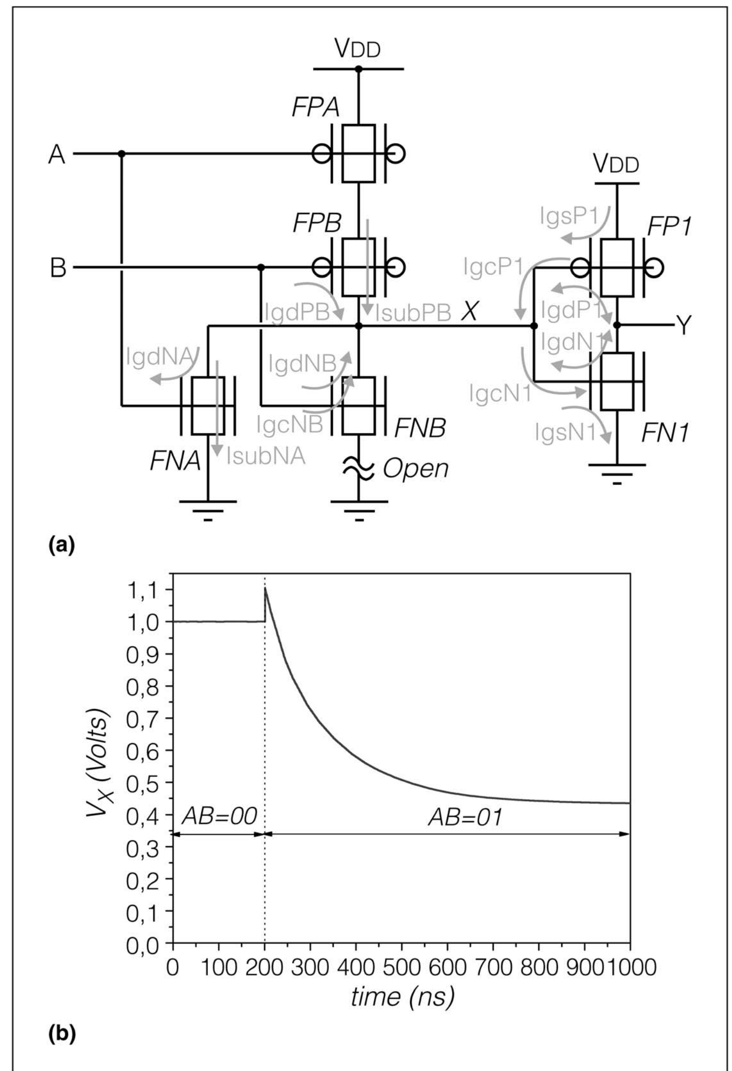


Figure 3. 2NOR gate and its electrical response under an SOF defect. (a) 2NOR gate having an SOF at transistor FNB with the leakage components for the activating vector. (b) Response of node-V_X of the 2NOR with an SOF in transistor FNB. $AB = 00$, ($t < 200$ ns), $AB = 01$, ($t > 200$ ns).

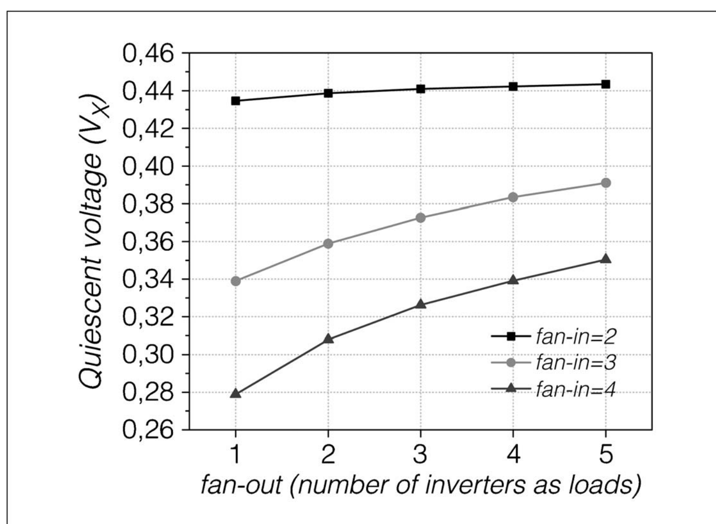


Figure 4. Quiescent behavior of node V_X of the NOR gate having an SOF at transistor FNB for different *fan-in* and *fan-out*.

2) *Discharging component:* It is the leakage currents exiting the high impedance node. These current leakages decrease the voltage at the high impedance node. This makes the detection of the SOF located in the nMOS network more difficult. The currents are indicated by arrows exiting the high impedance node (Figure 3a).
3) *Charging/discharging component:* These leakage currents may change their direction depending on the change in voltage at high impedance node. They are indicated by a line with arrows at both ends (Figure 3a). Their presence makes it more difficult for SOF detection because they initially exit the high impedance node. They reverse their current when the voltage at the high impedance node drops to the threshold voltage of the driven inverter.

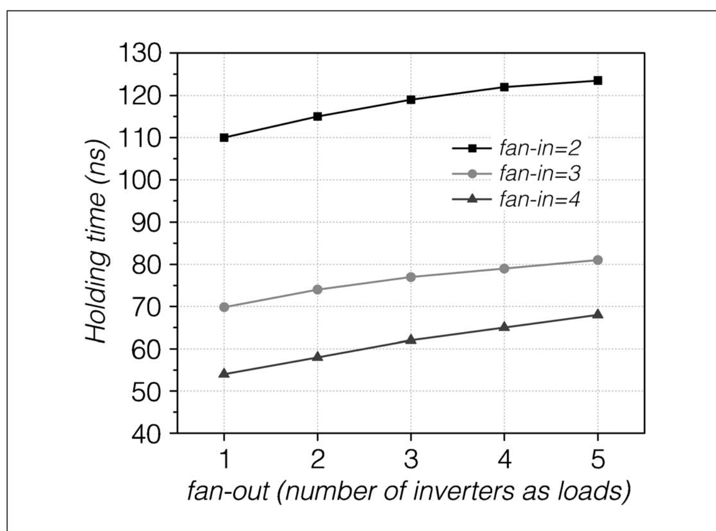


Figure 5. Holding time dependence on the fan-in and fan-out for the NOR gate having an SOF at transistor FNB.

Behavior of a gate with a SOF

The effects of leakage currents on node-V_X of the 2NOR gate for the activating vector are shown in Figure 3b. The drive ON current of the designed transistors is strong enough that proper logic and timing behavior exist in normal operating mode. For the nMOS devices, the drain saturation current is 3.061 mA at $V_{GS} = V_{DS} = 1$ V, and the subthreshold current current is 1.75 nA at $V_{GS} = 0$ V, $V_{DS} =$ 1 V. Node-V_X (Figure 3a) was partially discharged in a relatively short time (Figure 3b). The time constant was about 100 ns compared to several seconds in older technologies. This lowered voltage may be interpreted as a logic low state by the next stages. Notice that node-V_X is discharged to a steady state voltage around $V_{DD}/2$. Other steady values may appear depending on the technology, topology of the affected gate, loading gate(s) and interconnect capacitance. Waveforms in real ICs are quite noisy, and not smooth as is the simulation of Figure 3b. This means that the output nodes are subject to noise during most of the discharge time.

The dependence of the quiescent behavior of the defective NOR gate on its fan-in and fan-out is shown in Figure 4. The quiescent voltage (V_X) decreases for higher fan-in. Intermediate voltages may be non-correctly interpreted and are subject to noise.

Holding time behavior

Holding time is the time for Node-V_X to discharge from V_{DD} to $V_{DD} - |V_{TP}|$. It is a measure related to the delay induced by the SOF defect. Beyond this voltage both inverter transistors turn-on and enter the high gain transition region causing a rapid response. The holding time was simulated for the NOR gate with different fan-in and fan-out (see Figure 5).

Holding time has a strong dependence on the number of leakage paths from the output node to GND. The number of subthreshold leakage paths from the output node to ground increases as the

number of inputs of the NOR gate increases leading to smaller values of the hold time. The holding time increases as the number of inverters connected to Node-V_X increases. These results suggests that slower clock periods increase the chances of error detection. Hence, a strict SOF model assumption no longer applies for semiconductor technologies having significant leakage.

Improving robustness of SOF detection

Controlling gate leakage at the driven gates

Proposed test exciting conditions. We can increase the robustness of SOF detection by controlling the gate leakage at the driven gates. Gate-to-channel and EDT leakage currents may be present for a turned-on transistor. The four possible states of a turned-on nMOS transistor are shown in Figure 6a. The current directions are as indicated.

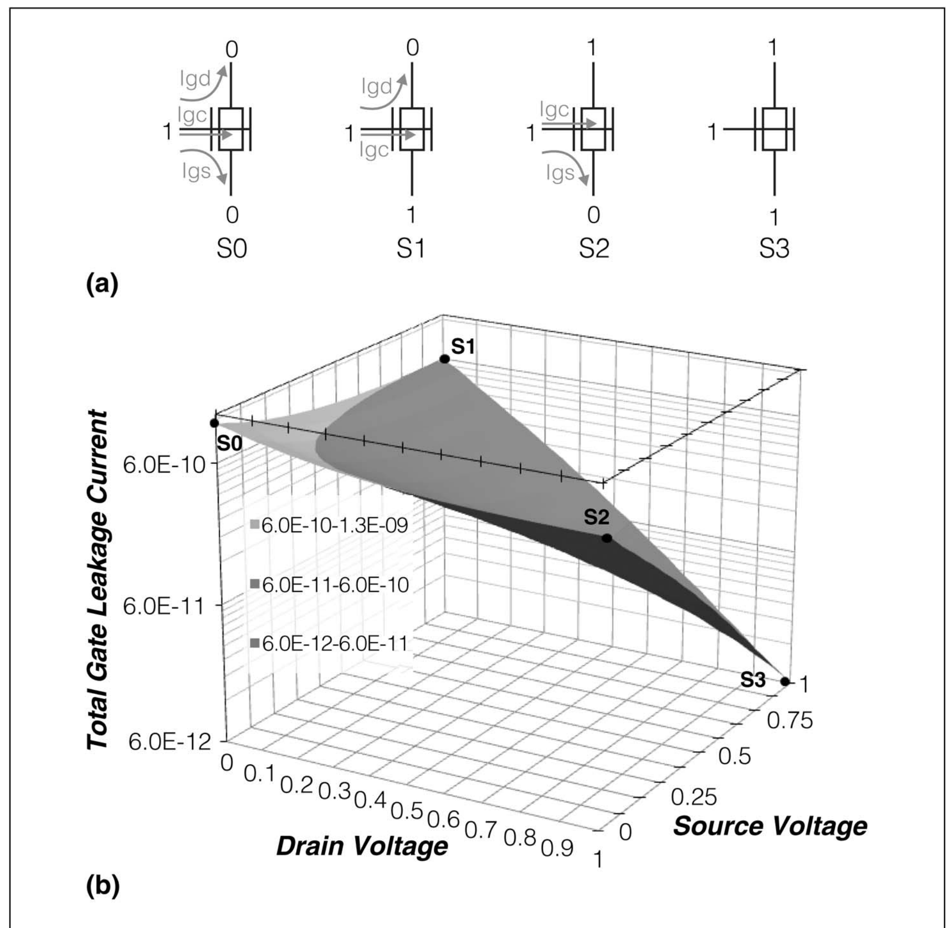


Figure 6. Possible gate leakage states of an nMOS FinFET transistor and its gate leakage current for ON condition. (a) States for an ON nMOS transistor and (b) gate leakage current for an ON nMOS transistor.

Figure 6b plots the gate leakage currents of a turned-on transistor as a function of its drain/source voltages. The gate leakage reduces as the voltages at the drain/source terminals increases. The gate leakage current maximizes at the state S0 ($V_S = 0$ V $V_D = 0$ V), reduces at the states S1 and S2 ($V_S = 0$ V $V_D = 1$ V and $V_S = 1$ V $V_D = 0$ V), and minimizes at the state S3 ($V_S = 1$ V $V_D = 1$ V). A small gate leakage current remains at this state. Actually, the voltages at the drain/source terminals of some serial transistors may only reach $V_{DD} - V_{TN}$.

Similarly, four possible states appear for a turned-off nMOs transistor. In this case, there is no gate-to-channel leakage current, and the direction of the EDT leakage currents reverses. The four possible states of a pMOS transistor can be analyzed in a similar way. Table 1 summarizes the drain and source voltage conditions to minimize/maximize the leakage current for the nMOS and pMOS transistors. Because of this, proper logic conditions at the drain/source terminals can be applied to improve robustness of SOF detection. Robust conditions to test for SOFs in the pMOS network can be stated similarly.

A 2NAND gate with an open in the drain of transistor FNB is considered (Figure 7). After

Table 1 Conditions to minimize/maximize gate leakage.

		V_G	V_S	V_D	**Nmos** leakage	**Pmos** leakage
On nMOS	S0	1	0	0	Maximize	Maximize
Off pMOS	S3	1	1	1	Minimize	Minimize
Off nMOS	S0	0	0	0	Minimize	Minimize
On pMOS	S3	0	1	1	Maximize	Maximize

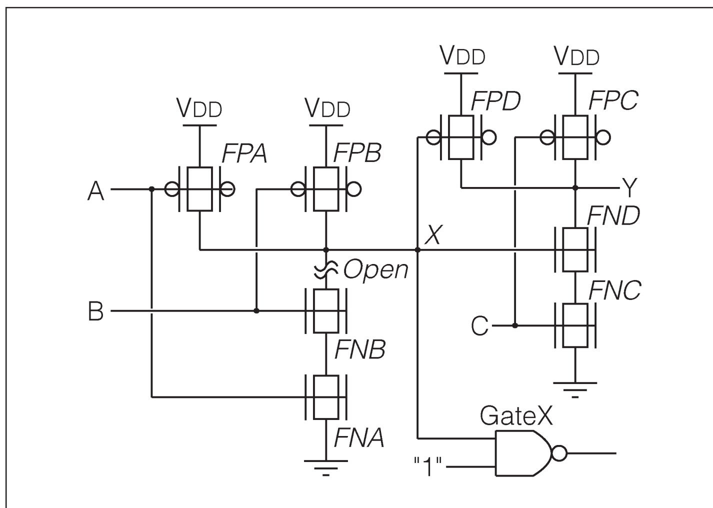


Figure 7. 2NAND gate with an SOF in the nMOS network.

application of a two-vector test pattern, the output of the defective 2NAND gate is initialized to a high logic to test an SOF in the nMOS network, and is in a high impedance state due to the presence of the open. As a consequence, the gate leakage of the driven gates exits the high impedance node. The gate leakage lowers the voltage at the high impedance node jeopardizing the SOF detection. Taking into account our previous gate current leakage analysis, the following conditions are stated for improving the detection of an SOF in the 2NAND nMOS network.

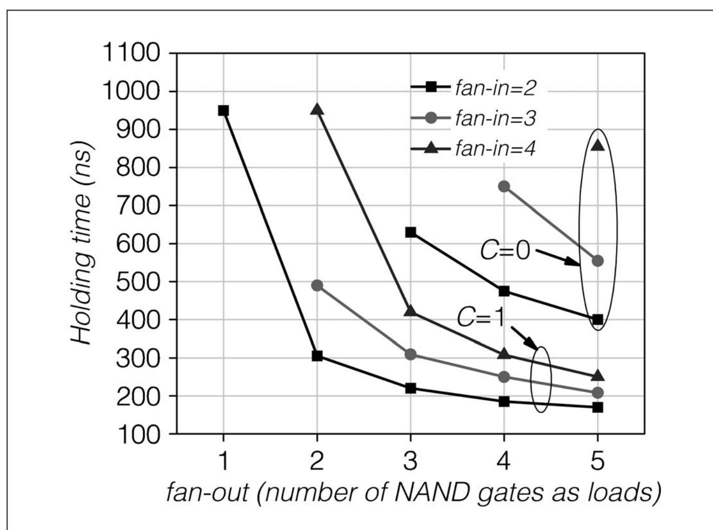


Figure 8. Holding time behavior of the NAND gate with and SOF in the nMOS network for two exciting test conditions.

- *Condition I:* Minimize the gate leakage current of the turned-on nMOS transistor(s) of the driven gate(s) connected to the high impedance node. This condition is achieved when the drain/source voltages of the turned-on transistor(s) are biased at state S3 (see Figure 6b and Table 1).
- *Condition II:* Minimize the gate leakage current of the turned-off pMOS transistor(s) of the driven gate(s) connected to the high impedance node. This condition is achieved when the drain/source voltages of the turned-off pMOS transistors are biased at state S3 (Table 1).

The output of the defective NAND gate is propagated properly through the GateX (Figure 7). Fanout refers to the number of loading gates with a controlling input "C". For the driven NAND gate(s) in Figure 7, condition I is achieved for input-C set to logic-0. Condition II is also achieved for input-C set to logic-0. Under this input, the drain voltages of transistors FND and FPD go to logic-1. Hence, the leakage current exiting the high impedance node decreases. The holding time behavior of a defective NAND gate for the two possible exciting conditions of input-C is shown in Figure 8. The holding time values for input-C set to logic-0 are larger than for input-C set to logic-1. Hence, setting input-C to logic-0 gives a more robust condition to test for an SOF due to an open in the drain of transistor FNB (Figure 7).

Tables 2 and 3 show the results for two possible gate topology configurations. Different open locations have been considered. Table 2 (Table 3) shows the results for a defective 2NAND (2NOR) gate having a 2NOR (2NAND) as load. Op1 is the open located at the drain of the upper (lower) nMOS (pMOS) transistor of the defective NAND (NOR) gate, Op2 is the open located at the source of the lower (upper) nMOS (pMOS) transistor, Op3 is the open located at the drain of a parallel pMOS

Table 2 Benefits reached with our test exciting strategy for a 2NAND-NOR gate configuration.

	HT (Best Case)	HT (Worst Case)	ΔHT
Op1	994ns	887ns	12%
Op2	1.34μs	1.1μs	21.8%
Op3	400ns	200ns	100%
Op4	644.2ns	313.3ns	105.6%

(nMOS) transistor, and Op4 is the open located at the source of a pMOS (nMOS) transistor. "Worst case" in Tables 2 and 3 stands for the worst test vector condition at the inputs of the load gate, and "best case" states for the best test vector condition (our proposal).

For the 2NAND-NOR configuration, an increment in the holding time (HT) is observed for the considered open locations. This makes more robust SOF detection. More increment in holding time (ΔHT) is observed for open locations located in the pMOS network. For these opens, the gate leakage current, which is under control by the exciting vector, is due to nMOS transistors that have higher leakage values than the pMOS transistors. For the 2NOR-NAND configuration, opens located in the pMOS network (Op1 and Op2) also present better test improvements than opens located in the nMOS network (Table 3). In these cases, the value at the output node of the defective gate never reaches V_{TN} (marked with - at Tables 2 and 3). However, from quiescent analysis, it is observed that the values at the output of the defective gate are much closer to 0 V when the best exciting conditions are applied.

Test pattern generation vectors with improved test conditions. The previous test exciting conditions were implemented using a modification of a reported test pattern generation tool [24]. Then, test vectors were generated for various ISCAS benchmark circuits synthesized using inverters, NAND and NOR gates. The following actions (Table 4) take place for each gate of a circuit (an SOF in the pMOS network is assumed).

- Force a "0" logic value at the output of the gate under analysis and justify this value at the primary inputs. The percentage of gates satisfying this condition is shown in column *Pre* 0 (Table 4).
- Force a "1" logic value at the output of the gate under analysis. For the case of parallel transistors this is made for each branch. One of the fan-out gates is selected to propagate the information of the gate under analysis, and the improved test exciting conditions are applied to the rest of the load gates. The values are justified at the primary inputs. If this is not possible, a new attempt is made through another load gate until covering all the options. Finally, the information of the defective gate is propagated through the selected gate to a primary output. The percentage of cases (including parallel transistors) satisfying this procedure is shown in column *Post* 1 (Table 4).

Table 3 Benefits reached with our test exciting strategy for a 2NOR-NAND gate configuration.

	HT (Best Case)	*HT* (Worst Case)	Δ*HT*
Op1	–	–	–
Op2	–	–	–
Op3	114.6ns	75.7ns	51.2%
Op4	116.2ns	76.2ns	52.4%

A similar procedure also has been implemented for SOFs in the nMOS network. The test exciting conditions are implemented according to the type of gate. Let us consider an input *i* in a NAND gate, Condition I is accomplished by placing a logic 1 (0) for all the transistors above (below) the one under analysis. A similar process has been used for the other test conditions for the different gates. Table 4 shows that the defective gate can be properly initialized for most cases. This is given by Pre 0 (Pre 1) for SOFs in the pMOS (nMOS) network. The sensitization vectors with improved test conditions can also be generated for most cases. This is given by Post 1 (Post 0) for SOFs in the pMOS (nMOS) network.

Controlling subthreshold leakage of a transistor stack at the defective gate

The output of the defective gate is determined by the cross point of the leakage components entering

Table 4 Percentage of successful test pattern generation cases with improved test conditions for SOFs.

ISCAS	Pre 0	Post 1	Pre 1	Post 0
C17	100	100	100	100
C432	100	94.7	100	95.5
C499	97.3	92.1	97.3	93.5
C880A	100	94.7	100	95
C1355	95.4	91.7	95.8	92.5
C1908	100	88.3	100	90.9
C2670	100	96.9	100	97.7
C3540	100	95.1	100	92.1
C5315	100	96.1	100	96.1
C6288	98.6	83.8	98.7	84.1
C7552	100	90.1	100	89

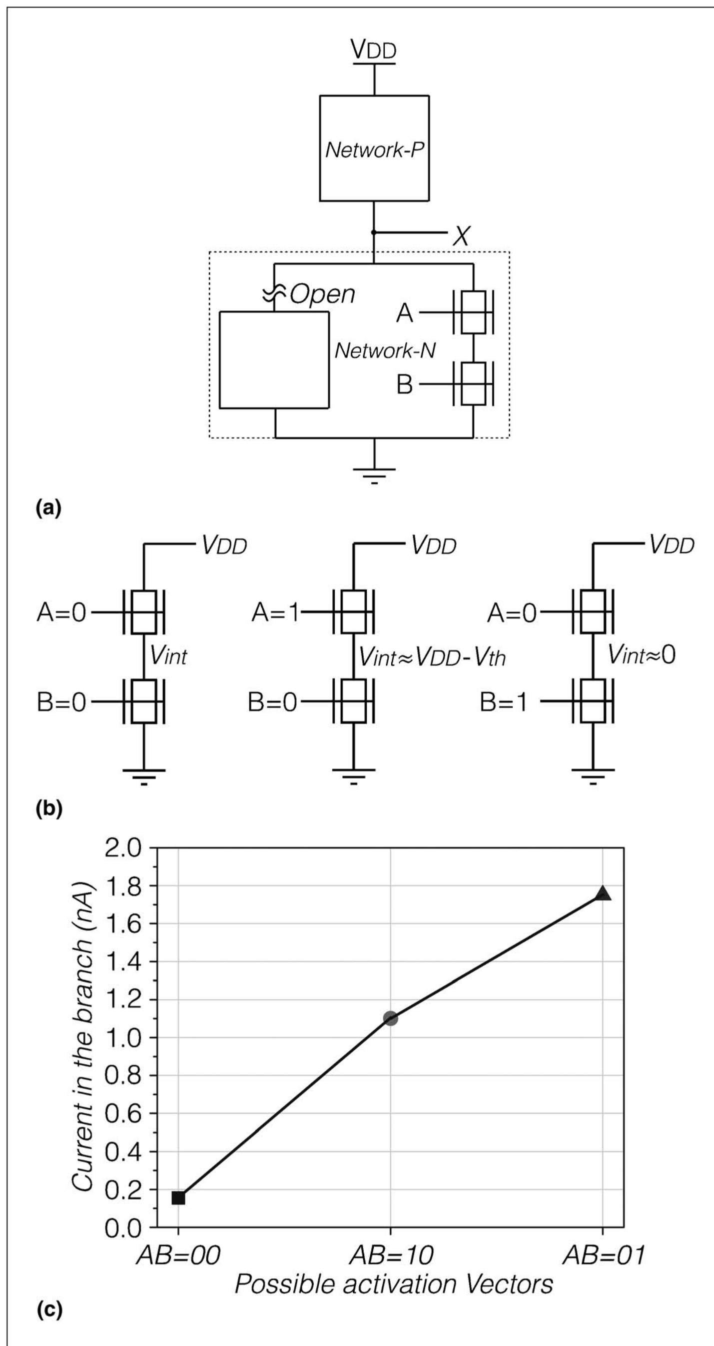


Figure 9. Subthreshold leakage behavior of a two stack transistors. (a) Defective gate; (b) possible activation vectors; (c) subthreshold leakage.

and exiting the high impedance node [20]. The steady-state voltage at the high impedance node increases (decreases) as the leakage that enters (exits) the high impedance node increases. Therefore, a proper input pattern can be chosen to control the subthreshold leakage due to the stacking transistor in the defective gate in order to improve the detectability of SOFs.

Figure 9a shows a possible nMOS network topology with an SOF in one branch having another parallel branch formed with two stacked nMOS transistors. For the stacked transistors, there are three possible activation conditions (Figure 9b). The activation vectors $AB = 01$ and $AB = 10$ put $V_{DS} = V_{DD}$ and $V_{DS} = V_{DD} - V_T$ at the turned-off nMOS transistors, respectively. As a consequence, the subthreshold current through the nMOS network for $AB = 01$ is higher than for $AB = 10$ (Figure 9c).

The subthreshold leakage current is minimized for the vector $AB = 00$. This is because two stacked nMOS transistors significantly reduce the subthreshold leakage current compared to a single turned-off transistor. For the two stacked transistors the intermediate voltage (V_{int}) raises above 0 V [13]. As a consequence, the top nMOS transistor (Figure 9a) suffers: a) a negative V_{GS}, and b) a V_{DS} reduction. The subthreshold leakage current through the stack decreases with the number of turned-off transistors in the stack.

From our previous analysis, the following condition is stated for improving the detection of an SOF in the nMOS network:

- *Condition III:* Minimize (or maximize) the subthreshold leakage current in the nMOS (pMOS) network. This condition is achieved by turning-off the nMOS transistors in the stack.

A simple AOI gate having an inverter as load (Figure 10) has been analyzed. Different open locations were considered. It is assumed that the defect lets one branch open while the other branch remains connected to the output. This situation may appear in a complex gate depending on the complexity of its boolean function and layout. Table 5 shows the results and also the applied sensitization vectors (ABCD). Significant increment in the Holding Time (ΔHT) is obtained for opens Op1 and Op2 (Table 5) making more robust their defect detection. Lower benefits are found for opens Op3 and Op4. The quiescent voltage in node-V_X for open Op4 does not arrive to the voltage value defining the Holding Time for the best case. For opens located in the nMOS (pMOS) network the output of the defective gate is initialized at a high- (low-) logic

level. Because of a higher drain voltage at the drain of the upper nMOS transistor at the moment of the sensitization vector, the leakage current has a higher impact on the increment of the holding time for opens located in the nMOS network with respect to opens located in the pMOS network.

Influence of temperature, process variations and high-K dielectric on SOF behavior

Effect of temperature and process variations

The temperature has a strong influence on the threshold voltage [2] which significantly impacts the subthreshold leakage current. However, gate tunneling current is almost insensitive to temperature variation [25]. The dependence of the quiescent behavior (V_X) of a defective NOR gate (Figure 3a) on the temperature is shown in Figure 11a. A NOR gate with fan-out of 1 and different fan-in was considered. For a given fan-in, the quiescent voltage decreases as the temperature increases. The subthreshold current of the NOR nMOS network rises at a higher rate than the subthreshold current of the pMOS network as the temperature increases. The temperature impact is more acute for larger fan-in because more leaking branches are added. The holding time dependence on temperature is plotted in Figure 11b. The holding time also decreases as the temperature increases. Depending on the particular topology and sizing of the gate(s) the temperature adds fluctuations on the leakage current levels.

The behavior of SOFs under process parameter variations was analyzed [13], [26]. Variations in channel length (L_{ch}), fin width (T_{si}) and gate oxide thickness (t_{ox}) were considered [13]. The subthreshold current is influenced by all the considered parameters while the gate leakage is mainly influenced by the gate oxide thickness. Random dopant fluctuations has not a strong impact in the electrical parameter in these devices [26]. In a Monte Carlo simulation, Gaussian distributions with $3\sigma = 15\%$ variation was considered for the three considered parameters ($L_{ch}, T_{si}, t_{\text{ox}}$). For the defective 2NOR gate shown in Figure 3a, the mean value of the holding time is 82 ns with 3σ of 49.43 ns. These results indicate that due to process variations the holding time may significantly reduce for a significant number of fabricated gates. Hence, the SOF detection may be invalidated for these gates. The results may be influenced by the impact of correlated parameter variations. However, the illustrated impact of random process variations on SOF behavior remains.

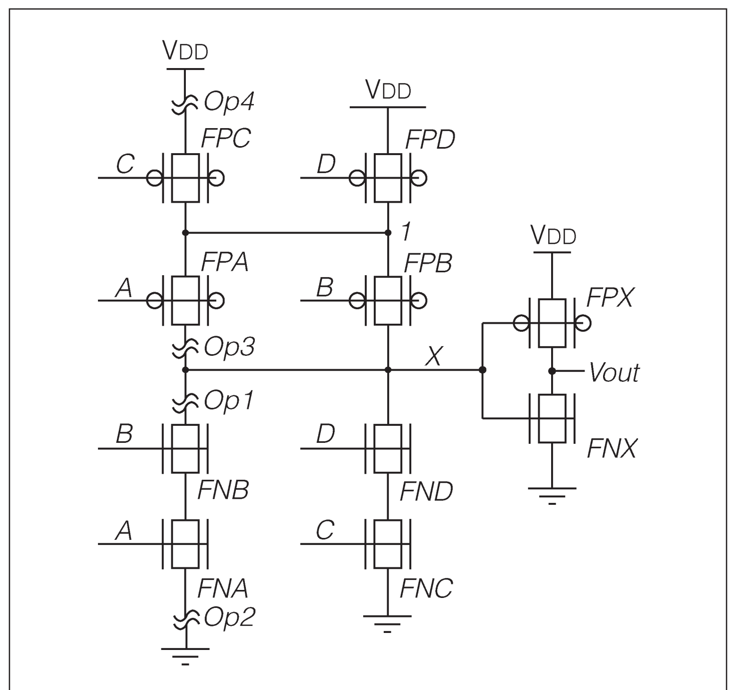


Figure 10. AOI gate with some possible open drain locations.

Influence of using a high-k as dielectric

The test implications of SOFs for technologies using a high-k gate dielectric (Si_3N_4) were investigated. When Si_3N_4 is used as a gate dielectric in the NOR gate shown in Figure 3a ($fan-out = 5$), the holding time is 460 ns for $fan-in = 2$ and 140 ns for $fan-in = 4$. Although the subthreshold leakage decreases due to the high-k gate dielectric it continues to impact the behavior of the SOF. The quiescent voltage at node-V_X and the holding time exhibits dependence with the fan-in of the defective gate. The gate leakage significantly reduces due to

Table 5 Summary of the benefits reached with our proposal testing methodology

	HT (Best Case)	*HT* (Worst Case)	ΔHT
Op1	(ABCD=1100) 270.7ns	(ABCD=1110) 116.5n	132.36%
Op2	(ABCD=1100) 270.9n	(ABCD=1110) 112n	141.87%
Op3	(ABCD=0110) 209.5n	(ABCD=0100) 171.2n	22.37%
Op4	(ABCD=0001) Vx=0.293	(ABCD=1001) 317.1n	–

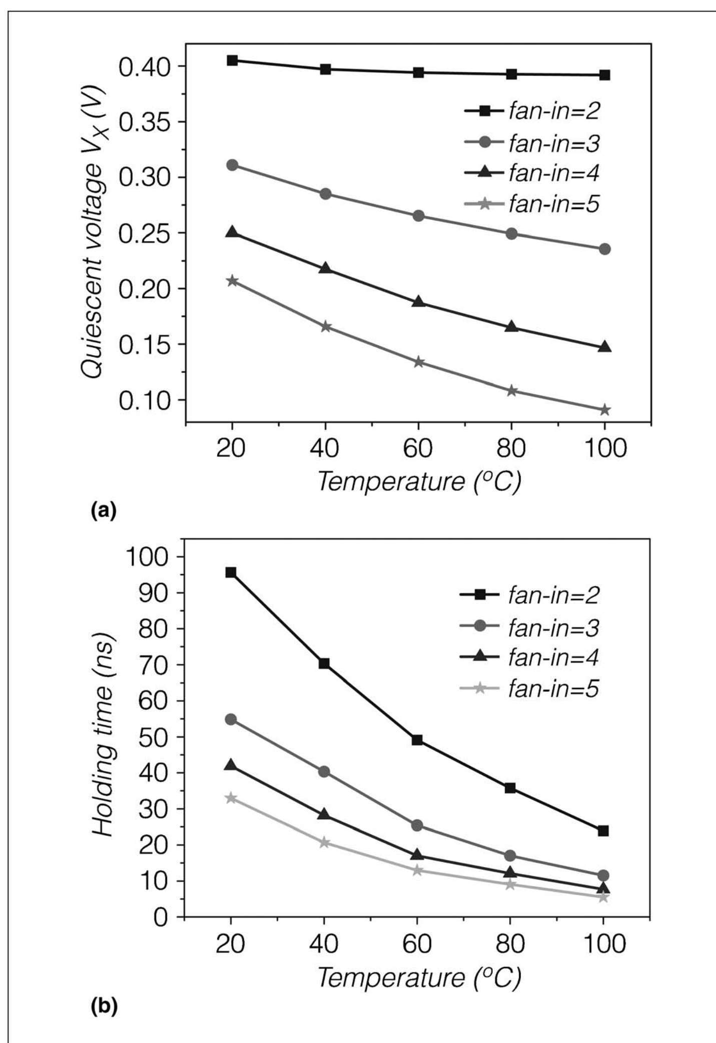


Figure 11. Dependence of the behavior of a defective NOR gate on the temperature. (a) Quiescent state and (b) holding time.

the higher thickness of the high-k dielectric [13]. Hence, the gate leakage influence on SOF behavior is less significant. However, this dielectric thickness will also scale downward over time and ultimately face the same gate leakage problem.

Test engineers must understand the reality and complexity of the SOF in modern ICs. The data here indicate that the classical SOF behavior is modified by the increased transistor off-state leakage current and smaller node capacitances in nanometer technologies.

The modern IC SOF response is a mix of classical and nonclassical responses that are functions of fan-out, fan-in, clock period, local leakage environment, noise, V_{DD} and temperature. Two vector strategies were proposed to improve the robustness of SOF detection in the presence of leakage currents. The first is based on controlling the gate leakage current at the fan-out gates, and the second is based on controlling the subthreshold leakage current at the defective gate. SOF detection in technologies using high-k dielectric is more robust due to the significant reduction of the gate leakage current. However, gate leakage ultimately will become again important as the dielectric scale downward. The complex nature of SOF is also strongly technology driven.

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