

## Resistive bridge defect detection enhancement under parameter variations combining Low $V_{DD}$ and body bias in a delay based test

Hector Villacorta<sup>a,b,\*</sup>, Victor Champac<sup>a</sup>, Sebastià Bota<sup>b</sup>, Jaume Segura<sup>b</sup>

<sup>a</sup> Dept. of Electronic Engineering, National Institute for Astrophysics, Optics and Electronics – INAOE, Puebla, Mexico

<sup>b</sup> GSE-UIB, University of Balearic Islands, Mallorca, Spain

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### ABSTRACT

Resistive bridges are a major class of defects in nanometer technologies that can escape test, posing a serious reliability risk for CMOS IC circuits. The increase of process parameter variations represents a challenge for resistive bridge detection using traditional test methods, and requires more efficient test methods to be developed. In this work, we show that resistive bridge detection improves by correlating the defect-induced extra circuit delay with the power supply voltage value and the reverse body bias (RBB) applied. A *Timing Critical Resistance* ( $R_{crit}^t$ ) is defined as a metric to quantify the resistive bridge detection enhancement in the presence of process variations under a delay based test. We show that the smaller the supply voltage, the higher the resistive bridge detection which further enhances by applying RBB. Results are presented for a 65 nm CMOS technology.

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### 1. Introduction

Manufacturing defects stand as an important issue in nanometer technologies among which resistive bridges represent a major class and have received increased attention. A bridge defect is an unintentional connection between two or more circuit nodes which may induce unexpected circuit electrical behavior. For sufficiently small resistance values, these bridge defects cause a failure that can be detected by traditional test methods. If the resistance is not so small, these defects do not produce circuit failures and hence escape detection when traditional test methods are used [1]. However, a quiescent current path between the power supply and ground appears due to the bridge defect. This path may cause high stress and increased power consumption in the circuit, constituting a reliability risk in nanometer CMOS ICs [2–5]. Moreover, it has been extensively shown that the impact of process parameter variations is becoming a challenge in nanometer technologies. Process variations have a negative impact on test performance and various test techniques have been developed to improve resistive bridge detection [6]. In [7] a method is presented to determine the critical resistance of a bridge defect whose value is the limit between a correct logic value and a fault. In [8] the advantage of test application at reduced  $V_{DD}$  was analyzed, showing that resistive

bridge defects fault coverage depends on the supply voltage applied during test. The work in [9] analyzed the effectiveness of low voltage testing, low temperature testing, and their combination on the detection of resistive bridge defects through logic testing. They showed that the fault coverage increased significantly when Low  $V_{DD}$  testing was applied and when more test time was available. In a preliminary work [10] we investigated the delay variance dependence on the progressive supply voltage lowering and defined a dynamic critical resistance to analyze the effectiveness of low voltage testing on the detection of resistive open and bridge defects. In [6] an automatic test generation method considering process variation for static defects is proposed.

Body biasing is a design technique proposed to enhance optimum power consumption and performance for microprocessors manufactured using dual  $V_{TH}$  in sub-100 nm technology generations [11]. In particular, it has been shown that forward body bias (FBB) reduces the transistor threshold voltage ( $V_{TH}$ ) variance [11]. The impact of body bias on delay fault testing was analyzed in [12]. The results show that the delay test cost overhead, in terms of the number of paths to be tested, could be reduced by adopting FBB. Reverse body bias (RBB) is another body bias technique that was applied to improve  $I_{DDQ}$  testing as it increases the transistor threshold voltage and contributes to intrinsic leakage current reduction. In [13] a multi-parameter test technique, based on correlating the intrinsic leakage to the microprocessor frequency, was analyzed taking RBB as a third parameter to enhance the test resolution. However, RBB provided minimal leakage reduction diminishing test sensitivity. In [14] a low voltage test combined to substrate biasing was proposed showing that this method could

\* Corresponding author at: GSE-UIB, University of Balearic Islands, Mallorca, Spain. Tel.: +34 618686052.

E-mail addresses: [h.villacorta@uib.es](mailto:h.villacorta@uib.es), [hvillacorta@inaoep.mx](mailto:hvillacorta@inaoep.mx) (H. Villacorta), [champac@inaoep.mx](mailto:champac@inaoep.mx) (V. Champac), [sebastia.bota@uib.es](mailto:sebastia.bota@uib.es) (S. Bota), [jaume.segura@uib.es](mailto:jaume.segura@uib.es) (J. Segura).

detect defects that were not detected by  $I_{DDQ}$  tests. The scalability of body-biasing technique to sub-100 nm CMOS technologies is affected by smaller body effect [15]. Nevertheless, in [16] the sensitivity of the threshold voltage to the body bias for NMOS and PMOS transistors is analyzed. It was found that the  $V_{TH}$  sensitivity to the body bias reduces only 12% for NMOS and 10% for PMOS transistors when going from 90 nm to 22 nm. This shows the feasibility of using body bias for manipulating the transistor threshold voltages in nanometer technologies [17–19]. The work in [20] points to the need of detecting high-resistance bridging defects highlighting that these defects cannot be detected by logic test methods.

In this work we propose a method to improve resistive bridge detection by applying Low  $V_{DD}$  and reverse body bias on delay testing. Given the influence of supply voltage and RBB modulation on the parameter variations impact on delay, a new specific metric is defined to quantify this effect. The work is applied to a 65 nm CMOS commercial technology. The rest of the paper is organized as follows: Section 2 presents the impact of process variations on correlated delay. A simple gate delay model is used to define the delay variance as a function of  $V_{DD}$  and process parameters. In Section 3 the *Timing Critical Resistance* ( $R_{crit}^t$ ) is defined in terms of process parameters providing also the resistive bridge detection conditions. The effectiveness of combining Low  $V_{DD}$  with reverse body bias (RBB) is evaluated in Section 4 while in Section 5 the results are presented. In Section 6 a comparison with logic test and test cost evaluation are presented. Finally, in Section 7, the conclusions are given.

## 2. Impact of process variations on correlated delay

### 2.1. Delay model considering process parameter variations

Using the alpha power law developed in [21], the delay of a CMOS gate at the position  $i$  in a path is given by,

$$T_D(i) = \frac{C_i V_{DD} L T_{ox}}{\mu \epsilon_{ox} W (V_{DD} - V_{TH})^\alpha} \quad (1)$$

where  $C_i$  is the capacitance at the gate output,  $V_{DD}$  is the supply voltage,  $V_{TH}$  is the transistor threshold voltage,  $\alpha$  is the Sakurai's index,  $L$  is the transistor channel length,  $W$  is the transistor channel width,  $\mu$  is the carrier's mobility,  $T_{ox}$  is the gate oxide thickness, and  $\epsilon_{ox}$  is the gate oxide permittivity.

In this work we consider symmetric gates with equal high-to-low and low-to-high propagation delays. According to Eq. (1), the delay of a gate at position  $i$  depends on process parameters ( $L$ ,  $W$ ,  $T_{ox}$ ,  $V_{TH}$ ) which are considered random variables. Thus,  $T_D$  can also be considered a random variable, and their variations can be approximated to follow a normal distribution. Subsequently, the mean and standard deviation of a single delay path ( $\mu_{path}$  and  $\sigma_{path}$ ) composed of  $N$  identical gates connected in series, assuming no-correlation between gates, can be estimated by a multi-variable Taylor-series expansion [22]. Assuming process parameter to be independent, then,

$$\mu_{path} = N T_D \left( 1 + \left( \frac{1}{2} \frac{\alpha(\alpha+1)\sigma_{Vth}^2 + \sigma_W^2}{(V_{DD} - V_{TH})^2 + W^2} \right) \right) \quad (2)$$

$$\sigma_{path}^2 = N \left( \frac{C_i V_{DD}}{\mu_n \epsilon_{ox} (V_{DD} - V_{TH})^\alpha} \right)^2 \left[ \left( \frac{\alpha L T_{ox}}{W (V_{DD} - V_{TH})} \right)^2 \sigma_{Vth}^2 + \left( \frac{T_{ox}}{W} \right)^2 \sigma_L^2 + \left( \frac{T_{ox} L}{W^2} \right)^2 \sigma_W^2 + \left( \frac{L}{W} \right)^2 \sigma_{Tox}^2 \right] \quad (3)$$

where  $T_D$  is the nominal delay of a single gate given by Eq. (1) and  $N$  is the number of gates in the circuit path.  $\sigma_{Vth}$ ,  $\sigma_L$ ,  $\sigma_W$ ,  $\sigma_{Tox}$  are the

standard deviation of  $V_{TH}$ ,  $L$ ,  $W$  and  $T_{ox}$ , respectively. It is observed that  $\mu_{path}$  and  $\sigma_{path}$  depends on  $V_{DD}$ , as  $V_{DD}$  decreases,  $\mu_{path}$  and  $\sigma_{path}$  increases. The values of  $\sigma_{Vth}$ ,  $\sigma_L$ ,  $\sigma_W$ , and  $\sigma_{Tox}$  are similar for NMOS and PMOS transistors. We evaluated the impact of the variations on  $\sigma_{path}$  through simulations and obtained a deviation below 5%. Therefore, for simplicity they are assumed to be the same in Eq. (3).

### 2.2. Correlating the power supply voltage and path delay in the presence of process variations

Eqs. (2) and (3) are used to obtain the path delay distribution of a 10-inverter chain.  $\mu_{path}$  and  $\sigma_{path}$  depend on the supply voltage ( $V_{DD}$ ). Lowering  $V_{DD}$  reduces the gate voltage overdrive which increases the transistor resistance with consequent gate delay increase. Thus, the mean delay and delay variance increase as  $V_{DD}$  reduces (See Fig. 1) [10,23]. The relative impact on  $\mu_{path}$  and  $\sigma_{path}$  as  $V_{DD}$  reduces play an important role to determine the effectiveness of a delay based method at a Low  $V_{DD}$ . This will be further analyzed in the next section.

## 3. Resistive bridge detection

### 3.1. Resistive bridge model

Let us assume an inverter chain with a resistive bridge defect between an inverter output and the power supply located at the middle of the chain (Fig. 2). The reduced complexity of this inverter chain circuit allows to make an in depth theoretical analysis of the bridge behavior at Low  $V_{DD}$  under process variations. The main variables affecting bridge detection are identified.  $R_{br}$  is the bridge resistance and  $C$  represents the gate load capacitance at the defective node.

The extra delay due to the resistive bridge defect is computed using the mathematical model proposed in [24]. Eq. (4) indicates the extra delay due to resistive bridge defect,  $t_{dbr}$ ,

$$t_{dbr} = \left( -c \times \log_2 \left( \frac{0.5 - h}{g - h} \right) - 1 \right) \times t_{DX}, \quad (4)$$

where  $t_{DX}$  is the nominal delay at node  $X$ . The parameters  $c$ ,  $h$  and  $g$  are calculated according to the input pattern [24]. Since  $R_{br}$  is connected to  $V_{DD}$  and  $R_n$  is the pull down network resistance, these parameters are given by,

$$c = \frac{R_{br}}{R_n + R_{br}}, \quad g = 1, \quad h = 1 - \frac{R_{br}}{R_n + R_{br}}, \quad (5)$$

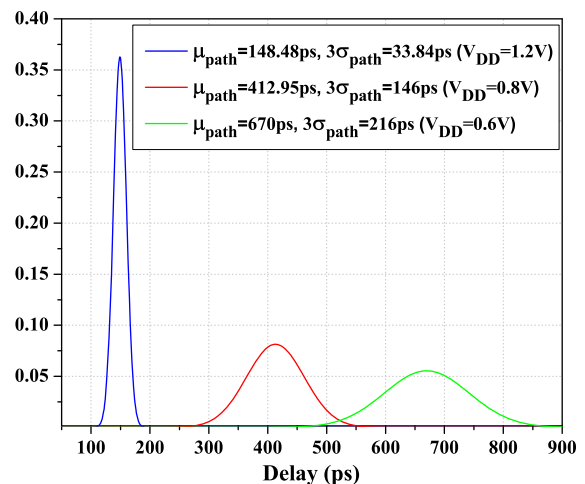


Fig. 1. Delay distribution for 65 nm at  $V_{DD} = 1.2$  V,  $V_{DD} = 0.8$  V, and  $V_{DD} = 0.6$  V.

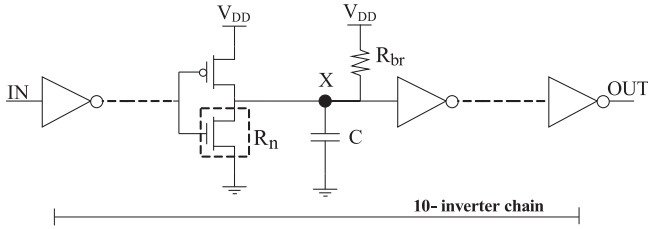


Fig. 2. Resistive bridge fault model.

$R_n$  is computed as the ratio of the drain–source voltage and the drain current in the linear region. The extra delay induced by the defect ( $t_{Dbr}$ ) is added to the mean delay of the defect-free circuit ( $\mu_{path}$ ). The delay increment is inversely proportional to the value of  $R_{br}$ .

### 3.2. Resistive bridge detection condition

As has been extensively shown in the literature, the detection of the resistive bridge defects depends on the resistor divider formed by the pull down resistance of the NMOS transistor,  $R_n$ , and bridge resistance,  $R_{br}$  (See Fig. 2). When the defect is activated, there is a competition between  $R_n$  that pulls the defective node X to ground and the bridge resistance that pulls this node to  $V_{DD}$ . The final state of node X will depend on the relationship between  $R_n$  and  $R_{br}$ .

When the resistive bridge defect has a high resistance value, the delay distributions of the defective circuit and of the defect-free circuit may overlap (See Fig. 3), and because of this detection is not clear for some delay values. Some good circuits can be consider as fail circuits causing yield loss, or fail circuits can be consider good circuits causing reliability issues.

If  $V_{DD}$  reduces, the transistor resistance,  $R_n$ , increases, and the bridge resistance,  $R_{br}$  gains more control over the defective node. This increases the mean delay value of the defective logic path shifting the delay distribution of the defective path toward higher values. On the other hand, the lower the supply voltage, the higher the spread of the delay distribution given the asymptotic behavior of the delay with  $V_{DD}$  [10]. Therefore, the bridge detection through delay testing at reduced  $V_{DD}$  depends on the relationship between  $\mu_{path}$  and  $\sigma_{path}$  at such  $V_{DD}$ . Guaranteeing bridging defect detection requires non-overlapping between the defective and defect-free distributions (See Fig. 4). Such condition holds for a sufficiently low bridging defect resistance value. The higher resistance value for which both distributions do not overlap is such that the defective circuit mean ( $\mu_D$ ) can be approximated by  $\mu_D = \mu_{path} + 6\sigma_{path}$ . This condition ensures that all the possible defective delay values can be clearly discriminated from the defect-free ones.

Therefore, ensuring a bridging defect detection in the presence of process variations, requires the following condition to be satisfied,

$$\mu_D - \mu_{path} > 6\sigma_{path} \quad (6)$$

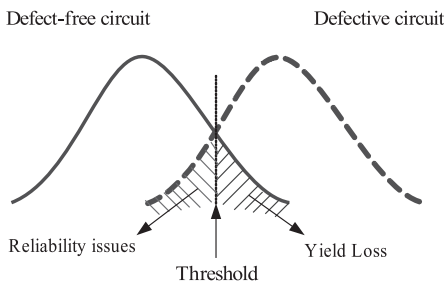


Fig. 3. Delay distribution for a defect-free circuit and for a defective circuit with high bridge resistance.

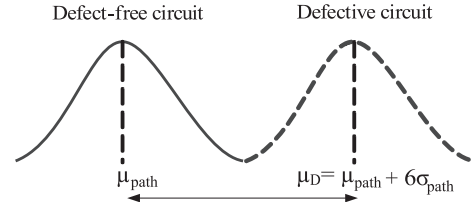


Fig. 4. Delay distribution for a defect-free circuit and for a defective circuit with small bridge resistance.

where  $\mu_D$ ,  $\mu_{path}$ , and  $\sigma_{path}$  vary with  $V_{DD}$ . It is assumed that the  $\sigma_{path}$  for the defect-free and defective circuit is the same. The previous conditions can be used to illustrate the behavior of the bridging defect at Low  $V_{DD}$  under process variations. To analyze the combined impact of  $\mu_D$ ,  $\mu_{path}$  and  $\sigma_{path}$  on resistive bridging detection, the metric  $\Delta\mu/6\sigma_{path}$ , is defined. It represents the normalized delay increment due to the resistive bridge defect.  $\Delta\mu$  ( $=\mu_D - \mu_{path}$ ) is the extra delay introduced by the bridge defect under a particular  $V_{DD}$  and is given by Eq. (4).  $\sigma_{path}$  is the circuit delay standard deviation (Eq. (3)) for a given  $V_{DD}$ .

$$\frac{\Delta\mu}{6\sigma_{path}} \approx \frac{-R_{br} \ln\left(\frac{(-0.5 + \frac{R_{br}}{R_n + R_{br}})(R_n + R_{br})}{R_{br}}\right)}{6\sqrt{N}(R_n + R_{br}) \ln(2) \sqrt{\left(\frac{\alpha L T_{ox}}{W(V_{DD} - V_{TH})}\right)^2 \sigma_{Vth}^2 + \beta}} \quad (7)$$

$$\beta = \left(\frac{T_{ox}}{W}\right)^2 \sigma_L^2 + \left(\frac{T_{ox} L}{W^2}\right)^2 \sigma_W^2 + \left(\frac{L}{W}\right)^2 \sigma_{Tox}^2 \quad (8)$$

Fig. 5 plots  $\Delta\mu/6\sigma_{path}$  as function of  $V_{DD}$  for a given resistive bridge defect of 27 K $\Omega$ . It is shown that  $\Delta\mu/6\sigma_{path}$  increases as  $V_{DD}$  reduces. When  $\Delta\mu/6\sigma = 1$ , the bridge detection can be guaranteed in the presence of process variations. At this point the impact of the defective circuit mean delay increase becomes more important than the combined impact of the increase in both the standard deviation and mean delay of the defect-free circuit.

To quantify the benefits of delay testing at Low  $V_{DD}$  to test bridging defects, a *Timing Critical Resistance* ( $R_{crit}^t$ ) is defined. For any bridge resistance below  $R_{crit}^t$  a delay failure in the presence of process variations is assured. This concept is an extension of the *Dynamic Critical Resistance* introduced in [10].

An expression for  $R_{crit}^t$  is derived to quantify the benefits of resistive bridge detection at a lower  $V_{DD}$ , in the presence of process

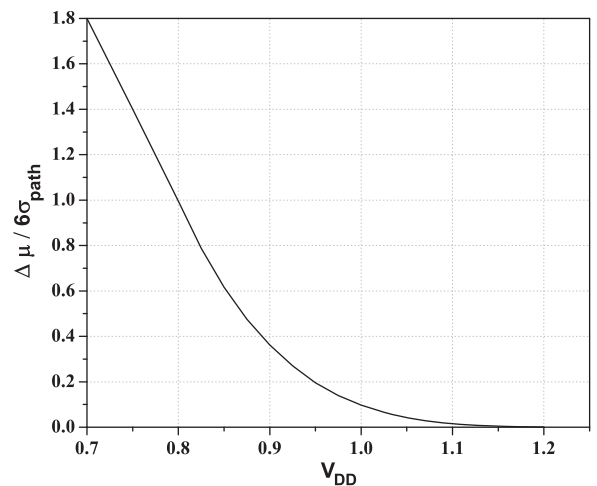


Fig. 5.  $\Delta\mu/6\sigma_{path}$  as function of  $V_{DD}$  for a resistive bridge defect  $R_{br} = 27 \text{ K}\Omega$ .

variations.  $R_{crit}^t$  is obtained when the extra delay due to bridge defect,  $t_{Dbr}$ , (Eq. (4)) equals to  $6\sigma_{path}$ :

$$6\sigma_{path} = \left( -c \times \log_2 \left( \frac{0.5 - \left( 1 - \frac{R_{crit}^t}{R_n + R_{crit}^t} \right)}{1 - \left( 1 - \frac{R_{crit}^t}{R_n + R_{crit}^t} \right)} \right) - 1 \right) t_{DX} \quad (9)$$

Fig. 6 shows the  $R_{crit}^t$  dependance on the supply voltage. It is shown that  $R_{crit}^t$  increases as  $V_{DD}$  reduces. Hence, the bridge detection at a lower power supply voltage is improved when the increase in  $\mu_D$  is much higher than the combined increase in  $\mu_{path}$  and  $\sigma_{path}$  (Eq. (6)) at Low  $V_{DD}$ .

**4. Using reverse body bias to improve resistive bridge detection**

It has been reported that body bias impacts the circuit delay variation through the modulation of the transistor threshold voltage [12]. In particular, reverse body bias (RBB) increases the threshold voltage of the transistor and consequently increases the transistor equivalent resistance. Therefore, application of RBB in conjunction with  $V_{DD}$  reduction causes a further  $R_n$  increase, with respect to only lowering  $V_{DD}$ , making the resistive bridge to have a stronger impact on the defective node behavior. Regarding parameter variations, both the standard deviation and the mean delay increase as RBB increases. Similarly to  $V_{DD}$  lowering, the actual improvement in resistive bridge detection depends on the relative contribution of the different parameters affected by RBB as stated by Eq. (6). The bridge detection under RBB is improved when the increase in  $\mu_D$  is much higher than the combined increase in  $\mu_{path}$  and  $\sigma_{path}$ . Fig. 7 plots the ratio  $\Delta\mu/6\sigma_{path}$  as function of  $V_{DD}$  and RBB for the 10-inverter chain with a resistive bridge of 35 K $\Omega$ . The plot shows that the application of RBB in conjunction with lower  $V_{DD}$  improves even more the resistive bridge detection.

**5. Simulation results**

Without lose of generality the impact of resistive bridges on the delay of 10-inverter chain were simulated for 65 nm CMOS technology. The defect-free path delay was simulated at the nominal and reduced  $V_{DD}$ . Monte Carlo simulations were run using Spectre simulator to obtain the delay distributions. Gaussian distributions with  $\pm 3\sigma$  variation around the nominal value were used. A resistive bridge was connected between one inverter output in the middle of the chain and  $V_{DD}$ . Fig. 8 shows the delay increase induced by

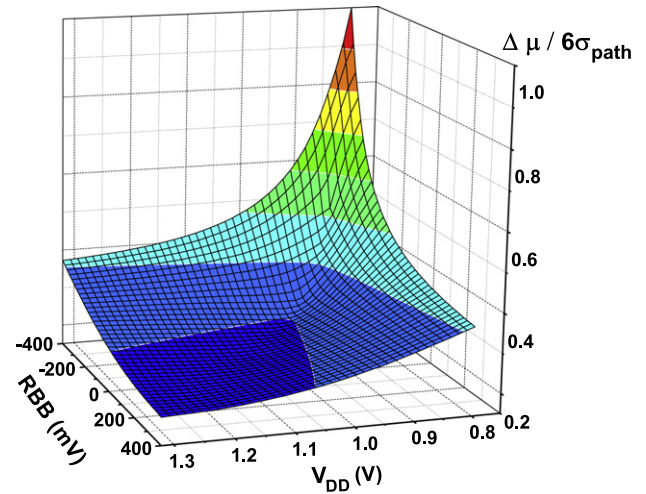


Fig. 7.  $\Delta\mu/6\sigma_{path}$  as a function of  $V_{DD}$  and RBB.

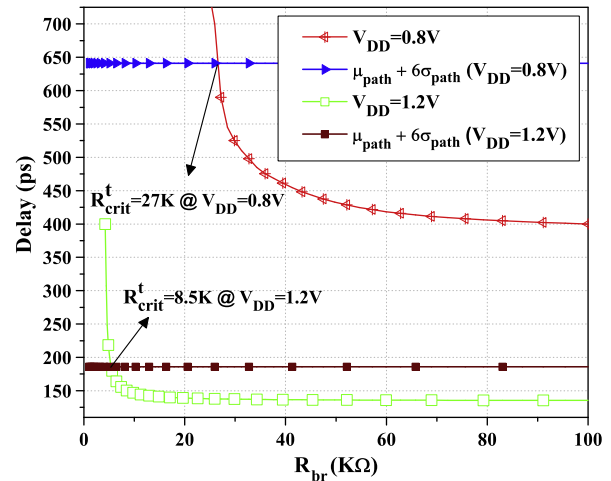


Fig. 8. Delay as a function of resistive bridge defect at nominal  $V_{DD}$  and Low  $V_{DD}$ .

the  $R_{br}$  at the nominal  $V_{DD}$  and at low  $V_{DD}$ . As expected, when  $R_{br}$  increases the circuit delay tends to the mean value of the delay distribution ( $\mu_{path}$ ). The intersection of the straight line at  $\mu_{path} + 6\sigma_{path}$  with the delay defective curve gives the  $R_{crit}^t$  value. For 65 nm technology at nominal  $V_{DD}$ ,  $R_{crit}^t = 8.5$  K $\Omega$  while for low  $V_{DD}$ ,

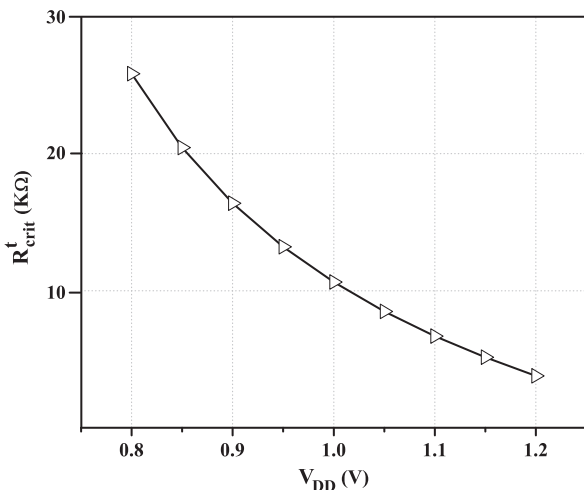


Fig. 6.  $R_{crit}^t$  as a function of  $V_{DD}$ .

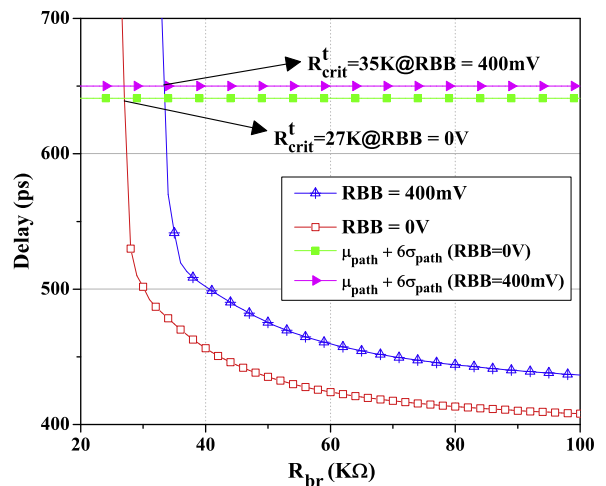


Fig. 9. Delay as a function of resistive bridge defect at low  $V_{DD}$  considering RBB.



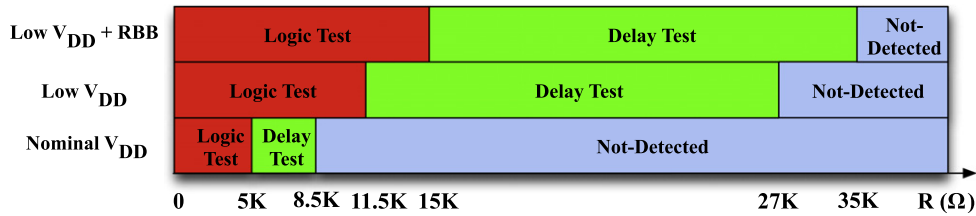


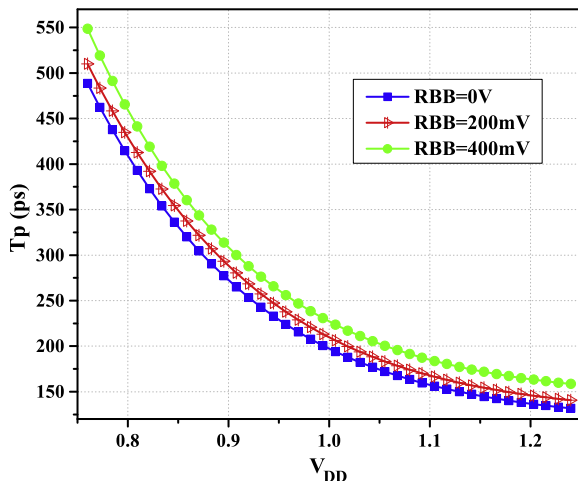
Fig. 10. Critical resistances for logic test and delay test under process variations for different test escenarios.

$R_{crit}^t = 27K\Omega$ , being more than three times the  $R_{crit}^t$  value at nominal  $V_{DD}$ .

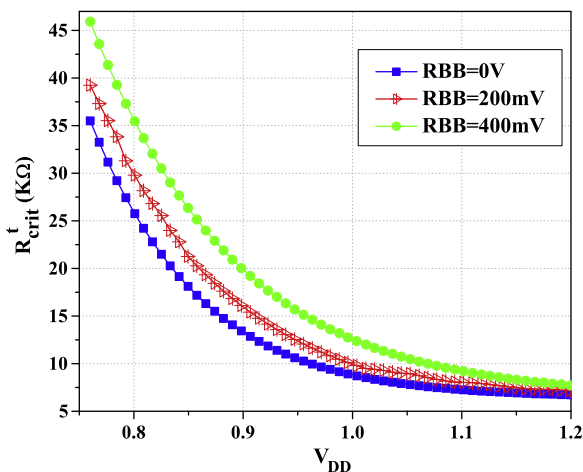
Fig. 9 shows the delay increase due to resistive bridge at Low  $V_{DD}$  for no body bias, NBB ( $RBB = 0V$ ), and for  $RBB = 400mV$ . For NBB,  $R_{crit}^t = 27K\Omega$ , while when  $RBB = 400mV$  is applied,  $R_{crit}^t = 35K\Omega$ . The  $R_{crit}^t$  improves by 30% when applying RBB at Low  $V_{DD}$ , being more than four times the  $R_{crit}^t$  value at nominal  $V_{DD}$  without RBB.

### 6. Comparison with logic test and test cost

Fig. 10 shows a comparison between logic and a delay based tests using Low  $V_{DD}$  and RBB. Process variations were considered



(a)  $T_p$  vs  $V_{DD}$



(b)  $R_{crit}^t$  vs  $V_{DD}$

Fig. 11.  $T_p$  and  $R_{crit}^t$  as a function of  $V_{DD}$  RBB = 0V, 200 mV, 400 mV.

for both logic test and a delay test. A 10-inverter chain was used for the analysis. At nominal  $V_{DD}$ , the critical resistance for a logic test is  $5K\Omega$  and slightly increases to  $8.5K\Omega$  for a delay test. At Low  $V_{DD}$ , the critical resistance increases to  $11.5K\Omega$  for the logic test. Note, that the range of resistances covered by delay test at nominal  $V_{DD}$  is covered by the logic test at Low  $V_{DD}$ . The critical resistance increases significantly until  $27K\Omega$  at Low  $V_{DD}$  using delay test. Furthermore, the critical resistance increases even more when both Low  $V_{DD}$  and RBB are used.

Fig. 11 shows the delay propagation ( $T_p$ ) of the 10-inverter chain and  $R_{crit}^t$  as a function of  $V_{DD}$ , for NBB and for  $RBB = 400mV$ . The test time is proportional to the  $T_p$  value. Test time increases when Low  $V_{DD}$  and RBB are used. The ratio of critical resistance improvement to the test time penalty is higher when RBB is used at a lower value of  $V_{DD}$  (e.g.  $V_{DD} = 0.8V$ ) than when RBB is used at a higher value of  $V_{DD}$  (See Fig. 11). This suggest that RBB is more efficient when is applied in conjunction with a low value of  $V_{DD}$ .

Regarding area penalty, this test scheme requires an on-chip power network to distribute body voltages. For a chip with an already implemented body bias infrastructure this would not be required. Given that body bias is not modified at speed, very little current is required in the power supply grid, and thus minimum metal width can be used to distribute bias voltages [25,26]. Therefore, area overhead is not critical.

The proposed test technique is applied lowering power supply voltage and manipulating body bias when the circuit under verification is in test mode. The power supply voltage can be reduced as low as possible from the nominal value until the circuit can work properly [27]. To set such minimum  $V_{DD}$  the impact of lowering power supply voltage on delay variance should be considered. Several techniques have been proposed to search for a valid min  $V_{DD}$  [28]. Body bias is usually applied when there is proper isolation between NMOS and PMOS transistors, and is successfully applied in twin/triple well CMOS process [25].

### 7. Conclusions

The impact of combining both  $V_{DD}$  reduction and reverse body bias (RBB) on resistive bridge fault detection through delay testing, considering the influence of process parameter variations, has been analyzed. A *Timing Critical Resistance* ( $R_{crit}^t$ ) is introduced as a metric to account for the impact of process variations on the efficiency of a delay based test. Results show that the smaller the supply voltage, the higher the resistive bridge defect detection capability. The increase of the defective circuit mean delay with respect to the defect-free value is more significant than the increase of the standard deviation when  $V_{DD}$  is lowered. Furthermore, RBB in conjunction with a low value of  $V_{DD}$  is an efficient way to enhance resistive bridge detection under a delay based test. The proposed test approach allows increasing the resistance range of bridge defects (high resistive bridges) which may escape logic testing and pose a reliability concern. This test method is compatible with standard logic and delay test techniques.

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