A very compact CMOS class AB current mirror for Low Voltage Applications

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Abstract

This paper presents a compact bidirectional current mirror suitable for low voltage applications. The idea is to use complementary transistors in subthreshold which are able to set a reduced bias current through the mirror. The circuit presents a class AB operation with a THD near to 1% at 1MHz. The bandwidth is above 10MHz as shown by simulations using Spectre with 0.5µm CMOS technology parameters.

1. Introduction

The current mirror is a basic analog building block which is widely used in OTA's, OP-AMP´s and other complex current mode circuits. Nowadays low-power requirements lead analog designers to consider class AB circuits due to their low quiescent current features and their capability to handle currents several times larger. Furthermore, voltage supply shrinking in modern fine line technology reduces considerably the voltage headroom for analog design; therefore, solutions capable to work with a low-voltage condition and class AB operation are mandatory. Many class AB current mirrors have been proposed. In [1], extra circuitry is included for achieving class AB operation but consequently, this extra complexity increases the minimum voltage requirement for the overall circuit. Other class AB approaches [2-4] improves the input/output impedance of the current mirror, however do not work for bidirectional currents and are not able to work for low-voltage applications. The low impedance node of the FVF (*Flipped Voltage Follower*) has been extensively used for many applications including current mirrors [5-6]; in [5] the use of a FVF and a simple current mirror achieves class AB operation and low-voltage. Although an interesting solution, it is desirable to reach even simpler solutions at least for some applications. In this work, a very compact bidirectional current mirror is presented, which is able to deal with currents several orders of magnitude larger than the bias current.

This paper is organized as follows: In the next section the proposed circuit is presented and explained. Section 3 present simulations and discussion and finally; in section 4 some conclusions are given.

2. Compact class AB current mirror

The definition for a low-voltage circuit is given in [7]. A given circuit works in low-voltage mode if its voltage supply V_{DD} is less than the sum of the complementary threshold voltages of NMOS and PMOS, i.e. $V_{DD}<|V_{THp}| + V_{THn}$.

Figure 1, depicts the class AB current mirror proposed in [1]. Here transistors M3 and M4 set the bias current I_{bias} in the input branch. Therefore, these transistors can fix a reduced bias current for reduced static power consumption. Nevertheless, the branch of transistors M1 and M2 defines the minimum voltage supply requirement for the circuit, i.e. $V_{DDmin}=2V_{DSsat}+V_{GSp}+V_{GSn}$. Where V_{DSsat} is the MOS overdrive drain-source voltage for saturation condition,

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these considered from current sources I_{bias} implemented by a single transistor. V_{GSp} is the MOS voltage gate-source which must fulfill $V_{GSp}>|V_{THp}|$ and $V_{GSn}> V_{THn}$.

For 0.5µm CMOS technology with V_{THn}=0.65V and $|V_{THp}|$=0.95V, this minimum supply must fulfill V_{DDmin} > 2V, so, the proposal is not suitable for low-voltage applications.

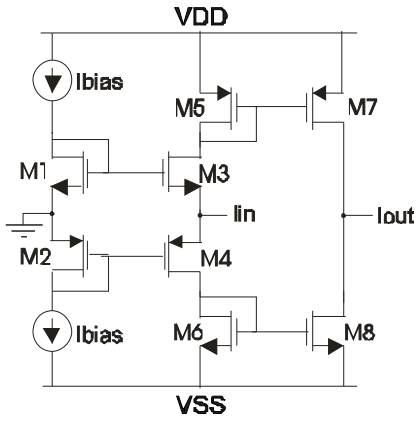

Figure 1.- Class AB current mirror

In Figure 2a) another class AB current mirror is presented [8], here the bias current at the input branch is defined by current sources I_{bias}. This input branch resembles that in Figure 1. Again the minimum supply required is V_{DDmin}= $2V_{DSsat}+V_{GSp}+V_{GSn}$ which is not suitable for low voltage.

The proposed circuit is presented in figure 2b). This circuit is a simplified version of the two previous circuits.

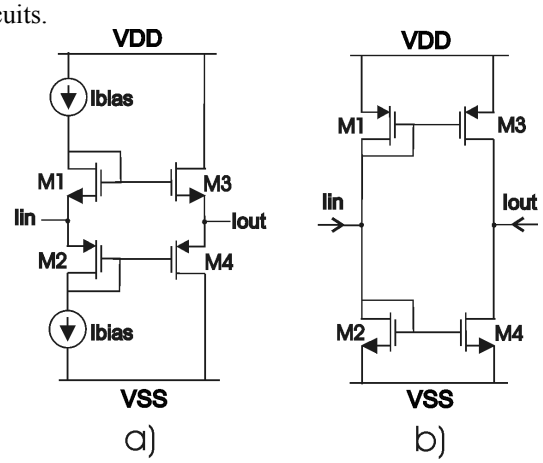

Figure 2.- a) Class AB current mirror, b) Proposed current mirror.

From Figure 1, the absence of transistors M3 and M4 lead to the circuit in Figure 2b). Since for low voltage operation $V_{DDmin}<|V_{THp}| + V_{THn}$, this condition leads M1 and M2 in Fig 2b) to work in subthreshold.

The MOS subthreshold conduction at drain has an exponential dependency on V_{GS}, for V_{DS}>200mV this is [9]:

$$I_D = I_0 \cdot \exp\frac{V_{GS}}{\zeta V_T} \qquad (1)$$

Where $V_T = kT/q$, and $\zeta > 1$ is a nonideality factor.

This special feature fixes a very small bias current on both branches, preserving the class AB operation. Thus, when a given current i_{in} is introduced into the circuit the input node goes high turning M1 PMOS "off" and turning M2 NMOS "on". Therefore, the input current is well copied by the M2-M4 mirror. In case i_{in} is extracted from the circuit, input node goes low, therefore, M2 NMOS is turned off and M1 turned on bringing i_{in}. In this case the input copy is achieved by the PMOS counterpart to the output.

3. Simulation Results

The circuit proposed in Figure 2b) was simulated using Spectre with BSIM3 ver 3.1 model parameters of ON Semi 0.5µm technology available through MOSIS. Transistors aspect ratio are W/L=24.6µm/1.5µm for all NMOS and W/L=73.8µm/1.5µm for PMOS transistors.

In Figure 3, the bias current of the circuit is plotted against different V_{DD} values. As can be noticed, bias current goes from several pA to µA.

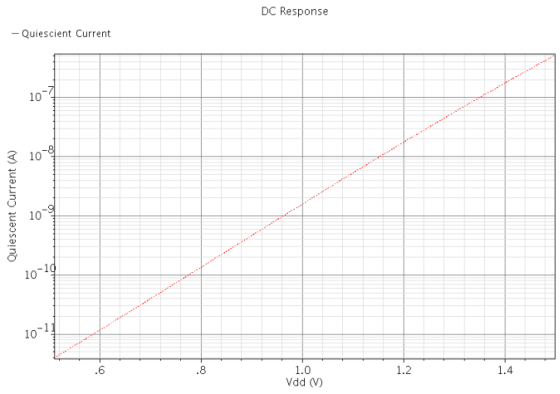

Figure 3.- DC simulations results, Bias current vs. V_{DD}

In Figure 4, a parametric DC sweep simulation of I_{in} vs I_{out} is shown, V_{DD} changes from 0.8V-1.5V. The simulation shows the linearity of the current mirror for

different V_{DD} values. For V_{DD} = 0.8V, it is important to notice that the circuit handles more than 100,000 times its bias current, showing a class AB behavior.

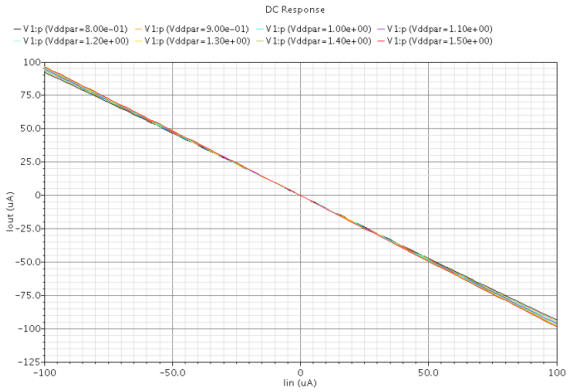

Figure 4.- Transfer function for different V_{DD} values.

Figure 5, shows the simulated AC response, the results show a cutoff frequency beyond 20MHz for C_L=0. Since the circuit only presents a high impedance node at the output it has an unconditionally stable behavior.

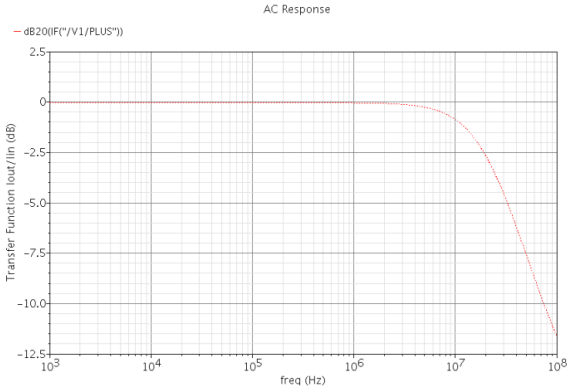

Figure 5.- AC simulation response.

The simulated output spectral response is shown in Figure 6, for 100µA_p@1MHz input signal. Distortion is introduced mainly by the third harmonic which is -49dB below the fundamental.

A Simulation of the input amplitude vs. THD is shown in Figure 7. As can be noticed maximum THD is 1.3% for 20µA_p, 1MHz input signal.

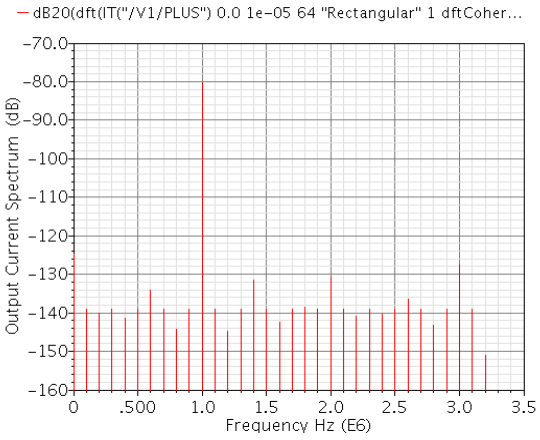

Figure 6.- Simulated output spectral response.

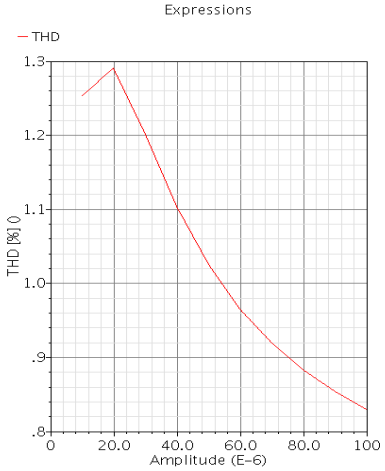

Figure 7.- Simulated input amplitude vs. THD.

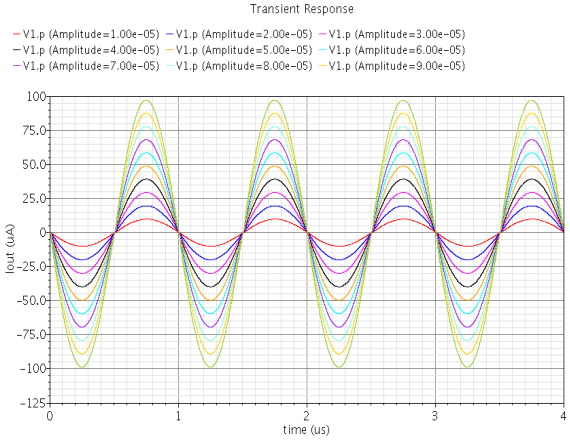

Figure 8.- Simulation of the current mirror transient response for several amplitudes

Finally, Figure 8, shows the current mirror transient response for several input amplitudes at 1MHz frequency.

4. Conclusions

In this work, a very compact low-voltage, class AB current mirror is presented. The circuit can drive currents at several orders of magnitude larger than its static current as shown through simulations. Since the circuit only presents a high impedance node, it has an unconditionally stable behavior and no compensating passive elements are required.

The simplicity of the circuit makes it feasible for many low-voltage applications.

5. References

[1] S. Kawahito, Y. Tadokoro, "CMOS Class-AB Current Mirrors for Precision Current-Mode Analog-Signal-Processing", IEEE Trans. On Circuits and Systems, part II, vol. 43, No. 12, pp. 843-845, 1996.

[2] Hassan Faraji Baghtash and Seyed Javad Azhari, "Very low input impedance low power current mirror", Analog Integrated Circuits and Signal Processing, vol. 66, no. 1, pp. 9-18, 2011.

[3] F. Esparza-Alfaro, A. J. Lopez-Martin, Jaime Ramirez-Angulo and R. G. Carvajal, "High-Performance Micropower Class AB Current Mirror" , Electronics Letters, vol. 48, no. 14, 2011.

[4] A. J. Lopez-Martin, J. Ramirez-Angulo, R. G. Carvajal and J. M. Algueta, "Compact Class AB CMOS Current Mirror" Electronics Letters, vol. 44, no. 23, 2008.

[5] A. Torralba, R. G. Carvajal, M. Jimenez, F. Muñoz and J. Ramírez-Angulo, "A true low voltage class AB current mirror" IEICE Electronics Express, vol. 2, no.4, pp. 103-107, 2005.

[6] J. Ramirez-Angulo, R. G. Carvajal and A. Torralba, "Low Supply Voltage High Performance CMOS Current Mirror with Low Input and Output Voltage Requirements" IEEE Trans. on circuits and Systems II, vol. 51, no. 3, pp.124-129, 2004.

[7] J. Ramirez-Angulo, R. Gonzalez-Carvajal, A. Torralba, F. Muñoz, J. Martinez J. Tombs, "Some techniques for low-voltage continuous-time analog circuit operation", Proc. of the IEEE 2nd Dallas CAS Workshop on Low Power/Low Voltage Mixed-Signal Circuits and Systems, pp. W90-130, 2001.

[8] R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, New York: John Wiley, 3rd Ed., 1993.

[9] B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw Hill, 2001.