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Short communication

MOHOS-type memory performance using HfO_2 nanoparticles as charge trapping layer and low temperature annealing

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ABSTRACT

In this work, HfO_2 nanoparticles (np-HfO_2) are embedded within a spin-on glass (SOG)-based oxide matrix and used as a charge trapping layer in metal–oxide–high-k–oxide–silicon (MOHOS)-type memory applications. This charge trapping layer is obtained by a simple sol–gel spin coating method after using different concentrations of np-HfO_2 and low temperature annealing (down to 425 °C) in order to obtain charge–retention characteristics with a lower thermal budget. The memory's charge trapping characteristics are quantized by measuring both the flat-band voltage shift of MOHOS capacitors (writing/erasing operations) and their programming retention times after charge injection while correlating all these data to np-HfO_2 concentration and annealing temperature. Since a large memory window has been obtained for our MOHOS memory, the relatively easy injection/annihilation (writing/erasing) of charge injected through the substrate opens the possibility to use this material as an effective charge trapping layer. It is shown that by using lower annealing temperatures for the charge trapping layer, higher densities of injected charge are obtained along with enhanced retention times. In conclusion, by using np-HfO_2 as charge trapping layer in memory devices, moderate programming and retention characteristics have been obtained by this simple and yet low-cost spin-coating method.

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1. Introduction

Over the last years, obtaining higher non-volatile memory (NVM) device performance is becoming quite difficult since we are now reaching the physical limits offered by scaled-down conventional materials and thus, new materials/architectures for memory applications are needed in order to meet the stringer specifications imposed on these devices [1,2]. Among the current memory technologies available (still dominated by the floating-gate flash technology), the silicon–oxide–nitride–oxide–silicon (SONOS)-memory, or floating-trap memory, is one attractive candidate to realize flash-memory vertical scaling [3,4]. In a floating gate device, the charge is stored at the polysilicon floating gate as free carriers having a continuous spatial distribution in the conduction band, while the SONOS memory stores charge in spatially isolated deep trap levels within the nitride oxide [5–7]. Also, in a SONOS-memory it is possible to both increase its programming speed and to lower its operating voltage by reducing the tunnel oxide thickness [8]. However, this seriously degrades the charge retention capability of the device so that the SOHOS (silicon–oxide–high-k–oxide–silicon) flash memory has emerged as a way to increase its charge retention time by replacing the silicon nitride with a higher dielectric constant material as charge trapping layer [9]. Because of the higher dielectric constant, the electric field across the tunneling oxide is enhanced thus enabling a greater injection of charge from the silicon into the trapping layer and also, enables the use of thicker oxide tunnel layers so that the levels of leakage current tunneling back to the substrate are decreased as well, the combined effect being that of better charge injection/retention characteristics. Besides the conduction mechanisms used for charge injection, quite important for effective programming of these devices [10], several high-k materials have been explored for SOHOS-type memories, they include Al_2O_3 [11–14], HfO_2 [15–17], HfAlO [18–20] and many other materials that are currently under research and which are important to enhance the performance of memory devices based on charge trapping phenomena.

In order to increase the charge-based writing/erasing capacity and data retention time of SOHOS-type memory devices using low thermal budgets (by promoting larger defect densities at the charge trapping layer after lower annealing temperatures and which are useful as charge-trapping centers), this work study the ability of np-HfO_2 (embedded within a SOG–oxide matrix) to act as charge trapping centers in a metal–oxide–high-k–oxide–silicon (MOHOS) capacitor structure. We quantize the general charge trapping

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capacity of the high-k layer in MOHOS devices by measuring both the shift in their flat band voltage (ΔVfb) after writing/erasing operations and their charge retention time while correlating all results to different concentrations of np-HfO_2 within the oxide matrix and annealing temperature. Since the np-HfO_2 based trapping layer shows itself a large memory window for charge trapping, we then exploit this characteristic in order to inject just enough charge at the memory device (under low-electric field conditions) so that a steady increase/decrease in ΔVfb is obtained during writing/erasing operations. We show that ΔVfb is dependent on both the np-HfO_2 concentration and the annealing temperature applied at this charge trapping layer. On the other hand, given that the writing/erasing speed operations are usually taken by measuring flat-band/threshold voltage (Vfb/Vth) shift vs. stressing time and since they are measured in terms of the applied gate voltage, having thinner oxide stacks (including all blocking/trapping/tunneling oxides) would then increase the current density being injected into the trapping layer so that lower operation voltages would be needed to proportionally shift Vfb/Vth in any particular direction. This effect could be mistakenly interpreted as a higher efficiency of the high-k layer to trap charge since lower operations voltages are needed. By integrating the injected gate current density J_g with time, we are able to quantize the effective density of charge being injected at the memory device, Q_{inj}:

$$Q_{inj} = \int_0^t J_g \, dt \quad [\mathrm{C/cm^2}] \tag{1}$$

where Q_{inj} is injected charge density, J_g is gate leakage current density and t is stressing time. The units for Q_{inj} are C/cm^2. This measurement can be applied to similar memory devices having oxide structures with different gate areas and blocking/trapping oxide thicknesses (different leakage current densities) so that the intrinsic capacity of the whole oxide stack for writing/erasing operations could be measured in a more realistic way, that is, dependent only on the injected charge density and independent of gate area and oxide stack thickness. Finally, after chemically oxidizing the silicon surface (in order to get an ultra-thin tunneling oxide), the charge trapping layer based on np-HfO_2 can be easily deposited atop the oxidized silicon surface by the sol–gel spin coating method, which is also used for deposition of the thicker blocking oxide. Therefore, the fabrication cost of the MOHOS-memory is dramatically reduced since film formation using sol–gel spin coating is a simple method in comparison with atomic layer deposition (ALD), physical vapor deposition (PVD), or chemical vapor deposition (CVD) and the sol–gel materials used for both the blocking and charge trapping layers are economic and readily available.

2. Experimental

2.1. Silicon cleaning and surface preparation

For all experiments, we used silicate-type SOG materials (from Filmtronics, Corp., 15A), N-type silicon wafers (100) with resistivity of 5–10 Ω cm, and np-HfO_2 having granular diameter around 100 nm (99.9% purity from American Elements). Standard RCA-cleaning procedures (to eliminate organic/metallic silicon surface contaminants) were applied to all wafers and then dipped in HF solutions so that HF-last surfaces were obtained. The oxide stack fabrication was realized sequentially thus obtaining (1) an ultra-thin tunneling chemical oxide SiO_x, (2) a high-k trapping oxide based on np-HfO_2 and (3) a thick blocking oxide based on SOG–SiO_2. The thin tunneling oxide SiO_x was obtained by immersion of the HF-last silicon wafers into H_2O_2 at 75 °C by 16 min so that a thin chemical oxide (with thickness of 2.4 nm, after ellipsometry) was developed at the silicon surface.

2.2. Preparation and deposition of np-HfO_2 by spinning

The np-HfO_2 charge trapping layer was obtained by preparing a np-HfO_2:H_2O:CH_3COOH:SOG solution in which the concentration ratios of np-HfO_2 to SOG were 5, 10, 15 and 30%. The solute concentration was measured with an analytical balance AG285 from Mettler-Toledo. These np-HfO_2 were then hydrolyzed in the SOG solutions and subjected to water bath (baine marie, 80 °C, 2 h) treatments in order to obtain homogeneous solution mixtures. It is important to notice that the final prepared solution is of colloidal nature (instead of suspension solution) thus confirming proper homogeneous distribution of all components within the solution and no visible sediments were observed. The final np-HfO_2:SOG solutions were directly applied on the wafers' surfaces and spinned at 7000 rpm by 20 s.

2.3. Annealing of charge trapping layer based on np-HfO_2

After np-HfO_2:SOG application, all films were initially baked at 200 °C (10 min in N_2 ambient) in order to evaporate most of the organic solvents. A second thermal treatment was also performed within a quartz furnace so that better film densification and solvent removal could be obtained. This was done at 800, 600 or 425 °C (30 min in N_2) so that charge trapping performance of this np-HfO_2 layer could be compared after using all these different annealing temperatures.

2.4. Deposition and annealing of SOG-based blocking oxide

The SiO_2 blocking oxide was also formed by direct deposition of a silicate SOG solution on the wafer surface and spinned at 7000 rpm by 20 s. This last film was also baked at 200 °C (10 min in N_2) and 1000 °C (30 min in N_2) so that all previous oxide films are covered with this thicker blocking oxide.

2.5. Metallization and dangling-bond passivation

For electrical *C–V* and *I–V* characterization, all oxide films were metalized with 1 μm of aluminum by evaporation and unless otherwise stated, a gate capacitor area of 13.34e-4 cm^2 was used for all MOHOS devices. Following metallization, a last thermal treatment (450 °C in forming gas ambient, 5% H_2 + 95% N_2) was applied to all samples in order to passivate Si dangling bonds with this H_2-based annealing. The final memory device is then composed of a metal/oxide/high-k/oxide/silicon or MOHOS structure.

2.6. Physical and electrical characterization methods

The thicknesses for all oxide films were measured with a Gaertner ellipsometer L117 and a Tencor alpha-step equipment. The average thickness for the blocking and trapping oxide layers is 130 and 120 nm, respectively. These thicknesses are result of averaging at least 10 different ellipsometry and perfilometry measurements after analyzing 10 different spots/steps during those readings. All results had variations within ±10% of the reported average values. Finally, *C–V* and *I–V* measurements were done by using a Keihtley Model 82-DOS Simultaneous *C–V* system and an HP 4156B Semiconductor Parameter Analyzer, respectively.

3. Results and discussion

3.1. Idealized energy band diagram of a MOHOS device

Fig. 1 shows a schematic of the fabricated sample and the idealized energy band diagram in (a) and (b), respectively. The energy conduction and valence band offsets of the HfO_2 material

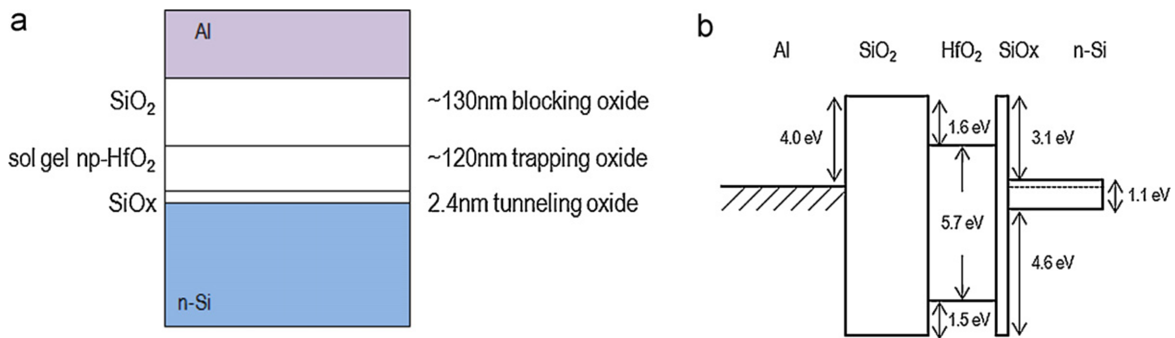

Fig. 1. (a) Schematic of the MOHOS memory containing the blocking/trapping/tunneling oxides. (b) Idealized energy band diagram for the memory structure shown in (a). The energy conduction and valence band-offsets are also shown for reference.

with respect to SiO_2 show a moderate energy barrier for electrons and holes, respectively [21,22], thus limiting the applied electric field to lower values (below Fowler–Nordheim conduction regime) in order to avoid leakage of carriers out of the HfO_2 trapping layer via a Fowler–Nordheim (F–N) or other high-field conduction mechanism. This is important since the injection of carriers (for both writing/erasing steps at the trapping layer) from the silicon substrate is usually done via a moderate gate electric field and hot carrier injection (HCI) mechanism both applied simultaneously to a SONOS/SOHOS structure. In some cases, channel hot electron injection (writing condition), and band-to-band tunneling induced hot hole injection (erase condition) are used [22–24]. Trapping of charge via HCI could decrease the general reliability of a metal-oxide-semiconductor field-effect transistor MOSFET device [25–27] and likewise, the reliability of a FET-based memory device after overstressing the charge trapping layer with this mechanism. In this work, we are able to inject electronic charge to the np-HfO_2 trapping layer after applying a small gate electric field only (without using any HCI mechanism) so that a memory device with enhanced reliability is expected. On the other hand, since our MOHOS-type memories make use of different np-HfO_2 concentrations for the charge trapping layer (5–30%), increasing the Hf content in the prepared solutions produces an increase in the magnitude of the absorption peak related to the Hf—O chemical bond and which is found at 752 cm^{-1} [28,29]. Also, the electrical performance of the SOG-based SiO_2 blocking layers has been previously obtained and good insulating properties were confirmed [30]. These oxides presented very low gate current densities so that, along with *C–V* measurements, it has been demonstrated that the blocking oxide layer presents good electrical quality, high enough to use it as blocking barrier for injection of charge carriers within the proposed memory structure.

3.2. Electrical I–V and C–V characterization

Fig. 2(a) shows the *I–V* data for the MOHOS memory structure in which the trapping oxide layer has an np-HfO_2 concentration of 15% and which has been subjected to different annealing temperatures. For the highest annealing temperatures, a very low conduction state is initially shown under accumulation up to $V_g \sim 4$ V, then a different conduction mechanism increases the current flow steeply until breakdown is reached at about 5 V and these same characteristics appear for the other memory samples in which a more restrained breakdown voltage is developed. Once $V_g = 10$ V, we measure the gate current back to 0 V and we confirm that the memory structure remains at the high conduction state, thus limiting the gate voltage range that can be applied to the trapping layer for charge injection to $V_g < 3$ V (since the minimum gate voltage needed for a hard-breakdown event to occur is around 3 V, we use V1 as stressing voltage in order to inject some charge before this breakdown occurs). Considering this large conductivity window between the LOW/HIGH conduction states (OFF/ON conditions) of about 7–9 orders of magnitude, we think there is plenty of room to inject large densities of electronic charge at the trapping oxide layer in order to properly modulate Vfb/Vth in memory devices without needing to overstress the stacked oxide using any HCI mechanism. Under this high conduction state, we also measure the gate current flow in inversion (from $V_g = 0$ to -10 V) so that we could obtain the complete picture of electronic conduction for this memory structure. After breakdown, the electronic conduction properties of the memory devices are quite similar to those of a metal/semiconductor rectifying contact, which makes sense if one considers the existence of a conductive filament path connecting both the silicon substrate to the aluminum metal gate. Fig. 2(b) shows the *C–V* data for the same memory structures before breakdown. Even though their Vfb is slightly shifted toward negative values (indicative of a large density of positive charge within the oxide stack), there is a noticeable difference in the accumulation capacitance (Cox) for the same np-HfO_2 concentration after different annealing temperatures applied to the charge trapping layer. For the highest annealing temperatures, we notice a reduced Cox in the MOHOS capacitors as compared to the lowest thermal treatments. Generally, higher annealing temperatures produce a more densified thin film which in turn, increases Cox since we would be dealing now with thinner oxides. The later is possible because of temperature-driven H_2O outgassing out of the SOG oxides and also reduction in its organic components [30–32]. This is not the case for our samples and we think this is related to a temperature-driven migration/diffusion of np-HfO_2 embedded within the SOG-based oxide matrix. Following thermodynamic principles and as the annealing temperature decreases, less efficient metal nanoparticle's migration/diffusion within an oxide matrix occurs [33,34]. By using low temperatures, we think that migration/diffusion of np-HfO_2 out of the MOHOS active gate area could be reduced thus retaining a higher dielectric constant (and increasing Cox) as expected. This is a subject which requires in-deep further study given the importance of embedding metal nanoparticles within oxide matrices and which are useful for several electronic applications. On the other hand, as the annealing temperature is reduced, more physical and/or electronic defects are thought to develop at the bulk of the charge trapping layer as well at its interfaces. This is noticed in our *C–V* curves annealed at 425 °C by a "kink" shown at inversion and which is commonly related to an increase in the interface-states density Dit for these devices [35]. Also, a lower slope from accumulation to depletion region for the samples annealed at higher temperatures is also shown. This last feature could hinder proper Vfb calculation after *C–V* measurement but we have tried to minimize the error by obtaining Vfb from at least 10 different devices having similar *C–V* characteristics and even to obtain Vfb after differentiating the initial C^{-2} vs. V_g curve

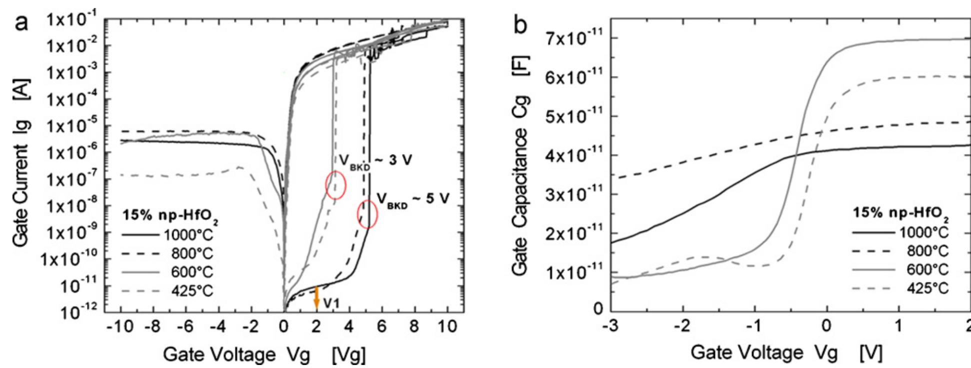

Fig. 2. (a) *I–V* characteristics for a MOHOS memory whose charge trapping layer is based on 15% np-HfO_2 concentration and different N_2 annealing temperatures. Since breakdown occurs at $V_g \sim 3, 5$ V, electron injection into the trapping layer is done at V1 = 2 V. (b) *C–V* characteristics for the same MOHOS memory structures before breakdown. For the highest annealing temperatures, we notice a reduced Cox in the MOHOS capacitors as compared to the lowest thermal treatments.

and finding Vfb at the maximum slope of the left flank [36]. Therefore, each Vfb data point presented in the subsequent figures is the average result of electrically measuring 10 different devices and using at least two different methods in order to extract Vfb.

3.3. Programming performance based on writing/erasing times

Fig. 3(a–b) show the Vfb shift found in MOHOS devices after injecting substrate electrons and substrate holes (writing/erasing condition) with time. First, we notice larger Vfb shift for devices having greater np-HfO_2 concentration. Because of a higher dielectric constant, the electric field across the tunneling oxide is enhanced thus enabling greater injection of charge from the silicon into the trapping layer. Also, we can see that the magnitude of positive/negative Vfb shift is dependent on the programming time for all conditions. It is thought that Vfb shifts because of electron/hole trapping mechanisms at the np-HfO_2 trapping layer. By looking at the idealized energy band diagram of Fig. 1(b), we notice that the conduction/valence band offsets of HfO_2 to silicon substrate are 1.5 and 3.1 eV, respectively. During writing, electrons accumulate at the substrate's surface and they gain enough energy from the applied gate voltage V_g enabling them to cross the tunneling oxide's energy barrier with energies well below 3.1 eV (the tunneling oxide is thin enough so that electrons can tunnel directly) and be trapped at the np-HfO_2 trapping layer, thus shifting Vfb to positive values. During erasing, a negative gate voltage inverts the silicon surface thus increasing the hole density and because of the electric field, these holes are trapped at the np-HfO_2 layer (where they could annihilate some already trapped electrons), thus shifting Vfb to negative values. The former process would occur after the holes are able to tunnel through the thin tunneling oxide and also have enough energy, well below 4.6 eV (valence band offset of SiO_x to silicon substrate), to be trapped at the np-HfO_2 trapping layer. In Fig. 3(b), we notice that for the np-HfO_2 with 10% concentration, the erasing condition does not recover the Vfb shift completely, and this effect can be due to the existence of deep trap levels [5–7] within the np-HfO_2 trapping layer thus making harder to annihilate the initially trapped electrons. Figs. 4(a and b) and 5(a and b) show that by both increasing the np-HfO_2 concentration and by reducing the annealing temperature to 600 °C and 425 °C for the charge trapping layer, greater charge injection densities are able to produce larger Vfb shifts for the writing/erasing conditions. Compared to an 800 °C annealing which shift Vfb to a maximum of 100 mV after the same writing time, lower thermal treatments are able to shift Vfb up to 500 mV for a 30% np-HfO_2 concentration and more than 200 mV for the lowest concentrations. On the other hand, the erasing condition for the charge trapping layer annealed at lower temperatures shows that the initially shifted Vfb is not recovered completely during erasing and gets even worse for the samples annealed at 425 °C (specially for the 30% np-HfO_2 concentration in which the Vfb remains almost constant at around 350 mV). We think that lower annealing temperatures for the charge trapping layer are prone to produce a higher density of physical/electronic defects at the high-k layer which in turn, create deep-trap levels for injected carriers that make more difficult to annihilate or excite the initially trapped electrons to the conduction band. The former makes sense if we notice that for the writing condition, lower annealing temperatures for the charge trapping layer increases Vfb shift considerably even if the same np-HfO_2 concentrations are used. Finally, even though similar performance could be obtained after programming memory devices processed at lower temperatures (like those found in Fig. 5(a) for instance), these low-temperature annealing conditions for the charge trapping layer are quite important in order to obtain different memory performance when analyzing other memory parameters like erasing conditions and/or data retention times. Therefore, at lower annealing temperatures for the charge trapping layer, the performance of the whole memory structure is quite dependent on composition.

3.4. Programming performance based on injected charge density Q_{inj}

Up to now, we have obtained the memory performance of MOHOS structures by applying a constant gate voltage and measuring their Vfb shift with respect to their writing/erasing times. However, since having thinner memory oxide stacks (scaled devices) would increase the charge density being injected to the trapping layer, shift of Vfb/Vth to any particular direction could be done using lower operating voltages and/or reduced writing/erasing speeds and this could be mistakenly interpreted as a higher efficiency of the high-k layer to trap charge. By integrating the injected gate current density J_g with time, see Eq. (1), we are able to quantize the effective density of charge being injected at the memory device, Q_{inj}, and its influence on Vfb shift. By plotting the Vfb shift data of Figs. 3–5 using Q_{inj} instead of writing/erasing times, we are able to measure the intrinsic capacity of the whole oxide stack for writing/erasing operations being only dependent with the injected charge density and independent of gate area and oxide stack thickness. This can be useful for comparison of scaled memory devices based on trapping of injected charge. Figs. 6–8 show the ability of our MOHOS devices to shift Vfb during writing/erasing conditions after charge injection using the same stressing voltage V1. Fig. 6(a and b) show that the memory structures having the largest np-HfO_2 concentration shift Vfb to larger values because they are able to handle and trap larger densities of injected charge, in this case, up to 1×10^{-6} C/cm^2. Trapping layers with lower

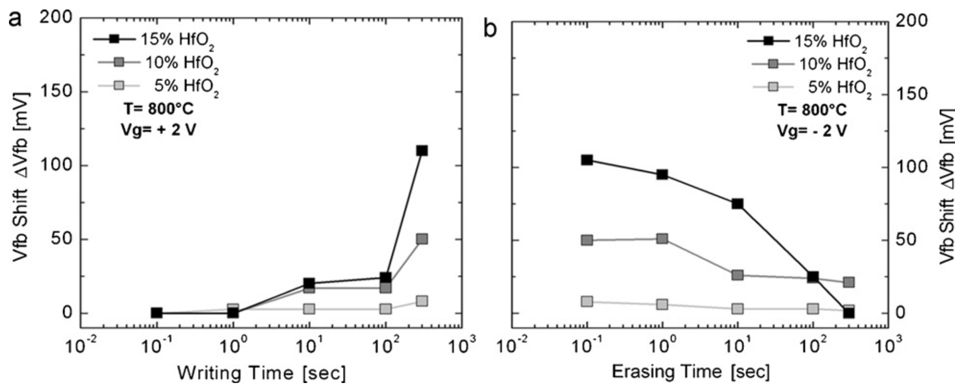

Fig. 3. (a) Vfb shift vs. writing time (electron injection) for a MOHOS memory with different concentrations of np-HfO_2 and annealed at 800 °C. Vfb shift increases with writing time and with np-HfO_2 concentration so that a maximum Vfb shift of 100 mV is obtained. (b) Vfb shift vs. erasing time (hole injection and/or electron annihilation) for the same MOHOS memory. A complete Vfb recovery is observed for the memory having greater np-HfO_2 concentration.

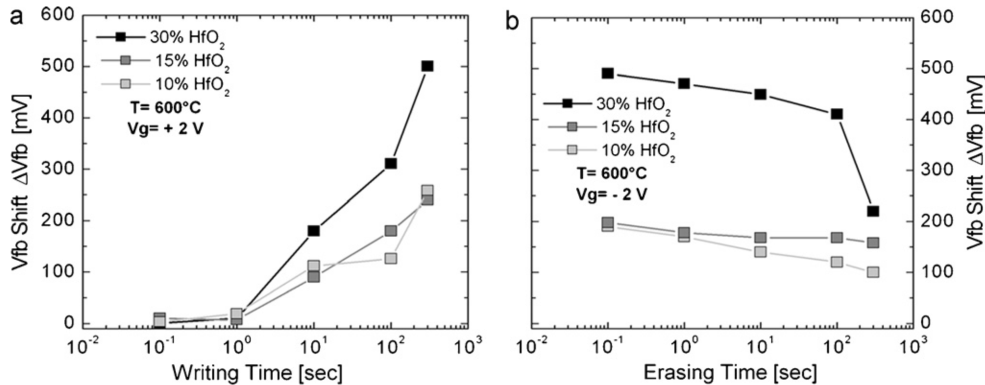

Fig. 4. (a) Vfb shift vs. writing time for a MOHOS memory with different concentrations of np-HfO_2 and annealed at 600 °C. Vfb shift increases with writing time and with np-HfO_2 concentration so that a maximum Vfb shift of 500 mV is obtained. (b) Vfb shift vs. erasing time for the same MOHOS memory. Incomplete recovery of Vfb shift is observed and this is related to deep-trap levels that might be generated at the charge trapping layer after lower annealing temperatures.

np-HfO_2 concentrations are unable to inject large Q_{inj} values, thus less charge is trapped producing smaller Vfb shift. On erasing, we also notice that a trapping layer having a larger np-HfO_2 concentration is able to recover Vfb more efficiently after using the same hole injection density. In other words, there is a steeper slope of Vfb recovery for the device having a 15% concentration of np-HfO_2 as compared to the others and a very small $Q_{inj} \sim 1 \times 10^{-6}$ C/cm^2 is enough to recover all or most of the initially shifted Vfb. Figs. 7(a and b) and 8(a and b) show that by both increasing the np-HfO_2 concentration and by reducing the annealing temperature to 600 °C and 425 °C for the charge trapping layer, greater charge injection densities are able to produce larger Vfb shifts for the writing/erasing conditions. On writing and for a 600 °C annealing temperature, it is clear that a higher np-HfO_2 concentration produces larger Vfb shifts because an increased dielectric constant is able to inject more charge for the same electric field. If we consider the same $Q_{inj} = 1 \times 10^{-6}$ C/cm^2 density, Vfb is shifted by about 100, 200 and 300 mV for np-HfO_2 concentrations of 10, 15 and 30% respectively, thus giving a sense of electrical correlation to the physical characteristics of the charge trapping layer. On

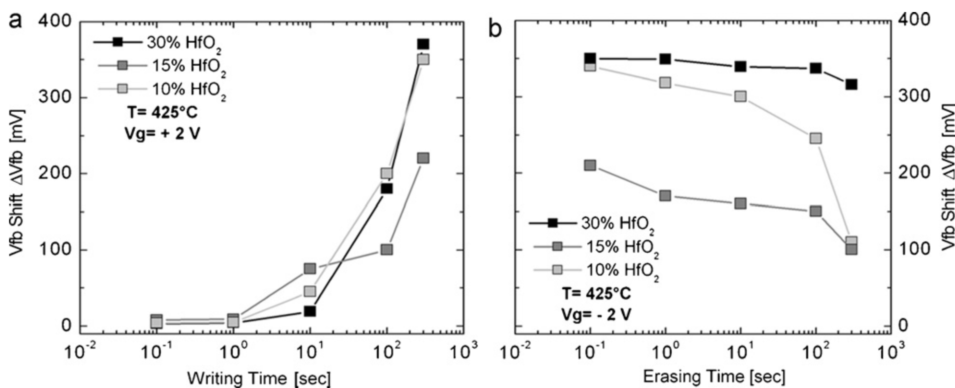

Fig. 5. (a) Vfb shift vs. writing time for a MOHOS memory with different concentrations of np-HfO_2 and annealed at 425 °C. Vfb shift still increases with writing time even though there is no clear correlation of this parameter to np-HfO_2 concentration. A maximum Vfb shift of ~400 mV is obtained. (b) Vfb shift vs. erasing time for the same MOHOS memory. Incomplete recovery of Vfb shift is again observed and this worsens for np-HfO_2 with 30% concentration since Vfb remains almost constant at ~300 mV during hole injection.

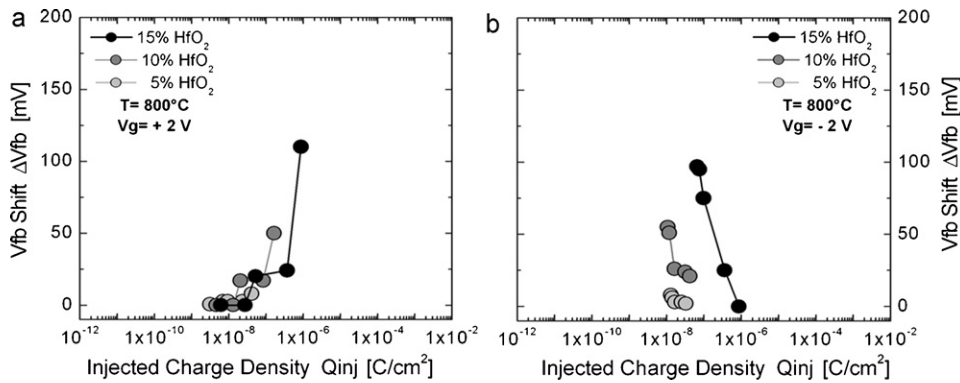

Fig. 6. (a) Vfb shift vs. injected charge density Q_{inj} (writing) for the MOHOS memory having different concentrations of np-HfO_2 and annealed at 800 °C. The memory structure having the largest np-HfO_2 concentration is able to trap more injected charge and thus, shift Vfb to larger values. (b) Vfb shift vs. injected charge density Q_{inj} (erasing) for the same MOHOS memory. The memory structure having the largest np-HfO_2 concentration is able to fully recover Vfb by using larger Q_{inj}. In both cases, a small charge density of $\sim 10^{-6}$ C/cm^2 is enough to completely shift and recover Vfb.

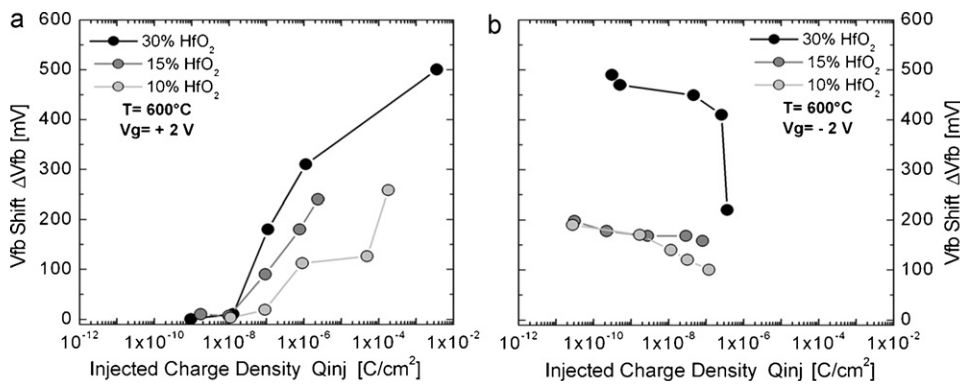

Fig. 7. (a) Vfb shift vs. injected charge density Q_{inj} for the MOHOS memory having different concentrations of np-HfO_2 and annealed at 600 °C. The memory structure having the largest np-HfO_2 concentration is able to trap more injected charge and thus, shift Vfb to even larger values. (b) Vfb shift vs. injected charge density Q_{inj} for the same MOHOS memory. For all np-HfO_2 concentrations, Vfb are not fully recovered since a small $Q_{inj} < 1 \times 10^{-6}$ C/cm^2 is used in all conditions.

erasing, even though Vfb is not fully recovered to its original state, we still observe a faster Vfb recovery for the highest np-HfO_2 concentration after $Q_{inj} > 1 \times 10^{-7}$ C/cm^2. This is important since efficient recovery of Vfb shift is not quite dependent on erasing time but on injected charge density Q_{inj} which simultaneously correlates both erasing time and gate current density J_g through Eq. (1). By reducing annealing temperature to 425 °C, the writing condition no longer produces the largest Vfb shift for the greatest np-HfO_2 concentration (considering the same Q_{inj} density) and also, the shift in Vfb is hardly recovered even after using higher densities of Q_{inj} on erasing. The former is related to a combination of physical and electronic defects' generation under lower annealing temperatures for the charge trapping layer.

3.5. Data retention time characteristics

Finally, the retention time characteristics for MOHOS memories based on np-HfO_2 are shown in Figs. 9–11. The normalized

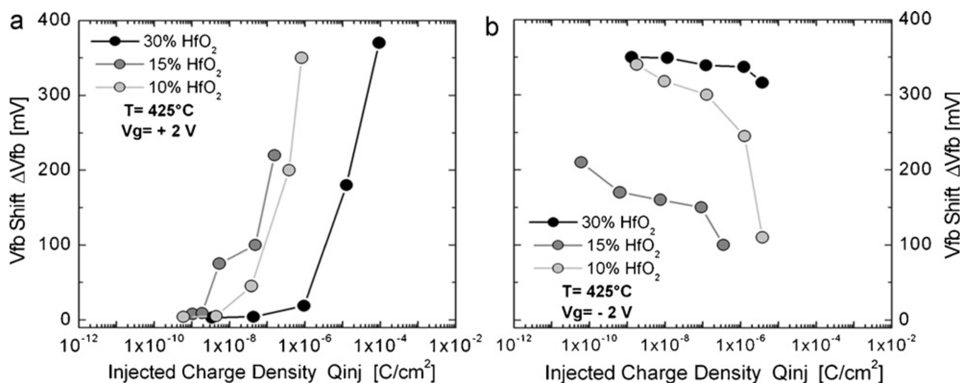

Fig. 8. (a) Vfb shift vs. injected charge density Q_{inj} for the MOHOS memory having different concentrations of np-HfO_2 and annealed at 425 °C. Interestingly, at the same Q_{inj} level this condition produces a larger Vfb shift for the lowest np-HfO_2 concentrations and the final Vfb reached is lower as compared to other annealing temperatures. (b) Vfb shift vs. injected charge density Q_{inj} for the same MOHOS memory. Vfb is only partially recovered for the lowest nanoparticles' concentrations but is hardly recovered for the 30% concentration in which Vfb remains almost constant at ~300 mV.

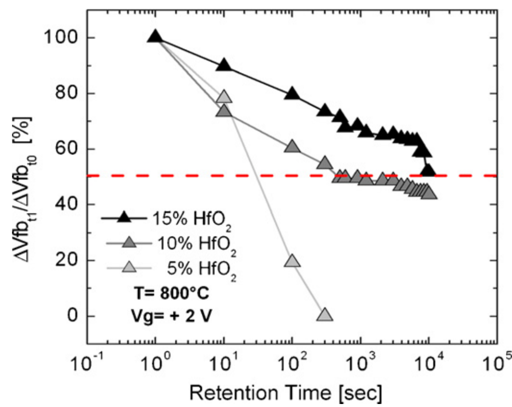

Fig. 9. Retention time characteristics for the MOHOS memory having different concentrations of np-HfO_2 and annealed at 800 °C. A continuous charge loss with time is observed for all conditions with complete loss of data for the lowest np-HfO_2 concentration of 5%.

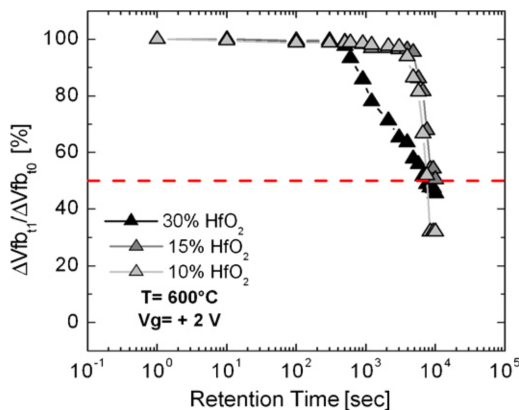

Fig. 10. Retention time characteristics for the MOHOS memory having different concentrations of np-HfO_2 and annealed at 600 °C. Initially, the trapped charge is almost fully retained with time (no charge loss) but then a sudden charge loss behavior is observed so that about 50% of charge is lost during the last seconds of measurement.

Vfb shift is defined as the ratio of Vfb shift at the time of interest and at the beginning (t_1 and t_0, respectively). The curves are obtained after writing in which a V_g = +2 V produced the maximum Vfb shift already shown in Figs. 3(a), 4(a) and 5(a) at room temperature. The charge loss with time is observed for all np-HfO_2

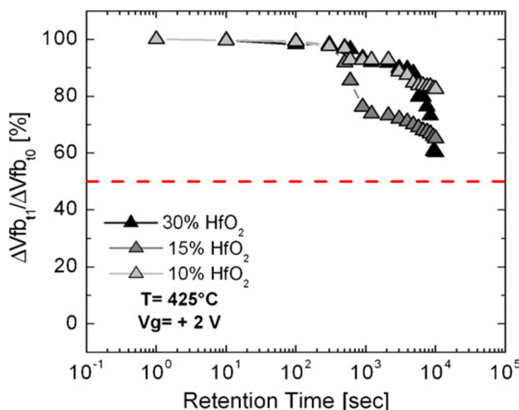

Fig. 11. Retention time characteristics for the MOHOS memory having different concentrations of np-HfO_2 and annealed at 425 °C. Here too the trapped charge is almost fully retained with time (no charge loss) but then a monotonous charge loss behavior is observed so that about 20–40% of charge is lost at the final stage of measurement.

concentrations and annealing temperatures of this charge trapping layer. For an 800 °C annealing, the initially trapped charge is lost faster as compared to lower annealing temperatures. Here, a 5% concentration of np-HfO_2 in the charge trapping layer losses its charge after about 300 s whereas higher nanoparticles' concentrations are able to retain the stored charge down to half of its original value after 1×10^4 s. For 600 and 425 °C annealing, the charge is almost fully retained after the first 1×10^3 s for all concentrations; upon after, the trapped charge is rapidly lost and reaches half of its original Vfb value after 1×10^4 s. As for the mechanisms related to charge loss characteristics, they are a subject for in-depth additional studies since we are dealing with a memory structure in which a process-induced damage (lower annealing temperatures) can be directly correlated to faster degradation of retention times, these results will be published elsewhere. With the exception of 5% np-HfO_2 concentration annealed at 800 °C, all samples have moderate retention characteristics where only half of the charge has been lost after 1×10^4 s, thus demonstrating the potential of using HfO_2 nanoparticles for memory applications based on charge trapping mechanisms. Finally, we think that is of the outmost importance to correlate the electrical performance of the memory devices presented in this work to any physical changes occurring at the charge trapping layer based on np-HfO_2 after annealing. For this purpose, analytical characterization based on TEM, SIMS, XRD and other analytical techniques are important in order to solve many interesting questions being raised for this important material. In particular, determining whether is there any temperature-driven diffusion and/or migration mechanism for these np-HfO_2 (to any of its interfaces) is important for the purpose of establishing a physically based mechanism able to explain the electrical phenomena here reported.

4. Conclusions

Using np-HfO_2 as a charge trapping layer in MOHOS memory devices has been demonstrated. Following a N_2-based annealing, it is possible to modulate the electrical *I–V*/*C–V* characteristics of these MOHOS devices by shifting their breakdown voltage Vbkd, flat-band voltage Vfb and their accumulation capacitance Cox. From the perspective of memory performance, it is shown that larger charge densities can be injected to the trapping layer of memory structures having greater concentration of np-HfO_2 and they produce larger Vfb shifts for both the writing and erasing conditions. Also, even with a small substrate injection of electrons ($Q_{inj} = 1 \times 10^{-6}$ C/cm^2) it is possible to modulate the Vfb of these devices from 100 mV up to 400 mV during writing operations. This is important since by using scaled down devices having thinner gate oxide stacks, higher densities of injected charge could easily modulate Vfb with shorter writing/erasing operation times. After annealing the charge trapping layer at lower temperatures, the memory performance is increased after comparing writing/erasing and data retention time characteristics and this is thought to be related to an increase in the density of physical/electronic defects present at this active layer. On the other hand, charge injection is done via substrate injection of carriers so that the Hot-Carrier Injection mechanism was avoided during programming the memory structures (which is expected to enhance the overall reliability of a memory device). Also, we use injection charge density Q_{inj} instead of writing/erasing times in order to measure the intrinsic capacity of the whole oxide stack for memory operations being only dependent with the injected charge density and independent of gate area and oxide stack thickness. We believe this procedure can be useful to compare the basic performance of scaled memory devices (having smaller gate areas and thinner oxide stacks) during charge injection operations.

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