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Performance improvement of low-temperature a-SiGe:H thin-film transistors

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ABSTRACT

This paper presents the study of an interface preparation procedure in the source/drain regions of the active layer, prior to deposit the n+ a-Ge:H contact layer in the fabrication process of low-temperature a-SiGe:H thin-film transistors. The devices were fabricated on corning 1737 substrates at 200 °C. The improvement in metal–semiconductor interface by the interface preparation procedure was demonstrated. This interface improvement translates in higher mobility and better values of off-current, on/off-current ratio, subthreshold slope and threshold voltage.

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1. Introduction

Electronic devices fabricated on flexible and large-area substrates are the subjects of growing attention within both the research and the industrial community. Thin-film transistors (TFTs) based on a-Si:H technology have attracted interest due to potential low-temperature process to be integrated in flexible electronics technology.

Since the reduction in process temperature below 200 °C leads to change the deposition mechanisms, as result, the concentration of defects (dangling Si bonds) increases, the mass density decreases, and the doping efficiency drops [1]. Therefore, a-Si:H TFTs fabricated at low-temperatures ($\leqslant$200 °C) suffers of high-contact resistance and have poor stability, higher values of threshold voltage, off-current and subthreshold slope than those deposited at higher temperatures [2,3]. In order to improve the TFT performance, have been reported procedures which reduce the contact resistance and improve the main device interfaces [4–8]. In the inverted staggered structure, as the thickness of the active layer is reduced, the series resistance associated to this thickness decreases while the contact and channel resistances remain unchanged [9]. However, it is well known, that the density of defects increases as the amorphous film becomes thinner. For this reason, an overetching in the source/drain regions of the active layer prior to deposit the n+ contact layer can reduce the series resistance of the TFT, without reducing the thickness of the active layer. Therefore, because the n+ contact layer and the induced-channel get close, some parameters can be improved such as mobility and on/off-current ratio.

In this paper, an interface preparation procedure in the source/drain regions prior to deposit the n+ contact layer is studied. In order to achieve a high quality insulator–semiconductor interface, high quality SiO_2 films by Spin-On Glass (SOG) diluted with deionized water (DI) and cured at 200 °C was used as gate insulator [10].

2. Experiment

The low-temperature a-SiGe:H TFTs used the inverted staggered structure and were fabricated in corning 1737 substrates. The process flow and cross section of the a-SiGe:H TFTs are shown in Fig. 1. The simplified process flow is as follows: first, to planarize the gate electrode, 100 nm-thick of SOG diluted with DI and cured at 200 °C was used [10]. Then, photoresist was applied and patterned to leave opening for the gate. Later, the SOG was etched by Reactive Ion Etching (RIE) leaving the place of the gate. The SOG was etched with CF_4 plasma at a pressure of 160 mTorr and RF power of 50 Watts. Finally, as shows Fig. 1a, the planarized gate is formed by lift-off process of 100 nm-thick of e-gun evaporated Al. Afterwards, 80 nm-thick of SOG diluted with DI and cured at 200 °C was used as the gate insulator. Then, 100 nm-thick of undoped a-SiGe:H and 100 nm-thick of SiNx films were deposited using low frequency (110 kHz) plasma enhanced chemical vapor deposition (PECVD) at 200 °C, pressure of 0.6 Torr and an RF power of 300 W (Fig. 1b). Later, the SiNx film was patterned as passivation layer above the a-SiGe:H active layer using RIE. In this step, an

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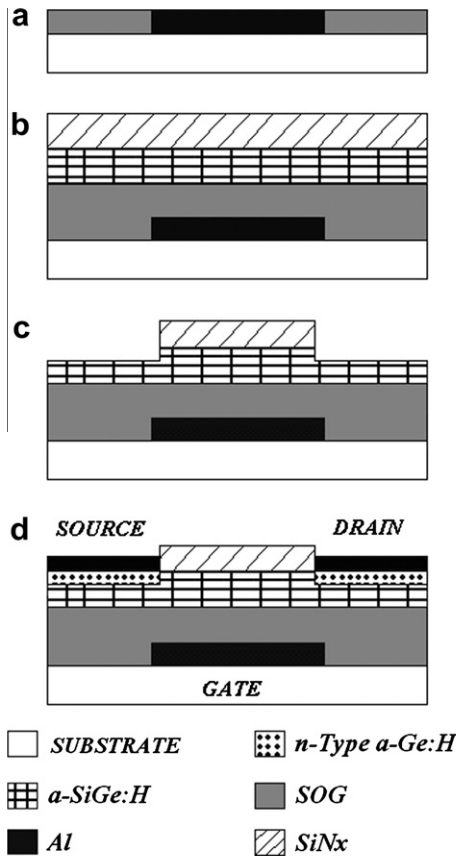

Fig. 1. Process flow and cross section of the inverted staggered a-SiGe:H TFTs (not to scale). (a) planarization of the gate electrode, (b) deposit of gate insulator, active layer and passivation layer, (c) passivation layer patterned and overetching process and (d) deposit of n+ contact layer and formation of the source/drain contacts.

overetching in the a-SiGe:H film was done by RIE as shown in the Fig. 1c. The time of the overetching was of 30 s (20% of the a-SiGe:H film thickness). After that, hydrogen plasma was done at 200 °C, with H_2 flow of 3500 sccm, pressure of 0.6 Torr and RF power of 300 W for 5 min. To compare the effects of this hydrogen plasma on the electrical characteristics of the TFT, other TFTs without hydrogen plasma were fabricated. Next, 40-nm thick of n-type a-Ge:H film was deposited using low frequency PECVD at 200 °C with a pressure of 0.6 Torr and RF power of 300 W. Then, 300-nm thick of Aluminum was e-gun evaporated and patterned to form the source and drain electrodes. After, the n-type a-Ge:H film was etched using RIE (Fig. 1d). Finally, a thermal treatment at 180 °C for 40 min was done.

In order to compare the effects of the overetching process, a-SiGe:H TFTs with higher overetching were fabricated. The time of the overetching was of 2 min (80% of the a-SiGe:H film thickness). Also, hydrogen plasma and thermal treatment were done.

3. Results and discussion

The electrical characterization of the devices was conducted using the *HP 4156B Semiconductor Parameter Analyzer*. All the measurements were done under dark conditions. The transfer characteristics of a-SiGe:H TFTs with and without hydrogen plasma application are shown in Fig. 2. Better electrical characteristics, such as on-current, off-current and on/off-current ratio, are observed for a-SiGe:H TFTs with applied hydrogen plasma. The poor electrical characteristics of a-SiGe:H TFTs without hydrogen plasma application are due to plasma-induced damage occasioned by the overetching process [11,12].

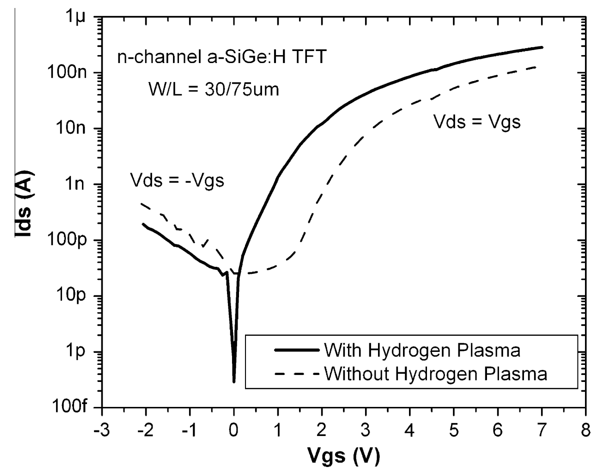

Fig. 2. Comparison of the transfer characteristics of a-SiGe:H TFTs with and without hydrogen plasma application.

For the a-SiGe:H TFTs with applied hydrogen plasma, it can be observed an on/off-current ratio approximately of 10^6 and an off-current approximately of 300 fA at 0 V_{gs} which are in the range of those in high-temperature a-Si:H TFTs. The subthreshold slopes values for both a-SiGe:H TFTs with and without hydrogen plasma application were 0.56 and 0.61 V/DEC, respectively. Typically, in a-Si:H TFTs, the subthreshold slope is largely decided by the quality of gate insulator/active layer interface. In the a-SiGe:H TFT, the subthreshold slope is dependent on the trap density in the active layer a-SiGe:H (N_T) and at the SOG/a-SiGe:H interface (D_{it}). The subthreshold slope can be approximated as the following equation [13]:

$$S = qK_B T(N_T tS + D_{it})C_{OX}\log(e) \quad (1)$$

where q is the electron charge, K_B is the Boltzmann constant, T is the absolute temperature, tS is the a-SiGe:H thickness and C_{OX} is the SOG insulator capacitance per unit area. If N_T or D_{it} is separately set to zero, the respective maximum values of N_T and D_{it} are obtained. The N_T and D_{it} values for a-SiGe:H TFTs were of 2.65×10^{17} cm^{-3} eV^{-1} and 2.65×10^{12} cm^{-2} eV^{-1} for TFTs with applied hydrogen plasma, respectively, and for TFTs without hydrogen plasma application the values were of 2.88×10^{17} cm^{-3} eV^{-1} and 2.88×10^{12} cm^{-2} eV^{-1}, respectively. Because the error estimates of the subthreshold slope are ±0.03 V/DEC for both a-SiGe:H TFTs, the differences in subthreshold slope, N_T and D_{it} values are considered as a statistical fluctuation. Since both of the a-SiGe:H TFTs have identical insulator–semiconductor interface and the overetching process only affects the source/drain regions, we do not expect any difference in the quality of the insulator–semiconductor interface of the devices.

Fig. 3 shows the relation between square root of I_{ds} and V_{gs} of the TFT at saturation mode (V_{ds} = V_{gs}). In this relation the threshold voltage and field-effect mobility can be extracted from the intercept with V_{gs} axis, using Eq. (2) of the saturation region.

$$I_{ds} = \mu_{FE} \cdot C_{OX}(W/2L)(V_{gs} - V_T)^2 \quad (2)$$

where μ_{FE} is the field-effect mobility, C_{OX} is the capacitance per unit area of the gate insulator, W and L are the channel width and the length, respectively, and V_T is the threshold voltage. The measured threshold voltage and field-effect mobility for a-SiGe:H TFTs were of 0.7 V and 0.85 cm^2/Vs for TFTs with applied hydrogen plasma, respectively, while 1.86 V and 0.52 cm^2/Vs were for TFTs without hydrogen plasma application, respectively.

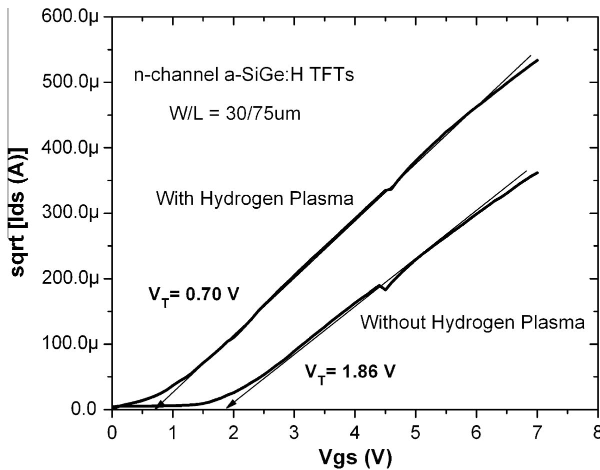

Fig. 3. Square root of I_{ds} vs V_{gs} of a-SiGe:H TFTs with and without hydrogen plasma application at saturation mode ($V_{ds} = V_{gs}$).

It is well known that hydrogen saturates dangling bonds in the amorphous film [14]. Thus, since the mobility and on-current can be affected by the quality of the metal–semiconductor interface, the higher values of mobility and on-current mean that the applied hydrogen plasma improves the metal–semiconductor interface by reducing the plasma-induced damage in the source/drain regions of the a-SiGe:H film and, as result, the series contact resistance of the device is improved.

From Fig. 4 can be observed the improvement in the metal–semiconductor interface for a-SiGe:H TFTs with applied hydrogen plasma. In the output characteristics of TFTs without hydrogen plasma application a high contact resistance appears in the bias range of 0–1 V of V_{ds}. The high contact resistance not appears in TFTs with applied hydrogen plasma. Also, the I_{ds} values of TFTs with applied hydrogen plasma indicate their better driving current capability. These results confirm that plasma-induced damage by the overetching process is reduced with the applied hydrogen plasma and the interface preparation procedure in the source/drain regions leads to form good ohmic contacts.

Since the SiNx passivation film could let remains between the n+ contact layer and a-SiGe:H active layer due to process variations, the overetching process assures the etching of the SiNx passivation film and gets close the n+ contact layer and the electron induced-channel at positive gate bias.

To compare the effects of the overetching process in the source/drain regions, transfer characteristics of a-SiGe:H TFTs with higher overetching are shown in Fig. 5. Poor electrical characteristics were obtained, even with the applied hydrogen plasma and thermal treatment, the subthreshold slope was of 0.98 V/DEC, the on/off-current ratio was approximately 10^3 and the off-current was approximately 200 pA at 0 V_{gs}.

The calculated maximum values of the trap density in the active layer a-SiGe:H (N_T) and in the SOG/a-SiGe:H interface (D_{it}) were 4.63×10^{17} cm^{-3} eV^{-1} and 4.63×10^{12} cm^{-2} eV^{-1}, respectively.

The measured threshold voltage and field-effect mobility for the a-SiGe:H TFTs with higher overetching were of 1.58 V and 0.56 cm^2/Vs, respectively. On the other hand, in the output characteristics a high contact resistance appears in the bias range of 0–1 V of V_{ds} (Fig. 6). From these results, the poor quality in the metal–semiconductor interface by the higher overetching process is evident. The plasma-induced damage results in high series contact resistance and cannot be reduced even with the applied hydrogen plasma and thermal treatment.

Previously, it was mentioned that we did not expect any difference in the quality of the insulator–semiconductor interface of the devices, since the overetching process only affects the source/drain regions. However, the increase in the value of the subthreshold slope from 0.56 to 0.98 V/DEC is not explained at all by the high contact resistance. Therefore, the subthreshold region of the device may also be affected by other mechanism and the plasma-induced damage near of the insulator–semiconductor interface by the higher overetching process seems to be the main reason.

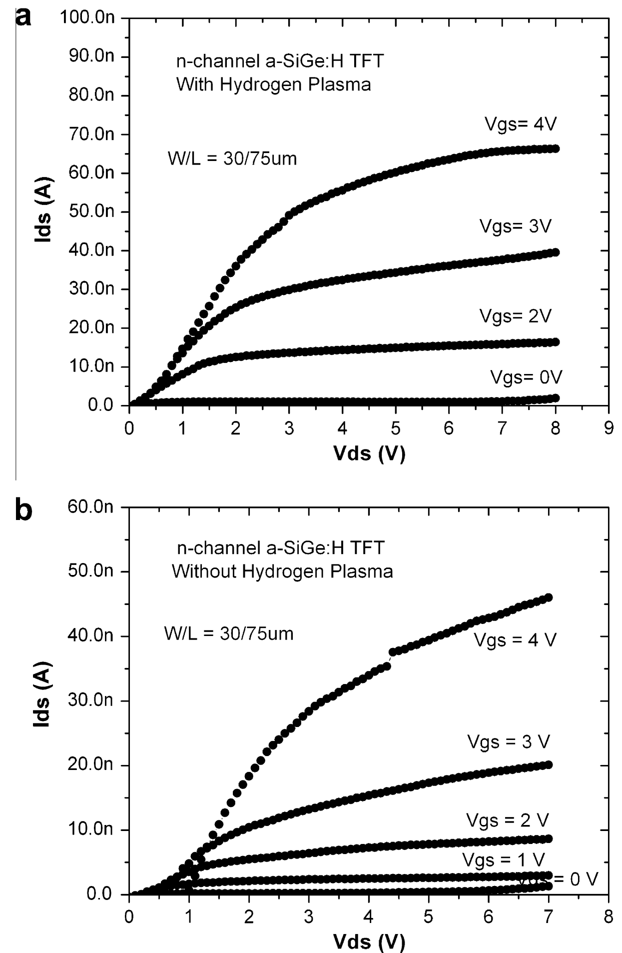

Fig. 4. Comparison of the output characteristics of a-SiGe:H TFTs, (a) with and (b) without hydrogen plasma application.

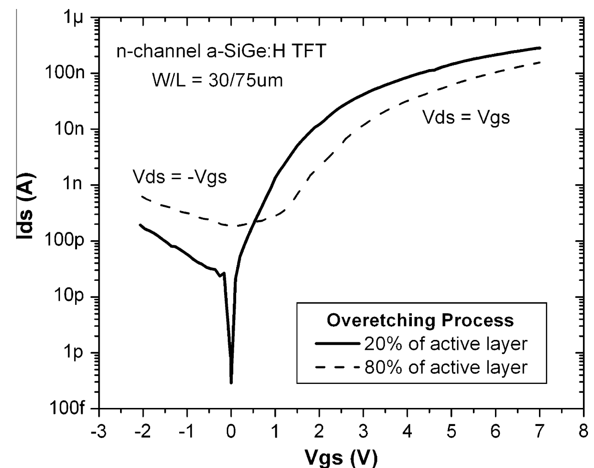

Fig. 5. Transfer characteristics of a-SiGe:H TFTs with higher overetching process.

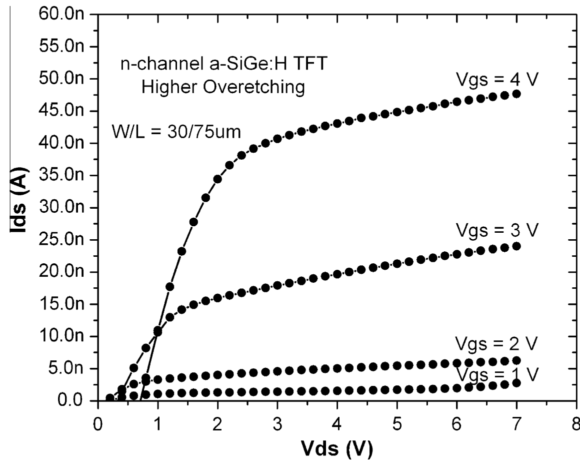

Fig. 6. Output characteristics of a-SiGe:H TFTs with higher overetching process.

4. Conclusions

In summary, the interface preparation procedure leads to achieve a good quality metal–semiconductor interface, which translates in low contact resistance. This interface improvement translates in higher mobility and better values of off-current, on/off-current ratio, subthreshold slope and V_T. An overetching in the source/drain regions of approximately 20% of the a-SiGe:H thickness can improve the TFT performance, since the overetching process assures the etching of the SiNx passivation film and gets close the n+ contact layer and the electron induced-channel at positive gate bias. Besides, the plasma-induced damage by the overetching process can be reduced with the hydrogen plasma application and thermal treatment. While the plasma-induced damage in TFTs with an overetching in the source/drain regions of approximately 80% of the a-SiGe:H thickness cannot be reduced even with the hydrogen plasma application and thermal treatment.

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