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Binary Genetic Encoding for the Synthesis of Mixed-Mode Circuit Topologies

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Abstract A binary genetic encoding (BGE) representation for the automatic synthesis of mixed-mode circuit topologies, is introduced. First, the genetic encoding of unity-gain cells (UGCs), such as voltage (VF) and current followers (CF), and voltage (VM) and current mirrors (CM), is presented. New BGEs for the VM and CM are introduced. Second, the UGC's chromosomes are combined to synthesize mixed-mode circuit-topologies, namely current conveyors and current-feedback operational amplifiers (CFOA). Five strategies for the combination or superimposing of UGCs are introduced. The proposed BGE has been implemented in MATLAB^{TM}, and links SPICE to evaluate the populations with different integrated circuit technologies. Some new synthesized circuit topologies are shown along with their chromosome description.

Keywords Evolutionary electronics · Genetic encoding · Nullor · Circuit synthesis · Unity-gain cell · Current conveyor · Current-feedback operational amplifier

1 Introduction

Nowadays, electronic design automation tools are very useful to accelerate the integrated circuit design process [10, 15]. Basically, these tools automate many repetitive

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design tasks. However, for the automatic construction or synthesis of complex building blocks from basic cells, analog design automation is still in the beginning, compared with digital design automation. For instance, from the logic gates NOT, NAND and NOR, complex digital architectures can be created. On the other hand, the goal of this article is devoted to showing that from the combination or superimposing [27] of four unity-gain cells (UGCs) [22], namely: voltage (VF) and current followers (CF) [20, 31], and voltage (VM) and current mirrors (CM) [1, 29], more complex analog devices can be created. Furthermore, the automatic synthesis of mixed-mode circuit topologies is performed from a proposed binary genetic encoding (BGE) of UGCs.

If an analog circuit drives voltage signals at its ports, it is said to work in voltage-mode [8, 12], as for the VF and VM. If it drives current signals, it is said to work in current-mode [14, 33], as for the CF and CM. On the other hand, when an analog circuit drives both kinds of signal, i.e. voltage and current, it is working in mixed-mode [5]. Examples of these mixed-mode circuits are the current conveyor [17, 21, 24, 30], the operational transconductance amplifier (OTA) [34], the operational transresistance amplifier (OTRA) [16, 19], the current-feedback operational amplifier (CFOA) [2, 6, 7, 13, 23, 32], and other topologies described in [18] using pathological elements.

In this work, we introduce the automatic synthesis of mixed-mode active devices, such as current conveyors and CFOAs, using a simple genetic algorithm [26, 28]. That way, in Sect. 2 a BGE representation is introduced. In Sect. 3 five proposed strategies for combination or superimposing of UGCs [27] are presented. In Sect. 4, the automatic synthesis of mixed-mode circuits is described. In Sect. 5, discussion on the proposed BGE approach and challenges are given. Finally, in Sect. 6 some conclusions of this work are summarized.

2 Proposed Binary Genetic Encoding Representation

The first task of a genetic algorithm is related to how to encode the individuals in the population to be evolved. For the case of electronic circuits, a genetic encoding for analog filters was introduced in [3]. From this work, many encoding approaches have been presented up to now. Among them, the one proposed in [11] highlighted the application of evolutionary algorithms to synthesize different kinds of analog circuit. That way, this section introduces our proposed BGE representation for every kind of UGC. It is worthy to mention that the usefulness of the UGCs in analysis and design of analog circuits has been demonstrated in [4, 5, 18, 20, 22, 23, 27, 29].

As already shown in [26], the BGE of the VF can be performed from a topology consisting of nullators (O). Every element O is joined with a norator (P), leading to the combinations shown in Fig. 1. Figure 1(a) can be considered as two combinations, one for node i as the joint connection between O and P, and the other combination considering node j. Figures 1(b) and (c) show one joint node either i or j. These four combinations are encoded by two bits into gene *genSS*. As shown by Fig. 1(d), an O–P pair is replaced by a MOSFET, where the joint node is the source terminal, and it can be N-channel or P-channel, leading to the creation of a one-bit gene called

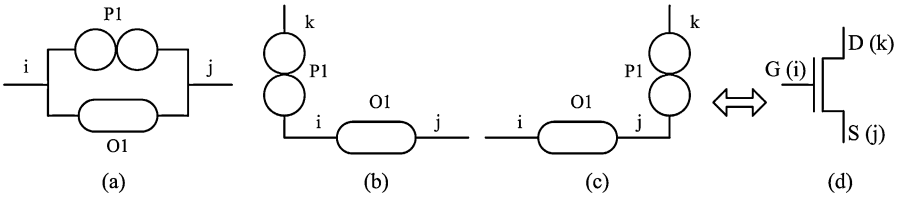


Fig. 1 (**a**) Parallel connection of the O–P pair, (**b**) joint node i, (**c**) joint node j, and (**d**) synthesis of the O–P pair in (**c**) by a MOSFET

Table 1 Length of the chromosome for the VF(CF)

VF(CF)	nullators(norators)	Chromosome	Length
1 MOS	1	*genMOS*(1).*genCM*	7 bits
2 MOS	2	*genMOS*(1).*genMOS*(2).*genCM*	12 bits
N MOS	N	$genMOS(1).\cdots.genMOS(N).genCM$	$5N+2$

Table 2 Chromosome 336860

Hexadecimal	0x0523DC				
Binary	(00)000101001000111011100				
Chromosome	*genMOS* (M1) 00010	*genMOS* (M2) 10010	*genMOS* (M3) 00111	*genMOS* (M4) 10111	*genCM* 00
genSS	00	10	00	10	
genSMos	0	0	1	1	
genBias	10	10	11	11	

genSMos. The biasing is performed by addition of DC voltage and current sources which are encoded by two bits into gene *genBias*. Many non-valid biased topologies are eliminated according to the rules provided in [25]. Finally, in every valid topology, the current biases are replaced by a CM using the gene *genCM*, whose length depends on the number of CMs in a library.

In this article, we modify the BGE for the VF introduced in [26]. Our new BGE is valid for any number of nullators in *genSS*, and basically each O–P pair (MOSFET) is grouped with its genes as shown in Table 1, where *genMOS* is the concatenation of the other three genes, $genMOS = genSS.genSMos.genBias$.

To generalize the chromosome description, we use hexadecimal notation, but some zeroes at the left can be deleted to have exactly the number of bits from Table 1. As an example, from a four nullators topology, the length of the chromosome is 22, then the hexadecimal (0x) description completes 24 bits to have six hex numbers. Table 2 shows one example where MOSFETs M1–M4 are depicted in Fig. 2(a). In this case, $genCM = 00$ for the simple CM, but it changes to 01 for the cascode CM shown in Fig. 2(b), and it changes to 10 and 11 for the Wilson and Improved Wilson CMs, as mentioned in [26].

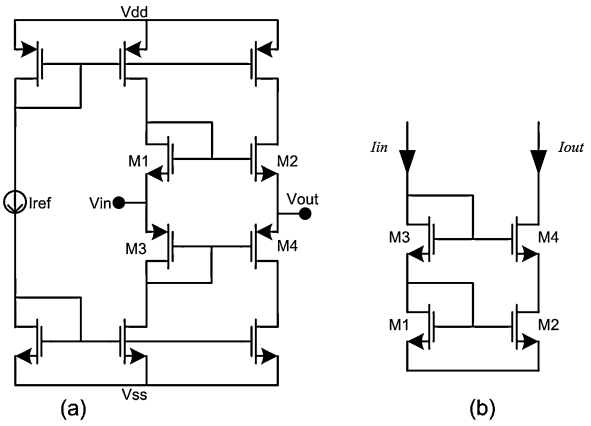


Fig. 2 (**a**) VF synthesized with simple CM. (**b**) Cascode CM

Table 3 Encoding for *genBias*

Bits	Drain	Source	Gate
0 0	Idd	Iss	V+
0 1	Iss	Idd	V+
1 0	Idd	Iss	V−
1 1	Iss	Idd	V−

Analogous to the BGE for the VF, the description of the CF begins by using norators [31]. In this case, a nullator (O) is added to the norator (P), to form O–P pairs. Then *genSS* and *genSMos* are the same as for the VF. Gene *genBias* is slightly modified, where both the drain and source terminals are connected to bias currents, and the gate to a voltage bias (V+ or V−), as shown in Table 3. Again, in the valid CF topologies, every current bias source is replaced by a CM using the gene *genCM*. Therefore, the BGE for the CF is the same as for the VF shown in Table 1, but changing VF by CF and nullators by norators.

The BGE of the CMs is quite different as for the VF and CF. The CM can be described using two (to synthesize a simple CM), three (to synthesize a Wilson CM) or four (to synthesize a cascode CM) norators, as shown in Fig. 3.

For instance, from Fig. 3(d), nullators and/or bias sources are added to nodes A, B, C and D. All O–P pairs are replaced directly by N- or P-channel MOSFETs, depending on the voltage bias level, so that *genSS* and *genSMos* are not necessary. However, *genBias* is more elaborated, for example, in Fig. 3(d) nodes C and D are connected to current sources, and each gate can be connected to nodes A, B, C, D, a voltage level V_{BIAS}, Vdd, or to an extra node (see Table 4). In the synthesis process the input (I_{in}) and output (I_{out}) nodes are identified through gene *genIO*, as shown in Table 4. For each O–P pair (MOSFET), gene *genN* is encoded as shown in Table 5.

In summary, our proposed BGE for the CM is shown in (1). The main advantage of this new BGE is the inclusion of level shifters. The length of *genBias* $= 3$ bits for each MOSFET (N), so that the length in (1) equals $6N + 3$ bits. Therefore, for $N = 4$ in Fig. 3(d) the length of (1) becomes 27 bits. In its hexadecimal representation we add one bit at the left. As an example, the chromosome 610304 is

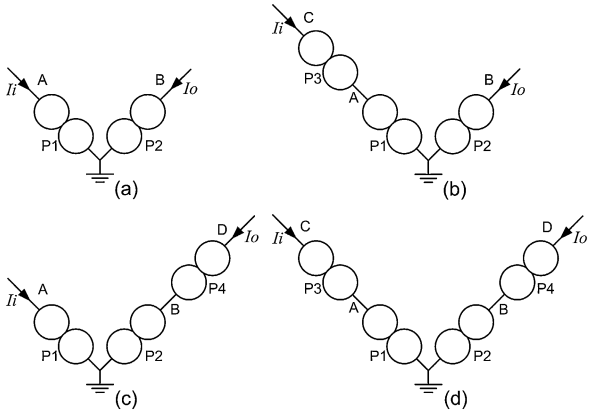
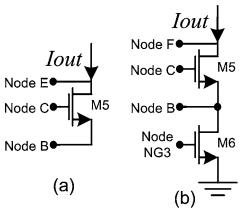


Fig. 3 Norator-based descriptions to synthesize CMs

Table 4 Input and output nodes of the CM from Fig. 3(d)

genIO	Input	Output	Nodes at I_{OUT}
0 0 0	Node A	Node B	
0 0 1	Node A	Node D	
0 1 0	Node A	Node E	
0 1 1	Node A	Node F	
1 0 0	Node C	Node B	
1 0 1	Node C	Node D	
1 1 0	Node C	Node E	
1 1 1	Node C	Node F	



equivalent to 0x0095000. The binary string is (0)00000001001010100000000000, where $genBias(M1) = genBias(M2) = 000$, $genBias(M3) = genBias(M4) = 010$, $genIO = 101$, and $genN(M1) = genN(M2) = genN(M3) = genN(M4) = 000$. From this chromosome, the synthesized CM is the cascode one shown in Fig. 2(b).

$$Chromosome_{\mathrm{CM}} = genBias.genIO.genN \tag{1}$$

For the BGE of the VM we use the three topologies shown in Figs. 4(a), (b) and (c). In Fig. 4(a) the O1–P1 pair is replaced by a MOSFET, and the other nullator by a VF, as shown in Fig. 4(d). In Figs. 4(b) and (c), P1 and P2 are parallel and series connected, respectively. They can be replaced by the topologies in Figs. 4(e) and (f). Then we have three variants for the BGE of Figs. 4(a), (b) and (c). Each O–P pair is encoded by *genSMos* to decide if it is N- or P-channel. The bias is encoded by *genBias*, as shown in Table 6 for each MOSFET, where node N = node 1 or 2, and node NA = opposite to node 1 or 2. Finally, *genIO* is used to decide the input and output port.

Therefore, the BGE for the VM is shown in (2). The length of *genSMos* is 1-bit for Fig. 4(a) and two bits for Figs. 4(b) and (c), and *genBias* = 4 bits for each MOSFET. Then the length in (2) equals 10 bits for Fig. 4(a) and 11 bits for Figs. 4(b) and (c).

$$Chromosome_{\mathrm{VM}} = genSMos.genBias.genIO \tag{2}$$

Table 5 Encoding of gene *genN*

genN	MOS 1	MOS 2	MOS 3	MOS 4
000	N_A, NG1, 0.1V	N_A, NG2, 0.1V	N_C, NG3, 0.1V	N_C, NG4, 0.1V
001	N_A, NG1, 0.7V	N_A, NG2, 0.7V	N_C, NG3, 0.7V	N_C, NG4, 0.7V
010	Vdd, Iref, NG1, N_A	Vdd, Iref, NG2, N_A	Vdd, Iref, NG3, N_A	Vdd, Iref, NG4, N_A
011	N_A, N_D, NG1	N_A, N_D, NG2	N_A, N_D, NG3	N_A, N_D, NG4
100	N_A, N_B, NG1	N_A, N_B, NG2	N_B, N_A, NG3	N_A, N_B, NG4
101	N_A, Vref, NG1	N_A, Vref, NG2	NG3=VBIAS	Vref, N_B, NG4
110	NG1=Node A	NG2=Node A	NG3=Node C	N_C, N_B, NG4
111	R1, NG1, N_A	Vdd, Iref, NG2	NG3=Node D	Vdd, gate3, NG4, gate1

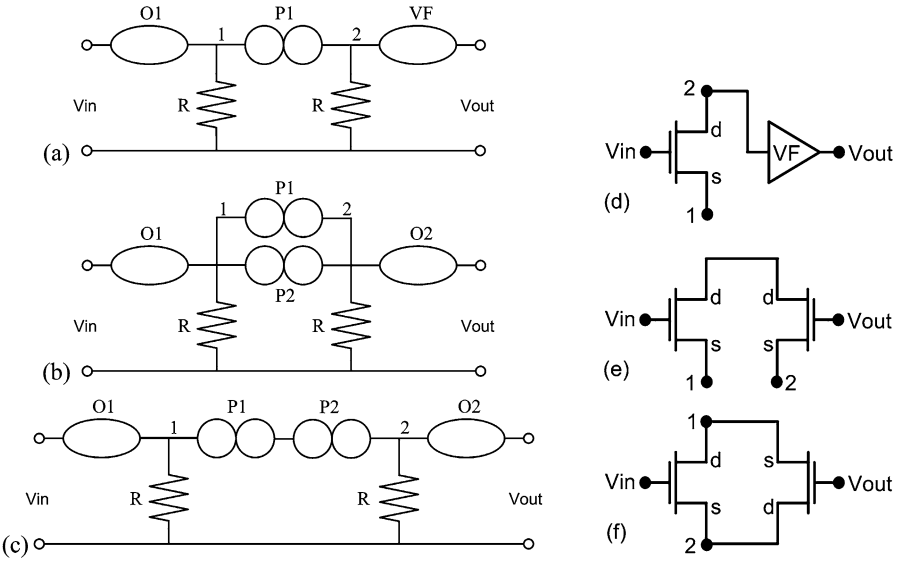
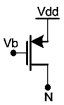
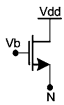
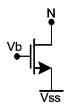
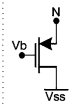
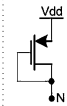
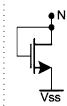
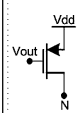
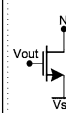
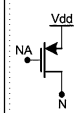
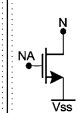
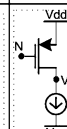
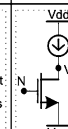


Fig. 4 Descriptions of the VM

Table 6 Encoding of *genBias* in the VM

0000	0001	0010	0011	0100	0101	0110	0111
							
1000	1001	1010	1011	1100	1101	1110	1111
							

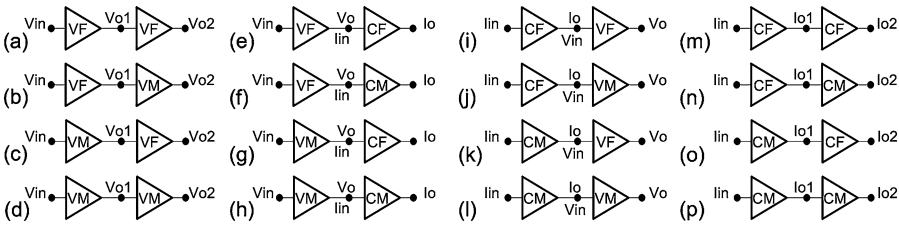


Fig. 5 Combinations among two UGCs

3 Synthesis of Mixed-Mode Circuit Topologies

Two UGCs are combined or superimposed [27] to create complex topologies, as shown in Fig. 5. Several topologies describe some kinds of current conveyor [30]. The chromosome of each UGC is taken from Sect. 2.

For instance, the negative and positive types second generation current conveyors (CCII−/+) can be generated from Figs. 5(e) and (f), and their inverting realizations (ICCII−/+) from Figs. 5(g) and (h). The superimposing [27] of Figs. 5(f) and (k), generates the CFOA. Basically, it is the connection of three blocks VF-CM-VF, or equivalently, the CCII+ in cascade connection with a VF [9]. Furthermore, to synthesize the mixed-mode circuit topologies from Fig. 5, we propose five strategies.

1. Simple union: This is the most simple design because two UGCs are cascade-connected by a cable. However, it is only suitable for Figs. 5(b) where $V_{o1} = V_{in}$ and $V_{o2} = -V_{in}$; (d) where $V_{o1} = -V_{in}$ and $V_{o2} = V_{in}$; (i) where $I_o = I_{in}$ and $V_o = V_{in}$; (j) where $I_o = I_{in}$ and $V_o = -V_{in}$; (k) where $I_o = -I_{in}$ and $V_o = V_{in}$; and (l) where $I_o = -I_{in}$ and $V_o = -V_{in}$.
2. Duplicating output: This synthesis strategy duplicates the output of the UGC. This can be applied to Figs. 5(a) where $V_{o2} = V_{o1} = V_{in}$; (c) where $V_{o2} = V_{o1} = -V_{in}$; (m) where $I_{o2} = I_{o1} = -I_{in}$; and (o) where $I_{o2} = I_{o1} = I_{in}$.
3. Duplicating middle-output: This strategy consists of duplicating the output of the first UGC. It can be performed for Figs. 5(n) where $I_{o2} = -I_{o1} = -I_{in}$, and (p) where $I_{o2} = -I_{o1} = I_{in}$.

4. Creation of node Z: It consists of modifying the synthesis of the bias current sources in the VF or VM to create an output current. It is performed for Fig. 5(f) where $V_o = V_{in}$ and $I_o = -I_{in}$, corresponding to the description of the CCII+, and Fig. 5(h) where $V_o = -V_{in}$ and $I_o = -I_{in}$, corresponding to the description of the ICCII+ [30].
5. Combination of nullators–norators: This procedure combines nullators (describing a VF) with norators (describing a CF). It is applied to Fig. 5(e) where $V_o = V_{in}$ and $I_o = I_{in}$, corresponding to the description of the CCII− [27], and Fig. 5(g) where $V_o = -V_{in}$ and $I_o = I_{in}$, corresponding to the description of the ICCII− [30].

The BGE of the CFOA can be created from the cascade connection of a CCII+ with a VF [9, 30], or equivalently the combination of three UGCs: VF-CM-VF. To synthesize first and third generation current conveyors [30], and other mixed-mode circuits [18], other combinations among three or four UGCs can be performed.

4 Automatic Synthesis of Mixed-Mode Circuit Topologies

This section shows several new UGC topologies and the creation of new current conveyors and CFOAs. The synthesis begins by selecting the device to be created, then the BGEs from Sect. 2 are manipulated by a genetic process [28]. The main steps are:

- Kind of active device: One selects the topology to be synthesized, UGC [26, 31], Current Conveyor or CFOA.
- Desired performances: Gain, bandwidth, impedance [28].
- Kind of circuit simulator: TOP-SPICE, H-SPICE, Tanner-SPICE.
- Kind of integrated circuit technology:
  - AMI Semiconductor: 0.35 μm, 0.50 μm.
  - IBM Semiconductor: 0.18 μm, 0.25 μm, 0.35 μm, 0.50 μm.
  - Taiwan Semiconductor (TSMC): 0.18 μm, 0.25 μm, 0.35 μm.
- Size of the population (Pop), mutation percentage, maximum number of generations and minimum error for the fitness evaluation.

1. The individuals (chromosomes) are randomly created to generate the initial population of size Pop.
2. The crossover is performed to create an offspring of size Pop, then the total population becomes size 2Pop (parents and children). The population is mutated by 3%.
3. The chromosomes are verified by simple inspection of the genes connection, some guidelines are provided in [25] (the input and output ports cannot be connected to the power supply, for instance), so that non-valid topologies are eliminated automatically.
4. Each valid chromosome is decoded to generate its SPICE-netlist, to be simulated with the selected technology.
5. Every individual is evaluated and the whole population is ranked by elitism to select the new parent population of size Pop.

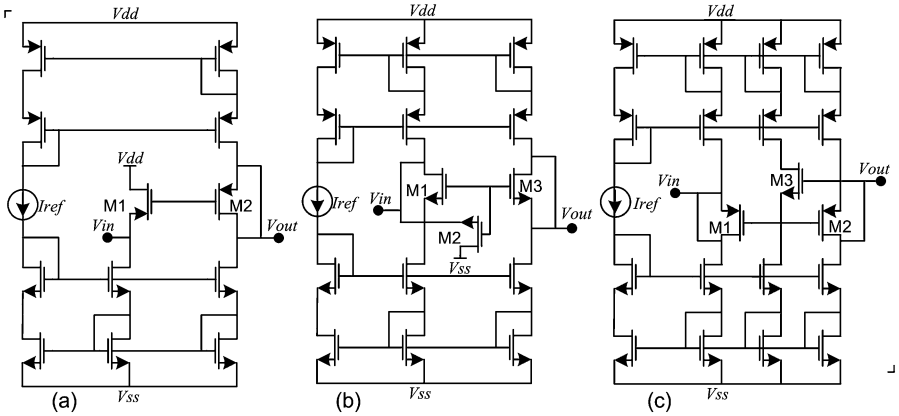


Fig. 6 New synthesized VFs: Chromosomes (**a**) 0x4BB, (**b**) 0x3419B, and (**c**) 0x3F717

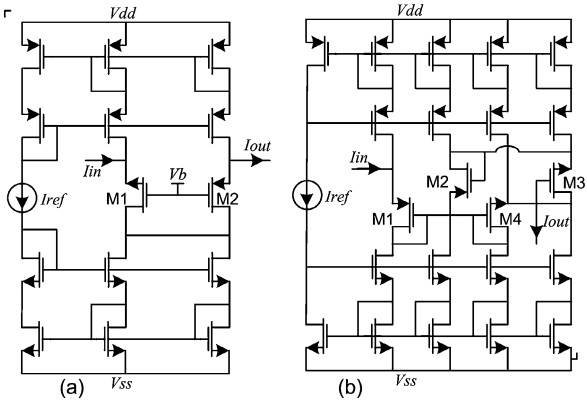


Fig. 7 New synthesized CFs: Chromosomes (**a**) 0x16B, and (**b**) 0x5ED3CE

Table 7 Performances of the VFs from Fig. 6

Topology	Gain	BW	R_{IN}	R_{OUT}
6(a)	0.943	10.7 MHz	108 KΩ	7.63 KΩ
6(b)	0.971	25.0 MHz	15.1 KΩ	7.0 KΩ
6(c)	0.958	24.8 MHz	24.7 KΩ	24.7 KΩ

4.1 Synthesis of UGCs

We selected the VF as active device, unity-gain, bandwidth and resistances as performances, Tanner-SPICE, technology of 0.35 µm AMI Semiconductor, size of 40 individuals and 150 generations. The synthesis process created the three VFs shown in Fig. 6. Table 7 list the performances with sizes L = 1.2 µm, WN = 1.0 µm and WP = 4.4 µm. Besides, a multi-objective evolutionary algorithm can be used to optimize more performances, as shown in [28].

For the other UGCs: Two new CFs are shown in Fig. 7, six new CMs are shown in Fig. 8, and four VMs are shown in Fig. 9.

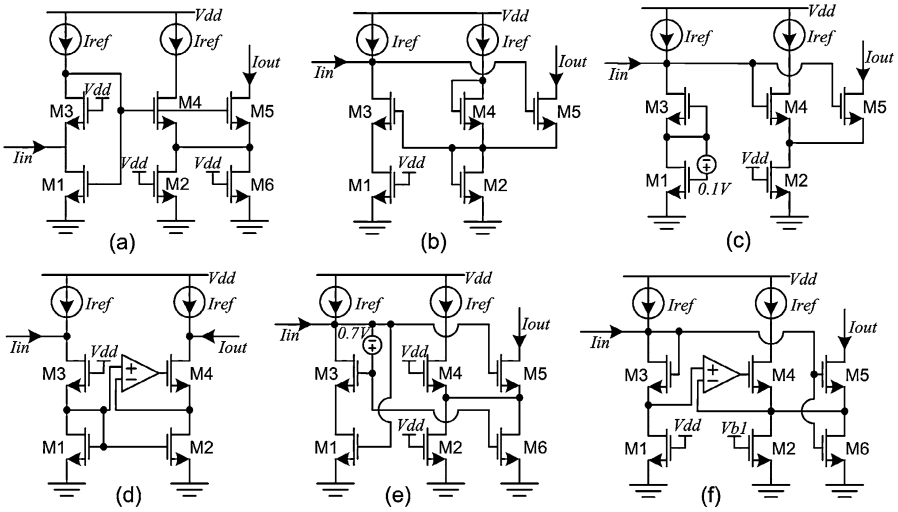


Fig. 8 New synthesized CMs: Chromosomes (**a**) 0x2913A1C, (**b**) 0x425EAA6, (**c**) 0x781615C, (**d**) 0x7135C0C, (**e**) 0x29E7F88, and (**f**) 0x4ABFBE4

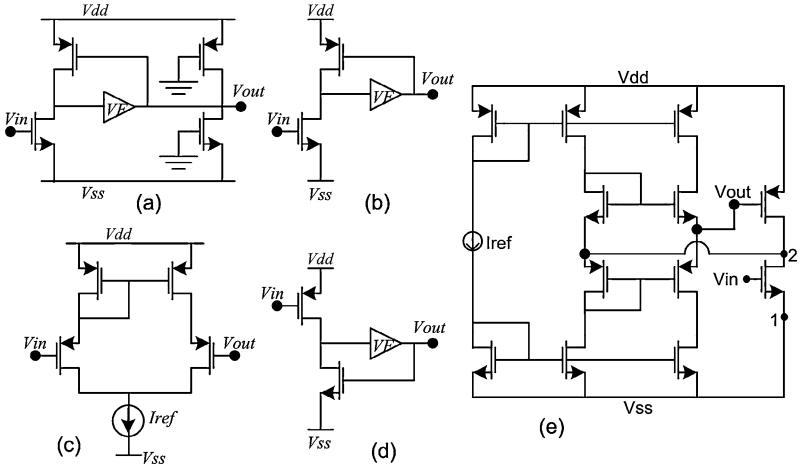


Fig. 9 Synthesized VMs: Chromosomes (**a**) 0x034, (**b**) 0x035, (**c**) 0x719, and (**d**) 0x217. (**e**) The implementation of the VF in (**b**)

4.2 Synthesis of Current Conveyors and CFOAs

This subsection shows several topologies synthesized according to the strategies introduced in Sect. 3. Figure 10 shows one topology for each kind of UGC with duplicated outputs. Two new CCIIs are shown in Fig. 11. Finally, two new CFOAs are shown in Fig. 12.

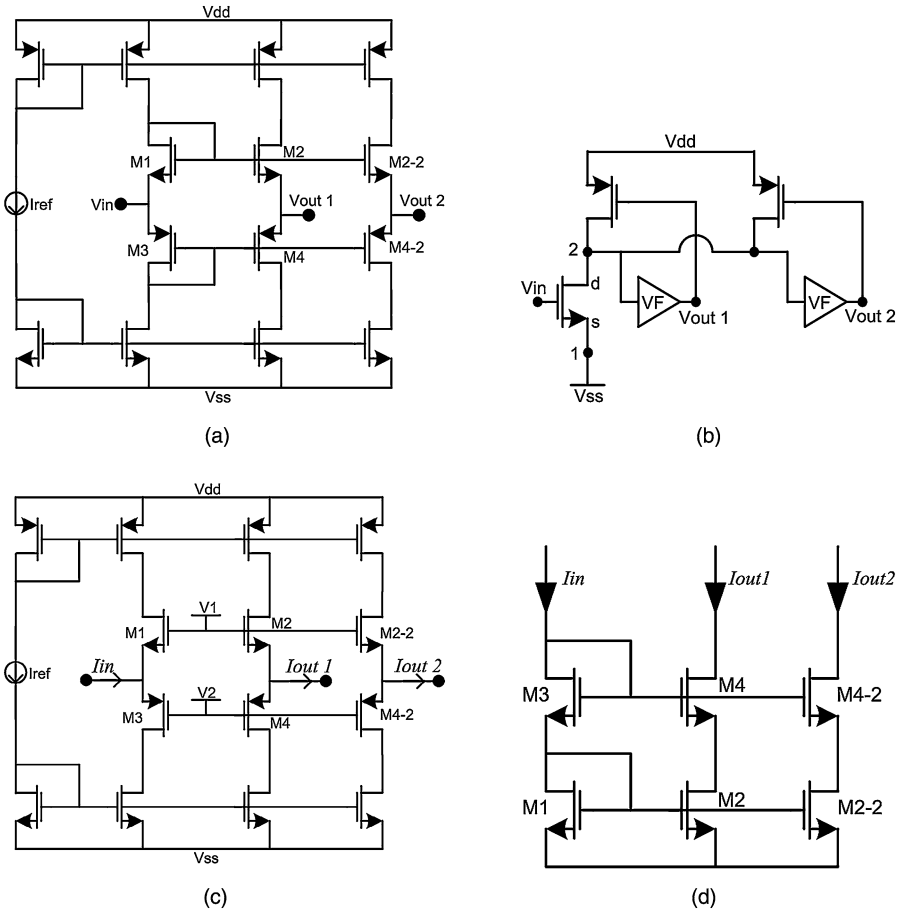


Fig. 10 (**a**) VF, (**b**) VM, (**c**) CF and (**d**) CM with two outputs

5 Discussion

Many works presenting synthesis approaches are mainly focused on the proper biasing and sizing of analog circuits; and the few ones creating new topologies combine basic building blocks as differential pair, current mirror, level shifter, common-source, common-drain, common-gate transistors, and so on. But they have a library which is static. That is because the real synthesis problem is not well solved; furthermore the bottle neck in the synthesis process is still the selection of the right circuit topology. In this manner, our proposed BGE allows us to create a very huge number of circuit topologies from which one can apply selection approaches to design the optimal circuit. In this case, evolutionary algorithms are a good alternative to generate sets of solutions of feasible circuit topologies and sizes. That way, this work highlights a new BGE representation suitable for the synthesis of almost all kinds of mixed-mode circuit topology. This new BGE improves the one for the VF introduced in [26], it is valid for any number of transistors, it is new for the CM with the main

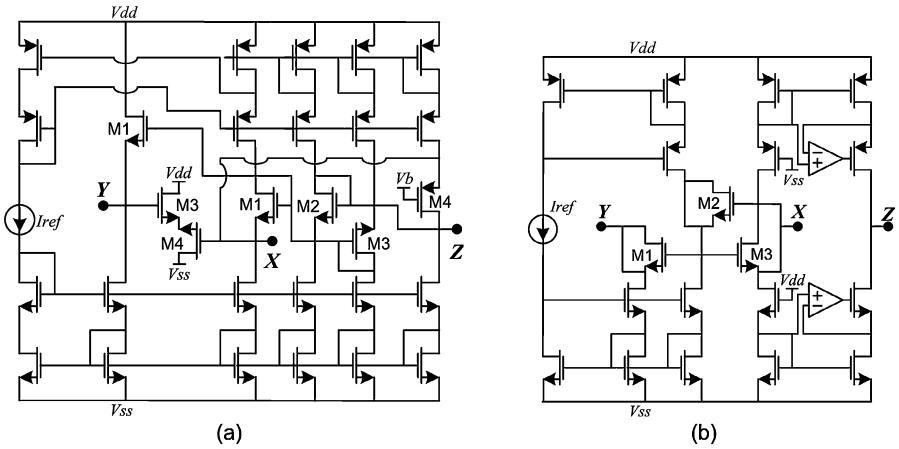


Fig. 11 New (**a**) CCII− by superimposing VF 0x1080F with CF 0x465B3A [27], and (**b**) CCII+ by combining VF 0x31B9A with CM 0x7135C0C

advantage of including level shifters, and it is also new for the VM. The chromosomal notations are done using hexadecimal (0x) numbers to have a unique representation for each BGE.

Taking the four UGCs (VF, CF, VM and CM) as basic cells, their interconnection or superimposing leads us to generate already known and new mixed-mode circuit topologies. For instance, in Sect. 3 five strategies were described for the interconnection or superimposing two UGCs to generate CCIIs topologies. Moreover, more complex mixed-mode circuits can be generated by interconnecting or superimposing more than two UGCs. For example, three UGCs are required to synthesize first (CCI) and third (CCIII) generation current conveyors, and their inverting topologies [30]. In a similar way, other mixed-mode circuit topologies as the ones shown in [18], can be generated by developing new interconnecting or superimposing strategies among two or more UGCs. For instance, in Sect. 4 new UGCs are shown in Figs. 6 to 9, new UGCs with duplicated output are shown in Fig. 10, two new CCIIs are shown in Fig. 11, and two new CFOAs are shown in Fig. 12. In all cases their binary strings are represented by hexadecimal numbers in order to have a unique meaning when they are decoded to create transistor-based circuits. Every generated circuit was simulated by HSPICE, but many non-valid topologies were eliminated according to the rules provided in [25, 26].

New challenges are oriented to develop new interconnecting or superimposing strategies among two or more UGCs, to generate all kinds of mixed-mode topology [18, 30], and to explore parallel simulations to accelerate the evaluation of the generated topologies within an evolutionary algorithm [28].

6 Conclusion

A new binary genetic encoding (BGE) representation for the automatic synthesis of mixed-mode circuit topologies, has been introduced. The chromosomal representa-

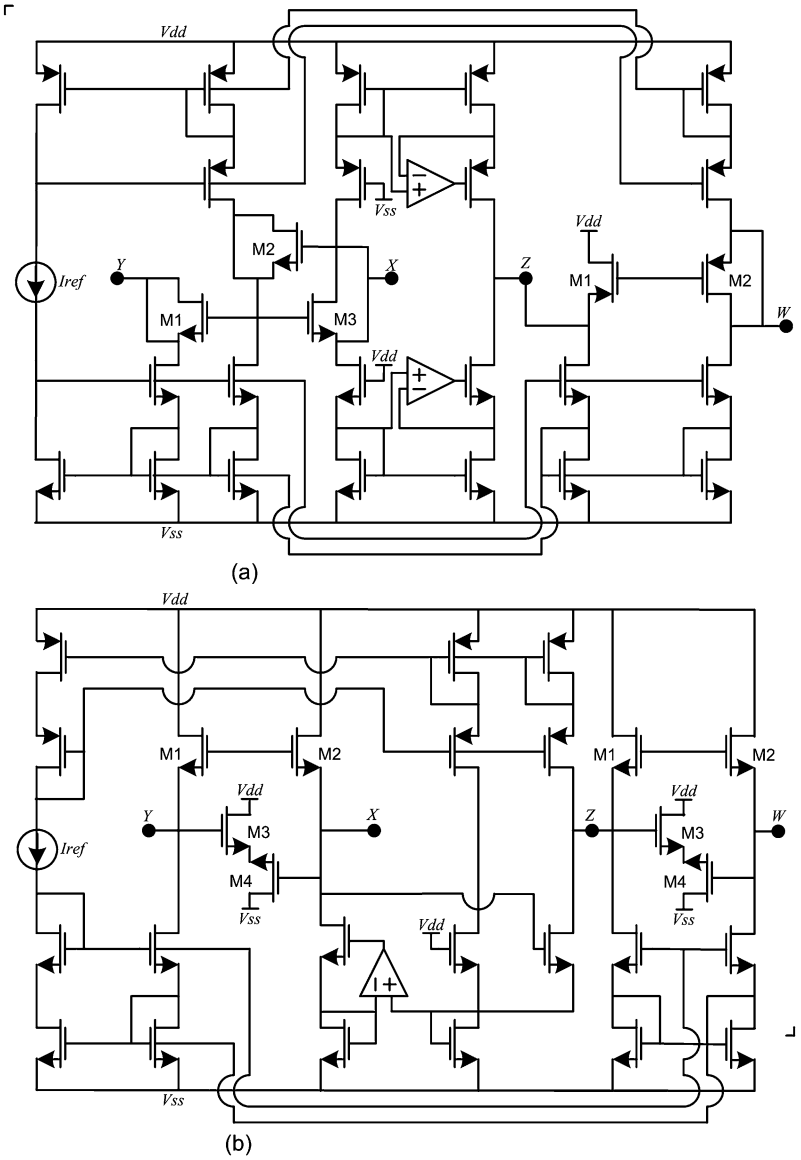


Fig. 12 New CFOA by combining chromosomes: (**a**) 0x31B9A.0x7135C0C.0x4BB, and (**b**) 0x01080F.0x03E6CA1.0x01080F

tion of every kind of UGC has been generated from nullator/norator descriptions, and the binary strings were represented by hexadecimal numbers, in order to have a unique meaning when they are decoded to create the transistor-based circuits. The combinations when connecting or superimposing two UGCs were detailed by proposing five strategies: Simple union, duplicating output, duplicating middle-output, creation of node Z, and combination of nullators–norators. From these strategies, the

chromosomes representing current conveyors and CFOAs were developed. To synthesize first and third generation current conveyors [30], and other mixed-mode circuits [18], other combinations among three or four UGCs can be performed. Finally, several new UGCs and mixed-mode circuits were synthesized through genetic operations. As a result, our proposed BGE representation is quite useful to search for the creation of other novel mixed-mode circuits, because the searches spaces are quite huge.

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