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Study and comparison of CMOS layouts for applications in analog circuits

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This study presents different layouts techniques (serpentine, concentric, interdigitated) applied to a differential amplifier designed in commercial technology CMOS (0.6 µm). It was observed that serpentine technique improves by 6 to 7 electrical parameters, where area was reduced (64%) and power consumption diminishes until a 57% with respect to conventional technique. Thus designer can optimally use different abstraction levels during integrated circuits (IC) design, by applying the best layout technique towards efficient systems.

Keywords: Integrated circuit (IC), Layout, Operational amplifier, Serpentine

Introduction

With advances in submicron technologies for manufacturing integrated circuits (IC's), it is now possible to obtain systems that may contain millions of transistors with optimal characteristics considering figures of merit [integration density, speed, slew rate (SR) and power consumption][1]. In particular, geometric aspect (layout) of devices within modules or systems represents a decisive factor that determines performance of analog circuits[2]. Currently, the characteristics (reduced space, high speed, reduced power consumption and a high immunity to noise) require to be optimized for all kind of IC's, analog, digital or mixed-mode[3,4]. This study presents a two-stage amplifier, where geometric aspects are analyzed and characterized using three strategies for designing layout in order to optimize figures of merit [integration density, power consumption, gain, power supply rejection ratio (PSRR), common mode rejection ratio (CMRR) and SR] of amplifier. The design was realized using a 0.6 µm-complementary metal oxide semiconductor (CMOS) technology, which uses three metal and two poly layers, and a high resistance layer. In addition, Layout Virtuoso of CADENCE®[5] that includes parasitic elements of circuit was used.

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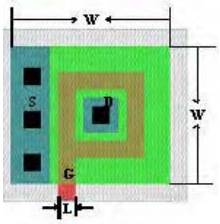
Experimental Section

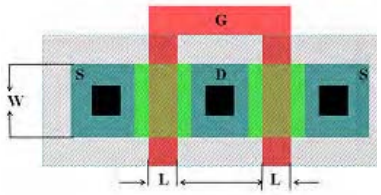
Layout Techniques

Different layout techniques for analog, digital and mixed-mode IC's generally are intended to reduce parasitic elements of devices. This is particularly important when high performance circuits are designed (reduced delay and power consumption, high immunity to noise, etc.). Layout of an IC can be realized using different approaches. This study is considering only those techniques that allow for obtaining high speed circuits (concentric or closed form[6,7], interdigitated or Comb[8], and serpentine) and conventional technique will be used as a reference for comparison of obtained results. Among these techniques (Fig. 1), serpentine, which has been used for analog circuits[9], has demonstrated to improve integration density and power consumption in digital circuits.

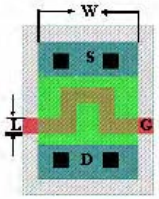
In any MOS circuit, capacitance in a certain signal node (C_L) is given by the sum of three components as $C_L = C_{in} + C_{int} + C_{out}$, where C_{out} is output capacitance (self-load) of the driver, C_{int} is interconnection capacitance and C_{in} is input capacitance (load) of the circuit to be derived. C_{in} per area for a CMOS gate and C_{int} per length, respectively, are given as[10].



a) Concentric



b) Interdigitated



c) Serpentine

Fig. 1—Layout styles

$$C_{in} = \left(\frac{e_{ox}}{t_{ox}}\right)\left(\sum W_n + \sum W_p\right) L_{min} \quad \ldots(1)$$

$$C_{int} = e_{ox}\left\{\frac{W_{int}}{t_{ox}} - \frac{H_{int}}{2t_{ox}} + \frac{2p}{\ln\left[1+\frac{2t_{ox}}{H_{int}}\left(1+\sqrt{1+\frac{H_{int}}{t_{ox}}}\right)\right]}\right\} \quad \ldots(2)$$

where e_{ox} and t_{ox} are silicon dioxide permittivity and thickness, respectively; W_n and W_p are contributions in width for all connected transistors that form the gate and the input node; and $L_{mín}$ is minimum length of channel, H_{int} is interconnection length and W_{int} is interconnection width.

In agreement with Eq. (1), C_{in} of gate is not a function of layout style. The same occurs to C_{int}, which is a function of W_{int}, H_{int} and t_{tox}. C_{int} decreases when three values are approximately the same. C_{out}, on the other hand, is formed by diffusion capacitances (C_d) of transistors determined by the areas defined for source and drain. C_d can be considered as[11] $C_d = C_{jd}A_d + C_{jsw}P_d$, where C_{jd} and C_{jsw} are junction capacitances per area and the periphery capacitances per length, respectively. Values of these capacitances were determined by the technology used in this study; A_d and P_d are the area and perimeter of drain, respectively.

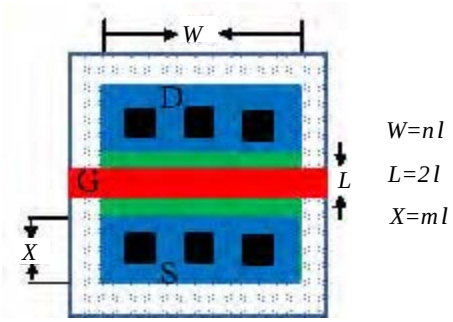


Fig. 2—Conventional layout

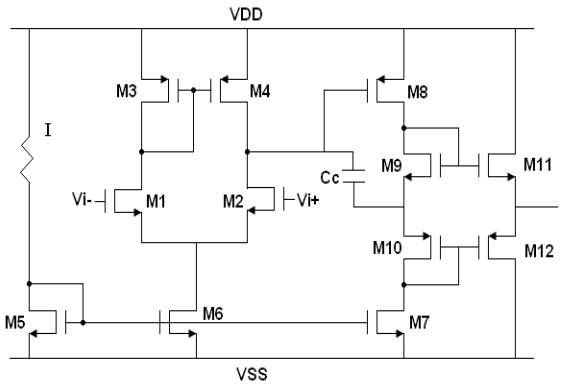


Fig. 3—Amplifier schematic

Table 1—Influence of techniques in the area and perimeter of transistor

Technique	W/L, µm	A_d, µm²	A_s, µm²	P_c, µm	P_s, µm
Conventional	24/1.2	36	36	27	27
Concentric	24/1.2	22	33	35	48
Interdigitated	2.4/1.2	36	21.2	18	54
Serpentine	24/1.2	23.5	25	13	20

In layout of a MOS transistor (Fig. 2) using conventional technique, l is scaling factor associated to fabrication process (which normally is half of the minimum dimension allowed for the technology), m is length of drain or source and n is width of transistor. Area and perimeter of source and drain (Fig. 2) are given as $A_d = A_s = W * X = l^2(m*n)$ and $P_d = P_s = 2(W+X) = 2l(m+n)$ respectively, where A_s and P_s are area and perimeter of source, respectively. Designer can improve performance of circuits by modifying area and perimeter of transistors and thus the value of parasitic capacitances. Table 1 shows difference in areas and perimeters of drain and source using different

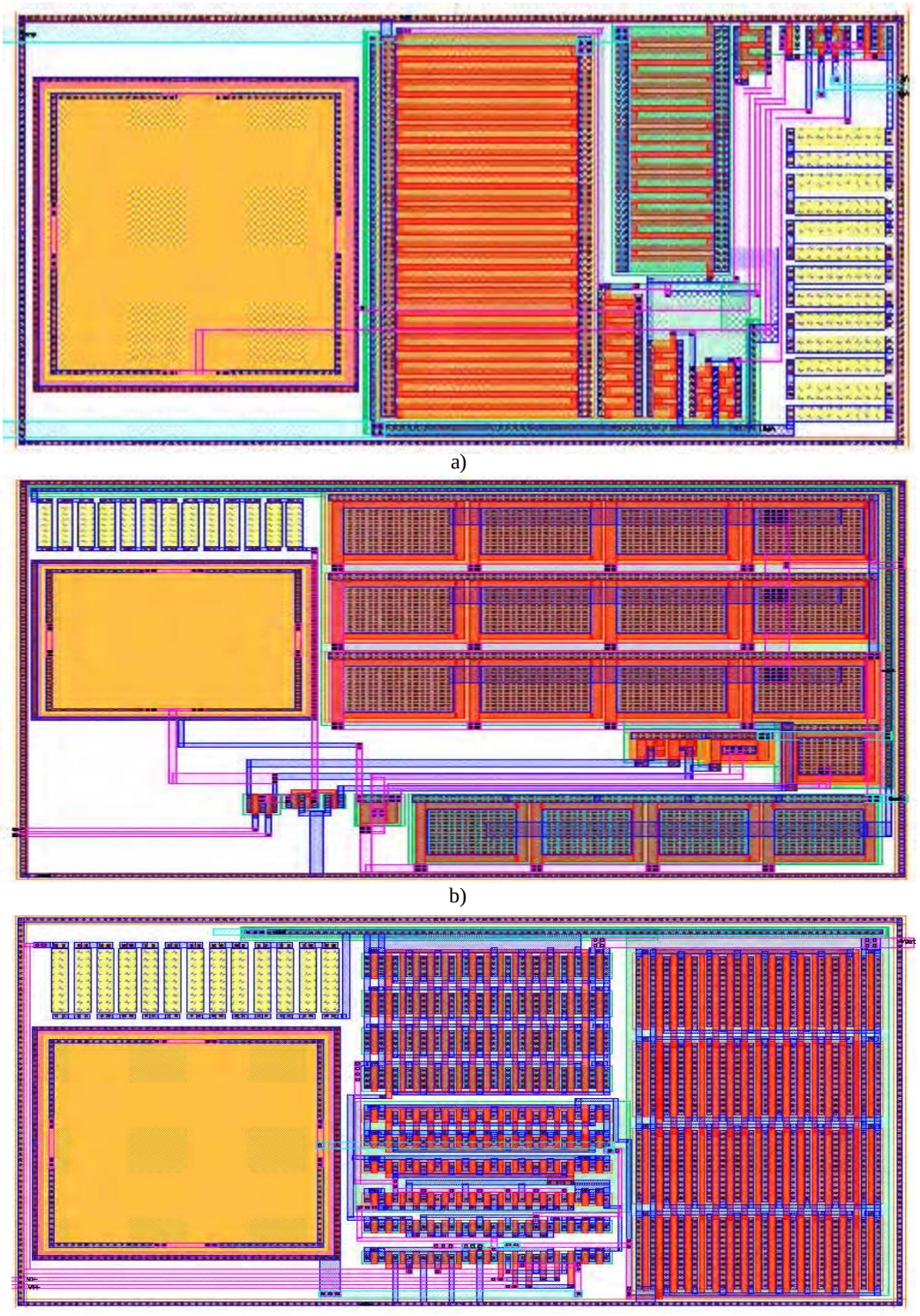


Fig. 4—Layout of amplifier applied to: a) *Serpentine* technique; b) *Concentric* technique; and c) *Interdigitated* technique

layout techniques in a MOS transistor. For *Interdigitated* technique, areas and perimeters of source and drain, as well as total width of transistor, must be multiplied by a factor of 10.

Characterization

In technologies for submicrometric IC's, reduction of effective area is an important parameter to include a larger number of circuits per chip; this reduces parasitic

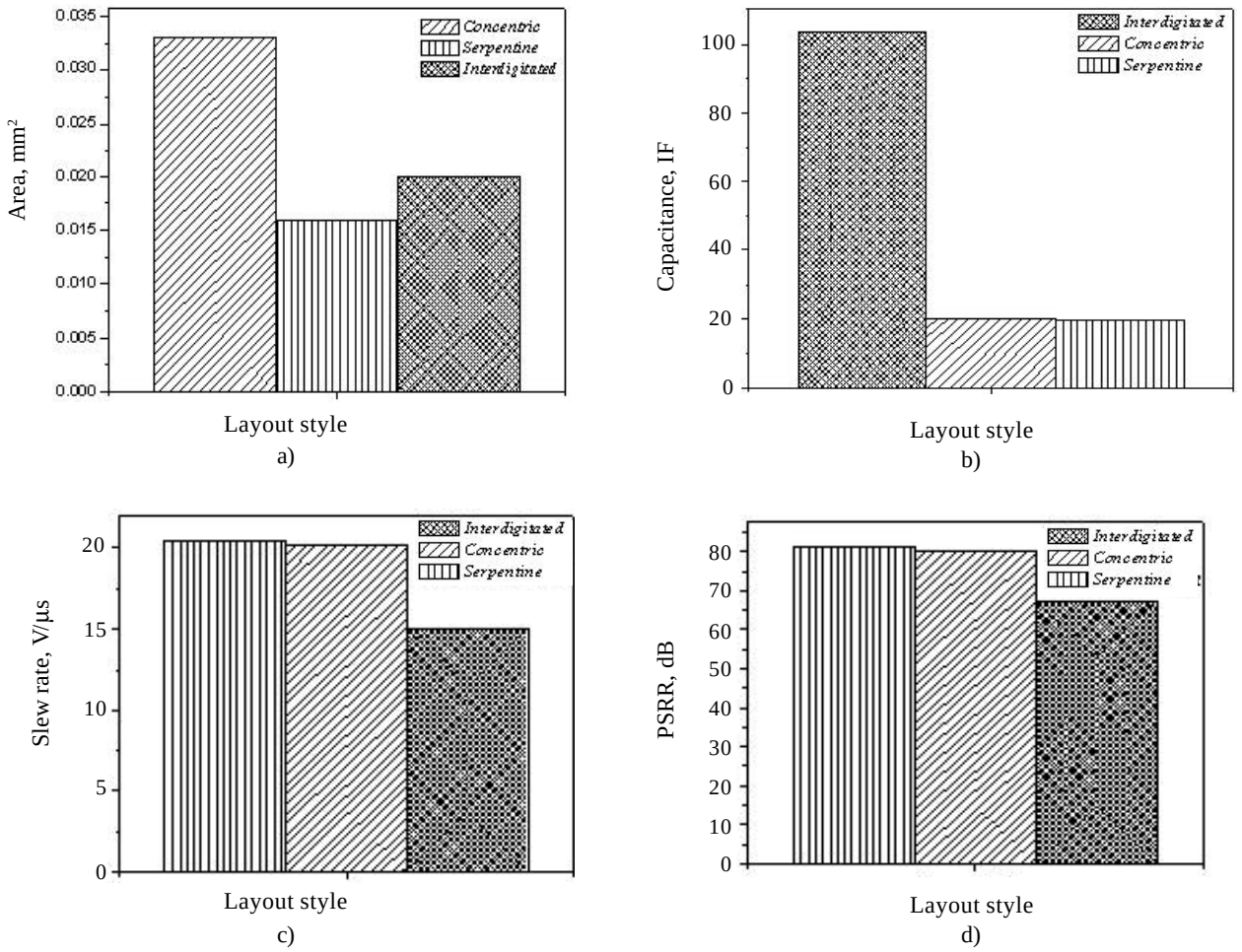


Fig. 5—Comparison of three techniques based on following parameters: a) Amplifier area; b) Output capacitance; c) Slew rate; and d) PSRR

capacitances, since dominant capacitance at any node of circuit is C_d. This is why, in this study, these components are varied to obtain circuits with reduced areas and power consumption. For efficient evaluation of different layout techniques, an analog circuit was used with different design criteria. A class AB analog amplifier (Fig. 3) was used. All geometric patterns were generated using minimum dimensions allowed by design rules of *ON Semiconductor*[12] technology, which allows, to a great extent, for the reduction of parasitic capacitances in all relevant nodes. For all implementations, same size of transistors (*W*/*L*: M1-M2, 7.2/1.2; M3-M4, 16.8/1.2; M5-M7, 4.8/1.2; M8, 33.6/1.2; M9, 24/1.2; M10, 74/1.2; M11, 360/1.2; and M12, 1197/1.2 µm) and values for load elements (capacitances and resistances) were used, as well as same input signal and operating frequency. Size of transistors M11 and M12 were designed to handle the load and to connect themselves directly to an output terminal (PAD) without a buffer. This amplifier is designed for its use in medical applications for registry of neuronal activity, electrocardiograms and measurements of pH.

Parasitic elements of circuits were extracted using Virtuoso tool *Extracted* (CADENCE®), using technological parameters of 0.6 µm process of *ON Semiconductor* technology. Electrical results of simulations were obtained from the analysis conducted with circuit simulator *spectreS*. These environments conduct simulations of performance and transistor level behavior, in such a way that they will be very close to those shown by fabricated IC's. Exactitude of simulation will depend on the model used for transistors, which in present case is BSIM3v3.3 model[13]. This simulator calculates all the second order effects (saturation of velocity, degradation of mobility, modulation of channel length, body effect, etc.)[14]. In layout of the op amp

Table 2—Electrical specifications

Parameters	Serpentine	Concentric	Interdigitated
Gain, dB	63.2	63.1	59.3
CMRR, dB	79	78	78
PSRR, dB	81	80	67
Power, mW	5.2	5.4	11.4
Slew rate, V/μs	20.4	20.1	15.0
Offset, mV	160	150	75
Area, mm^2	0.016	0.033	0.020

(Fig. 4), designed using different techniques, total circuit includes the area occupied by transistors P and N, as well as the input, output and power supply lines.

Results and Discussion

Considering the area used by amplifier, it is observed that circuit uses less area for *Serpentine* and *Interdigitated* techniques (Fig. 5a), corresponding the smallest area to the first one. Input capacitance is practically the same in each circuit, independent of layout technique. Variation existing between the techniques comes from capacitance due to polysilicon lines outside the active area of transistors. Therefore, it is verified that input capacitance, determined by effective ratio of width to length of transistor, does not depend on layout style. Techniques with smaller output capacitance (Fig. 5b) were *Concentric* and *Serpentine*, thus faster circuits can be achieved with these techniques. In order to obtain a better estimation of the operation of designed op amp using different layout techniques, electrical simulations were conducted to obtain some electrical parameters (gain, offset, power consumption, SR, CMRR and PSRR). Faster circuits (Fig. 5c) and improved PSRR (Fig. 5d) are produced by *Concentric* and *Serpentine* techniques. Considering power consumption, one sees that the most efficient techniques for analog IC's were *Concentric* and *Serpentine*. Considering Power-Delay-Area Product (PPDA), *Serpentine* technique leads to smaller PPDA products, being therefore most efficient for its application in IC's design. Table 2 shows simulation results and characteristics of different circuits.

Conclusions

In different layout techniques applied to a two-stage amplifier, *Serpentine* technique reduces area (64%) and power consumption (57%) as compared to conventional technique. Also, *Serpentine* technique increased slew rate mainly due to reduction of the areas of source and drain, which reduces parasitic capacitances of interconnection and between devices. Electrical simulations demonstrated that *Serpentine* technique improves the values of 6 out of 7 electrical parameters obtained. Considering 3 (area, delay and power) of 4 parameters, which determine performance of an IC, *Serpentine* technique must be adopted to obtain the best PPDA product.

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