Design of a data acquisition system for radioastronomical activities.

By

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A mis padres, Verónica y Amado, quienes me han dado apoyo incondicional en todas las etapas de mi vida, por creer plenamente en mí y por darme constante ánimo.

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RESUMEN

TITULO:

Diseño de un sistema de adquisición de datos para actividades radioastronómicas

AUTOR:[1] Adán Torralba Ayance

PALABRAS CLAVE: Detectores de Radiación, Circuitos electrónicos de lectura, Fotomultiplicadores de Silicio, Preamplificador, Circuitos integrados de aplicación específica.

DESCRIPCIÓN:

Un detector de radiación es un sistema complejo cuyo principal objetivo es extraer información de tiempo y energía de la radiación incidente y convertirla en información digital para poder ser almacenada y analizada en el futuro. Los circuitos electrónicos que lo componen se llaman circuitos electrónicos de lectura, y están construidos de múltiples bloques más pequeños. El preamplificador es el primer bloque que directamente interactúa con el sensor, por lo tanto, requiere acondicionar la señal del sensor, amplificarla, y enviarla a las siguientes etapas, este circuito define la arquitectura de los circuitos electrónicos de lectura y norman en gran medida parte del desempeño de todo el sistema.

Los sensores de tipo Fotomultiplicadores de Silicio (SiPM por sus siglas en inglés) prometen ser una tecnología consolidada y económica para una amplia cantidad de aplicaciones que requieran la detección de bajos niveles de luz. No obstante, debido a sus características particulares, las arquitecturas de circuitos electrónicos de lectura tradicionales ofrecen poco desempeño cuando son aplicados a sensores de tipo SiPM. Actualmente la metodología de diseño para detectores de radiación encontrados en la literatura está basada en estas arquitecturas tradicionales.

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Con esto en mente, este trabajo de tesis introduce una metodología de diseño especialmente enfocada en la síntesis y diseño de circuitos electrónicos de lectura implementados en tecnología CMOS y basados en sensores de tipo SIPM. Dado que la influencia del preamplificador en la arquitectura y el desempeño de estos circuitos de lectura, el diseño, síntesis y evaluación del desempeño de un preamplificador es utilizado como vehículo en el desarrollo del trabajo.

SUMMARY

TITLE:

Design of a data acquisition system for radioastronomical activities

AUTHOR:[2] Adán Torralba Ayance

KEY WORDS: Radiation detectors, Front-end electronics, Silicon Photomultipliers, Preamplifier, Application Specific Integrated Circuit.

DESCRIPTION:

A radiation detector is a complex system whose main objective is to extract the timing and energy information from the incident radiation and convert it to a steam of data for storage and future analysis. The electronic circuitry that composes it, called the front-end electronics, is built out of multiple smaller blocks. The preamplifier is the first block that directly interacts with the sensor therefore it requires to condition the sensor signal, amplify it and send it to the following stages, this circuit defines the architecture of the front-end electronics and rules a great part of the performance of the whole system.

Silicon Photomultipliers (SiPM) sensors promise a well consolidated and cost effective technology for a large range of applications that required the detection of low light levels, however given their peculiar characteristics, traditional readout electronics architectures offer poor performance when coupled to SiPM sensors. Currently the design methodology for radiation detectors found in the literature are based on those traditional architectures.

With this in mind this thesis work introduces a methodology specially focused in the synthesis and design of CMOS front-end electronics based on SiPM sensors. Given the influence of the preamplifier in the architecture and performance of the front-end

[2]INAOE. Electronics Department. Integrated circuit design.

electronics, the design, synthesis, and evaluation of the performance of a preamplifier is used as a vehicle in the development of this work.

Nomenclature

$\overline{V_{n,in}^2}$ Equivalent input voltage noise white power spectral density

$\overline{V_{n,out}^2}$ Equivalent output voltage noise white power spectral density

σ_t Time Jitter

σ_V Output Voltage Noise in RMS

C_F, C_S Fast and Slow equivalent capacitance

G_{FE} Gain of a front-end

Q_F, Q_S Fast and Slow equivalent charge

Q_n Charge Resolution

$Q_{1\mu cell}$ Charge generated from a single fired microcell

ADC Analog-to-Digital Converter

BW Bandwidth

CAD Computer-Assisted Design

CB Current Buffer

CSA Charge Sensitive Amplifier

DDA Differential Difference Amplifier

DR Dynamic Range

ECR Event Count Rate

EI Event Interval

ENC Equivalent Noise Charge

FVFCS Flipped Voltage Follower Current Sensor

FWHM Full Width Half Maximum

GBW Gain-Bandwidth product

GM-APD Geiger-mode avalanche photodiodes

IRN Input-Referred Noise

LA Limiting Amplifier

NMR Noise-to-Microcell Ratio

PE Pile-Up Error

PET Positron Emission Tomography

PMT Photomultipling tubes

RMS Root Mean Square

SPAD Single-Photon Avalanche Diodes

TDC Time-to-Digital Converter

ToF Time-of-Flight

VA Voltage Amplifier

VGA Variable Gain Amplifier

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Chapter 1

Introduction

1.1 Background

Some of the main objectives of the radiation detector technology in the last decades, is the detection of unique photons over a great variety of wavelengths, measure with great precision its arrival time and reconstruct with great accuracy its special path [1]. That implementation is specially required in Positron Emission Tomography (PET) systems [2], for cancer detection, spectroscopy, research and detection of materials and particles, astronomical telescopes [3], Positron Emission Mammography (PEM), as well as Laser Imaging Detection and Ranging (LiDAR) [4] to be used in optical radars applied to autonomous vehicles , tridimensional and topographical aerial scanners. Currently these tasks have not been totally solved using the most recent commercial imaging sensors [1].

To detect high-energy particles[1] or to detect subatomic particles like the ones used in PET systems for cancer topographies, particle accelerators, neutron detection systems used to identify radioactivity, scintillator materials are required [5]. When high energy photons react with the electrons inside the scintillator material, those increment its energetic level, forcing the electron to release the excess of energy by means of flashes of visible light, this process is called photoluminescence. These flashes normally contain

[1] High-energy particles have a is much higher than the bandgap $E_{ph} \gg E_g$ of the sensor material. For example, high energy X-rays have $E_{ph} > 10keV$ and the indirect bandgap of silicon is $E_g = 1.11eV$ [1].

a reduced number of photons and have a duration of some nanoseconds. On the other hand when a charged subatomic particle such as protons or free electrons pass through a medium of a certain refractive index in which its speed exceeds the speed of light passing thought that medium, the molecules where the particle passed begin to polarize in an asymmetrical manner, to compensate that asymmetry, small flashes of light with a duration of a few nanoseconds is generated, this visible light is called the Cherenkov radiation [6].

Radiation detector specialized on these tasks are fabricated in a modular way with the objective of simplifying repairs, maintenance labor, and in case of necessity, scale the size of the system. Furthermore, this radiation detectors are developed using Photomultipling tubes (PMT) sensors which require from hundred to thousand volts to bias, are physically voluminous, fragile and often require cooling [7]. One promising alternative is the use of Silicon Photomultiplier sensors (SiPM) [8], it consist of an array of thousand of Geiger-mode avalanche photodiodes (GM-APD) connected in parallel, this sensors require a low bias voltage, tens of volts, are compact, light and immune to magnetic fields.

1.1.1 Motivation

To fully exploit the advantageous characteristics of the SiPM sensors a suitable readout front-end electronics is required. Usually the front-end electronics are realized in the form of Application-Specific Integrated Circuits (ASICs) fabricated in deep-submicron standard CMOS technologies and whose technological advances have allow the fabrication of complete systems on a chip by combining both analog and digital functions at an affordable cost.

The classical multichannel readout architecture based on the direct charge integration usually employed in radiation detectors and implemented in CMOS technology offer poor performance when applied to the SiPM sensors due to the large equivalent capacitance and large charge amplification factor that this kind of sensors offer. However most of the design methodology for radiation detectors found in the literature is

based in this architecture.

Even thought a large amount of information about the working mechanism, characterization of the SiPM sensor and front-end electronics implementations are found in papers published in specialized journals, a methodology specially focused in the design and synthesis of front-end electronics for SiPM sensors implemented in standard CMOS technologies is absent. The exposed situation increases substantially the initial difficulty to design the required electronics circuits because the interested individual would require to perform the time consuming task of investigate, analyze and generate its own methodology before even starting the electronic design.

1.1.2 Objectives

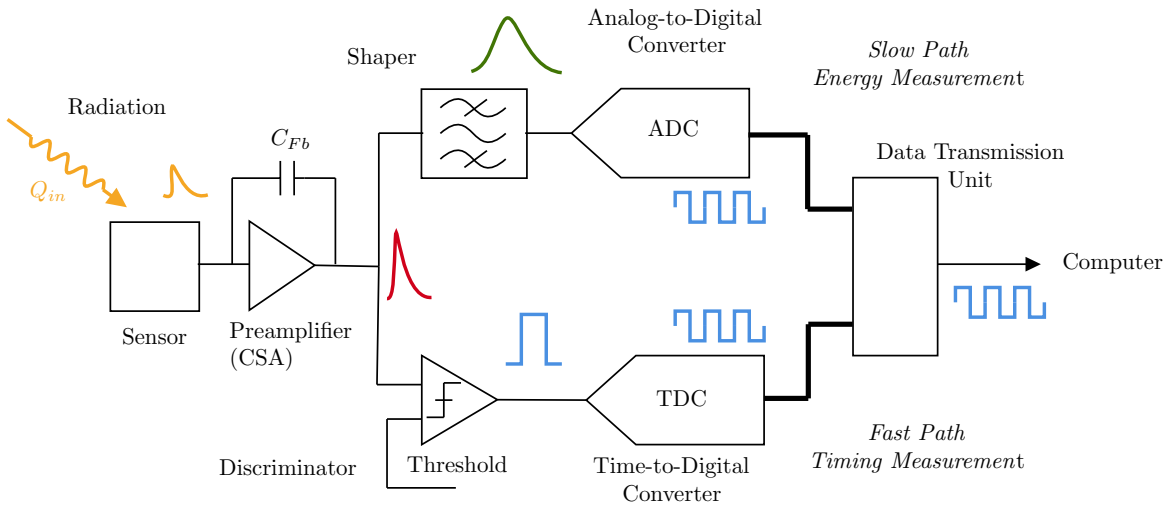
The general objective of this thesis is to generate a design methodology specially focused in the development of front-end electronics for SiPM sensors and to analyze, evaluate and select the optimal readout architecture according to the design specifications. As a crucial element that defines the architecture and the performance of a front-end electronics for radiation detectors, the design, synthesis and evaluation of the performance of a preamplifier is used as a vehicle.

To accomplish this purpose, the following specific objectives were established:

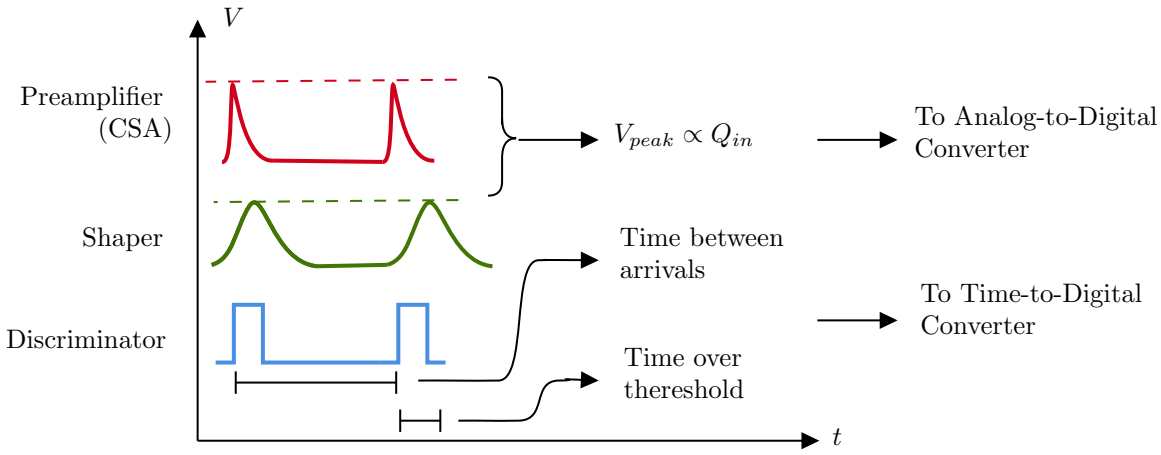
1. Investigate the fundamental blocks that compose a front-end electronics for radiation detectors, their relationship with the preamplifier and the key parameters that evaluate their performance.
2. Study the principle of operation of the Silicon Photomultiplier sensor and its equivalent electrical model.
3. Analyze the theoretical performance of the existing readout architectures for front-end electronics for SiPM sensors and correlate the studied information with the state of the art.
4. Propose a preamplifier topology from each of the readout architectures based on the study of the state of the art.

5. Design the preamplifiers proposals using the information from the key parameters of the radiation detectors, the theoretical performance of the readout architecture and the circuit equations.

6. Evaluate and validate the performance of the preamplifiers compared to the state of the art with the aid of simulations.



(a) Block diagram of a generic frond-end electronics.



(b) Charge and energy measurements in a radiation detector .

Figure 1.1: Generic Front-end electronics of a Radiation Detector.

1.2 Detector Systems Overview

A detector is a device capable to *detect* or recognize a physical phenomenon, like a smoke, gas or heat detector, a radiation detector, as its name implies, is used to measure nuclear, electromagnetic, or light radiation. All radiation detectors have the objective to extract the timing and energy information from the incident radiation and convert it to a stream of data for storage an analysis [9].

The circuitry designed for a radiation detector is called a front-end electronics and its composed of smaller blocks with specific functions [10], as visualized in Figure 1.1(a). In order to detect as many events as possible a radiation detector may have several *channels*, that is, independent sensors and front-end electronics constructed each one in parallel. In general a frond-end electronics for radiation detectors are build by the following blocks:

- **Sensor:** It converts the energy from a particle or photon to an small electrical signal.

- **Preamplifier:** The first stage that is directly connected to the sensor is called the preamplifier. Usually the preamplifier is implemented as a Charge Sensitive Amplifier (CSA) [2], so the output voltage is proportional to the charge of the sensor, illustrated in 1.1(b). The magnitude of the amplified signal is altered by statistical fluctuations caused by electrical noise, therefore the preamplifier must be designed to minimize that effect.

- **Discriminator:** Discriminates or validates an event according to the trigger pulse. When amplified signal exceeds a threshold, shown in Figure 1.1(b), it outputs a trigger pulse.

- **Time-to-Digital Converter (TDC) :** Measures the time between arrivals of

[2]It consists of a negative-feedback amplifier with a capacitor in its feedback loop C_{Fb}, since the sensor injects or sinks current, the output voltage is proportional to the integral of the current, that is the charge.

the pulses and the time over the selected threshold and translate it into a digital word.

- **Sharper** Since the energy of a signal is distributed in the frequency domain as a function of its Fourier transform, the noise and the signal spectrum differ each other, so to increase the signal-to-noise ratio, a filter is used to fit the input signal frequency components while attenuating the noise. By changing the frequency response unavoidably changes its time response, or the *pulse shape*. Increasing the signal-to-noise ratio commonly reduces the bandwidth and increases the duration of the pulse.

- **Analog-to-Digital Converter (ADC):** Translates the amplitude of the shaped signal into a discrete steps, each corresponding an individual bit code.

- **Data Transmission Unit:** Circuitry dedicated to transfer the digital data to a computer.

From Figure 1.1(a), it is observed that the preamplifier has two main tasks. Firstly, it needs to interact directly with the sensor, the pulse duration and its peak value are highly affected by the coupling of the sensor capacitance and the preamplifier input impedance, for this reason a correct coupling is required to accomplish the design specifications [11]. Secondly, it requires high speed, low noise, and a large gain value since the Sharper and the Discriminator uses its output signal to measure Energy and Timing respectively.

1.3 Key Parameters in Front-End Electronics

1.3.1 Peaking Time

The detector signals are very fast and preserving their shape in high fidelity would require circuits with a very large bandwidth and a huge power consumption. This signals are so fast that the current pulse from a sensor is modeled as a Dirac-delta.

Interestingly, the important information can be indeed extracted without keeping the original sensor shape [9].

One of the main key parameters in front-end electronics is the time required for the signal to swing from the baseline to its maximum value, physicist call it the peaking time and is a synonym of the therm rising time used by designers. Since the original sensor shape is so fast, the peaking time will be limited by the speed of the preamplifier.

1.3.2 Gain of the Front-End

To calculate the charge of an incident particle, the generated photocurrent needs to be integrated, the CSA preamplifier performs this functions and delivers a voltage proportional to the incident charge, as seen in figure 1.1(b) the output voltage of the front-end electronics is obtained form the CSA or the Shaper.

Unlike the gain of an amplifier A_o where is defined by designers as the amplification factor between the input and the output, the gain of a front-end G_{FE} is given by the ratio between the peak output voltage V_{peak} and the input charge or the number of the incident electrons [10], as shown in equation 1.1.

$$G_{FE} = \frac{V_{peak}}{Q_{in}} = \frac{V_{peak}}{N_{electrons}} \tag{1.1}$$

For example if the system is fed by a charge of 1fC, and the output voltage is $50mV$, the gain is $50mV/fC$. Additionally if 1fC is the charge of 1000 electrons, then the gain of the front-end is $50\mu V/electron$. The gain of a system should be selected so that the maximum signal of interest sets the amplifier at the border of saturation.

Once calculated the gain of a front-end G_{FE}, the input charge can be calculated from a signal with an arbitrary peak voltage with equation 1.2.

$$Q_{in} = \frac{V_{peak}}{G_{FE}} \tag{1.2}$$

In the same system, if a signal with a peak voltage of 1V is measured, it would have an equivalent input charge of $30fC$ or 20,000 electrons

1.3.3 Noise

Noise is a phenomenon caused by small fluctuations of the analog signal within the components themselves [12], it has its origins in the fact that mobile chargers in electronic devices are in finite numbers and move at finite speed, when the number of carriers or its speed changes, it causes a fluctuation of the voltage and current inside a circuit. Noise is a random process, therefore, to estimate its strength, its standard deviation is used, the quantity obtained is called the RMS (Root Mean Square) output noise.

In analog design, the Input-Referred Noise is a fictitious quantity unit where the output RMS noise $V_{n,rms}$ is divided by the circuit amplification factor A_o, this measurement indicates how much of the input signal is corrupted by the noise of the circuit.

In radiation detectors, the noise is usually given as an Equivalent Noise Charge (ENC) refereed to the amplifier input [9], that is the output RMS noise is divided by the gain of the front end , so:

$$ENC = \frac{V_{n,rms}}{G_{FE}} \tag{1.3}$$

For instance, a system with a gain of $50mV/fC$ and an rms output voltage noise of 1mV would have a ENC of $0.02fC$, that is 20 electrons. Similar to the Input-Refereed Noise, the ENC indicates the quantity of charge or electrons that degrade the input signal.

1.3.4 Dynamic Range

In analog design, Dynamic Range (DR) is defined as the maximum allowable voltage swing divided by the total noise of the band of interest [13] . Similarly, in front-end electronics the DR is the ratio between the maximum output voltage which the system still maintains its linear proportionality (between the input and output signal) and the rms noise level at the output [10]. Interestingly, with mathematical manipulation, the DR also can be calculated with the ratio between the maximum input charge and the ENC.

$$DR_{FE} = \frac{V_{peak,max}}{V_{n,rms}} = \frac{Q_{in,max}}{ENC} \tag{1.4}$$

As a metric to evaluate the point where the output peak voltage signal loses its linear proportionality, the 1dB compression ratio of was selected. Figure 1.2 shows a plot of the incident charge Q_{in} against the peak voltage of the amplifier V_{peak} which is proportional to the input charge.

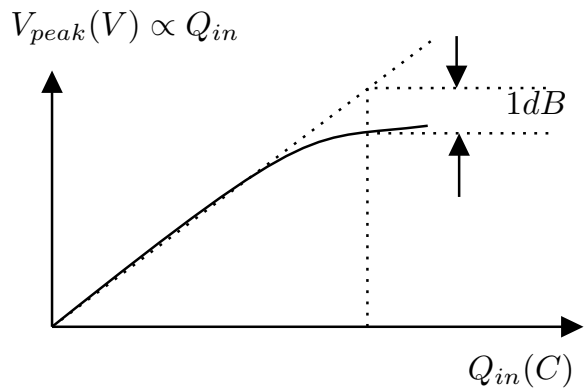
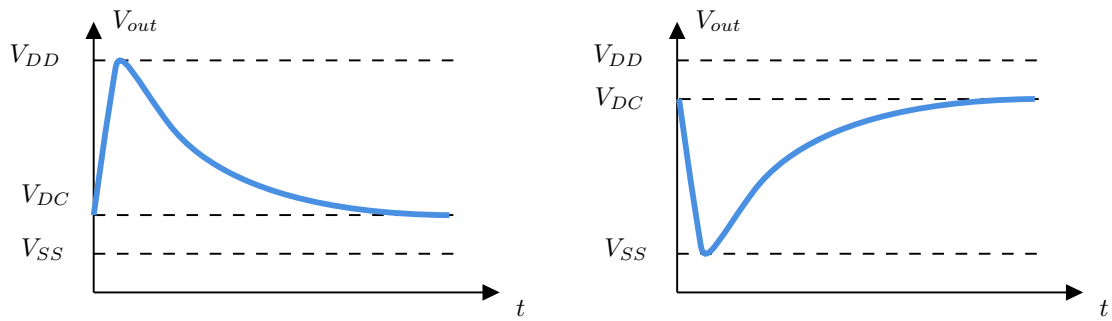


Figure 1.2: Compression ratio of the peak output voltage against the input charge.

Following the former examples, if the maximum peak voltage of the system is 1V, then the dynamic range is $DR = 1000$ or 60dB.

1.3.5 Signal Polarity

In analog design, the direct current (DC) level of an amplifier is generally selected in the middle of the positive and negative rails with the objective to give a proper headroom for sinusoidal signals. In radiation detectors, since the sensors only injects or sinks current, its output signal is unipolar and would only move upwards or downwards but not both, so to maximize the linear dynamic range, the DC level of the preamplifier should be selected closer to the positive or negative rails according to the specific sensor [10] as shown in Figure 1.3.



(a) DC baseline closer to V_{SS}.

(b) DC baseline closer to V_{DD}

Figure 1.3: DC baseline selection to increase input dynamic range.

1.3.6 Charge Resolution

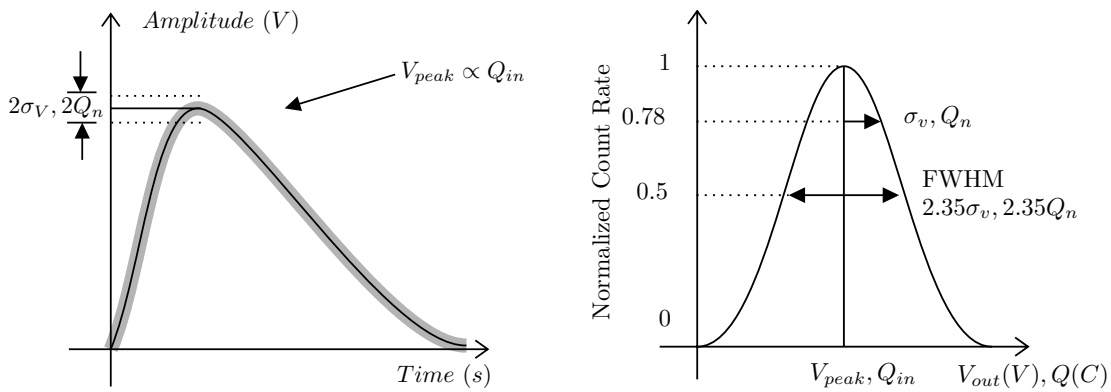
The minimum detectable signal is limited by the noise of the electronics. But noise not only affects the Dynamic Range, it also introduces fluctuations that alter the signal peak value of the Preamplifier or Shaper, as seen in Figure 1.4(a), and hence the charge measurement as expressed in Equation 1.2 .

If a stream of photons arrive to the system and the output of the Preamplifier or Shaper is observed, the peak value would have a Gaussian distribution whose standard deviation equals the RMS noise level Q_n, illustrated in Figure 1.4(b). The value Q_n is known as the Charge Resolution and quantifies the level of uncertainty in a charge measurement [9].

The width of the Gaussian distribution, is often expressed as the Full Width Half Maximum (FWHM) , which is 2.35 times the standard deviation. Physicist prefer to use the terminology *Count Rate* to reefer to the pulse rate or number of events used in the measurement.

1.3.7 Time Resolution

In radiation detectors, events must be ordered in time with a level of accuracy depending on the application. In high timing resolution applications, such as Time-of-Flight (ToF) where a particle is identified by the time it takes to travel a known distance, or LiDAR at which time measurements are used calculate a space coordinate, the required



(a) Fluctuations in a signal peak value caused by the electronic noise.

(b) Gaussian distribution of the Charge measurement.

Figure 1.4: Charge Variation and calculation of the charge resolution.

time resolution can be as low as 100ps RMS [14]. In contrast, in accumulative events applications where the system uses a window time, timing is not a real concern [10].

From Figure 1.1(a), it can be observed that the output of the preamplifier is connected to a comparator. When the amplified signal crosses a threshold value, the comparator fires a trigger pulse and the Time-to-Digital converter or similar circuitry starts to measure the time it takes until a new event arrives. If identical pulses are sent to the system periodically and the output of the comparator is observed, exemplified in Figure 1.5, the transition point moves back and forth in time around its average value. The random variations from the ideal position experienced by the output of the comparator are an effect called *Jitter* [13], and are caused by the noise present at the preamplifier output [10]. In order to reduce the uncertainty in timing measurements, the *Jitter* should be minimized.

To better understand this behavior and its origins, consider the rising edge of the preamplifier output signal, it can be approximated with a first order Taylor expansion like equation 1.5 where t_0 is the time when the signal crosses the threshold value, visualized in figure 1.6(a).

$$V_{out}(t) = V_{out}(t_0) + \left.\frac{dV}{dt}\right|_{t=t_0} (t - t_0) \tag{1.5}$$

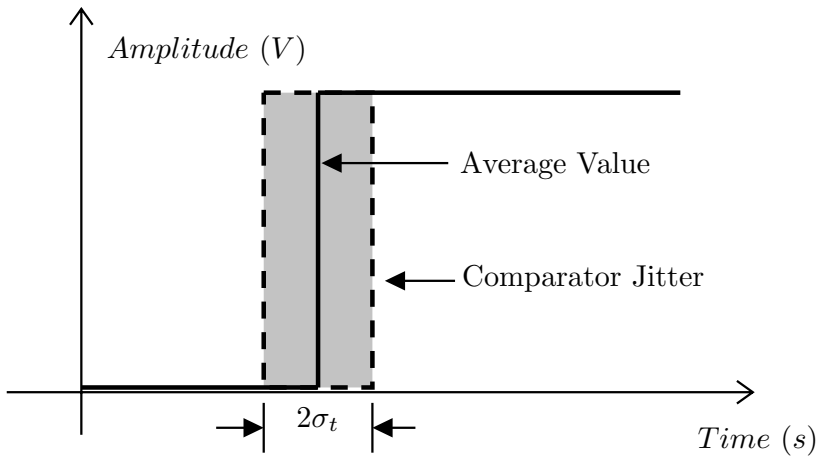
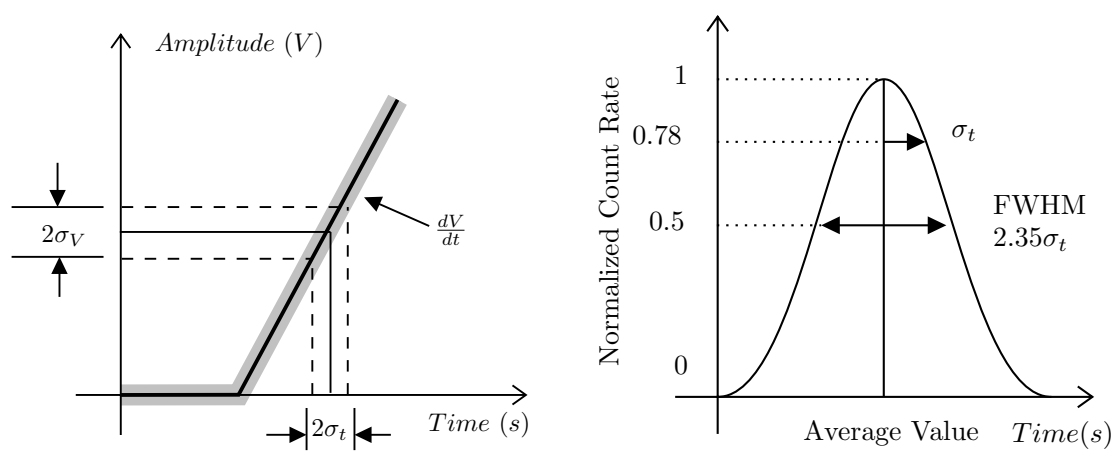


Figure 1.5: Visualization of the comparator Jitter caused by the noise of the preamplifier.

The slope of the preamplifier output signal is represented by the coefficient $(dV/dt)_{t=t_0}$, now when a signal is about to cross the threshold value, the noise will bring it up or down by an amount ΔV, as a consequence the comparator will switch earlier or later than the ideal value.



(a) Fluctuations in a signal amplitude crossing a thereshold translate into timming fluctuations.

(b) Gaussian distribution of the timming jitter.

Figure 1.6: Timming jitter.

The relationship between the voltage and time uncertainty is

$$\Delta V_{out} = \left.\frac{dV}{dt}\right|_{t=t_0} \Delta t \tag{1.6}$$

Since the noise is a random process, the noise standard deviation of the preamplifier output is assumed as a measure of ΔV, therefore.

$$\sigma_V = \left.\frac{dV}{dt}\right|_{t=t_0} \sigma_t \tag{1.7}$$

And finally the timing jitter is expressed as [9]:

$$\sigma_t = \frac{\sigma_V}{\left.\frac{dV}{dt}\right|_{t=t_0}} \tag{1.8}$$

Analyzing equation 1.8, the timing jitter is a ratio between the preamplifier RMS output noise σ_t and the signal slope around the threshold, in general the jitter is inversely proportional to the square root of bandwidth of the amplifier [10], so faster systems have better timing performance.

If identical pulses arrive periodically to the system and the time jitter is measured it would have a Gaussian distribution, illustrated in Figure 1.6(b). Just like the charge resolution, the timing jitter has a Gaussian distribution caused by the random nature of noise and its often expressed as the Full Width Half Maximum (FWHM).

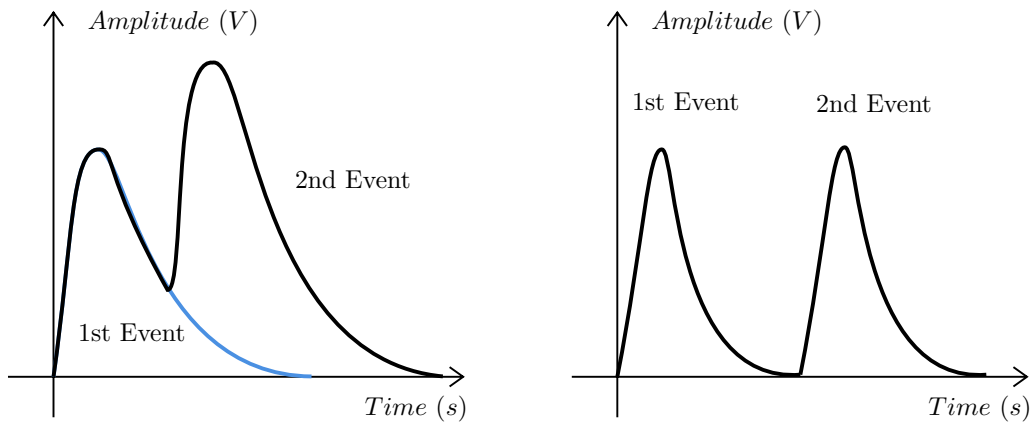
1.3.8 Pile-Up

The preamplifier output must return to its baseline before a new pulse can be processed, otherwise both signals will *Pile-up*, as shown in Figure 1.7.

Usually, the arrivals of the events in a radiation detector follows a Poisson distribution [10]:

$$P(k) = \frac{\lambda^k e^{-\lambda}}{k!}, \qquad \lambda = \frac{Pulse\ Duration}{Events\ Interval} \tag{1.9}$$

Equation 1.9 shows the probability function distribution of observing k events in a process which has a mean value of λ. As an example consider the case where a pulse has a duration of 100ns, and the event rate is 1MHz, so the average interval between events is $1\mu s$. In order to avoid Pile-Up errors, is required that no other pulses arrive, the probability of this to happen is obtained by selecting $k = 0$ and $\lambda = 100ns/1\mu s = 0.1$.



(a) Amplitude Pile-up occurs when two pulses overlap.

(b) Reducing the pulse duration allows the first pulse to return to the baseline before the second pulse arrives.

Figure 1.7: Pile-up effects in a radiation detector.

In this case 90% of the events will arrive with out Pile-Up errors and only the 10% of the pulses will overlap.

1.4 Silicon Photomultiplier Sensors (SiPM)

SiPMs are the most promising alternative to PMT technology because of its low voltage operation, low power consumption, insensitivity to magnetic fields and compactness [15]. SiPMs are good devices for light detection from single to several thousand photons, specially when fast timing resolution is required.

This sensors are widely used in LiDAR [16], optical spectroscopy [17], fluorescence light detection [18], quantum physics [19], quantum informatics [20], oncological diagnosis time of flight (ToF) in positron emission tomography (PET) [21], and when coupled to a scintillator, the SiPM senses Cherenkov light with great time precision [22]. The SiPM is a promising sensor technology that have entered in many fields of scientific research, engineering, and medical applications. Due to its great application potential the use of this sensor is selected in the development of this work.

1.4.1 From SPAD to SiPM

One alternative to substitute the photomultiplier tubes (PMT) technology to a compact, integrated, affordable and reliable semiconductor solution was the introduction to the Single-Photon Avalanche Diodes (SPAD) by Cova et al in 1981 [23]. The SPAD, as observed in Figure 1.8(a) is composed of a reversed bias Geiger-mode Avalanche Photodiode (GM-APD), and a stop resistor, also called a *quenching* resistor R_q.

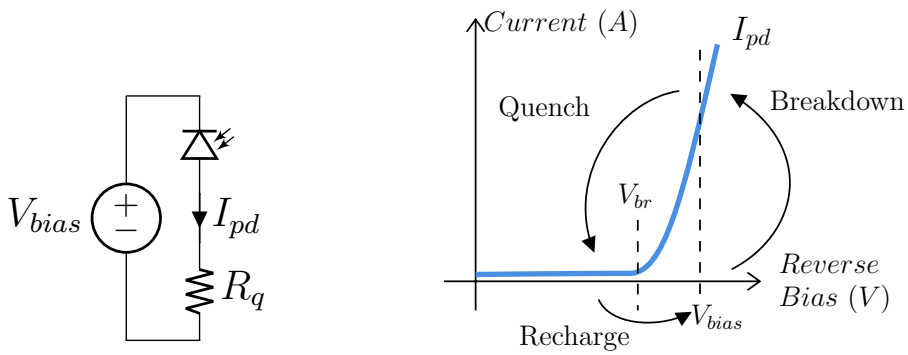
The operation of a SPAD is divided into three phases visualized in Figure 1.8(b) [24].

1. **Breakdown:** When a photon hits the p-n junction of the photodiode, a photoelectron is generated, given that the bias voltage of the GM-APD is high, the photoelectron is accelerated very quickly until it strikes another electron, the second electron is then released from the atom and strikes with a third one and so on, this creates an avalanche process. As a result, the silicon breaks down and become conductive, leading into a current flow. Like the PMT, a single photoelectron is multiplied several times until the charge reaches the anode of the photodiode.

2. **Quench:** Once the avalanche process has started the photodiode is blinded and cannot detect further photoelectrons. To settle this issue, the quenching resistor is connected in series to the photodiode, as the current of the photodiode increases, so does the voltage across the resistor, as a result the voltage across the photodiode decreases bellow the breakdown voltage V_{br}.

3. **Recharge:** When the avalanche process is stopped, the voltage across the GM-APD is increased to its bias level V_{bias} and the SPAD is ready to detect new photons.

The main limitations of the SPAD are [15]: the lack of information of the photon flux,(because the sensor functions only as a binary photon detector, that is, no matter the amount of incident photons, the output signal is identical for all the cases) and the extended period of blindness (from the moment when a photon reaches the photodiode to the time the avalanche process stops, the sensor is not capable to detect new events).

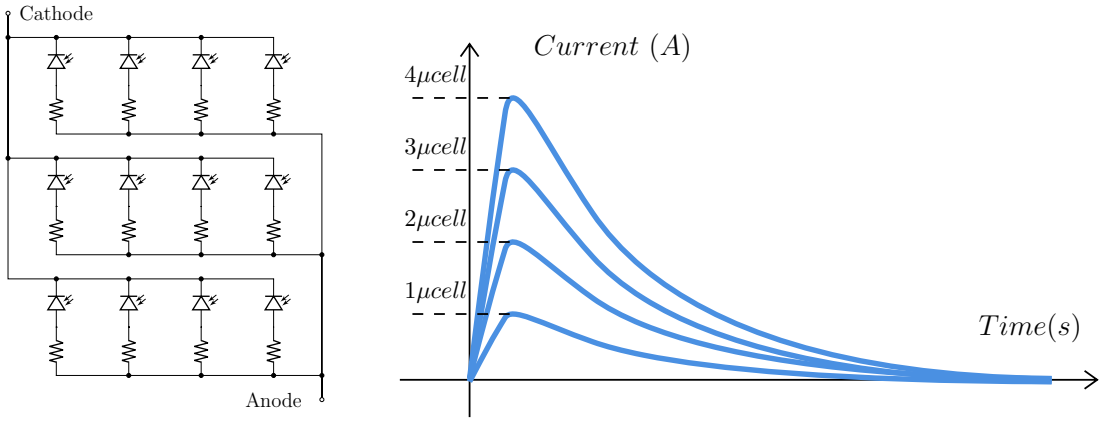


(a) Equivalent circuit.

(b) SPAD cicle of operation.

Figure 1.8: Single photon avalanche diode (SPAD).

To overcome the blindness period and the absence of information of magnitude information of the SPAD, an array of small SPADs, called microcells (μcell), connected in parallel and distributed in a square matrix shape, illustrated at 1.9(a), was proposed in late 1990s by Russian scientists Z. Sadygov and V.M. Golovin [25].



(a) A SiPM is composed of individual SPADs connected in parallel.

(b) Quasi-analog or discrete output signal of the SiPM.

Figure 1.9: Silicon Photomultiplier (SiPM).

The area of each microcell is kept sufficiency small (in the order of $50\mu m \times 50\mu m$), so that the probability of having more than one photon arriving simultaneously on the same photodiode is small, thus reducing the possibility of a blindness period [10]. Since the microcells are connected in parallel, the firing of one photodiode does not affect

its neighbors, resulting in a quasi-analog or discrete output signal whose amplitude is proportional to the number of incident photons [10], exemplified at Figure 1.9(b).

1.4.2 Biasing and readout

Figure 1.10 shows a typical configuration used to bias a SiPM sensor. The Geiger-mode avalanche photodiodes that compose the microcells of the SiPM require to be reverse biased. The minimum reverse bias voltage that assures the operation of the microcells is called the breakdown voltage V_{BD}, typically an overvoltage V_{OV} is applied to the sensor, this assures the proper operation of the SiPM and directly affects its Internal Charge Amplification Factor also called the *Gain of the SiPM* G_{SiPM} [8].

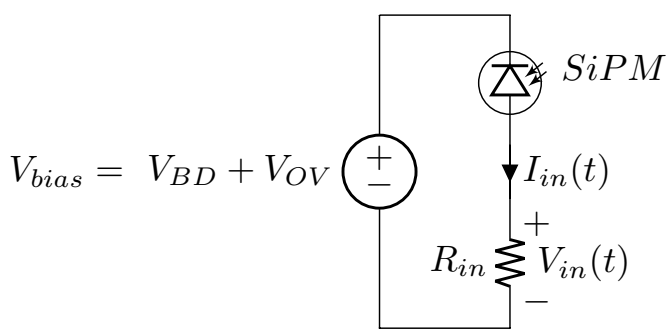


Figure 1.10: Biasing and readout of the SiPM.

The photocurrent of the SiPM I_{in} is typically converted into voltage V_{in} with the aid of a load resistor, in radiation detectors this resistor is called the *Input Resistor* R_{in} because is generally the first element of a front-end electronics in contact with the sensor [26].

1.4.3 Signal Shape

A typical output signal from a SiPM is showed in Figure. 1.11. In the beginning of an event, the signal shows a very fast rising that is defined by the photodiode resistance and parasitic capacitances forming a time constant τ_d. Once the peak is reached, the discharge phase is separated into a fast τ_F an slow τ_S time constants [8], [11] An detailed explanation of each time constant is made in Chapter 2 and appendix A.

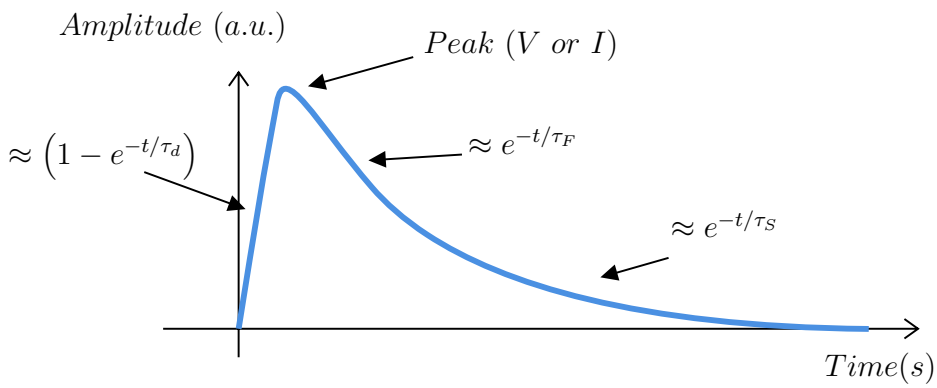


Figure 1.11: SiPM signal shape, not in scale.

1.4.4 Internal Charge Amplification Factor

To calculate the total charge generated from a SiPM and estimate the number of incident photons its necessary to understand one of its main characteristics, that is the Internal Charge Amplification Factor, also called the *Gain of the SiPM*.

The Gain of the SiPM G_{SiPM} is defined as the number of charge carriers created during an avalanche discharge of a microcell [8], that means, the charge generated from a single photoelectron, or a single fired microcell, will be increased by the internal charge amplification factor of the SiPM, as shown in Equation 1.10.

$$Q_{1\mu cell} = q_e G_{SiPM} \tag{1.10}$$

Two main factors affect G_{SiPM} [8]. First, the internal capacitance of the micocell $C_{\mu cell}$ who depends on the fabrication process and varies from sensor to sensor. And second, the overvoltage applied to bias the SiPM V_{OV} which can be selected from a range defined by the manufacturer.

$$G_{SiPM} = C_{\mu cell} V_{OV} = C_{\mu cell}(V_{bias} - V_{BD}) \tag{1.11}$$

The total charge generated form the avalanche process is obtained by integrating the SiPM photocurrent [8], since a SiPM is an array of microcells connected in parallel, the total output charge of the sensor is also the charge form a single microcell multiplied by the total number of fired microcells N_f.

$$Q_{SiPM} = \int I_{in}(t)dt = \frac{\int V_{in}(t)dt}{R_{in}} = N_f Q_{1\mu cell} \tag{1.12}$$

If the charge from a single fired microcell $Q_{1\mu cell}$ and the total charge is known Q_{SiPM}, the number of incident photons or fired micocells can be calculated with equation 1.13.

$$N_f = \frac{\int I_{in}(t)dt}{Q_{1\mu cell}} = \frac{\int V_{in}(t)dt}{R_{in}Q_{1\mu cell}} = \frac{Q_{SiPM}}{Q_{1\mu cell}} = \frac{Q_{SiPM}}{q_e G_{SiPM}} \tag{1.13}$$

Equations 1.12 and 1.13 offer an interesting observation, typically a SiPM has a number of microcells ranging from a hundred to a few thousand, given that the output charge of the sensor varies linearly with the amount of fired microcells, the preamplifier should be designed with a very large input Dynamic Range to support from very small to huge current signals [3].

1.4.5 Electrical Model

An effective electrical model with accurate parameters, capable to reproduce the signals generated form a SiPM sensor when coupled to a preamplifier is key when a front-electronic for radiation detector is designed and later evaluated with trustworthy simulations.

An accurate model of a SiPM coupled to a generic front-end electronics with input impedance R_{in} is shown in Figure 1.12 [26]. As stated before, this sensor contains a total number of microcells N_{tot}, in an event only a fraction of microcells is fired N_f, while the others remain inactive or passive $N_p = N_{tot} - N_f$. In this model the C_d is the capacitance of the avalanche photodiode, R_q is the quenching resistor and C_q is its parasitic capacitance, and C_g is the parasitic grid capacitance as a result of the connection of all the microcells.

[3] It must be noticed that the peak photocurrent value of a single fired microcell, in spite of having an internal charge amplification, is on the order of a few μA, considering that a SiPM has a hundred up to a thousand of microcells connected in parallel, the output current of all the fired microcells is on the order of tens of mA [8].

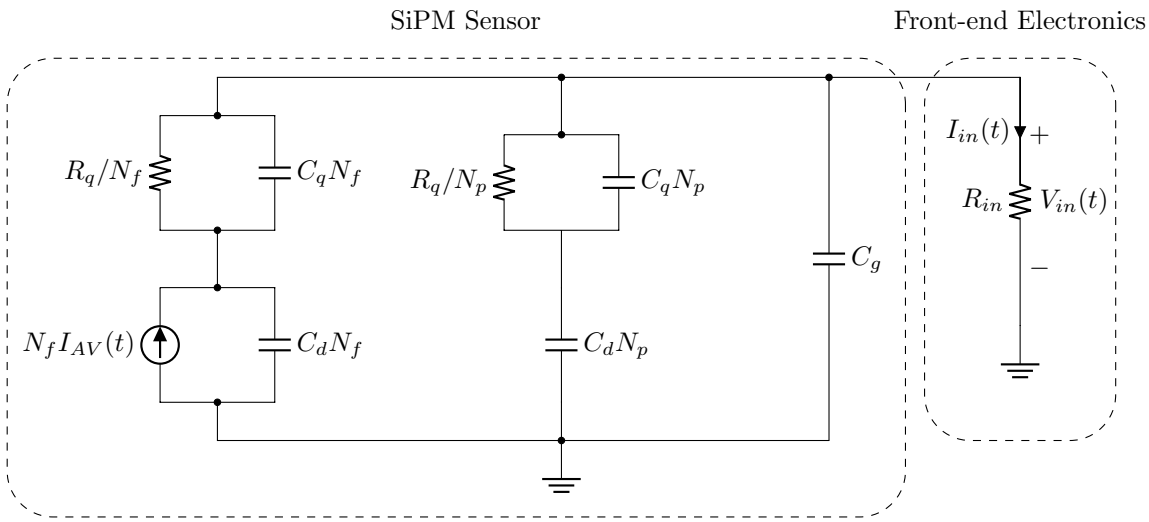


Figure 1.12: SiPM Electrical Model coupled to a generic front-end electronics.

The avalanche event is simulated with a current source $I_{AV}(t)$ with a proper shape, two options are proposed and should be chosen according to the design requirements.

If simulating the proper rising edge of the SiPM output pulse is of great interest, an exponential current source should be used [27].

$$I_{AV}(t) = I_0 e^{-t/\tau_d} \tag{1.14}$$

Where I_0 represents the current peak value given by the charge generated from a single microcell over the rising time constant τ_d.

$$I_0 = \frac{Q_{1\mu cell}}{\tau_d} \tag{1.15}$$

Generally, the rising edge of a SiPM signal is so fast that replicating its shape is not a great concern in practical applications [10], in this case the current source is replaced with a sort of Delta-Dirac pulse.

$$I_{AV}(t) = Q_{1\mu cell}\delta(t) \tag{1.16}$$

If the simulation of multiple events is required, thanks to the superposition principle, all the current sources that model the avalanche current of each fired microcell can be reduced to only one current source $I_{AV}(t)$, which generates all the Dirac-deltas

associated to each fired microcell triggered by M number of photons according to their arrival times $t_i, i = 1, 2, 3...M$ [26].

$$I_{AV}(t) = Q_{1\mu cell} \sum_{i=1}^{M} \delta(t - t_i) \tag{1.17}$$

The parameter extraction for a SiPM sensor is a complex task that requires extensive laboratory measurements, solving elaborate equations systems and an comprehensive study of its fabrication process [28] [29], elements which are outside of the scope of this thesis. Therefore, in this work the extracted and well-documented parameters of the SiPM Hamamatsu S10931-050P [26], a typical SiPM with 3600 microcells $50 \times 50\mu m$ with a total active area of $3 \times 3mm$, are used in the design of the proposed preamplifier.

(a) Extracted Electrical Parameters.

Parameter	**Values**
Q_{1ph}	$160fC$
R_d	1 kΩ
R_q	49.6 kΩ
C_d	80.14 fF
C_q	15.49 fF
C_g	18.24 pF
N_{tot}	3600

(b) Calculated Dynamic Parameters.

Parameter	**Values**
τ_F	$C_F \times R_{in}$
τ_S	$\tau_r + C_S \times R_{in}$
τ_d	95.6 ps
τ_r	3.24 ns
I_0	1.67mA
C_F	64.9 pF
C_S	306.7 pF

Table 1.1: Electrical and Dynamic Parameters of the SiPM sensor Hamamatsu S10931-050P.

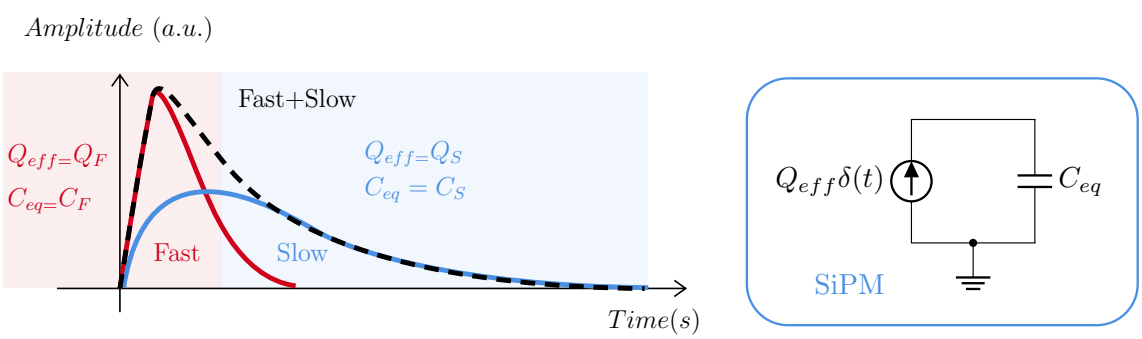
The extracted electrical parameters are shown in Table 1.0(a) [26], from this information, and equations found in appendix A, the dynamic parameters, the ones that define the shape of the signal, are calculated and displayed in Table1.0(b).

1.4.6 Simplified Electrical Model

In section 1.4.5 the complete model of the SiPM was presented. However, for hand calculations is preferable to simplify the circuit as much as possible.

The SiPM signal is actually constructed out of the superposition of a Fast and a Slow components, see Figure 1.13(a), each one defines the characteristic shape of the signal [11]. The Fast component dominates the leading edge of the current pulse produced by the sensor, and is relevant for timing measurements and the Slow component dominates the long tale of the pulse, and is important to energy measurements and Pile-up errors [30].

Each of the components can be analyzed individually using the simplified model, shown at 1.13(b), consisting of a pulse with effective charge Q_{eff} in parallel with an equivalent capacitance C_{eq} with its respective values [30].



(a) The SiPM signal is separated into a Fast and a Slow component.

(b) SiPM simplified electrical model.

Figure 1.13: Separation of the SiPM signal into its individual components.

Equations 1.18 and 1.19 show the value of the effective charge Q_{eff} and equivalent capacitance C_{eq} of the fast and slow components where $Q_{1\mu cell}$ is the charge of a single fired microcell, C_q is the parasitic capacitance of the quenching resistor and C_d is the capacitance of the avalanche photodiode. Finally, for timing and energy analysis the fast and slow equivalent values should be selected respectively[4]. A more detailed analysis

[4]In general $C_d \approx 4C_q$ [15], [29], [26], therefore the contribution to the total charge is approximately 70% Q_S and 30% Q_F

is studied in appendix A.

$$Q_F = Q_{1\mu cell}\frac{C_q}{C_d + C_q}, \qquad C_F = C_g + N_{tot}\frac{C_d C_q}{C_d + C_q} \tag{1.18}$$

$$Q_S = Q_{1\mu cell}\frac{C_d}{C_d + C_q}, \qquad C_S = C_g + N_{tot} C_d \tag{1.19}$$

1.5 Conclusions

A radiation detector is a complex system whose main objective is to extract the timing and energy information from the incident radiation and convert it into digital data for storage and analysis. The electronic circuitry that composes it is called the front-end electronics, and is built out of multiple smaller blocks. The preamplifier is the first circuit that directly interacts with the sensor and requires to condition its signal and send it to the subsequent stages who extract the required charge and time information. Due to the involved tasks of the preamplifier, this circuit rules a great part of the performance of the whole system.

To evaluate the performance of a radiation detector system, key parameters were presented, this parameters are different or variations of the ones usually used in analog circuit design, among the main important are noise, dynamic range, pile-up errors, charge resolution and time resolution.

The SiPM sensor is a matrix array of small SPADs, called microcells, interconnected in parallel that can be fired individually. If the charge of one microcell is previously known, the total amount of photons that arrive to the sensor from an event can be calculated. The biasing of the sensor directly affects the charge generated by each microcell and its readout method affects its signal shape and the way to calculate the charge, therefore understanding the working mechanism of the SiPM sensor, is mandatory to correctly design the front-end electronics of the radiation detector.

The presented electrical model of the SiPM is an accurate circuit that reproduces the signals generated from the sensor, since the extraction of the required parameters is an extensive task, which is out the scope of this work, the parameters from the well documented Hamamatsu S10931-050P SiPM sensor are used in the development of this thesis. The SiPM signal is constructed by a fast and a slow component, the former rules the rising edge of the signal and should be used for timing measurements, and the later contains the information required for energy measurements. This analysis lead to the introduction of a simplified electrical model of the sensor in which each component can be analyzed individually. s

Chapter 2

Front-end architectures for SiPMs

In the previous chapter, it was exposed the fundamental blocks that compose a radiation detector, the key parameters in front-end electronics and the main characteristics of a SiPM sensor. The studied information leads to recognize the importance of the preamplifier in a front-end electronics, because its interaction with the sensor directly defines some of the parameters of the detector and its output is used by the next blocks to measure timing and energy of the incident particle [26].

The architecture of the front-end electronics to readout the sensor must be carefully selected to achieve the desired detector specifications. To accomplish this objective this chapter analyzes the advantages and limitations of the main readout solutions to SiPMs with ideal models and finally reviews the state of the art of each implemented architectures.

2.1 Charge-Sensitive Amplifier

A Charge-Sensitive Amplifier (CSA) consists of an operational amplifier configured as an integrator by means of a feedback capacitor C_{Fb}, figure 2.1 shows the CSA coupled to the simplified electrical model of a SiPM.

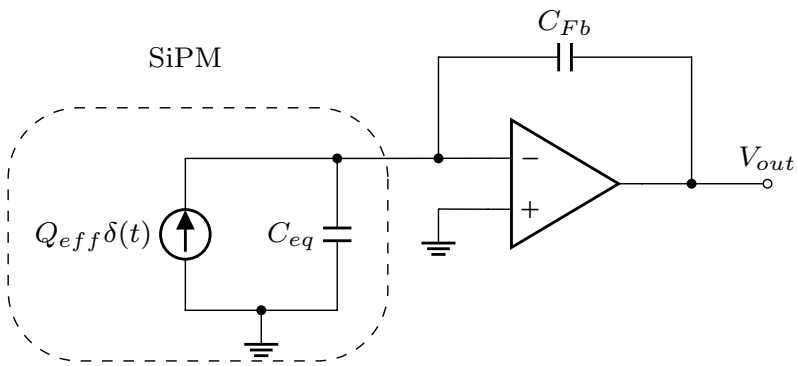


Figure 2.1: Charge-sensitive amplifier coupled to a SiPM.

2.1.1 Energy Measurements

This preamplifier is one of the most widespread read-out architectures to read radiation sensors[1] because the circuit directly integrates the current from the sensor as in equation 2.1 [9].

$$V_{out} = \frac{\int I_{in} dt}{C_{Fb}} \tag{2.1}$$

Therefore its peak voltage is proportional to the charge of the incident particle [26].

$$V_{peak} = \frac{Q_{eff}}{C_{Fb}} \tag{2.2}$$

When coupled to a SiPM, the CSA is very sensible to the charge of a small number of fired microcells. For instance consider the case where a peak voltage value of 1V is required for a charge of 10 fired micocells (that is 1.6pC for a SiPM with $Q_{1\mu cell} = 160fF$), to achieve this objective the necessary value of the feedback capacitance C_{Fb} is 1.6pF, a relative large number for an integrated circuit but still possible to implement. In contrast when a large number of microcells needs to be read, the preamplifier is limited by the size of C_{Fb}. Consider the same peak output voltage of 1V is required now for a 1000 fired micorells of the same SiPM, that is an input charge of 160pC, the

[1]Most physicist reefer to the CSA simply as a *Charge Amplifier*, this architecture is so widely used when coupled to other types of sensors that most of the radiation detector literature is based on this circuit [9] [26].

necessary feedback capacitance is 160pF, an enormous non practical value for integrated circuit design.

As seen in section 1.3.6, a factor that directly affects the charge resolution of the radiation detector is the output noise of the preamplifier. To evaluate the theoretical charge resolution of the CSA the calculation of its output noise is required. The total rms noise voltage at the output of the CSA $V_{n,RMS}$ results from all of the frequency components that fall in the closed-loop bandwidth [13]. The noise is evaluated by calculating the total area under the spectral density using equation 2.3 [9].

$$V_{n,RMS} = \sigma_V = \sqrt{\int_0^\infty \overline{V_{n,in}^2} \left| \frac{A_V}{1 + j\frac{2\pi f}{\omega_{CL}}} \right|^2 df} \tag{2.3}$$

In equation 2.3 A_V is the maximum voltage gain of the closed loop amplifier, $\overline{V_{n,in}^2}$ is its equivalent input voltage noise white power spectral density expressed in V^2/Hz [30] and ω_{CL} is the closed-loop bandwidth of the CSA.

The closed-loop bandwidth is calculated using the circuit shown in Figure 2.1. Let $A(s) = A_o/(1 + s/\omega_A)$ be the transfer function of the operational amplifier where ω_A and A_o are the open-loop bandwidth and gain of the amplifier respectively. The closed loop transfer function of the circuit in Figure 2.1 is:

$$\frac{V_{out}}{I_{in}} = -\frac{A(s)}{s(C_{Fb} + C_{eq} + A(s)C_{Fb})} = -\frac{A_o}{s(C_{Fb} + C_{eq} + \frac{(A_o C_{Fb})}{(1+s/\omega_A)})(1 + \frac{s}{\omega_A})} \tag{2.4}$$

Solving the denominator, the first pole is located at zero, as expected since the circuit behaves as an integrator [13], the second is located at:

$$\omega_p = \frac{(C_{Fb} + A_o C_{Fb} + C_{eq}\omega_A)\omega_A}{C_{Fb} + C_{eq}} \tag{2.5}$$

Expanding equation 2.5 and considering $A_o\omega_A C_{Fb}$ as the dominant therm, the closed loop bandwidth of the CSA is approximately [30]:

$$\omega_{CL} \approx A_o\omega_A \frac{C_{Fb}}{C_{Fb} + C_{eq}} \tag{2.6}$$

To obtain the closed-loop voltage gain A_V, the circuit in Figure 2.2 is analyzed and its value is .

$$A_V = 1 + \frac{C_{eq}}{C_{Fb}} \tag{2.7}$$

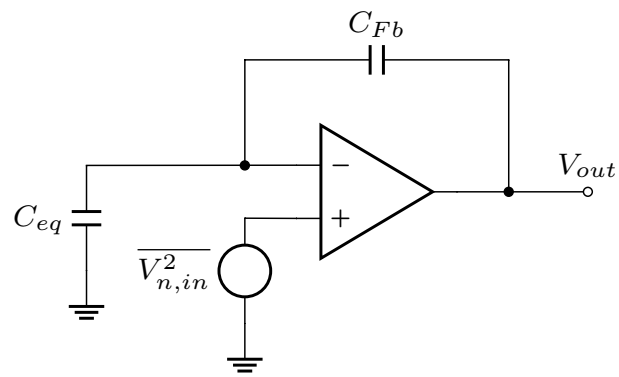


Figure 2.2: Charge-sensitive amplifier with its noise source.

Applying equations 2.6 and 2.7 in expression 2.3, the total noise voltage at the output of the CSA is [30]:

$$V_{n,RMS} = \sigma_V \approxeq \sqrt{\int_0^\infty \overline{V_{n,in}^2} \left(1 + \frac{C_{eq}}{C_{Fb}}\right)^2 \frac{1}{\left|1 + j\frac{2\pi f}{\omega_{CL}}\right|^2} df} = \frac{\overline{V_{n,in}}}{2} \sqrt{\left(1 + \frac{C_{eq}}{C_{Fb}}\right) A_o \omega_A} \tag{2.8}$$

From section 1.3.6, the charge resolution is directly affected by the output noise of the preamplifier, equation 2.8 shows that the output noise can be enhanced by increasing the feedback capacitance C_{Fb}, but it also impacts the required area of the layout and reduces the output peak voltage.

2.1.2 Time Measurements

Now, the parameter that quantifies the time resolution is the jitter of the preamplifier, to calculate it the rising edge of the output voltage of the CSA is approximated by a negative exponential function limited by the closed-loop bandwidth of the CSA and whose peak value is equation 2.2 [30].

$$V_{out}(t) \approxeq \frac{Q_{eff}}{C_{Fb}} e^{-\omega_{CL} t} \tag{2.9}$$

The maximum slope of the output signal is obtained by differentiating equation 2.9:

$$\left.\frac{dV_{out}(t)}{dt}\right|_{max} = \frac{Q_{eff}}{C_{Fb}} \omega_{CL} = A_o \omega_A \frac{Q_{eff}}{C_{Fb} + C_{eq}} \tag{2.10}$$

Evaluating equations 2.10 and 2.8 into expression 1.8, the time resolution for the CSA results in [30]:

$$\sigma_t \approxeq \frac{\overline{V_{n,in}}(C_{eq} + C_{Fb})}{2Q_{eff}} \sqrt{\left(1 + \frac{C_{eq}}{C_{Fb}}\right) \frac{1}{A_o \omega_A}} \tag{2.11}$$

Equation 2.11 shows that the jitter of the preamplifier when coupled to a SiPM is strongly limited by the large equivalent capacitance C_{eq}. Furthermore σ_t exhibits its minimum value when $C_{Fb} = C_{eq}/2$ but this value is extremely large and unpractical for implementation in integrated circuits [2]. Increasing C_{Fb} would lead to a reduction of the jitter but at the same time a reduction of the peak value leading to smaller amplitude signals thus affecting the performance of the comparator.

Finally, the CSA is recommended only for energy measurement of small SiPMs with a limited number of microcells, due to its high sensibility and reduced output dynamic range limited by C_{Fb}. For timing measurements, the equivalent capacitance of the sensor penalize both the slope and output noise voltage, to compensate its effects, the feedback capacitance should be increased, but by augmenting C_{Fb} the peak output voltage also is reduced which also affects the jitter.

2.1.3 Practical implementations

One of the implementations of the CSA in front-end electronics for SiPM sensors is the ASIC VATA64HDR16. This ASIC has been used with small gain SiPM coupled to scincillators in medical imaging applications [31] and in the detection of Cherenkov

[2] The equivalent fast capacitance C_F of the Hamamatsu S10931-050P, a $3 \times 3mm$ active area SiPM, according to the parameter extraction reported by Tuchetta et al. [26] is $64pF$.

light operating in photon counting mode [32]. It consists of 64 channels, each with a dynamic range of 55pC, maximum input current of $10\mu A$ and a power dissipation of 15mW [33].

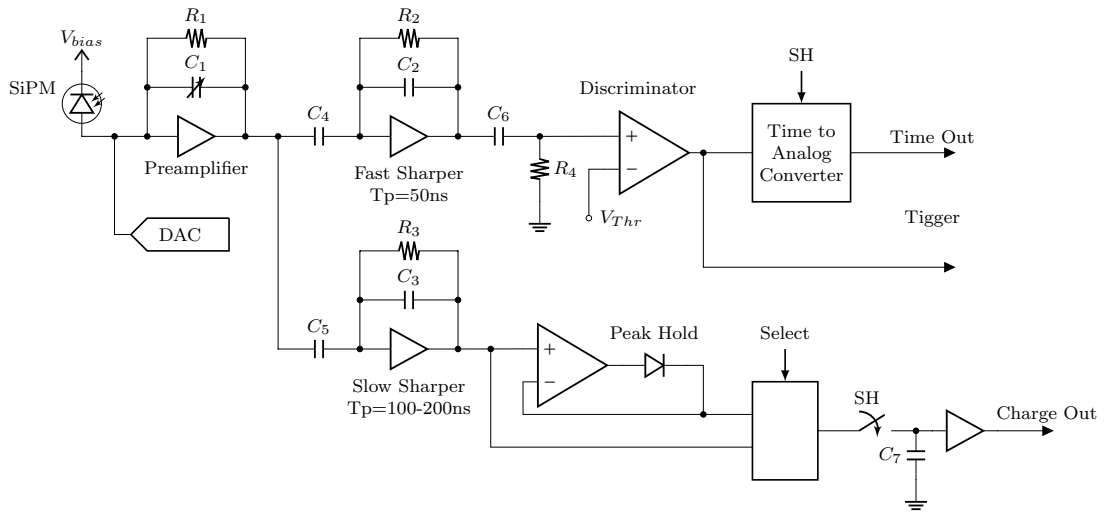


Figure 2.3: VATA64HDR16 ASIC architecutre.

A single channel, visualized in Figure 2.3, consists of a CSA as a preamplifier with a variable feedback capacitor, its output is used by a *fast* and a *slow* shaper to increase the noise to signal ratio. The *fast* sharper has a shaping time [3] of 50ns, its output is used by a discriminator[4] to be compared with a programmed threshold value, if the output is superior to the threshold, a trigger pulse is sent to a time to analog converter to measure the arrival time of the particle. The *slow* sharper has a variable shaping time of 100ns to 200ns, its peak output voltage is hold and then digitized with an analog-to-digital converter to measure the charge information of the event.

As previously mentioned, the CSA is recommended for small SiPMs with a limited number of microcells, the ASIC VATA64HDR16 confirms this observation. The integrated circuit has a limited dynamic range and therefore is used for single photon counting, considering a SiPM with a single fired microcell charge of $Q_{1\mu cell} = 160fF$, the preamplifier can read up to 344 microcells before saturation.

[3]The duration of the complete pulse from rising to falling edge.

[4]A discriminator is the name used in radiation detectors to a comparator.

2.2 Voltage amplifier and Current buffer

The voltage amplifier readout has been widely used for characterization of the SiPM sensor [28], [26], as well as in practical implementations [34], [35]. Figure 2.4(a) shows a representation of this architecture, a SiPM is connected to a load resistor R_{in}[5], the input signal V_{in} is magnified by a voltage amplifier, the output signal V_{out} is used by a comparator and an integrator to measure time and energy respectively.

The current buffer readout approach has found a broad application in the design of front-end electronics for SiPM sensors [11]. Figure 2.4(b) shows the basic principle of this readout approach, a current buffer with a very small input impedance R_{in} is coupled to a SiPM, the output signal of the current buffer is a high impedance replica of the current pulse generated by the sensor that can be reproduced to different gain factors.

Both voltage amplifier and current buffer preamplifiers follow a similar analysis, therefore in this section their charge and time resolution theoretical performance is evaluated together.

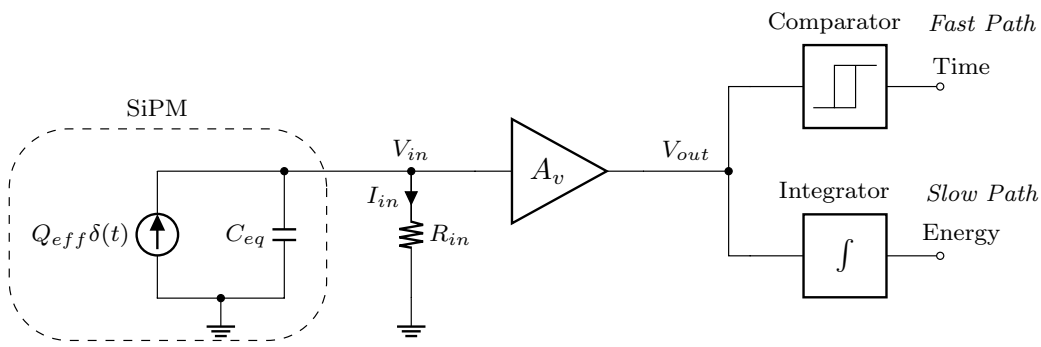
2.2.1 Energy Measurements

To begin with the analysis, the information required for energy measurements is primarily contained by the slow component of the SiPM signal, so for the simplified electrical model in both the voltage amplifier and current buffer illustrated in figure 2.4 the values are replaced by $Q_{eff} = Q_S$ and $C_{eq} = C_S$.

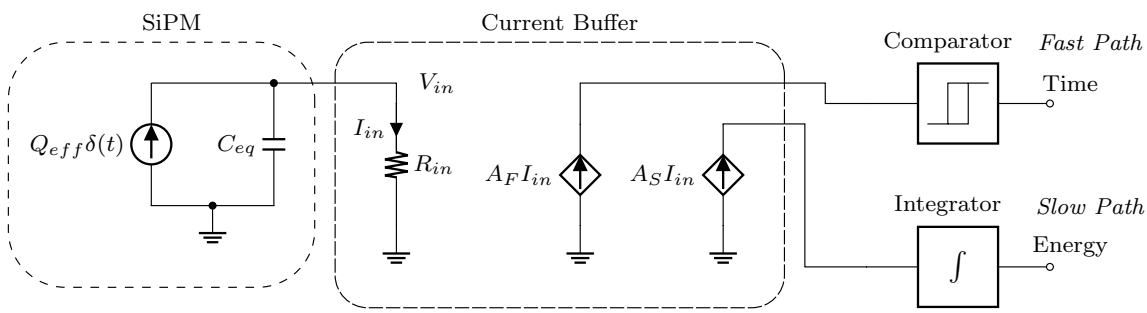
One of the main parameters that heavily impacts energy measurements is *Pile-Up*[6], so the tail of the signal should return to its ground level before the next event occurs, therefore is mandatory to know the elements that rule the duration of a pulse.

[5]In radiation detectors the load resistor directly coupled to the SiPM is called the *Input Resistor* R_{in} because is the first element to be in contact with the sensor, not be confused with the input impedance of the amplifier Z_{in}

[6]Accumulation of the pulses, it occurs when two or more events arrive at the same time, see section 1.3



(a) Voltage-Mode Readout with a voltage amplifier.



(b) Current-Mode Readout with a current buffer.

Figure 2.4: Voltage amplifier and current buffer readout.

Consider the moment when a microcell is fired, Figure 1.13(a) shows that the rising time of the slow component is actually very slow compared to the fast component, since the energy information is contained mostly in the slow component [11], the rising edge will be neglected in this analysis. The voltage in the input node V_{in} experiences an exponential decay with a peak value $V_{peak,slow} = Q_S/C_S$ and a time constant $\tau_S = \tau_r + C_S R_{in}$, where τ_r is the recovery time of the SiPM sensor, that is:

$$V_{in}(t) = \frac{Q_S}{C_S} e^{-t/\tau_S} \tag{2.12}$$

Neglecting the effect of the fast rising edge, and focusing into the exponential decay, the voltage at the output node V_{out} is approximately.

$$V_{out}(t) \approxeq A_v \frac{Q_S}{C_S} e^{-t/\tau_S} \tag{2.13}$$

According to mathematics, the moment when an exponential decay reaches 0.7% of its peak value is approximately 5τ, so the duration of the SiPM pulse is set by Equation 2.14. Figure 2.5(a) shows the simulation of a SiPM pulse against its time constant τ_S.

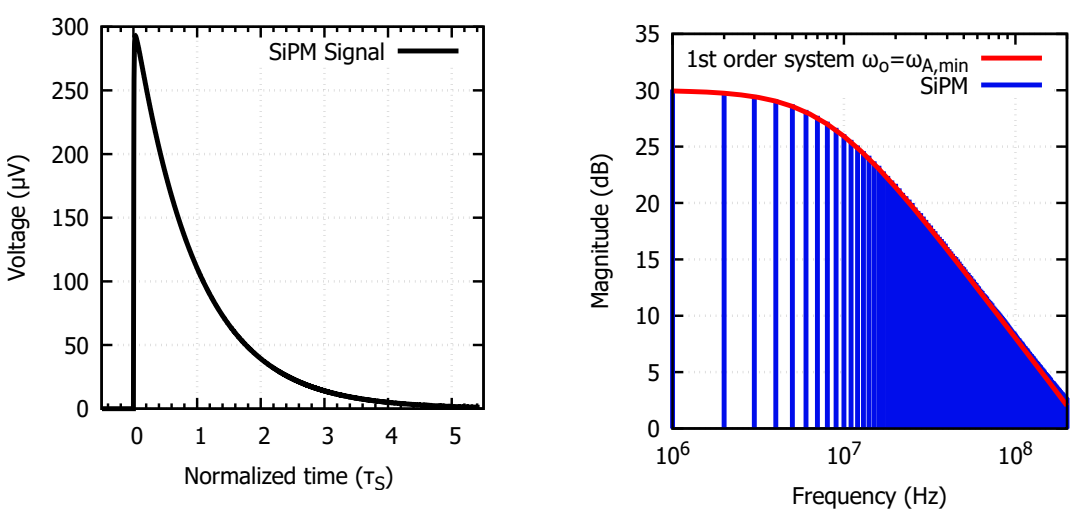
$$Pulse\ Duration = 5\tau_S = 5(\tau_r + C_S R_{in}) \tag{2.14}$$

Once the duration of the pulse is known, its necessary to recognize the frequency components that contain the energy of the event. Since the slow component is an exponential decay, its Fourier transform is similar to a first order system whose pole is located at $1/\tau = \omega_o$, shown in equation 2.15 and visualized in figure 2.5(b).

$$x(t) = e^{-t/\tau} \quad \rightarrow \quad X(s) = \frac{1}{1 + \tau s} \tag{2.15}$$

Therefore, the minimum bandwidth required of the amplifier to maintain the spectral information of the energy is given by the time constant τ_S:

$$\omega_{A,min} = \frac{1}{\tau_S} = \frac{1}{\tau_r + C_S R_{in}} \tag{2.16}$$



(a) Pulse duration in relationship with τ_S.

(b) Spectrum of the SiPM and a low pass filter with a cut-off frequency of $\omega_o = \omega_{A,min}$.

Figure 2.5: Slow component parameters of the SiPM signal.

Unlike the CSA where its output voltage is directly proportional to the charge, when a voltage amplifier readout is used, the output voltage needs to be integrated to calculate the charge. Considering A_v as the gain of the voltage amplifier, the charge is calculated by the following equation.

$$Q_S = \frac{1}{A_v R_{in}} \int V_{out}(t)dt \tag{2.17}$$

Figure 2.6 illustrates the variation of the charge generated form the SiPM Q_{in} and the charge calculated from equation 2.17 against the bandwidth of the preamplifier. After the bandwidth reaches $\omega_{A,min}$,it is visible that the charge variation is minimal.

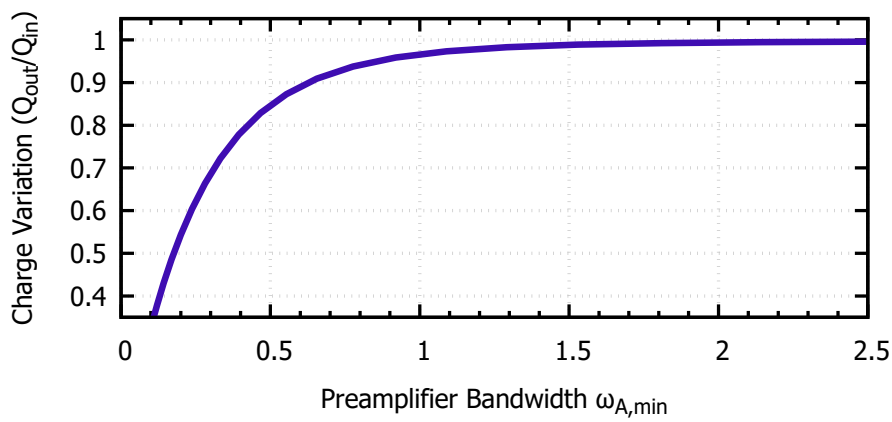


Figure 2.6: Charge variation vs preamplifier minimum bandwidth.

To calculate the parameters Gain of the front end and Charge Resolution of the radiation detector, described in section 1.3, in stead of being obtained directly form the output voltage, as in the specific case of the CSA, this are obtained using the output signal of the integrator.

The output noise analysis of the voltage amplifier is evaluated with equation 2.3, it results in the equation 2.18 where $\overline{V_{n,in}}$ is the equivalent input voltage noise white power spectral density and ω_A is the bandwidth of the voltage amplifier [26]:

$$V_{n,RMS} = \sigma_v = A_v \frac{\overline{V_{n,in}}}{2} \sqrt{\omega_A} \tag{2.18}$$

According to equation 2.18 the output noise is inevitably proportional to its gain and its bandwidth, using values equal or superior to $\omega_{A,min}$ ensures the conservation of the spectral components of the energy but at the same time increases the output noise of the preamplifier, penalizing the charge resolution.

Even thought the charge of the event is not directly obtained from the output voltage of the voltage amplifier and requires an additional method of integration, the noise of the voltage amplifier should be minimized to enhance the charge resolution. As a metric to estimate the Charge Resolution Q_n of the preamplifier signal after being integrated, the Noise-to-Microcell Ratio (NMR) is proposed in this work, which is defined as the relationship between the output RMS noise of the voltage amplifier σ_n over the amplified peak signal generated form the slow component of a single fired microcell.

$$NMR = \frac{Noise}{Micocell} \tag{2.19}$$

If identical photons are sent to the SiPM sensor periodically, the same amount of micorcells are fired, and the output of the preamplifier signal is integrated and then observed, the peak value would have a Gaussian distribution whose average value is the number of fired microcells N_f and its standard deviation equals $Q_n = NMR$, similar to the case exposed in section 1.3.6.

Equation 2.20 shows the Noise-to-Microcell ratio of the voltage amplifier.

$$NMR_{VA} = \frac{\sigma_v}{A_v V_{peak,slow}} = \frac{C_S \overline{V_{n,in}}}{2Q_S}\sqrt{\omega_A} \tag{2.20}$$

If the current buffer approach is selected, the input current is obtained by dividing the output voltage to its input resistance $I_{in} = V_{in}(t)/R_{in}$ and equations 2.14 and 2.16 are valid. Considering A_i as the gain of the current buffer, the charge is calculated by integrating the input current

$$Q_S = \frac{1}{A_i}\int I_{in}(t)dt \tag{2.21}$$

The noise analysis of the current buffer is evaluated with equation 2.3, it results in the equation 2.22 where $\overline{I_{n,in}}$ is the equivalent input current noise white power spectral

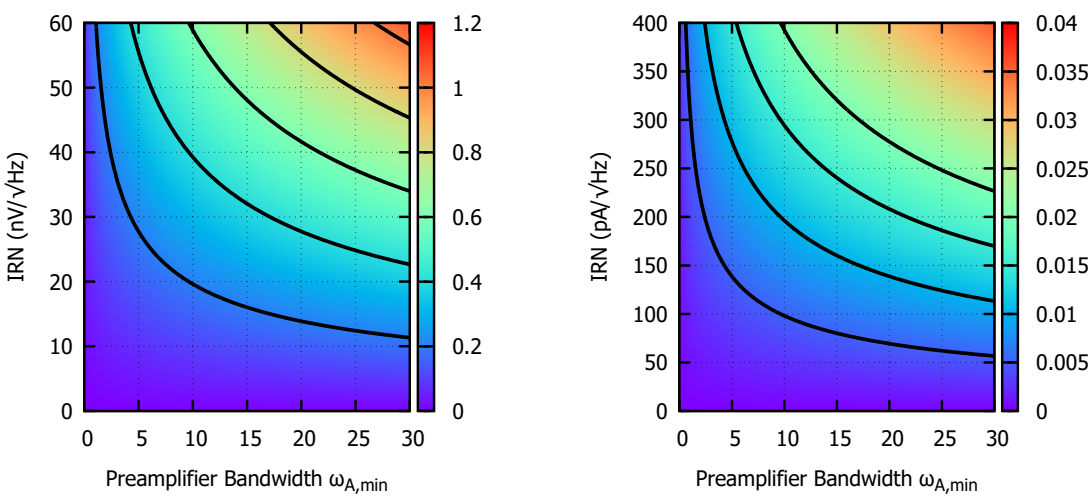
density and ω_{CB} is the bandwidth of the current buffer [26]:

$$I_{n,RMS} = \sigma_i = A_i \frac{\overline{I_n}}{2} \sqrt{\omega_{CB}} \tag{2.22}$$

Similar to the case of the voltage amplifier a metric to measure the charge resolution of the Current Buffer its Noise-to-Microcell Ratio (NMR) which is given by equation 2.23.

$$NMR_{CB} = \frac{\sigma_i}{A_i I_{peak,slow}} = \frac{R_{in} C_S \overline{I_n}}{2Q_S} \sqrt{\omega_{CB}} \tag{2.23}$$

Figure 2.7 compares the variation of the NMR to the bandwidth and the input referred noise of the voltage amplifier and current buffer approaches, it is visible that the current buffer delivers a better charge performance than the voltage amplifier.



(a) Voltage amplifier.

(b) Current buffer.

Figure 2.7: Noise-to-Microcell Ratio against the input referred noise and bandwidth of the preamplifier .

2.2.2 Time Measurements

For time measurements, the rising edge is dominated by the fast component of the SiPM signal, as shown un 1.13(a), therefore, $Q_{eff} = Q_F$ and $C_{eq} = C_F$ are used in Figure 2.4. Consider the moment when a microcell is fired, the voltage in the node V_{in} and the input current I_{in} experiences an abrupt variation and then descents at a time constant of $\tau_F = C_F R_{in}$, that is:

$$V_{in}(t) = \frac{Q_F}{C_F} e^{-t/\tau_F} \tag{2.24}$$

$$I_{in}(t) = \frac{Q_F}{R_{in} C_F} e^{-t/\tau_F} = \frac{Q_F}{\tau_F} e^{-t/\tau_F} \tag{2.25}$$

When the input voltage or current is amplified, the abrupt variation is slowed down by the speed of the amplifier given by its bandwidth, that is $\omega_A = 1/\tau_A$ and $\omega_{CB} = 1/\tau_{CB}$ for the voltage amplifier and the current buffer respectively, so the output signal behaves as a double exponential function [26]:

$$V_{out}(t) = A_v \frac{Q_F}{C_F} \left(e^{-t/\tau_F} - e^{-t/\tau_A} \right) \tag{2.26}$$

$$I_{out}(t) = A_i \frac{Q_F}{\tau_F - \tau_{CB}} \left(e^{-t/\tau_F} - e^{-t/\tau_{CB}} \right) \tag{2.27}$$

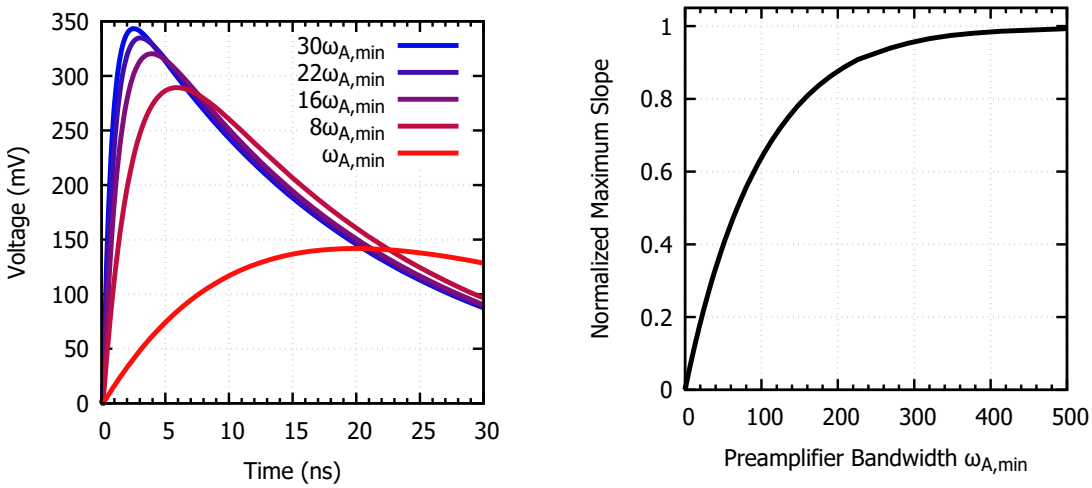
The maximum slope of the output signal is obtained by differentiating equations 2.26 and 2.27:

$$\left. \frac{dV_{out}(t)}{dt} \right|_{max} = A_v \frac{Q_F}{C_F} \frac{1}{\tau_A} = A_v \omega_A \frac{Q_F}{C_F} \tag{2.28}$$

$$\left. \frac{dI_{out}(t)}{dt} \right|_{max} = A_i \frac{Q_F}{\tau_F} \frac{1}{\tau_{CB}} = A_i \omega_{CB} \frac{Q_F}{\tau_F} \tag{2.29}$$

From equation 2.28 is visible that the slope of V_{out} is independent of R_{in}, on the other hand expression 2.29 shows that the the slope of I_{out} increases as R_{in} decreases. Figure 2.8(a) illustrates the output signal of a voltage amplifier with multiple bandwidth

values and 2.8(b) delivers the normalized maximum slope against the variation of the bandwidth of the preamplifier. In order to reproduce the rising edge of the SiPM signal the bandwidth of the preamplifier should reach an incredible value of $300\omega_{A,min}$, which is non practical due to the integrated circuit process technologies.



(a) Output signal.

(b) Normalized Maximum slope.

Figure 2.8: Variation of the output signal and its maximum slope as a function of the preamplifier bandwidth

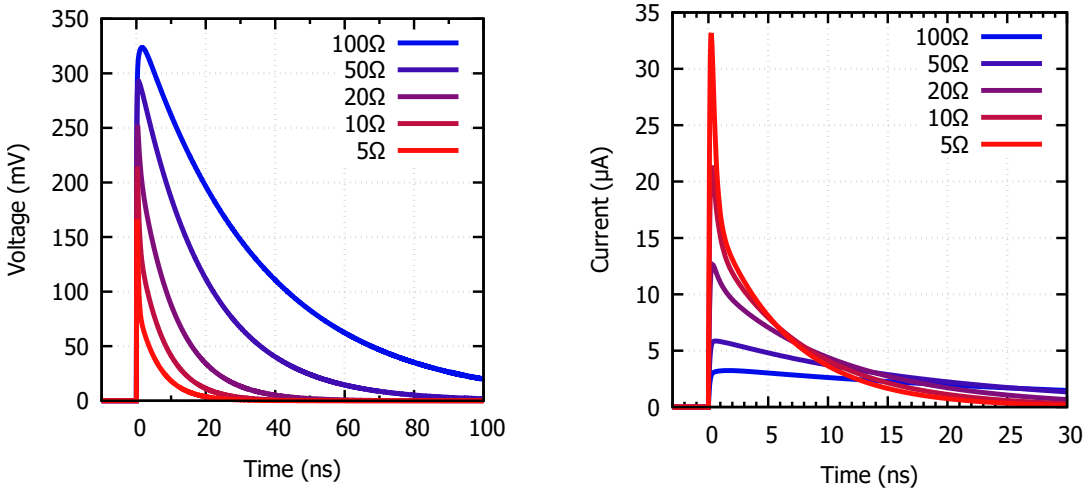
The peak value of the output signal is obtained by the following equations [26]:

$$V_{out,peak} \approxeq A_v \frac{Q_F}{C_F} \frac{\tau_F}{\tau_F - \tau_A} \left[\left(\frac{\tau_F}{\tau_A} \right)^{\frac{\tau_A}{\tau_A - \tau_F}} - \left(\frac{\tau_F}{\tau_A} \right)^{\frac{\tau_F}{\tau_A - \tau_F}} \right] \tag{2.30}$$

$$I_{out,peak} \approxeq A_i \frac{Q_F}{\tau_F - \tau_{CB}} \left[\left(\frac{\tau_F}{\tau_{CB}} \right)^{\frac{\tau_{CB}}{\tau_{CB} - \tau_F}} - \left(\frac{\tau_F}{\tau_{CB}} \right)^{\frac{\tau_F}{\tau_{CB} - \tau_F}} \right] \tag{2.31}$$

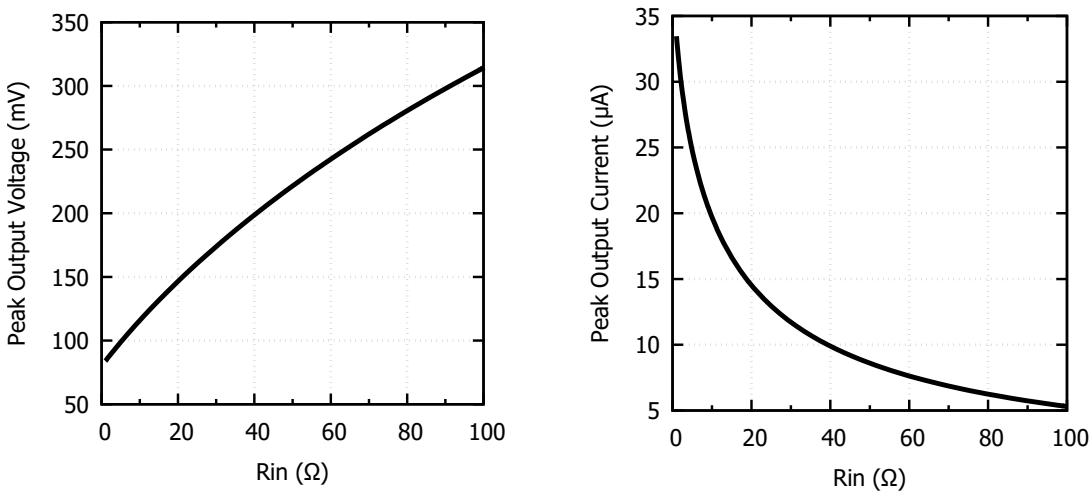
Simulations of the SiPM complete model demonstrates the validation of the mathematical analysis carried out in this section and illustrate the signal shape and peak value variation against the input resistance R_{in} in figures 2.9 and 2.10.

For the voltage amplifier V_{peak} increases as R_{in} increments, as a consequence the maximum slope expressed in equation 2.28 increments as well. For timing measurements R_{in} should be increased to assure the correct operation of the comparator. Nonetheless



(a) Voltage Signal. (b) Current Signal.

Figure 2.9: SiPM Pulse shape variation as a function of R_{in}.



(a) Voltage-Mode Readout. (b) Current-Mode Readout.

Figure 2.10: Peak value of the output signal as a function of R_{in}.

an increment of the input resistance also increments the duration of the long tail of the SiPM signal, seen in Figure 2.9(a), given that $\tau_S = C_S R_{in}$, so the maximum event rate is penalized.

For the current buffer I_{peak} increases as R_{in} decrements. For timing measurements

R_{in} should be reduced to guarantee a proper operation of the discriminator, this also reduces the duration of the SiPM pulse, and increments the maximum event rate as seen in Figure 2.9(b).

Evaluating equation 1.8 for the voltage amplifier and the current buffer, the jitter for both preamplifiers results in [30]:

$$\sigma_{t,VA} = \frac{\sigma_v}{\left.\frac{dV_{out}(t)}{dt}\right|_{max}} = \frac{\overline{V_{n,in}}C_F}{2Q_F}\sqrt{\frac{1}{\omega_A}} \tag{2.32}$$

$$\sigma_{t,CB} = \frac{\sigma_i}{\left.\frac{dI_{out}(t)}{dt}\right|_{max}} = \frac{\overline{I_{n,in}}R_{in}C_F}{2Q_F}\sqrt{\frac{1}{\omega_{CB}}} \tag{2.33}$$

Equation 2.32 shows that the capacitance of the SiPM inevitably affects the timing performance of the front-end, furthermore a reduction of the jitter is achieved with a voltage amplifier with a very large bandwidth in comparison with the required for energy measurements. In any case, its timing performance shows an improvement over the observed by the CSA, see equation 2.11, because of the lack of the feedback capacitance C_{Fb}.

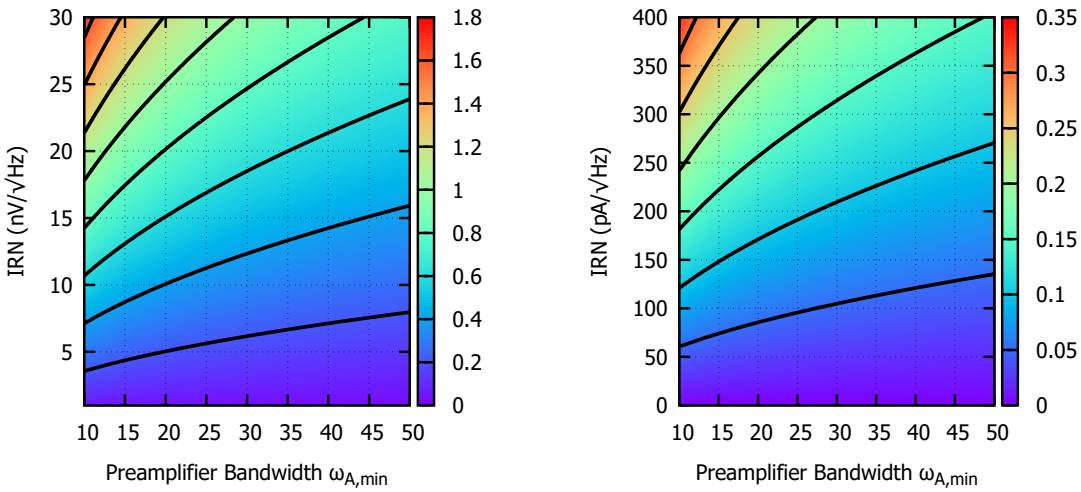
For the current buffer approach, equation 2.33 shows that for time measurements, a reduction in the R_{in} and a large bandwidth is required, which is easier to achieve than voltage amplifiers due to the absence of high impedance nodes [26].

Figure 2.11 compares the variation of the jitter to the bandwidth and the input referred noise of the voltage amplifier and current buffer approaches, the current buffer delivers a better time performance than the voltage amplifier due to the lower input referred noise expected from the current amplifiers.

2.2.3 Practical Implementations

Voltage Amplifier

The ASICs, SPIROC [36], PETIROC [37] and the EASIROC [34] are a family of integrated circuits designed by the Advanced Microelectronic General Organization (OMEGA in French) group from the Ecole Polytechnique in France, that implement



(a) Voltage amplifier.

(b) Current buffer.

Figure 2.11: Jitter variation shown in nanoseconds against the input referred noise and bandwidth of the preamplifier.

the voltage amplifier readout approach. This integrated circuits have been used in Calorimetry, and Positon Emission Tomography (PET) applications.

Due to the low noise and high speed specifications required in its design, the integrated circuits are realized in AMS 0.35μm SiGe technology rather than in standard CMOS due to its superior gain, speed and noise performance [38].

All the integrated circuits follow a similar architecture, so to analyze it the schematic of the EASIROC IC is used and it is visualized in Figure 2.12. First, the SiPM sensor is coupled to a input resistance R_{in} located outside the integrated circuit, then the voltage signal is then sent in parallel to a high and a low gain preamplifiers, with an amplification factor of 150 to 10 and 15 to 1 respectively. Both preamplifiers are implemented as an inverting voltage amplifiers with variable feedback capacitors. The maximum input charge of the preamplifiers is 320pC [34], which corresponds to the firing of 2000 microcells in a SiPM with a single fired microcell charge $Q_{1\mu cell}$ of 160fF, a substantial increment in comparison with the 344 microcells of the VATA16HDR16.

The output of both preamplifiers is integrated by a slow sharper with a variable shaping time form 25 to 170ns, this process reduces the noise of the integrated signal

according to equation 2.18 and enhances the charge resolution, their peak value is hold in an analog memory and digitized with a 12-bit Wilkinson ADC, its value is used to measure the charge of the incident event.

The output of the fast preamplifier is used by a bipolar sharper with a shaping time of 15ns, its output is used by a discriminator to be compared with a predefined threshold value, if the output is superior to the threshold a trigger pulse is sent to a time-to-digital converter to measure the arrival of the event. The power consumption of the EASIROC chip is 4.84mW per channel [34].

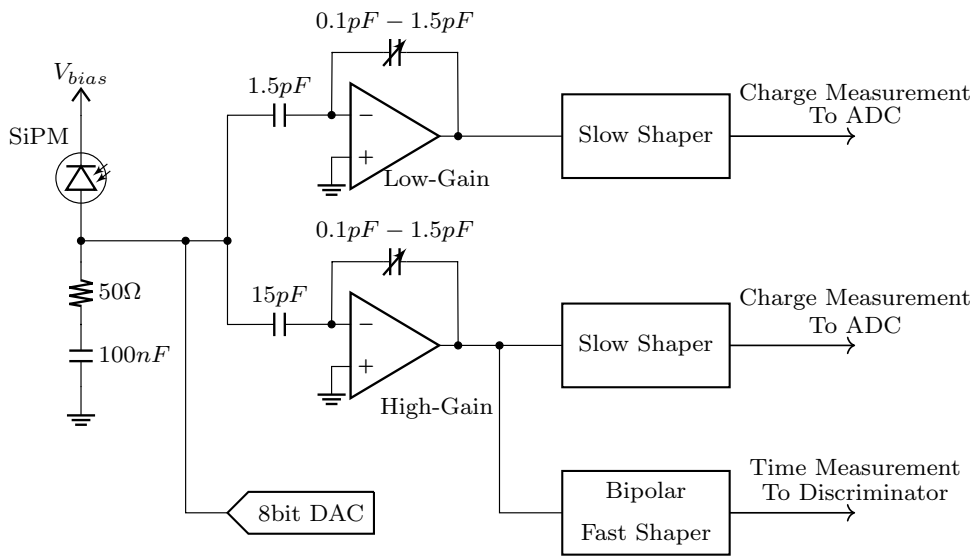


Figure 2.12: EASIROC simplified schematic.

A further implementation of the voltage readout preamplifier for SiPM is the front-end of the first version of the ASIC PETA [2]. This IC is fabricated in a standard 180nm CMOS technology, has 16 channels and has been designed to be used in ToF-PET applications, its block diagram is shown in 2.13.

With the objective to reduce the common noise of the overall system all the analog blocks of the the PETA IC are fully-differential [39], to obtain a fully differential input signal, the SiPM sensor is connected in the configuration visualized in Figure 2.13. The signal form the SiPM is separated into two paths. The *fast* path consists of a fully-differential voltage amplifier composed of a cascade of 5 low-gain stages to achieve a bandwidth of 900MHz and a total gain of 20V/V (26dB) [11], its output is compared

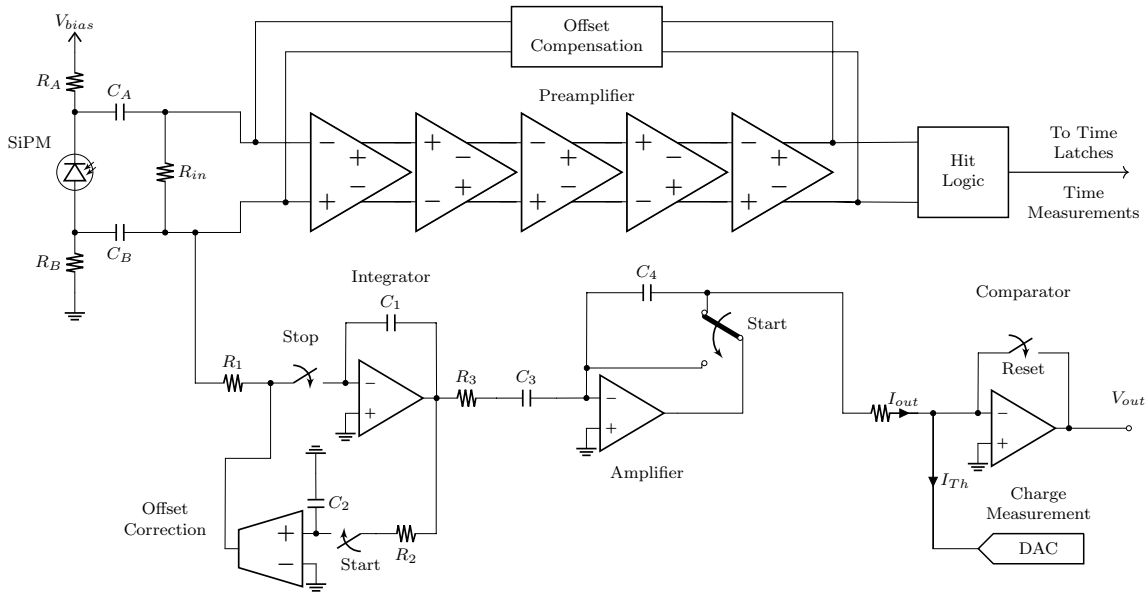


Figure 2.13: PETA simplified schematic.

with a threshold, the Time-over-Threshold (ToT) is used measure the time arrival and time duration of the event. The *slow* path is directly connected to the SiPM and not to the preamplifier, it consist of an integrator whose integration window time is set by the ToT signal, its output is digitized and used to measure the energy of the incident particle. The power consumption of the integrated circuit is 86mW per channel [39].

Discrete implementations have been carried out with commercial operational amplifiers and RF voltage amplifiers, in [28], Francesco et al. used a cascade of two LMH6703 operational amplifiers with a bandwidth of 100MHz and a voltage gain of 39V/V, this approach has a power consumption of approximate 200mW. In [40] a bipolar RF amplifier with a bandwidth of 1GHz and a gain of 12dB was used to timing measurements, the power dissipation is around 400mW.

The implementation described previously show interesting observations. First, in the EASIROC architecture, the use of SiGe technology allows a better gain, speed and noise performance than standard CMOS, this permits the use of operational amplifiers in the preamplifier block with a very small power consumption. In contrast the preamplifier implemented in the PETA IC uses the topology of a limiting amplifier[7] to reach the

[7] A cascade of multiple Fully-Differential amplifiers to achieve very high gains and bandwidths. It

required bandwidth but with a power consumption 17 times larger.

Secondly, both implementations use the dual *fast* and *slow* path approach in order to maximize both time and charge resolution. In the case of the PETA integrated circuit, this approach goes even further, the paths are separeted directly form the sensor output, the fast preamplifier is used to determinate the arrival and the duration of the pulse, and voltage integrator with a smaller bandwidth calculates the energy of the event.

Finally, since the voltage amplifier readout is general used for characterization of the SiPM sensor, it would be natural to consider the use this approach in the implementation of integrated circuits for radiation detectors. Nevertheless in order to achieve the large bandwidth values required in time measurements, a great power consumption of the voltage amplifiers is needed, therefore the implementation of a front-end electronics with a large number of channels in integrated circuits using standard CMOS technology are unpractical [11].

Current Buffer

The integrated circuit BASIC, is an 8 channel front-end that uses a current buffer to readout SiPM sensors. It was fabricated in a standard $0.35\mu m$ CMOS process and specially designed for medical imaging applications [41]. Its architecture is shown in figure 2.14.

As shown in figure 2.14, the SiPM is directly connected to the current buffer with an input impedance of 17Ω, a bandwidth of 250MHz and current consumption of $800\mu A$. This circuit reproduces the same input current at its high impedance output nodes without the infuence of the SiPM large parasitic capacitance. The output current passes to a current mirror where is copied to parallel paths with different gains. Once again the time and energy measurements are carried out in a *fast* and *slow* path respectively.

In the *fast path* a unitary gain copy of the input current is sent to a current discriminator, when the current input exceeds the current threshold value a trigger signal is activated which indicates the arrival of an event. In the *slow path* a scaled down replica

is mostly used in optical communications.

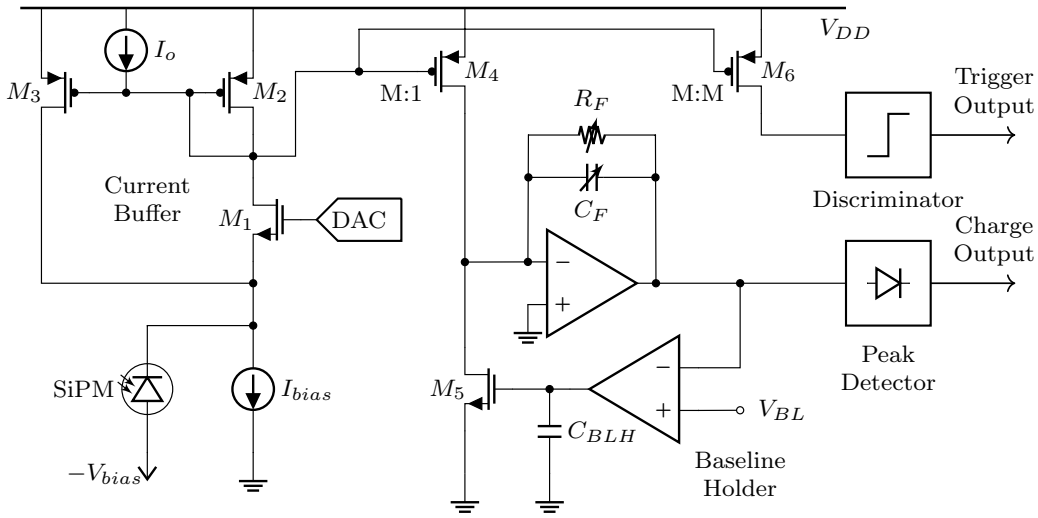


Figure 2.14: Architecture of the ASIC BASIC.

of the input current is send to a Charge Sensitive Amplifier (CSA) with variable gain and a repetition rate of 100KHz[8], the peak of the output voltage of the CSA measures the charge of the event, therefore a peak detector holds its value so a 8 bit Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) can digitalize it. The BASIC integrated circuit exhibits a maximum input charge of 70pC[9], an output noise voltage of $\sigma_v = 5mV$, and a time jitter about $\sigma_t = 650ps$.

Another implementation of the current buffer readout approach used for SiPM sensors is the ASIC DIET. This integrated circuit specially designed for PET and TOF-PET applications consists of a 64-channels each with infividual amplification and digitization of energy and time information. It was fabricated in a standard $0.18\mu m$ CMOS process and exhibits a power consumption of 5mW per channel [42].

Shown in figure 2.15 the architecture of the chip DIET, the SiPM sensor is directly connected to a current buffer with an input impedance of 50Ω, a bandwidth of $300MHz$ $C_{in} = 12pF$, a maximum input current of $5mA$ and a power consumption of less than a 1mW. The output current is send to a current mirror where is copied to a parallel *slow* and a *fast* paths.

In the *fast path* a input signal copy with a gain equal to the unity is sent to a

[8]The maximum frequency at which the output completely returns to its baseline [41]

[9]Considering a SiPM with a $Q_{1\mu cell} = 160fF$, the front-end can read up to 437 micocells.

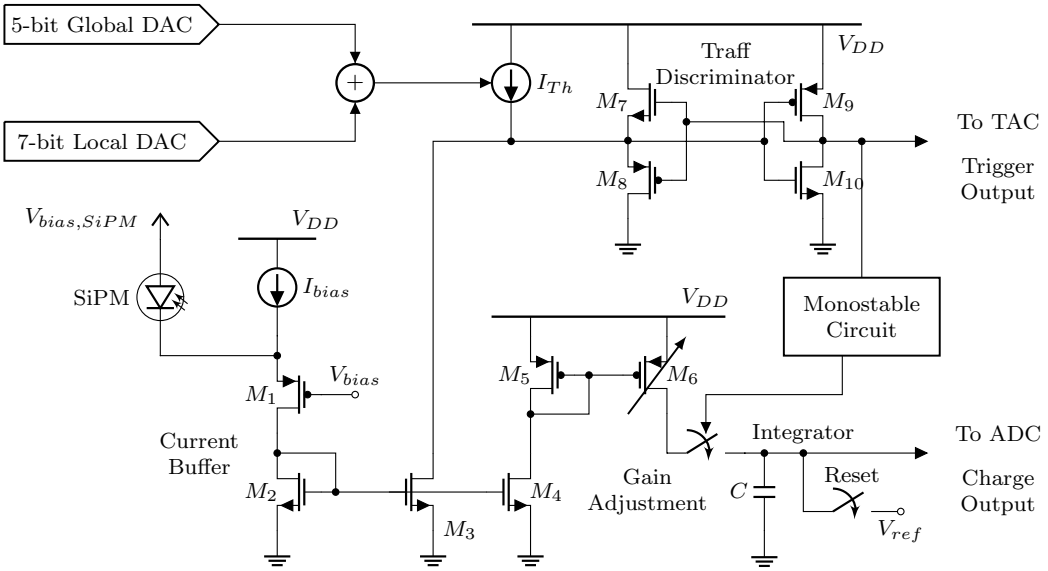


Figure 2.15: Architecture of the ASIC DIET.

Taff current comparator with a timing jitter of 25ps, the threshold current is adjusted with the aid of a 5bit global DAC (Digital to Analog Converter) and with a 7 bit local DAC for each individual channel. The output signal of the comparator is used by a Time-to-Amplitude Converter (TAC) that transforms the time of the pulse duration into voltage, to finally be digitized by a 10-bit Wilkinson ADC.

With the objective to achieve a maximum input charge of 96pC[10], the current signal of the *slow path* is sent to a second current mirror with adjustable gain factor, the attenuated signal is then integrated on a switched capacitor with an integration time window defined by the comparator signal, the voltage of the integrator which is proportional to the charge information, is digitized by a second 10-bit Wilkinson ADC.

Both implementations demonstrate that using the current buffer readout approach is possible to reach the a similar performance of the EASIROC chip in therms of charge resolution, timing resolution and power consumption using a standard CMOS process.

[10]Considering a SiPM with a $Q_{1\mu cell} = 160fF$, the DIET front-end can read up to 600 micocells before saturation

2.3 Conclusions

In this chapter an analysis of the three most commonly used front-end architectures were carried out using ideal models with the objective to identify their theoretical advantages and limitations. The observations delivered form the analysis were compared and confirmed with a review of the state of the art, a summary of this observations is visualized in Table 2.3. For this reason, the selection of a front-end architecture should be made according to the requirements of the radiation detector.

Parameter	CSA	Voltage Amplifier	Current Buffer
Input Dynamic Range	Limited by C_{Fb}	$\uparrow$ when a variable gain amplifier is used	$\uparrow$ when a variable gain current mirror is used
Charge Measurements	$V_{out} \propto Q_{in}$, high sensibility	Additional integrator required	Additional integrator required
Timing Measurements	Limited by C_{in}	$\uparrow R_{in}$ and $\uparrow BW$	$\downarrow R_{in}$ and $\uparrow BW$
Power Consumption	Moderate	Large	Small
Pile-up errors	$\downarrow$ Peak time	$\downarrow R_{in}$	$\downarrow R_{in}$
Complexity	Moderate no. of transistors	Large no. of transistors	Small no. of transistors
Noise	Limited by C_{Fb}	Moderate	Small

Table 2.1: Comparison between the front-end architectures for SiPM sensors

The Charge Sensitive Amplifier approach is widely used in the design of radiation detector, its main advantage lays in the fact that the output peak voltage is directly proportional to the charge of the sensor. To maximize the input dynamic range the size of the feedback capacitor should be increased, in contrast for timing measurements it needs to be reduced, so a compromise between time and charge measurements is made. Due to the disused reasons the CSA is recommended for applications where timing measurements are not a great concern, or when coupled to a SiPM with a small

number of microcells.

The Voltage amplifier readout is generally employed for characterization purposes of the SiPM sensor, and discrete implementations of radiation detectors, when it is used in integrated front-end implementations, the required high bandwidth (BW) and gain values for timing measurements are difficult to achieve in standard CMOS technology without a large power consumption, making this approach not effective when low levels of lights must be detected, on the other hand, when the input signal is large the voltage amplifier approach can be conveniently applied. Since the SiPM sensor has a very large dynamic range, the use of variable gain amplifiers is highly recommendable to detect as much fired microcells as possible. Finally the peak output value and the pulse duration are proportional to the value of the input resistance R_{in}, therefore a compromise between timing measurement accuracy and the maximum event rate is unavoidable.

The current buffer readout extracts the SiPM current signal form the influence of its large parasitic capacitance and reproduce it to parallel paths with a different gain factors. The input dynamic range can be maximized when the current buffer is connected to a current mirror. The reduction of the input impedance R_{in} increases the peak current value and reduces the duration of the pulse, both desirable effects that increase the timing measurement accuracy and the maximum event rate. Finally, large bandwidths with low power consumption are typically easier to achieve in current mode amplifiers because of its absence of high impedance nodes. The achieved performance of timing and charge measurements of the current buffer readout using a standard CMOS process is comparable with the voltage amplifier approach using SiGe technologies. From the discussed reasons, the current buffer technique has become popular in the design of integrated front-end electronics for SiPM sensors with a large number of channels.

From the theoretical analysis, it was found that the minimum required bandwidth to preserve the spectral components of the energy information is ω_{min}, a larger value indeed preserves the energy information but also increases the output noise of the preamplifier

thus penalizing the charge resolution. On the other hand a very large bandwidth is required to reduce the jitter and diminish the uncertainty of the timing measurements. To overcome this issue all of the reviewed front-end architectures utilize a dual path approach where the *fast path* contains a signal with a large bandwidth and is used to measure the arrival of an event and the duration of a pulse, and the *slow path* contains a signal with a smaller bandwidth and is employed to extract the energy information of an event.

Chapter 3

Preamplifier Proposal.

The Charge Sensitive Amplifier is the most popular implementation. However, It has serious limitations in the maximum input dynamic range and the timing measurements due to its feedback capacitance. The engineers solve this issue increasing the feedback capacitance. Nevertheless, it has a direct impact on its size making it non-practical for the design of integrated circuits. Therefore, the voltage amplifier and the current buffer architectures as the best options to design the readout for the SiPM sensor.

For that reason in this work two preamplifiers using the voltage amplifier and the current buffer approach are proposed an designed. Their performance evaluation in therms of charge resolution, time resolution and power consumption, will be hugely helpful in the the selection of the architecture that best fit the requirements of the radiation detector.

3.1 Voltage Preamplifier

In the implementation of the Voltage Amplifier approach, a Variable Gain Amplifier (VGA) is highly recommended to increase the input dynamic range of the radiation detector. Typically a variable gain voltage amplifier is implemented using an operational amplifier with a negative feedback loop which defines the amplification factor [1], accord-

[1] In an inverting amplifier configuration, the high gain of an operational amplifier, highly variable to manufacturing process and temperature, guarantees that the gain factor form the feedback loop,

ing to the state of the art the required gain and bandwidth values are very difficult to achieve in standard CMOS technology without a large power consumption making it non-practical when a large number of channels are required. For that reason the implementation of a VGA using the traditional operational amplifier with a negative feedback approach is only practical in SiGe technology due to its superior performance in therms of speed, noise and power consumption [37], [38]. For this reason its required the implementation of a VGA using alternative typologies.

3.1.1 Limiting Amplifier Topology

A Limiting Amplifier (LA) is a type of amplifier topology generally used in Optical Comunications Systems illustrated in Figure 3.1. It is build out of a Core amplifier and a offset compensation circuit. The core amplifier consists of a cascade of low gain differential voltage amplifiers, generally formed by a simple resistively-load differential pairs. The offset compensation feedback loop reduces the differential offset form the output voltage signals of the Core amplifier and is formed of a low-pass filter followed by an auxiliary differential amplifier.

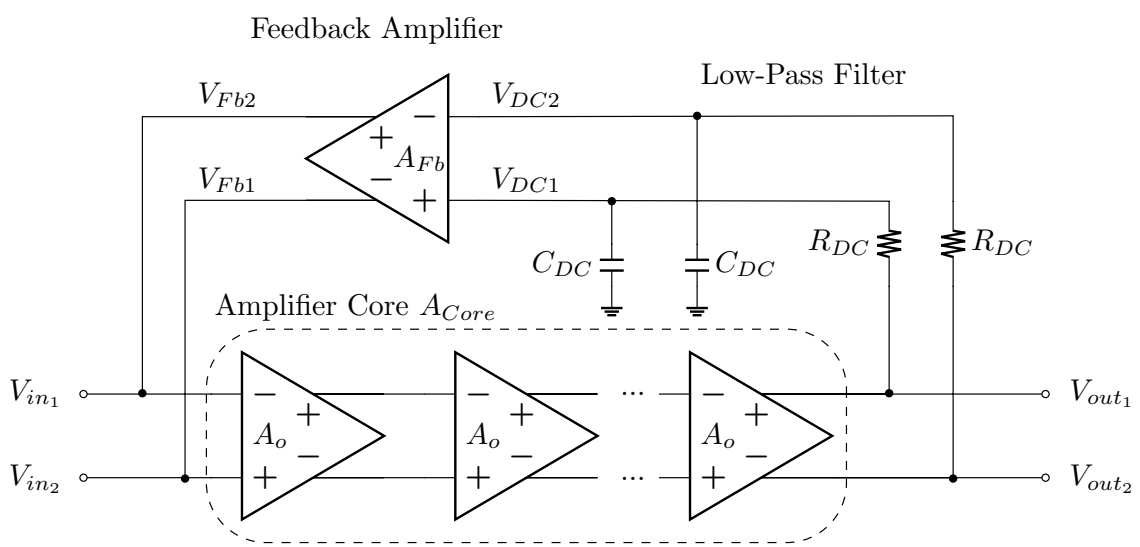


Figure 3.1: Block diagram of a LA with offset compensation.

typically defined as a ratio of two elements, defines its gain value

Almost all the LA are fully differential [2], this technique offers superior immunity to common mode and power supply variations performance at the expense of double the power consumption in comparison to single ended amplifiers [3] [13].

Gain and Bandwidth of the Amplifier Core

Typically an amplifier is implemented with an Operational Amplifier in a feedback loop and must be stable under the working conditions, a limiting amplifier do not require any stability requirements, only an offset compensation loop which is substantially slow in comparison with the main frequencies of the LA. For this reason a dominant pole is not a great concern and a cascade of low gain stages is possible [43].

Consider the circuit shown in figure 3.1, where the Amplifier Core is build out of a cascade of N ideal voltage amplifiers, each with a gain A_o, output resistance R_{out} and a load capacitance C_L, illustrated in 3.2. The overall transfer function of the Amplifier Core is:

$$H(s) = \left(\frac{A_o}{1 + \frac{s}{\omega_o}} \right)^N \tag{3.1}$$

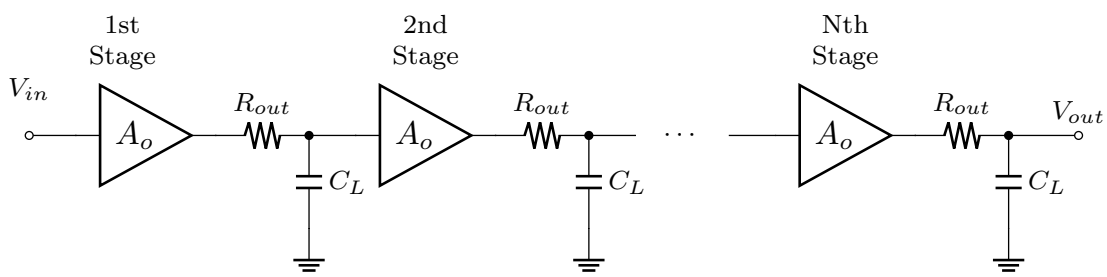


Figure 3.2: Cascade of ideal voltage amplifiers.

Where $\omega_o = 1/(R_{out}C_L)$ is the bandwidth of each stage. The total output gain of the core amplifier A_{Core} is equal to the gain of a single stage A_o times the number of stages:

[2] In a fully differential circuit both the input and output signals are represented by the difference of two voltages rather than a single voltage to ground.

[3] Some of their advantages are: reduced sensitivity to system noise, reduced generation of transient noise and improved voltage swing [43].

$$A_{Core} = A_o^N \tag{3.2}$$

Now to obtain the resulting bandwidth of the cascade of N amplifiers assume $s = j\omega_{tot}$.

$$\left(\frac{A_o}{\sqrt{1 + \left(\frac{\omega_{tot}}{\omega_o}\right)^2}} \right)^N = \left(\frac{A_o}{\sqrt[N]{2}} \right)^N \tag{3.3}$$

Solving for ω_{tot} the total bandwidth of the Amplifier Core results in:

$$\omega_{tot} = \omega_o \sqrt{\sqrt[N]{2} - 1} \tag{3.4}$$

Observing equation 3.4, shows that in order to obtain an output bandwidth of ω_{tot} the bandwidth of each stage ω_o should be larger than the total bandwidth. For instance, for a given total bandwidth ω_{tot} in a four stages LA $N = 4$, each stage should have a bandwidth of $\omega_o = 2.3\omega_{tot}$.

Once the total gain and bandwidth of the Amplifier Core has been calculated is imperative to calculate the optimal number of stages for a LA, so the gain-bandwidth extension of N cascaded stages compared to a single stage is calculated, resulting in:

$$\frac{GBW_{total}}{GBW_{stage}} = \frac{A_{Core}\omega_{tot}}{A_o\omega_o} = A_{Core}^{1-1/N} \sqrt{\sqrt[N]{2} - 1} \tag{3.5}$$

For example, to calculate the number of optimal stages in a LA with a total gain of $A_{Core} = 30dB$, equation 3.5 is ploted in figure 3.3. It shows that the Gain-Bandwidth (GBW) extensions finds its maximum at approximate 7 stages and then decreases continuously.

Therefore the optimal number of stages corresponds to the maximum gain-bandwidth extension per stage, differentiating equation 3.5 with respect to N, results in [44]:

$$N_{opt} = 2 \ln A_{Core} \tag{3.6}$$

The optimal number of stages using 3.6 is $N_{opt} \approx 7$. Nevertheless figure 3.3 shows that only in the first 5 stages the increment is very significantly, so a further increase has a negligible effect in the gain-bandwidth extension and only making the contribution of the noise for each stage significant. For this reason a cascade of amplifiers employ no more than 5 stages [44], [43].

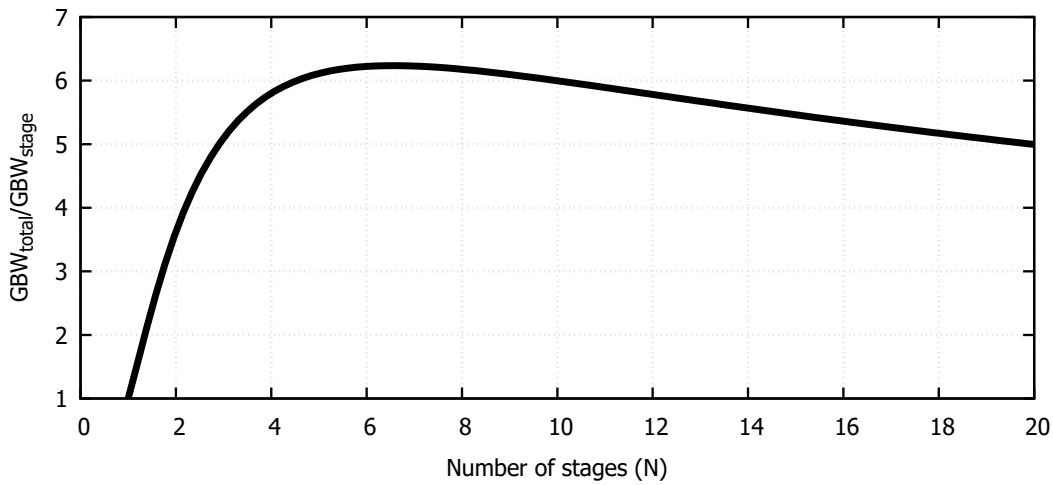


Figure 3.3: Gain-Bandwidth extension as a function of the number of stages N.

Noise of the Amplifier Core

The input-referred noise of limiting amplifiers is very important because as seen in section 2.2, noise is a factor that directly affects both energy and time measurements in a radiation detector. The large bandwidth of the LA produce a significant RMS output noise.

The input referred noise $\overline{V_{n,in}^2}$ of a limiting amplifier with N identical stages can be expressed as a function of the noise of a single stage $\overline{V_{n,i}^2}$ [45]:

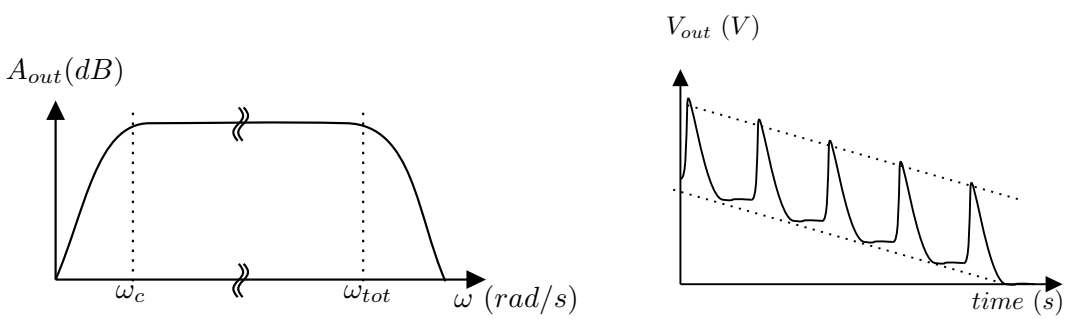
$$\overline{V_{n,in}^2} = \overline{V_{n,i}^2} \sum_{j=1}^{N} \frac{1}{A_o^{2(j-1)}} \tag{3.7}$$

Equation 3.7 demonstrates that the first stage of the limiting amplifier has the greatest contribution in the input-referred noise.

Offset Compensation

The offset of a limiting amplifier should be kept as low as possible to avoid saturation of the outputs due to device mismatch [46], therefore an offset compensation circuit is required [47]. Figure 3.1 illustrates a classical implementation of a limiting amplifier with an offset compensation circuit consisting of a low-pass filter and a feedback amplifier. The DC value of both voltage outputs is extracted trough a low-pass filter $R_{DC}C_{DC}$. The output offset value $V_{DC} = V_{DC2} - V_{DC1}$ is amplified by a Feedback Amplifier A_{Fb}, the output signal is returned to the input to reduce the output voltage offset until its becomes zero [47].

The offset compensation circuit diminish the unwanted offset voltage and some low-frequency components of the input signal. Therefore the frequency response of a Limiting Amplifier experiences a low-frequency cut-off [43], seen in Figure 3.4(a).



(a) Frequency response of a Limiting Amplifier with an offset compensation circuit.

(b) Baseline Wander in a Limiting Amplifier.

Figure 3.4: Effects of the offset compensation feedback loop.

For the configuration in Figure 3.1 the cut-off frequency is given by [47], [48]:

$$\omega_c = \frac{A_{Core}A_{Fb} + 1}{R_{DC}C_{DC}} \tag{3.8}$$

In Equation 3.8, $A_{Core}A_{Fb}$ is the closed-loop gain, since the gain of the amplifier core A_{Core} is one of the main specifications, the gain of the feedback loop is close to unity [46], [43], and the cut-off frequency should fall in the range of a few hertz up to tens of kilohertz to eliminate baseline wandering, visualized in Figure 3.4(b),

the required values of R_{DC} and C_{DC} for the low-pass filter are enormous. In CMOS technologies these high values can be implemented using MiM capacitor with high capacitance per unit square and high-ohmic poly resistors [47]. In order to reduce chip area, several implementations employ pMOS transistor in triode, cut-off or sub-threshold in combination with nMOS varactors, [46], [49], [50].

Just as any feedback system where its required to verify the stability of the loop, in the offset compensation feedback loop, this is not a issue because the dominant open-loop pole, required to be at a very low frequency to meet the ω_c requirements, is far form the high frequency poles, allowing a high loop gain without violating any phase margin [43]. A more detailed analysis of the offset compensation feedback loop is presented by Mullet et. all [45].

3.1.2 Proposed Voltage Preamplifier

As stated before, the proposed voltage preamplifier, illustrated in Figure 3.5, is based on the topology of a Limiting Amplifier because of its large bandwidth and gain characteristics as well as the possibility to analog process the output signal when a mechanism of gain adjustment is used, therefore the proposed amplifier is a fully-differential limiting amplifier with adjustable gain.

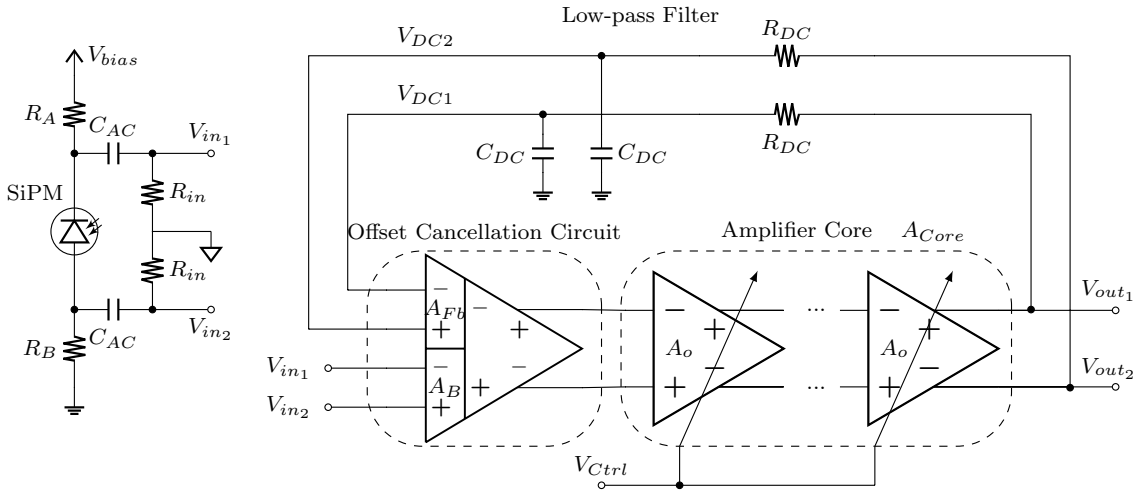


Figure 3.5: Proposed Variable Gain Amplifier.

In order to acquire the fully-differential signal that the LA requires, the cathode and anode of the SiPM is connected to an AC coupling capacitance C_{AC} and then to the input resistance R_{in} which form a high-pass filter. As a result only the high frequency components of the SiPM signal are visible to the input of the voltage amplifier and the circuit is isolated to the high DC bias voltage of the sensor, this connection is based on the one found in the PETA integrated circuit [39] however, to avoid the input signal from floating, the input resistance R_{in} is connected to analog ground.

The input signal passes through an offset cancellation circuit which has two main purposes, first serves as an input buffer for the SiPM signal A_B, and as a feedback amplifier A_{Fb} for the offset cancellation feedback loop. The output voltage is amplified by the amplfier core, consisting of a cascade of variable gain amplifiers controlled by an external potential V_{ctrl}. The variable gain characteristic of the amplifier core avoids the saturation of the voltage amplifier and thus increases its input dynamic range. Finally, the DC component of the output voltage is measured with a very low-pass filter, amplified by the feedback amplifier and used to reduce the differential output offset. Each of the functional blocks of the proposed voltage preamplifier are discussed bellow.

Single Stage of the Amplifier Core

Typically the gain of voltage amplifier is directly proportional to its transconductance, and its output load[4], therefore, to modify the amplification factor one of two is altered, usually the latter is selected, however the output load also establishes its bandwidth[5]. Additionally, as explained in section 3.1.1, a small reduction of the bandwidth in the single stages produces a significant reduction on the bandwidth of the amplifier core . So a mechanism to select the gain factor with a minimal alteration of the bandwidth is

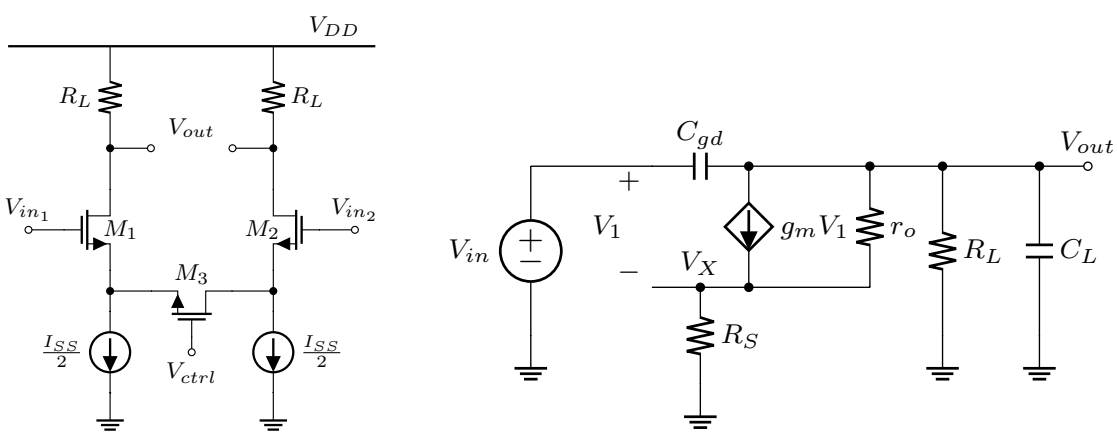
[4]The gain of a voltage amplifier is delivered by $A_o = G_m R_L$ where the transconductance G_m is the capability of transform the input voltage into an output current and the output load R_L converts this current once again into voltage.

[5]The output load of the amplifier and its capacitive load form a dominant pole in the transfer function of the amplifier, it is similar to the analysis in section 3.1.1.

required. Furthermore, in order to correctly bias a cascade of variable gain amplifiers, the common mode voltage should be constant regardless of the selected gain value, however in the resistively-loaded differential pair, the basic circuit of a limiting amplifier, the load resistor directly affects the output common voltage. Therefore the single stage of the core amplifier requires a mechanism to select the voltage gain with minimal alteration of the common mode voltage and bandwidth.

To achieve the discussed specifications a resistively-loaded differential pair with a variable degeneration resistor implemented with a MOS transistor in the triode region is proposed, illustrated in Figure 3.6(a). The gain is adjusted by the local feedback loop created by the degeneration resistor R_S implemented by transistor M3, leaving unaffected the load resistor R_L thus the bandwidth remains constant. In order to maintain the DC operating point unaffected, the tail current of the differential pair is spitted in two halves, this ensures a steady common-mode voltage because the degeneration resistor only affects the small signal behavior of the circuit [13].

With the objective to confirm the bandwidth and gain affirmations of the proposed amplifier, the small signal equivalent circuit, visualized in Figure 3.6(b), is analyzed.



(a) Proposed resistively-loaded differential pair with a variable degeneration resistor.

(b) Small signal equivalent of the proposed circuit.

Figure 3.6: Tuneable degeneration resistance.

The resulting transfer function $A_v(s)$ is:

$$A_v(s) = \frac{A_o\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_{out}}\right)} \tag{3.9}$$

Where ω_z and ω_{out} are the magnitude of the zero and pole respectively and A_o is the low-frequency gain. Interestingly, if an ideal transistor is used and the channel-length modulation is neglected, by making $r_o \to \infty$, the influence of the degeneration resistor R_S is eliminated to the pole as seen in equation 3.12.

$$A_o = -\frac{g_{m1}r_{o1}R_L}{R_L + r_{o1} + R_S + g_{m1}r_{o1}R_S} \approx -\frac{g_{m1}R_L}{1+g_{m1}R_S}\bigg|_{r_{o1}\to\infty} \tag{3.10}$$

$$\omega_Z = \frac{g_{m1}r_{o1}}{C_{gd1}(r_{o1} + R_S + g_{m1}r_{o1}R_S)} \approx \frac{g_{m1}}{C_{gd1}}\frac{1}{(1+g_{m1}R_S)}\bigg|_{r_{o1}\to\infty} \tag{3.11}$$

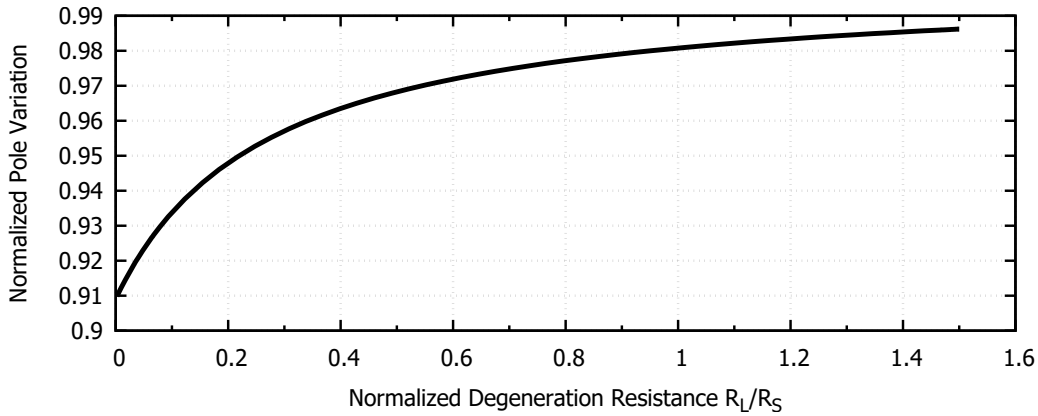
$$\omega_{out} = \frac{R_L + r_{o1} + R_S + g_{m1}r_{o1}R_S}{(C_{gd1}+C_L)(r_{o1} + R_S + g_{m1}r_{o1}R_S)R_L} \approx \frac{1}{(C_{gd1}+C_{out})R_L}\bigg|_{r_{o1}\to\infty} \tag{3.12}$$

Now to know at what extend the approximation of an ideal transistor is valid, the variation of the output pole from the ideal value against the degeneration resistance is ploted and visualized in Figure 3.7(a). It demonstrates, that its magnitude approaches to the ideal value as R_S is increased, so for a lower gain values, the bandwidth of the amplifier augments, and an overall variation of 10% is expected from the complete expression against the ideal transistor one.

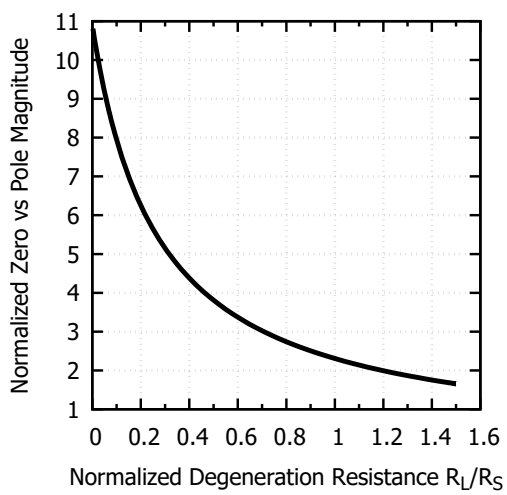
In order to avoid any influence of the zero in the operation of the amplifier, its magnitude ω_z should be two times larger than the pole ω_{out}. Figure 3.7(b) shows the normalized zero vs pole magnitude variation to R_S, the zero influence in the transfer function begins to be noticeable when $R_S > R_L$. Finally, the gain variation of the amplifier against R_S, shown in 3.7(c), is not linear, therefore when the degeneration resistor is reduced the gain is expected to increase rapidly. Since the current is proportional to the voltage in a MOS transistor when is in the linear region, the implementation of the degeneration transistor R_S is made by M3.

As shown in equation 3.13, the equivalent resistance of the transistor is proportional to its process constant $\mu_n C_{ox}$, length-to-width ratio and its overdring voltage, therefore by modifying its gate voltage the equivalent resistance can be manually selected.

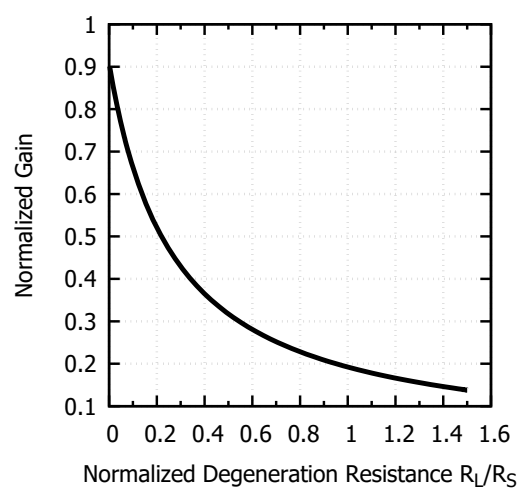
$$R_S = \frac{1}{\mu_n C_{ox}(V_{gs} - V_{th3})} \left(\frac{L}{W}\right)_{M3} \tag{3.13}$$



(a) Pole Variation agains the ideal value.



(b) Zero vs Pole magnitude.



(c) Gain vs normalized generation resistance.

Figure 3.7: Small signal parameters of the proposed differential pair against R_S.

Since the degeneration resistor is not located in the output branch, the output

common mode voltage $V_{CM,out}$ is only defined by the tail current and the output load resistor R_L. Therefore

$$V_{CM,out} = V_{DD} - \frac{1}{2} I_{SS} R_L \tag{3.14}$$

The input common mode voltage $V_{CM,in}$ must be high enough to ensure the correct operation of the tail current source and the input transistor but bellow the point where the input transistor exits saturation and reaches the triode region, this condition is valid for:

$$V_{gs1} + V_{sat,ISS} < V_{CM,in} < V_{CM,out} + V_{th} \tag{3.15}$$

The output voltage swing of a single branch of the voltage amplifier is defined by its tail current and its load resistor as:

$$V_{DD} - I_{SS} R_L < V_{out1,2} < V_{DD} \tag{3.16}$$

Since in a fully-differential circuit, the output voltage is equal to the difference of two potentials rather than a voltage to ground, its output swing is doubled, therefore the maximum voltage swing of the voltage amplifier is:

$$V_{swing} = 2 I_{ss} R_L \tag{3.17}$$

To compute the input referenced voltage noise, only a half of the differential pair is analyzed. The half part of the amplifier with its noise current sources is shown in in figure 3.8 and its input-referred noise is:

$$\overline{V_{n,in1}^2} = \frac{R_L^2}{A_o^2} \overline{I_{n,RL}^2} + \frac{\overline{I_{n,m1}^2}}{g_{m1}^2} + R_S^2 (\overline{I_{n,RS}^2} + \overline{I_{n,mIss}^2}) \tag{3.18}$$

Equation 3.18 indicates that the noise of the amplifier varies with respect to the value of R_S, the noise generated from the tail current is uncorrelated for each input transistor and therefore is added to the output voltage. Therefore the input referenced noise is dominated by the degeneration resistor $\overline{I_{n,RS}^2}$ and the tail current source $\overline{I_{n,mIss}^2}$. Since the voltage amplifier uses a fully-differential configuration, the input reference noise of the complete differential pair is the sum of both half circuits.

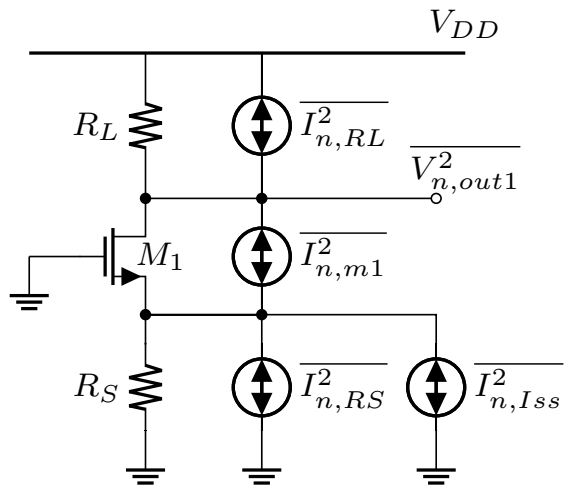


Figure 3.8: Noise equivalent circuit of the half part of the core amplifier.

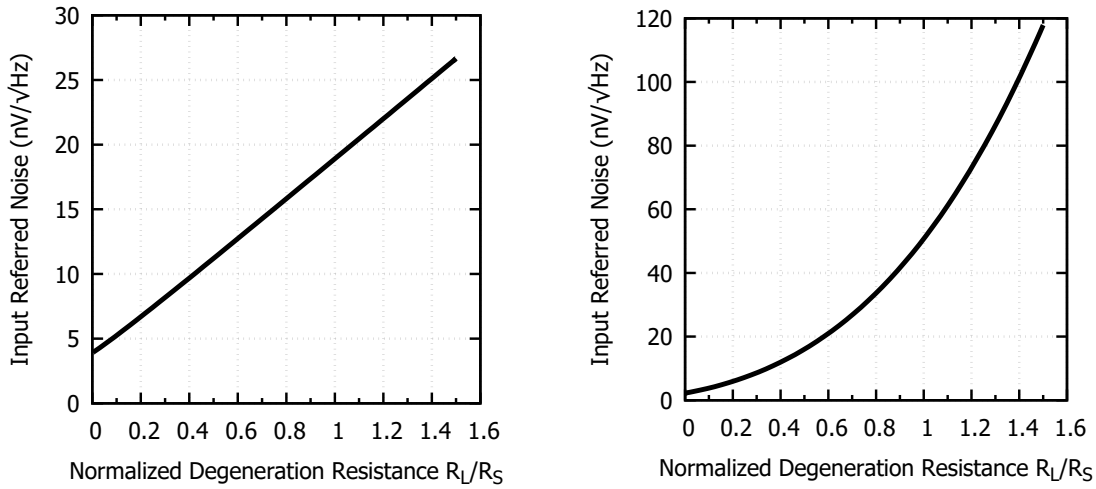
$$\overline{V^2_{n,in}} = \overline{V^2_{n,in1}} + \overline{V^2_{n,in2}} = 2\overline{V^2_{n,in,1}} \tag{3.19}$$

With the intention of evaluate the behaviour of the input referenced voltage noise with respect to the degeneration resistor R_S equation 3.18 is ploted and showed in Figure 3.9(a), as expected $\overline{V_{n,in1}}$ is directly proportional to R_S and in order to minimize its impact, a reduction on the tail current noise or an small degeneration value should be used. Now to estimate the noise of the complete amplifier core $\overline{V_{n,in,core}}$ against R_S, equation 3.18 is evaluated into equation 3.7, and selecting a total number of four stages $N = 4$, the input-referred noise of the amplifier core is ploted in Figure 3.9(b), it shows that the noise increases exponentially when a lower gain is selected.

Even thought the proposed amplifier core satisfy the gain, bandwidth and common mode voltage requirements, its noise performance is highly affected by the gain variation, therefore special attention into its calculation should be carried out to accomplish the radiation detector specifications.

Offset Cancellation Circuit

In Figure 3.1 the output of the feedback amplifier is directly connected to the input signal of the amplifier core which is attached to the input resistor R_{in}, as seen in previous



(a) Single Stage variable amplifier.

(b) Four stage variable amplifier core.

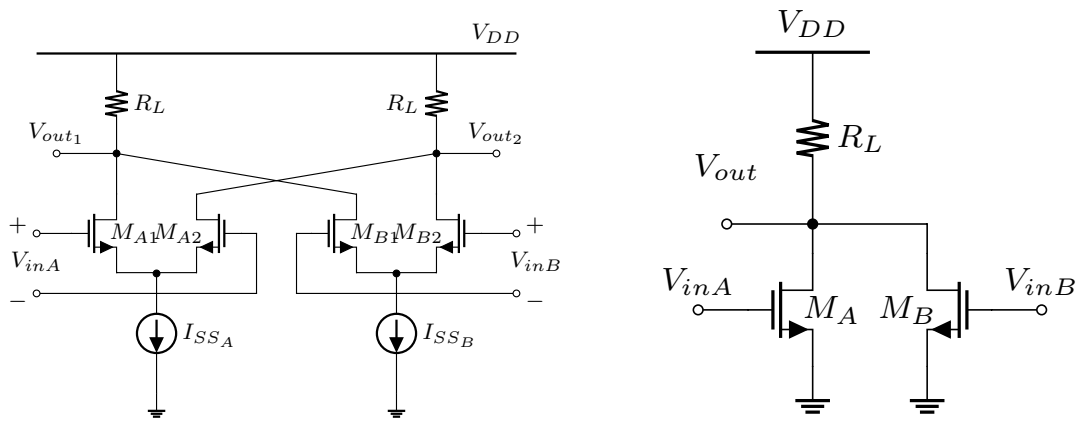
Figure 3.9: Input referred noise against the degeneration resistor R_S.

sections this resistor must have a small values, on the order of 50Ω, therefore, to modify this potential the feedback amplifier would require a large current consumption. The proposed offset cancellation circuit, seen in Figure 3.5, uses a Differential Difference Amplifier (DDA) , figure 3.10(a), that is, a differential amplifier with two inputs, one is used for the input signal and the other to the DC offset compensation.

The Differential Difference Amplifier subtracts the difference of two differential signals, consider the input signal V_{in_A}, its positive signal is converted into current by transistor M_{A1} $I_{D_{A1}}$ and sent to R_L, now the negative part of V_{in_B} generates a drain current in the transistor M_{B1} $I_{D_{B1}}$ and is also sent to R_L, since the potential of both input signals is reversed, the currents have different directions, thus the output voltage is the result of its subtraction. This behavior can be analyzed by only using the half-circuit equivalent of the DDA, seen in Figure 3.10(b).

In order to formally analyze the behavior of the DDA, the small signal equivalent circuit, seen in figure 3.11, is extracted from its half-circuit equivalent.

The output voltage is equal to the subtraction of both input potentials:



(a) Complete circuit. (b) Half-circuit of the DDA.

Figure 3.10: Differential Difference Amplifier.

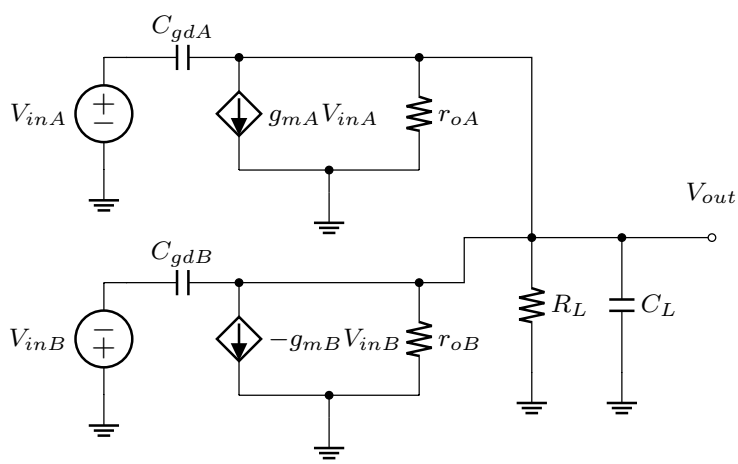


Figure 3.11: Small signal equivalent circuit.

$$V_{out} = -\frac{(g_{mA} - sC_{gdA})V_{inA} - (g_{mB} - sC_{gdB})V_{inB}}{\frac{1}{R_L||r_{oA}||r_{oB}} + (C_{gdA} + C_{gdB} + C_{out})s} \tag{3.20}$$

Now, if all the transistors are matched and have the same dimensions, then $C_{gdA} = C_{gdB} = C_{gd}$, $g_{mA} = g_{mB} = g_m$, then the output voltage is reduced to:

$$V_{out} = -\frac{(g_m - sC_{gd})(V_{inA} - V_{inB})}{\frac{1}{R_L||r_{oA}||r_{oB}} + (2C_{gd} + C_{out})s} \tag{3.21}$$

From Figure 3.5, is observed that $V_A = V_{in}$ is the input signal and $V_B = V_{DC}$ is the DC voltage of the output of the core amplifier, then the output voltage of the amplifier

is equal to

$$V_{out} = -\frac{(g_m - sC_{gd})(V_{in} - V_{DC})}{\frac{1}{R_L||r_{oA}||r_{oB}} + (2C_{gd} + C_{out})s} \tag{3.22}$$

Since V_{DC} has a much lower frequency component, the frequency components of the DDA only affects the input signal. The system has one zero and one pole located at:

$$\omega_{out} = \frac{1}{(R_L||r_{o1}||r_{o2})(C_{out} + 2C_{gd})} \tag{3.23}$$

$$\omega_z = \frac{g_m}{C_{gd}} \tag{3.24}$$

Now considering that the pole and the zero of the system are located far from the frequency components of the input signal, the output voltage is equal to the superposition of the input signal an offset correction factor amplified by the low frequency gain of the DDA:

$$V_{out} = -g_m(R_L||r_{oA}||r_{oB})(V_{in} - V_{DC}) = -A_{Fb}(V_{in} - V_{DC}) \tag{3.25}$$

As stated in section 3.1.1, by incorporating the feedback loop in the proposed voltage amplifier, its frequency response experiences a low-frequency cut off, the corner frequency of the proposed voltage amplifier is [48]:

$$\omega_c = \frac{A_c A_{Fb} + 1}{R_{DC} C_{DC}} \tag{3.26}$$

In equation 3.26, A_c, A_{Fb} are the gains of the Amplifier Core and the DDA respectively, R_{DC} and C_{DC} are the passive elements used to extract the DC component of the output voltage. Since the values of the low-pass filter are enormous, it would require a considerable amount of area if they are implemented with MiM capacitors or Poly resistors [49]. Given that in a radiation detector, the number of channels which can fit in an integrated circuit is inversely proportional to their area, a mechanism to reduce its required space is necessary. To minimize the chip area a pMOS transistors operating in cut-off region are employed as R_{DC} and a nMOS varactor is used as a C_{DC},

this implementation, visualized in 3.12, is based on the ones implemented by Huang et al [48] and Wu et al. [50].

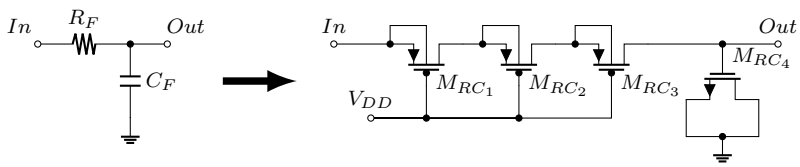


Figure 3.12: Low pass filter implemented with MOS transitors.

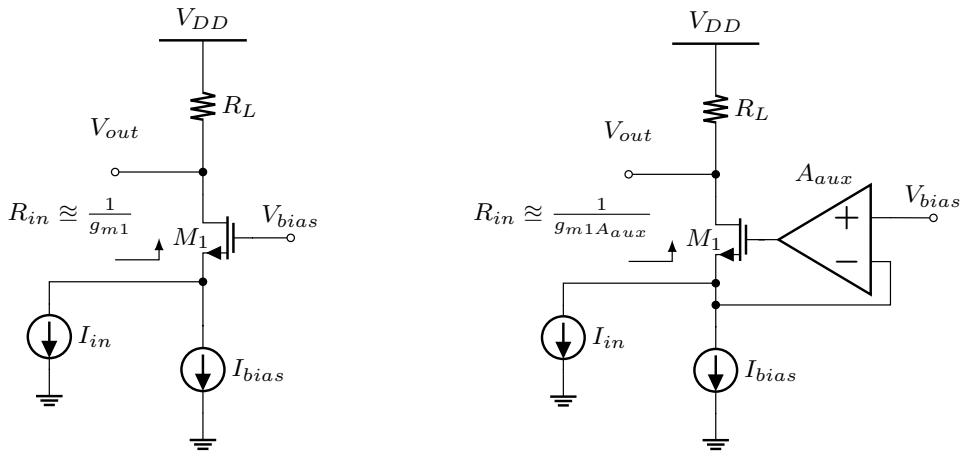
3.2 Current Preamplifier

In section 2.2 it was noted what the current buffer readout approach directly reads the SiPM sensor current in its low input impedance node and replicate it at a high impedance output node, when the output current is sent to a current mirror, the SiPM signal magnitude can be manipulated to achieve the required input dynamic range specifications. Furthermore, the large bandwidth specifications required for time measurements are much easier to achieve in current amplifier at a lower power consumption compared to a voltage amplifier readout [11].

Since the current amplifier inherently fulfill most of the preamplifier requirements, the input impedance R_{in} of the selected current buffer should be the greatest concern in the choice of the correct topology. Given that a lower R_{in} enhances the time measurement and increases the maximum event rate of the radiation detector, a topology with a very low input impedance is preferred.

Two of the most widespread current buffer architectures implemented in a radiation detector for SiPM sensors are the Common Gate (CG) amplifier and the Regulated Common Gate Amplifier (RCG), visualized in Figure 3.13.

For both amplifiers consider the case where their high frequency components do not interfere with their performance and only the low-frequency behavior is considered. In the case of a CGA the input impedance is approximately:



(a) Common Gate amplifier.

(b) Regulated Common Gate amplifier.

Figure 3.13: Commonly used current preamplifiers in radiation detectors.

$$R_{in,CGA} \approx \frac{1}{g_m} \tag{3.27}$$

Equation 3.27 is the smallest input impedance that a single transistor without a feedback loop can deliver. For instance, to ensure an input resistance R_{in} of 50Ω a transconductance of $g_{m1} = 20mS$ is required, this necessities ether a very large transistor, thus penalizing the high frequency behaviour of the amplifier, or to bias the transistor with a current of a few mA[6], therefore increasing the power consumption and rising the layout complexity because of the challenges that accompany the required size of the metal routing for such current.

One way to reduce the input impedance without increasing the size or the drain current of the transistor, is the use of a feedback loop. This is accomplished by the aid of an Auxiliar Amplifier that senses the source of M1 and then forces transistor M1 to reach V_{bias}, as a result the input impedance of the *Regulated* Common Gate amplifier is equal to the transimpedance of M1 times the voltage gain of the axuliar transistor A_{aux}.

[6]The transconductance of a MOS transistor using the first level model is $g_m = k'\frac{W}{L}(V_{gs} - V_{Th}) = 2I_D/(V_{gs} - V_{th})$, where k' is the constant process, W/L is the width-to-length ratio of the transistor, $V_{gs} - V_{th}$ is the overdrive potential, and I_D is the drain current of the transistor.

$$R_{in,RCG} \approx \frac{1}{g_m A_{aux}} \tag{3.28}$$

Even thought, this ensures a lower input impedance than the CGA, the gain of the auxiliary amplifier cannot be very large due to bandwidth limitations, furthermore the design of the auxiliary amplifier may increment the complexity of the current buffer.

The current readout implementation requires the low input impedance of the RCGA and the simplicity of the CGA. The Flipped Voltage Follower Current Sensor (FVFCS) has exactly this qualities. Its input impedance is even lower than the RCGA and it allows to its input to sink a large amount of current [51], a desirable characteristic when a SiPM with a large number of cells needs to read. For this reason in this work a FVFCS is proposed to readout SiPM signals.

3.2.1 Proposed Current Buffer Preamplifier

As mentioned above, the proposed current buffer is based on the FVFCS topology because of its very low input impedance R_{in}. The anode of the SiPM sensor is directly connected to the input node of the current buffer, illustrated in Figure 3.14. When a microcell is fired, the sensor produces a current which enters transistor M1, the internal feedback mechanism generates a potential V_X proportional to the input current I_{in}. Transistor M3 converts V_X into I_{out} and then, if required, is once again transformed into voltage V_{out} trough the load resistor R_L.

Interestingly, even thought the feedback loop of the FVFCS is composed by transistors M1 and M2, the M1 and M3 pair behave as a current mirror, thus if a chain of transistors is connected in parallel to M3 with various sizes, multiple copies of I_{in} with different amplification factors can be formed. As studied in section 2.2.3, a unitary copy may be used by the discriminator to measure time and a scaled down duplicate could be used by a CSA or an integrator to measure energy.

To analyze the behavior of the FVFCS when coupled to a SiPM sensor, the schematic of Figure 3.14 is redrawn with its simplified electrical model and the parasitic capacitances of the transistors resulting in Figure 3.15(a) and its small signal equivalent

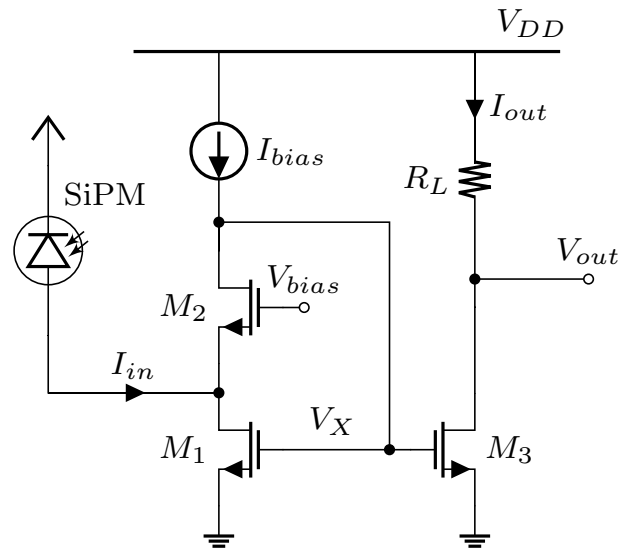


Figure 3.14: Proposed current preamplifier.

circuit in Figure 3.15(b).

From the small signal equivalent circuit of the FVFCS, the transimpedance R_o and the input impedance R_{in} transfer function are obtained. It is visible that R_o is the cascade of a transimpedance amplifier $R_X = I_{in}/V_X$ and a voltage amplifier $A_v = V_{out}/V_X$. R_{in} is calculated from V_{in}/I_{in}. Extracting the nodal equations and solving each section, the transfer function for R_o results:

$$R_o = R_X A_v = \frac{V_{out}}{I_{in}} \tag{3.29}$$

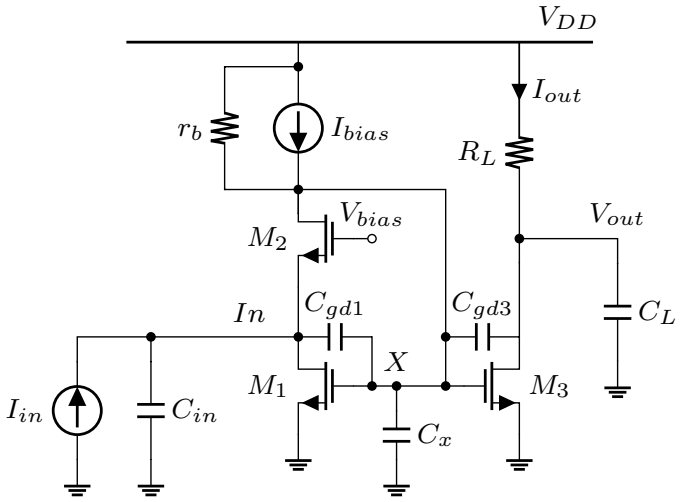
Where:

$$R_X = \frac{V_X}{I_{in}} \approxeq \frac{g_{m2} + \frac{1}{r_{o2}} + C_{gd1}s}{g_{m1}g_{m2} + \left(\frac{C_{in}}{r_b||r_{o2}} + C_X g_{m2}\right)s + C_X C_{in} s^2} \tag{3.30}$$

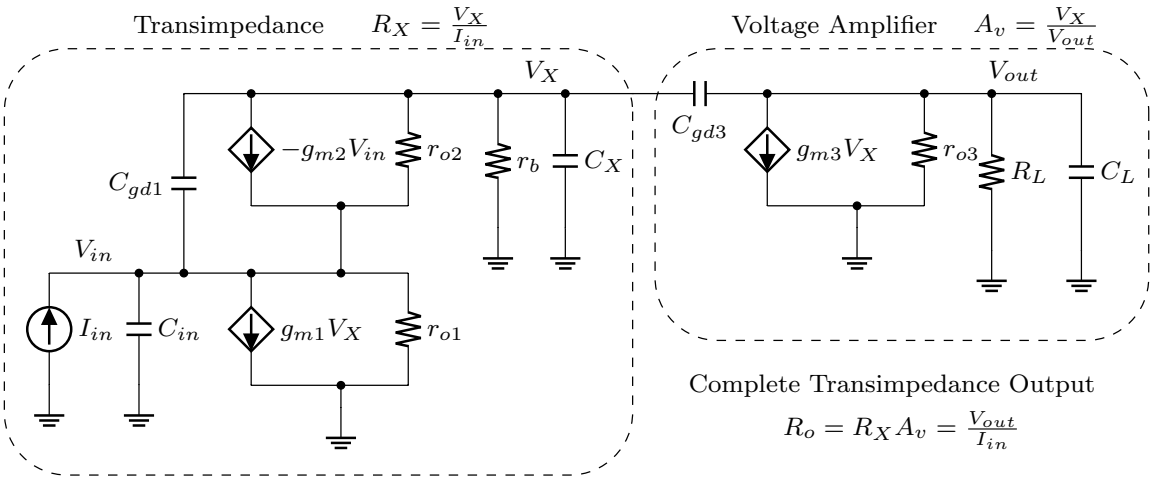
$$A_v = \frac{A_o\left(1 + \frac{s}{\omega_{Z_O}}\right)}{\left(1 + \frac{s}{\omega_{P1_O}}\right)} \tag{3.31}$$

And the transfer function of the input impedance of the FVFCS is:

$$R_{in} = \frac{V_{in}}{I_{in}} \approxeq \frac{\frac{1}{r_b||r_{o2}} + (C_{gd1} + C_x)s}{g_{m1}g_{m2} + \left(\frac{C_{in}}{r_b||r_{o2}} + C_X g_{m2}\right)s + C_X C_{in} s^2} \tag{3.32}$$



(a) FVFCS coupled to the simplified electrical model of the SiPM sensor.



(b) Small signal equivalent circuit of the FVFCS.

Figure 3.15: Flipped Voltage Follower Current Sensor.

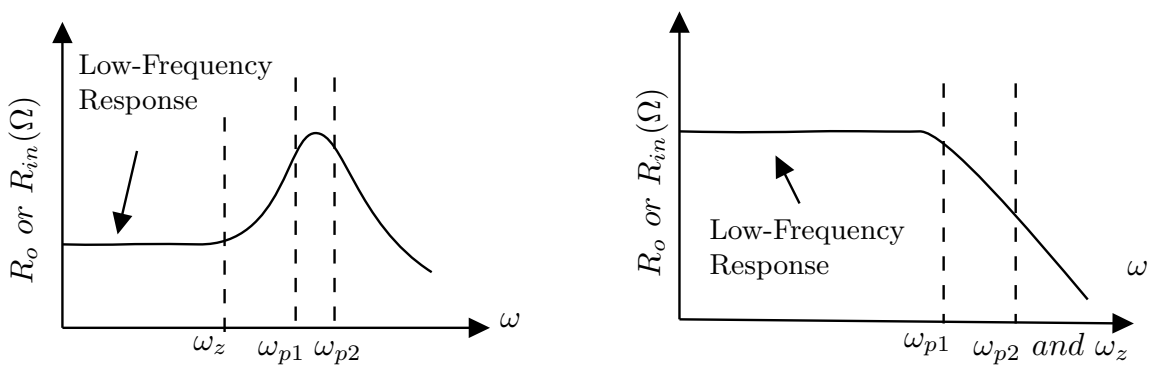
To better understand the frequency behavior of the FVFCS, the low-frequency value, dominant pole, secondary pole and zero of equations 3.30 ,3.31 and 3.32 are calculated considering the case where the input capacitance is very large $C_{in} \gg C_X$ [52], just like in the SiPM sensor, and summarized in Table 3.1.

Figure 3.16(a) illustrates the typical transimpedance R_o and input impedance R_{in}

	V_X/I_{in}	V_{out}/V_X	R_{in}
Low-Frequnecy Value	$R_o = \frac{1}{g_{m1}}\left(\frac{g_{m2}+\frac{1}{r_{o2}}}{g_{m2}}\right)$	$A_v = -g_{m3}(R_L\|\|r_{o3})$	$R_{in} = \frac{1}{g_{m1}g_{m2}(r_b\|\|r_{o2})}$
Dominant Pole	$\omega_{P1_X} \approx \frac{g_{m1}g_{m2}(r_b\|\|r_{o2})}{C_{in}}$	$\omega_{P1_O} = \frac{1}{(R_L\|\|r_{o3})(C_{gd3}+C_L)}$	$\omega_{P1_{Rin}} \approx \frac{g_{m1}g_{m2}(r_b\|\|r_{o2})}{C_{in}}$
Secondary Pole	$\omega_{P2_X} \approx \frac{1}{(r_b\|\|r_{o2})C_x}$	-	$\omega_{P2_{Rin}} \approx \frac{1}{(r_b\|\|r_{o2})C_x}$
Zero	$\omega_{Z_X} = \frac{1}{(r_{o2}\|\|\frac{1}{g_{m2}})(C_{gd1})}$	$\omega_{Z_O} = \frac{g_{m3}}{C_{gd3}}$	$\omega_{Z_{Rin}} = \frac{1}{(r_b\|\|r_{o2})(C_x+C_{gd1})}$

Table 3.1: Frequency response equations for the FVFCS.

behavior of the FVFCS. Note that ω_Z[7] occurs prior to ω_{P1} and ω_{P2} [8], which is undesirable for the SiPM readout because it rises the value of R_{in} and alters the duration of the pulse. Fortunately due to the very large equivalent capacitance of the SiPM, ω_Z is very close to ω_{P2}, therefore the influence of the zero is approximately canceled [52], and the low-frequency response begins to drop at ω_{P1}, as seen in Figure 3.16. To avoid the influence of the voltage amplifier in the frequency response of the FVFCS, ω_{P1_O} and ω_{Z_O} should be at least two times ω_{P1}.



(a) Typical behaviour of the FVFCS with its characteristic peaking.

(b) Behaviour of the FVFCS when a large input capacitance C_{in} is coupled.

Figure 3.16: Frequency response of the FVFCS.

[7]For the sake of simplicity, ω_{Z_X} and $\omega_{Z_{R_in}}$ are referred simply as ω_Z.

[8]Since the transfer function of R_o and R_{in} have the same denominator, their poles have the same magnitude therefore $\omega_{P1} = \omega_{P1_X} = \omega_{P1_{Rin}}$ and $\omega_{P2} = \omega_{P2_X} = \omega_{P2_{Rin}}$

Now, if all the high-frequency requirements are fulfilled, the low-frequency transimpedance gain of the FVFCS is proportional to the ratio of the transimpedance of transistors M1 and M3 times the load resistor R_L:

$$R_{O_{LF}} = \frac{1}{g_{m1}} \left(\frac{g_{m2} + \frac{1}{r_{o2}}}{g_{m2}} \right) g_{m3} R_L \approxeq \frac{g_{m3}}{g_{m1}} R_L \tag{3.33}$$

Since the transimpedance of a MOS transistor is equal to $g_m = \mu C_{ox} \frac{W}{L}(V_{gs} - V_{Th})$ and for both transistors $\mu C_{ox}(V_{gs} - V_{Th})$ is the same, because both are the same type of transistor and their gates are connected to the same potential V_X, the element that determines the amplification factor of the copy is the width-to-length ratio of both transistors β. Therefore $R_{o_{LF}}$ is equal to:

$$R_{O_{LF}} \approxeq \frac{(W/L)_{M3}}{(W/L)_{M1}} R_L = \beta R_L \tag{3.34}$$

If multiple transistors are connected in parallel of M3 with different width-to-length ratios β, several copies of the input current signal can be extracted and used to measure time and energy independently with out affecting each other.

Finally the low-frequency input impedance of the FVFCS:

$$R_{in_{LF}} = \frac{1}{g_{m1} g_{m2} (r_b || r_{o2})} \tag{3.35}$$

Equation 3.35 revels that the input impedance is proportional to the multiplcation of the transimpedance of transistors M1 and M2 times the equivalent impedance of the bias current source and the impedance of M2. The proposed circuit has a lower R_{in} than the one given by the conventional CG and the RCG typologies, therefore, a greater event rate and a better time measurement performance is expected than conventional implementations.

In order to correctly bias the FVFCS, V_{bias} should be selected so transistors M1 and M2 are in saturation. For M1 to be saturated is required $V_{gs1} - V_{th1} \leq V_{in} (= V_{bias} - V_{gs2})$ and $V_{bias} - V_{th2} \leq V_X (= V_{gs1})$. Therefore:

$$V_{gs2} + (V_{gs1} - V_{th1}) \leq V_{bias} \leq V_{gs1} + V_{th2} \tag{3.36}$$

In section 1.3.5, it was stated that the DC baseline of an amplifier should be selected closer to the positive or negative power rail in order to maximize the dynamic range of the output signal. Given that the voltage amplifier formed by transistor M3 inverts V_X, the output signal V_{out} is expected to move only downwards, illustrated in Figure 3.17. Therefore the DC baseline is given by $V_{out_{DC}} = V_{DD} - R_L \beta I_{bias}$ and the maximum output value is limited by the saturation voltage of M3 $V_{gs3} - V_{th3}$, thus the output voltage is located between:

$$V_{gs3} - V_{th3} \leq V_{out} \leq V_{DD} - R_L \beta I_{bias} \tag{3.37}$$

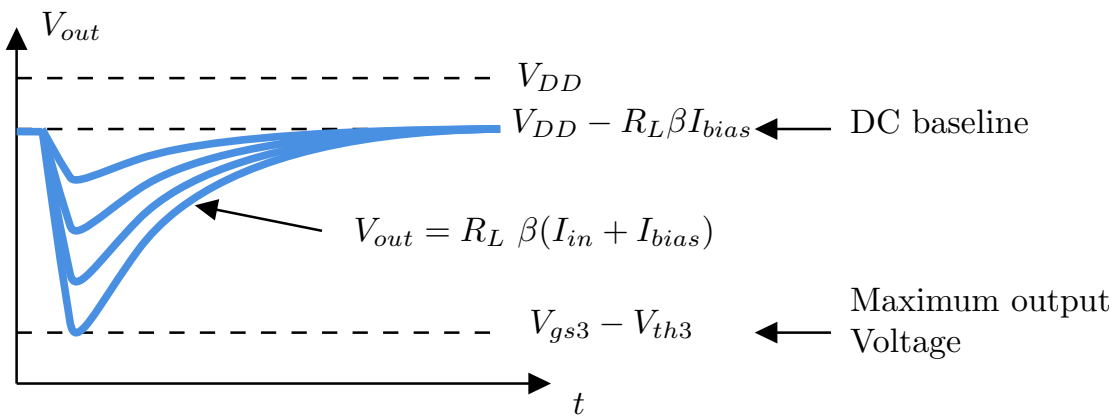


Figure 3.17: Output Voltage of the FVFCS.

For the purpose of incrementing the output dynamic range, the DC baseline must be as close as possible to V_{DD}, this brings the following issue: First, with the objective to increment the output transimpedance of the FVFCS, ether a large value of R_L or a greater width-to-length ratio β is required. Second, the increment of R_L, β or both, also increases the voltage across the load resistor R_L thus bringing the DC baseline downwards and reducing the output dynamic range. Therefore a tread-off between output transimpedance and output dynamic range should be made. One possible solution to this problem is to connect a current source in parallel to R_L whose task is to dis-balance the DC bias current βI_{bias}, and bring the DC baseline closer to V_{DD}, this approach could solve the discussed issue but it would increment the size of the output load capacitor C_L thus affecting the frequency response of the FVFCS.

Another factor that directly impacts the performance of the time and energy measurements is the input referenced current noise. It is calculated form the equivalent noise circuit shown in Figure 3.18. Applying the superposition principle in each of the noise current sources, the input-referred current noise is:

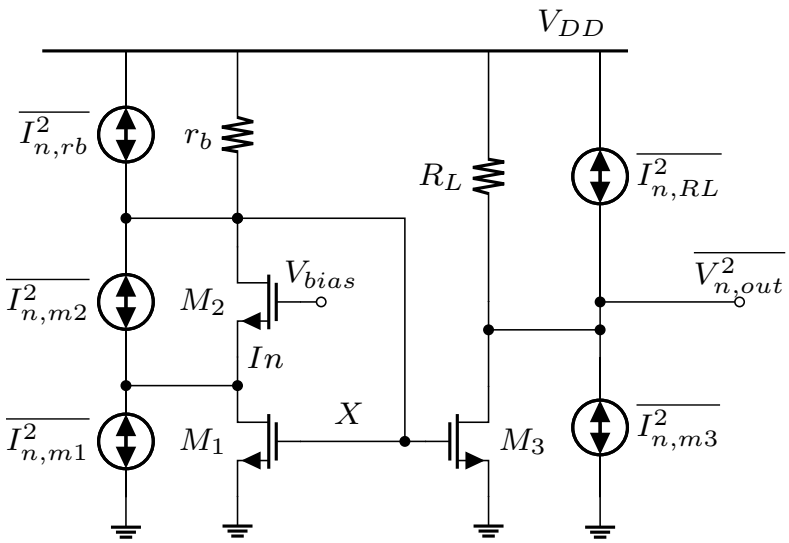


Figure 3.18: Equivalent noise circuit for the FVFCS.

$$\overline{I^2_{n,in}} = \left(\frac{g_{m1}}{g_{m3}}\right)^2 \overline{I^2_{n,RL}} + \left(\frac{g_{m1}}{g_{m3}}\right)^2 \overline{I^2_{n,m3}} + \overline{I^2_{n,m1}} + \frac{\overline{I^2_{n,m2}}}{(g_{m2}r_{o1})^2} + \overline{I^2_{n,rb}} \tag{3.38}$$

Equation 3.38 shows that the mayor noise constant contribution comes from the bias current source $\overline{I^2_{n,rb}}$ and transistor M1 $\overline{I^2_{n,m1}}$. Noteworthy, the contribution of the elements that conform the voltage amplifier, $\overline{I^2_{n,RL}}$ and $\overline{I^2_{n,m3}}$ are dependent on the inverse of the width-to-length ratio of both transistors β.

To study the noise behavior with respect to g_{m3}, equation 3.38 is ploted and shown in 3.19. If the signal copy is smaller than the unity $\beta < 1$, the noise contribution from $\overline{I^2_{n,RL}}$ and $\overline{I^2_{n,m3}}$ is rapidly amplified, on the contrary for $\beta \geq 1$, their contribution is not reduced substantially from the unitary case. With this information in mind, a unitary copy, in general used for timing measurements, would have the best noise performance, and an scaled down copy, generally used for energy measurements, would have a poorer noise performance.

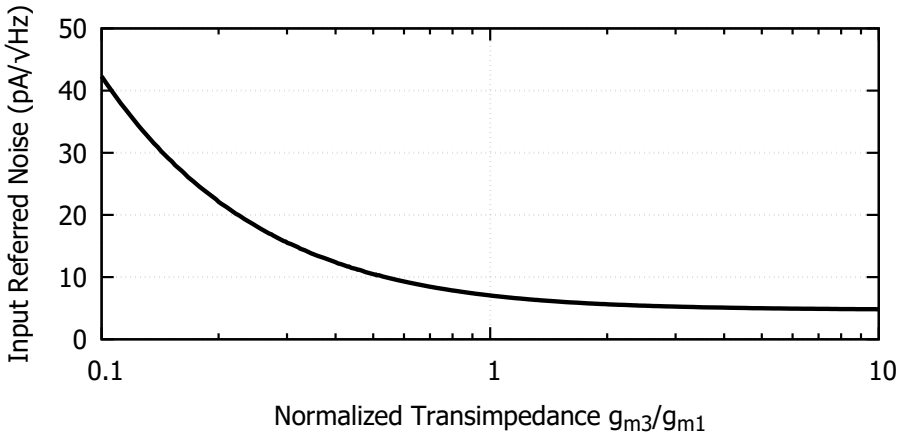


Figure 3.19: Output Voltage of the FVFCS.

3.3 Conclusions

According to the design requirements obtained for each readout approach in Chapter 2 a preamplifiers requires a large bandwidth, low noise and a sort of mechanism to modify its gain, from the three common readout approaches, the Charge-Sensitive-Amplifier, in spite of being the more used in radiation detectors, when coupled to a SiPM sensor has dynamic range and speed limitations due to its feedback capacitor. With this in mind, in this chapter the proposal of two preamplifiers using the voltage amplifier and current buffer approach has been introduced.

The voltage amplifier preamplifier is based on the Limiting Amplifier (LA) topology generally used in receivers for Optical Communication Systems (OCS). It consists of a cascade of fully-differential variable gain amplifiers, and a differential offset compensation feedback loop, composed of an auxiliary amplifier and a very low-pass filter. The variable gain mechanism of the proposed voltage amplifier maximizes its input dynamic range and keeps its bandwidth relatively unaltered, a highly required characteristic in timing measurements. Even thought the proposed topology satisfy the gain and bandwidth requirements, its noise performance is particularly sensible to the selected gain value, therefore special attention must be taken to fulfill the noise specifications.

For the current buffer readout, the proposed topology is based on the Flipped Voltage Follower Current Sensor (FVFCS), it exhibits a very-low input impedance, even

lower than the commonly used current buffer topologies used in SiPM readout implementations, which is highly recommended to increase the maximum count rate and enhance timing measurements. The FVFCS behaves as a current mirror which allows the creation of parallel paths with different gains ruled by the width-to-lenght ratio of the current mirror transistors β. This characteristic may be used to create independent paths to measure time and energy with their respective gain and bandwidth requirements. If the output current is converted into voltage, the transimpedance gain and the DC baseline is ruled by the load resistor R_L, therefore a tread-off between gain and dynamic range is unavoidable. The noise performance of the FVFCS degrades rapidly when a copy lower to the unity β is selected, on the contrary its performance is not enhanced for a larger copy gain values.

Chapter 4

Preamplifier Design.

From the existing readout architectures, the performance of the Charge-Sensitive Amplifier approach demonstrated to be limited in speed, noise and practicality due to the required value of its feedback capacitance, therefore the Voltage Amplifier and the Current Buffer proved to be the better suited to read signals form a SiPM sensor. In order to evaluate the performance of both alternatives, a design using both approaches is required to be later evaluated.

The objective of this chapter is to design both preamplifiers that fulfill the requirements of a generic radiation detector implemented with a SiPM sensor Hamamatsu S10931-050P with the requirements given in Table 4.1. This means to interpret the specifications of a radiation detector, translate them into electronic design parameters, design the required analog circuit to finally evaluate its energy and time performance.

Parameter	**Value**
ECR @ 10% PE	$\geq 1MHz$
Time Resolution	$\leq 1\mu s$
Charge Resolution	$\leq 1\mu cell$

Table 4.1: Generic Radiation Detector specifications.

4.1 Calculation of the Design Parameters

As described in section 1.3.8, the Pile-Up error (PE) is the probability that only one particle arrive at a given Event Interval (EI) , that is the Event Count Rate (ECR) time period, $EI = 1/ECR$. Since the arrival of the particles follows the Poisson distribution, as in equation 1.9, this probability is related to the SiPM pulse duration. According to equation 2.14, the pulse duration is associated to its slow time constant $\tau_s = \tau_r + C_S R_{in}$ which is proportional to the input resistance R_{in}. Combining this equations, the Pile-Up error probability of the SiPM is given by expression 4.1.

$$P(k=0) = 1 - e^{-\lambda}, \qquad \lambda = \frac{Pulse\ Duration}{Events\ Interval} = 5(\tau_r + C_S R_{in})ECR \tag{4.1}$$

Obtaining the equivalent slow capacitance of the SiPM C_S from table 1.1 and ploting equation 4.1, the probability of error in percentage against the Event Count Rate and the Input Resistance is shown in Figure 4.1.

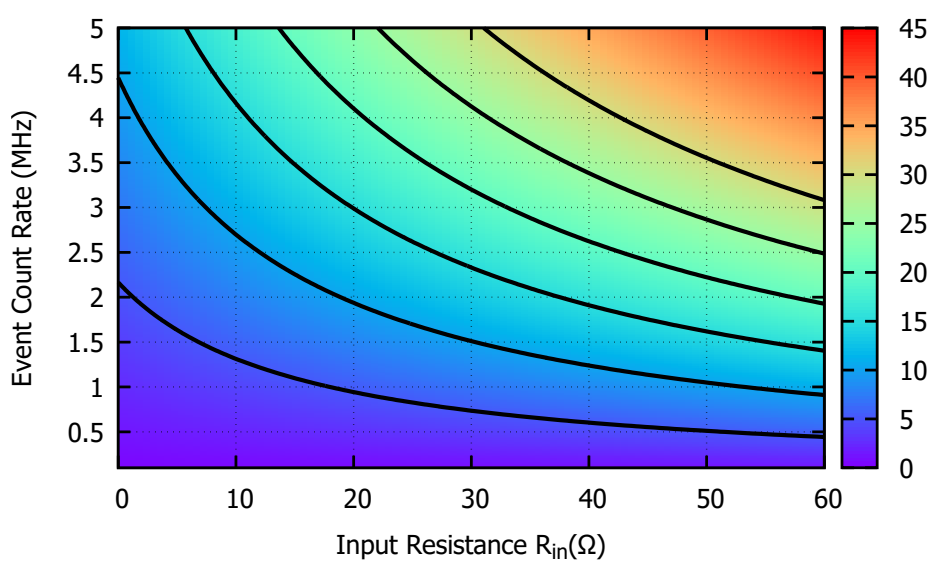
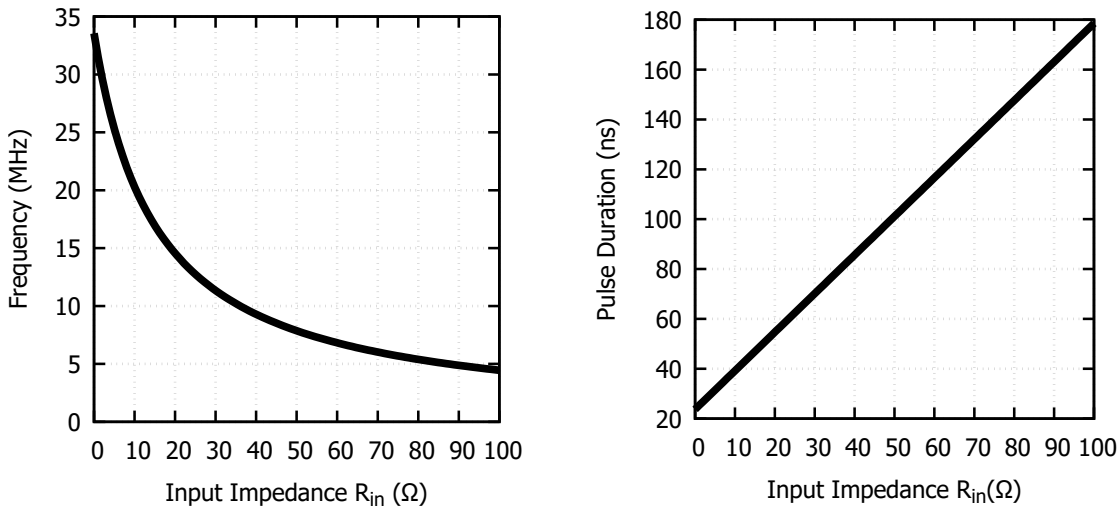


Figure 4.1: Pile-Up error percentage variation agains the Event Count Rate and the Input Resistance R_{in}.

By observing Figure 4.1 is visible that an input resistance of $R_{in} = 50\Omega$ is low enough to stay under the required 10% error margin, $P(k=0) = 7\%$, and sufficiently



(a) Minimum bandwith required for charge measurements vs Input Impedance R_{in}.

(b) Pulse Duration vs Input Impedance R_{in}.

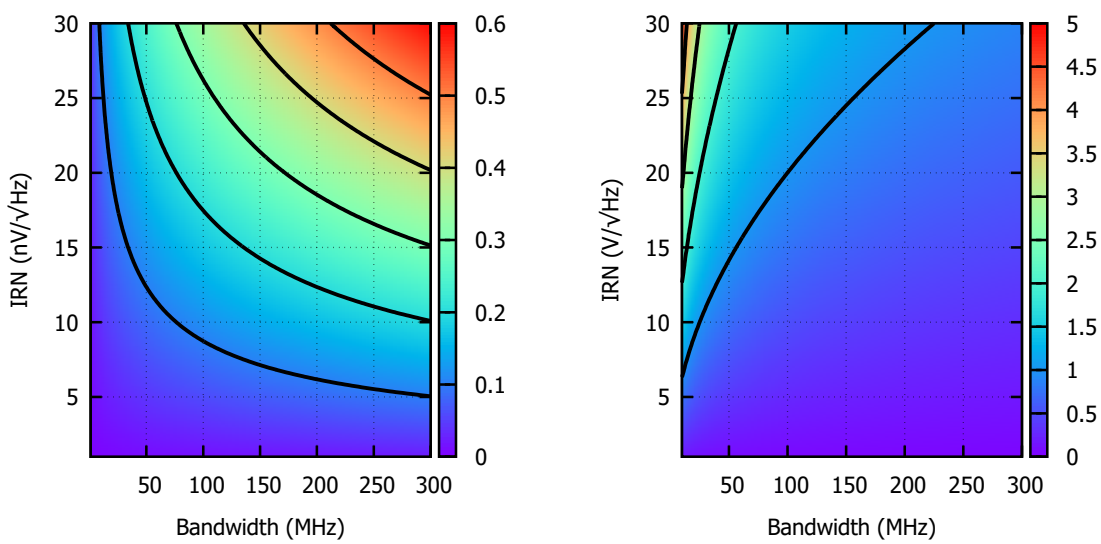
Figure 4.2: Pulse Duration and minimum bandwidth required for charge measurements

high to guarantee a high peak value, which is recommended for time measurements. Furthermore, the minimum bandwidth required for charge measurements is also proportional to τ_s, as exposed in equation 2.16. Figure 4.2(a) shows the variation of the minimum bandwidth required for energy measurements against R_{in}. When a 50Ω resistor is selected equation 2.16 leads to a $BW_{min} = 8MHz$. A reasonable low value if the integrator is implemented by means of an operational amplifier with a negative feedback loop.

Figure 2.5(a) demonstrates the linear relationship of the input impedance R_{in} and the duration of the SiPM pulse. A pulse duration of $5(\tau_r + \tau_s) = 100ns$ is obtained when $R_{in} = 50\Omega$, the time duration is important to estimate the available time of the radiation detector form detection to amplification, digitization, processing and transmission to the computer.

4.1.1 Voltage Amplifier

The voltage preamplifier by itself is not capable to measure time and energy, therefore, as explained in section 2.2, its output is used by a discriminator and an integrator to extract the required information, however the uncertainty of the charge and time measurements caused by the preamplifier can be estimated with the Noise-to-Microcell Ratio (NMR) and the Time Jitter, therefore both parameters should be minimized to achieve better performance. Both, the NMR and Jitter, equations 2.20 and 2.32, are proportional to the input referred voltage noise $\overline{V_{n,in}}$ but have an inverse relationship to the bandwidth of the preamplifier ω_A.



(a) Noise-to-Microcell Ratio (NMR).

(b) Time Jitter.

Figure 4.3: Variation of the Noise-to-Microcell Ratio (NMR) and the Time Jitter against its Bandwidth and the Input-Referred Noise (IRN).

Figures 4.3(a) and 4.3(b) show the expected NMR and the Jitter variation of the voltage amplifier with respect to the Input Referred Noise and Bandwidth. On one hand, the NMR remains inside of the required specifications even for large bandwidth and noise values, if the NMR specifications would be more strict, a mechanism to reduce the bandwidth of the signal would be required such as a sharper or a low-pass filter with a minimum bandwidth of 8MHz. On the other hand, to accomplish a jitter

lower than $1\mu s$ the bandwidth should be higher to 240MHz and the noise lower to $30nV/\sqrt{Hz}$. Therefore the noise and bandwidth deisgn specifications are set to meet the jitter requirements.

The peak voltage of a single microcell is approximately $400\mu V$, calculated with equation 2.24, if an output voltage of 1V is required for a single microcell, the gain of the preamplifier would be 2500 ($\approx 68dB$), resulting in a gain-bandwidth value of 652GHz, given the difficulty to achieve such large gain-bandwidth product, the maximum gain of the preamplifier is set to 100 (40dB). In order to maximize the number of readable microcells, its minimum gain is selected to be the unity (0dB). Finally the calculated design parameters of the voltage preamplifier are given in table 4.1.1.

Parameter	**Value**
Gain	0dB to 40dB
Bandwidth	$\geq 240MHz$
Input Referred Noise	$< 30nV/\sqrt{Hz}$
Input Resistor	50Ω

Table 4.2: Voltage Preamplifier design parameters

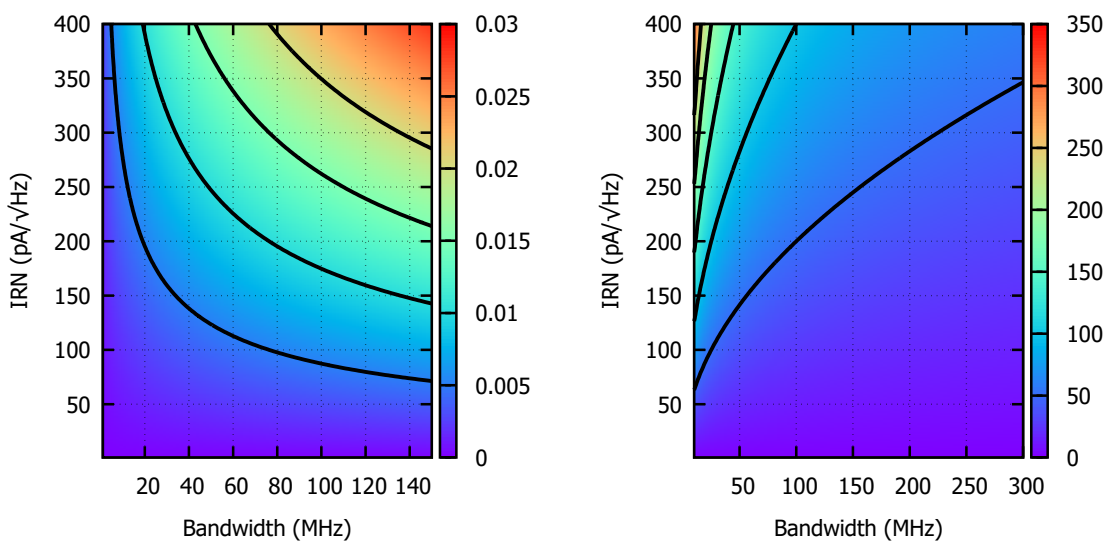
4.1.2 Current Buffer

For the current buffer approach, given the capabilities of the FVFCS to deliver a very low Input Impedance R_{in}, the duration of the SiPM pulse can be significantly reduced and the maximum count rate can be increased. From Figure 4.1 it is observable that for a input impedance of $R_{in} = 5\Omega$ an Event Count Rate of $ECR = 3.5MHz$ with a Pile-Up error of $P(k = 0) = 9.6\%$ is achievable. At the same R_{in} the minimum bandwidth required for charge measurements is equal to $BW_{min} \approx 26MHz$ and a pulse duration of $\approx 32ns$.

One of the main differences in the design of the current buffer with regard to the voltage amplifier, is the fact that its input impedance R_{in} and its transimpedance

R_o vary with respect to the coupled parasitic capacitance of the SiPM. Therefore for time measurements the design of the current buffer is realized by coupling the fast equivalent capacitance C_F and for energy measurements coupling the slow equivalent capacitance C_S. In order to maintain the required pulse duration, R_{in} should keep its value for BW_{min} when coupled to C_S. Considering that for most current amplifiers, their bandwidth is generally ruled by the input pole, the maximum expected bandwidth when an input impedance of $R_{in} = 5\Omega$ is selected are $103.7MHz$ and $490MHz$ for energy and time measurements respectively.

Figures 4.4(a) and 4.4(b) show the variation of the NMR and Jitter against the input-referred noise and bandwidth of the current buffer. It is observable that both parameters are located inside of the required specifications even for a large quantity of noise. To achieve a jitter lower than 100ps, the highest obtained in the voltage amplifier, a bandwidth higher than $100MHz$ and an input-referred current noise of $400pA/\sqrt{Hz}$ are required.



(a) Noise-to-Microcell Ratio (NMR).

(b) Time Jitter.

Figure 4.4: Variation of the Noise-to-Microcell Ratio (NMR) and the Time Jitter against its Bandwidth and the Input-Referred Noise (IRN) for a $R_{in} = 5\Omega$.

The peak current of a single fired microcell when $R_{in} = 5\Omega$ is approximately $80\mu A$,

calculated with equation 2.25, as a proposed requirement its output voltage is set at 10mV thus, the trasimpedance gain of the current buffer is required to be at least 125Ω. The final calculated design parameters of the current buffer preamplifier are shown in table 4.1.2.

Parameter	**Value**
Transimpedance	$> 125\Omega$
Bandwidth, $C_{in} = 64pF$	$\geq 100MHz$
Bandwidth, $C_{in} = 307pF$	$\geq 26MHz$
Input Referred Noise	$\leq 400pA/\sqrt{Hz}$
Input Impedance R_{in}	5Ω

Table 4.3: Current Buffer preamplifier design parameters

4.2 Proposed Voltage Preamplifier Design

4.2.1 Calculations

To achieve the large gain and bandwidth specifications, the voltage amplifier is based on the limiting amplifier topology, which consist of a cascade of low gain voltage amplifiers. Since the total gain is set at 40dB, the amplifier is proposed to have 4 stages, each with a gain of 10dB.

$$A_o = \frac{A_{Core}}{N} = \frac{40dB}{4} = 10dB(3.16V/V) \tag{4.2}$$

Given the bandwidth of the voltage amplifier is $BW_{tot} = 240MHz$, the bandwidth of each stage is proportional to the total number of cascaded amplifier, solving equation 3.4 for ω_o and selecting a $N = 4$ stages amplifier, the bandwidth of each stage is:

$$BW_o = \frac{BW_{tot}}{\sqrt{\sqrt[4]{2} - 1}} = 2.3BW_{tot} = 551.75MHz \tag{4.3}$$

As explained previously, the proposed limitng amplifier topology requires an offset feedback loop to compensate the differential offset generated by the transistors and resistors mismatch. Given the gain of the amplifier core $A_c = 40dB$, a proposed auxiliar amplifier with gain of $A_F = 2dB = 1.25$ and a corner frequency of 200Hz, the cut frequency of the low-pass filter needs to be:

$$LPF_c = \frac{A_{Core}A_{Fb} + 1}{F_c} = \frac{40dB \cdot 2dB + 1}{200Hz} = 0.64Hz \tag{4.4}$$

First the single stage of the core amplifier seen in figure 4.5 is designed, as a starting point, the dominant pole of a differential pair, seen in equation 3.12, is defined by its load impedance R_{L_A}, the parasitic C_{gdA1} capacitance and the load capacitance C_L of the next stage, considering that the input transistors of all the single stages have the same size, then $C_{gdA1} = C_{gsA2} = C_L = 0.25pF$ is proposed, the required load resistor is.

$$R_L = \frac{1}{2\pi BW_{stage}C_{out}} = \frac{1}{2\pi(551.75MHz)0.5pF} = 577.69\Omega \tag{4.5}$$

For a proposed common-mode-voltage output voltage of $V_{CM,out} = 0.5V$, the required bias current needs to be $I_{DMA1} = (V_{DD} - V_{CM,out})/R_{LA} = 556\mu A$. Calculating the transistor transconductance from the maximum achievable gain, making $R_S = 0$ in equation 3.10, gives $g_{mA1} = 5.46mS$. The use of the relationship $V_{sat} = 2I_D/g_m$ gives a saturation voltage of $V_{satA1} = 0.2V$. The width of a MOS transistor with respect to its transconductance is calculated with the following equation:

$$W = \frac{g_m^2 L}{2\mu_n C_{ox} I_D} \tag{4.6}$$

Considering the process constant of the TSMC 0.18μm technology[1] $\mu_n C_{ox} = 213\mu A/V$

[1]The parameters used in the hand calculations for the TSMC $0.18\mu m$ technology were extracted from the SPICE model and by performing the characterization procedure presented by Allen et all in [12]. For the NMOS transistor $\mu_n C_{ox} = 213\mu A/V$, $V_{th} = -0.4V$, $\gamma = 0.5$, $\lambda = 0.1$, $C_{gso,gdo} = 7.45 \times 10^{-10} F/m$ and for PMOS transistor $\mu_p C_{ox} = 47\mu A/V$, $V_{th} = 0.4V$, $\gamma = 0.4$, $\lambda = 0.1$, $C_{gso,gdo} = 6.52 \times 10^{-10} F/m$.

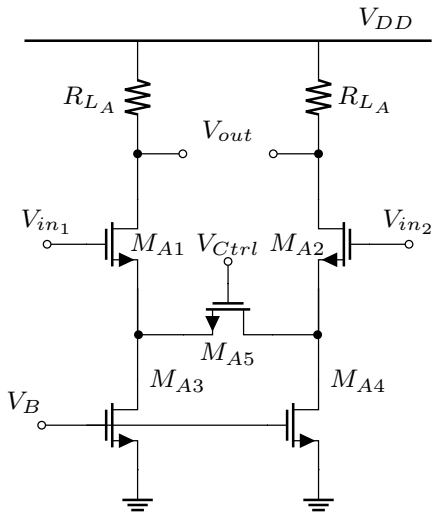
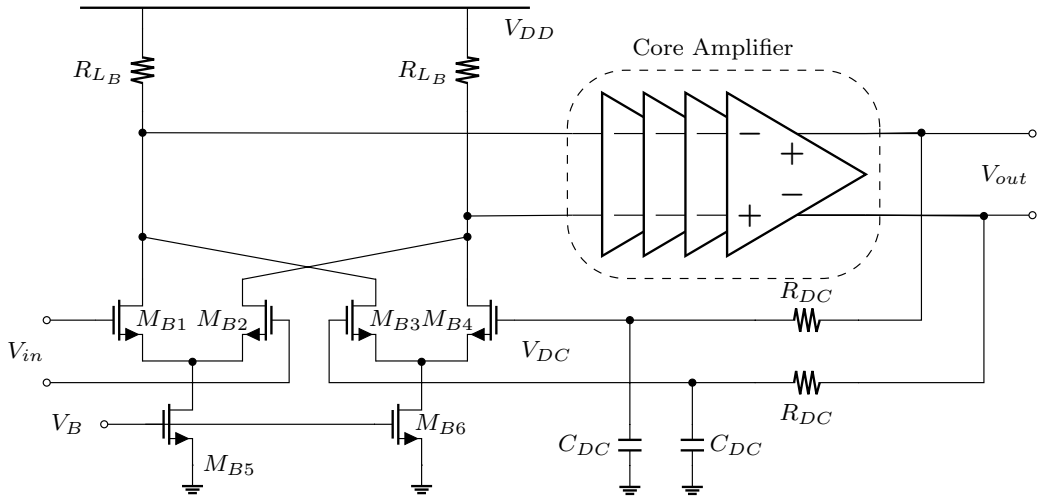
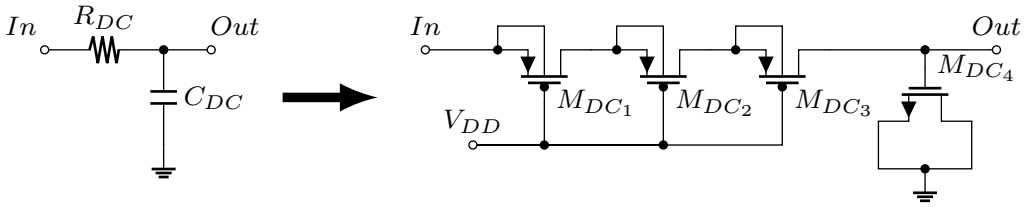


Figure 4.5: Single Stage of the Core Amplifier.



(a) Feedback network for offset cancellation.



(b) Low-pass filter implementation.

Figure 4.6: Offset compensation circuit.

and using a $L = 2L_{min} = 0.36\mu m$, equation 4.6 leads to $W_{A1} = 44.49\mu m \approx 50\mu m$. Due to the variable gain characteristic of the core amplifier, the minimum required voltage gain is 0dB, solving equation 3.10 for R_S, the maximum degeneration resistance is $R_S = 391\Omega$. Since the zero of the differential pair is smaller when R_S increases according to equation 3.11, the zero when a 0dB gain is selected is located at $F_{ZA} = 1.1GHz$ which is two times larger than BW_o thus, its effect does not affect the performance of the single stage.

Given that the degeneration resistance of the differential pair is implemented by a NMOS transistor in the linear region, its value is proportional to its width-to-length ratio and the gate-to-source voltage $V_{gsA5} = (V_{ctrl} - V_{satA3})$. For a maximum resistance $R_S = 391\Omega$, a tail transistors MA3,4 matched to the input transistor MA1,2 $V_{satA3} = 0.2V$, a threshold voltage of $V_{th} = 0.4V$ for a Nmos transistor, a control voltage $V_{ctrl} = 0V$ and a length of $L_{A5} = 2L_{min} = 0.36\mu m$ the width of transistor MA5 is

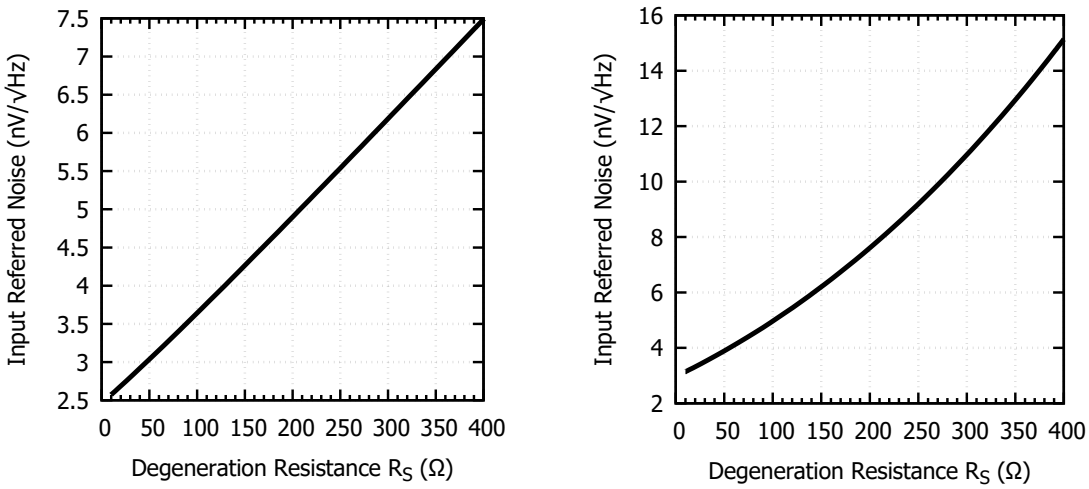
$$W_{A5} = \frac{L}{\mu_n C_{ox}(V_{gsA5} - V_{th5})} = 14.38\mu m \tag{4.7}$$

To ensure the operation of the differential pair, the input common mode voltage should be inside the range given by equation 3.15, $V_{gs1}+V_{satA3} < V_{CM,in} < V_{CM,out}+V_{th1}$, equation 4.8 leads to $V_{gs1} = 0.59V$, and the input common voltage must be inside the range of $-0.3V < V_{CM,in} < 0.9$. The output voltage is given by $V_{DD} - 2I_d R_{L_A} < V_{out} < V_{DD}$, that is: $0.26 < V_{out} < 0.9V$.

$$V_{gs} = \sqrt{\frac{2I_d L}{\mu_n C_{ox} W}} + V_{th} \tag{4.8}$$

The input referred noise of a single stage of the core amplifier is ploted in figure 4.7(a), as expected from equation 3.18, the noise increases as the degeneration resistor also increases and reduces the voltage gain of the amplifier. Figure 4.7(b) shows the input referred noise of the core amplifier by using expression 3.7, even thought the overall noise of the four stages in cascade is increased with respect to a single stage, its value remains within the amplifier specifications.

For the Differential Difference Amplifier (DDA) used in the offset compensation



(a) Single Stage variable amplifier.

(b) Four stage variable amplifier core.

Figure 4.7: Input referred noise against the degeneration resistor R_S.

circuit seen at figure 4.6(b) a similar procedure than the core amplifier is followed. The same load resistor $R_{L_B} = R_{L_A} = 578\Omega$, common output voltage $V_{CM,inB} = V_{CM,inA} = 0.5V$ and the bias current is halved $I_{DMB} = 0.5I_{DMA} = 278\mu A$, for a voltage gain $A_{Fb} = 2dB = 1.25$, equation 3.25 gives $g_{mB1} = 4.48mS$, and expression 4.6 leads to $W_{B1} = 15.31\mu m \approx 16\mu m$. Finally considering a parasitic capacitance of $C_{gdB} = 0.25pF$, from equation 3.24 the zero of the DDA results in $F_{ZB} = 2.85GHz$ just higher than BW_o, therefore no contribution is noticeable in the frequency response of the complete voltage amplifier.

The correct operation of the Differential Difference Amplifier is acheived when the the input common mode voltage is located inside the range provided by equation 3.15, $V_{gsB1} + V_{satB5} < V_{CM,in} < V_{CM,out} + V_{th1}$, equation 4.8 leads to a $V_{gs1} = 0.79V$, thus the input common voltage must be inside the range of $0V < V_{CM,in} < 0.9$. The output voltage is given by $V_{DD} - 2I_dR_{L_B} < V_{out} < V_{DD}$, which is the same than the core amplifier: $0.26 < V_{out} < 0.9V$.

Given that the low-pass filter requires enormous values of resistance and capacitance to obtain a cut-off frequency of $LPF_c = 0.64Hz$, traditional implementation techniques such as unsilicided polysilicon resistor and MiM capacitors require a huge amount or

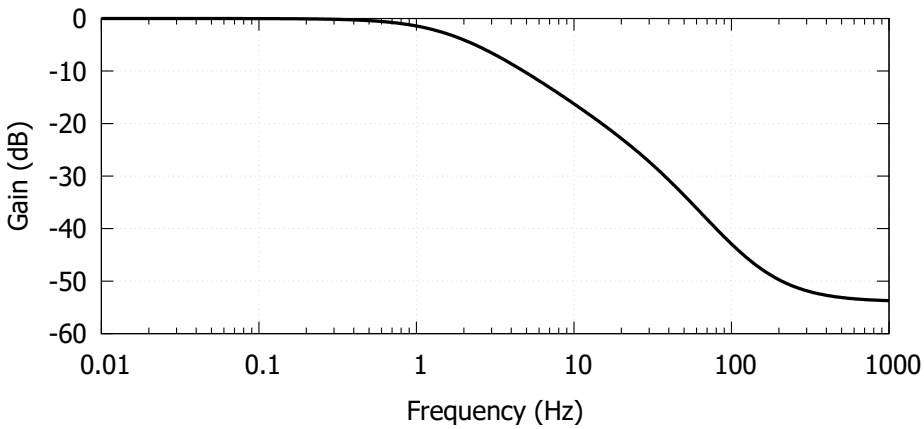


Figure 4.8: Low-pass filter AC response.

area, therefore the filter, visualized in Figure 4.6(b), is implemented with three pMOS transistors in the cut-off region and a nMOS varactor whose model is provided by the TSMC library, the equivalent values are $R_F = 2.3T\Omega$ and $C_F = 45fF$, with a cut frequency of $LPF_c = 1.63Hz$. Its frequency response is visualized in figure 4.8.

4.2.2 Simulations

All the hand calculated transistor dimensions, bias current and voltages are introduced into the Computer-Assisted Design (CAD) software Cadence Virtuoso in order to fine tune its values with the help of simulations. The final transistor sizes and their operating points are visualized in table 4.2.2 and the passive elements in table 4.2.2.

Transistor	**W**	**L**	**gm**	**gds**	**Cgd**	**Cgs**	**Vsat**	**Id**
MA(1-4)	$50\mu m$	$0.36\mu m$	$5.84mS$	$45.8\mu S$	$16.81fF$	$105fF$	$147mV$	$574.6\mu A$
MB(1-4)	$10\mu m$	$0.36\mu m$	$1.78mS$	$16.60\mu S$	$3.3fF$	$22.8fF$	$194mV$	$253\mu A$
MB(5-6)	$50\mu m$	$0.36\mu m$	$4.2mS$	$45.8\mu S$	$30fF$	$105fF$	$147mV$	$506\mu A$

Table 4.4: Sizes and operating point of the transistors form the proposed voltage amplifier

Table 4.2.2 shows the characterization of the proposed voltage amplifier when a large

Parameter	Value
W/L_{A5}	$50\mu m/0.36\mu m$
R_{L_A}	800Ω
R_{L_B}	800Ω
$W/L_{DC_{1-3}}$	$2\mu m/0.36\mu m$
$C_{M_{RC_4}}$	$45fF$

Table 4.5: Design parameters of the Voltage amplifier

and a low gain is selected. First, the only parameter that remains constant regardless of the amplification factor is the power consumption. Figure 4.10(a) shows the frequency response of the amplifier, the voltage gain is successfully selected form 46dB to 5dB by adjusting the V_{ctrl} potential, the cut-off frequency varies form 2.7Hz to 123Hz, the total bandwidth reaches 501MHz when the maximum gain is selected, then decreases to its minimum of 280MHz at approximately 0.3 V_{ctrl} and then increases once again for lower voltage gains, the minimum bandwidth remains higher than the design specifications.

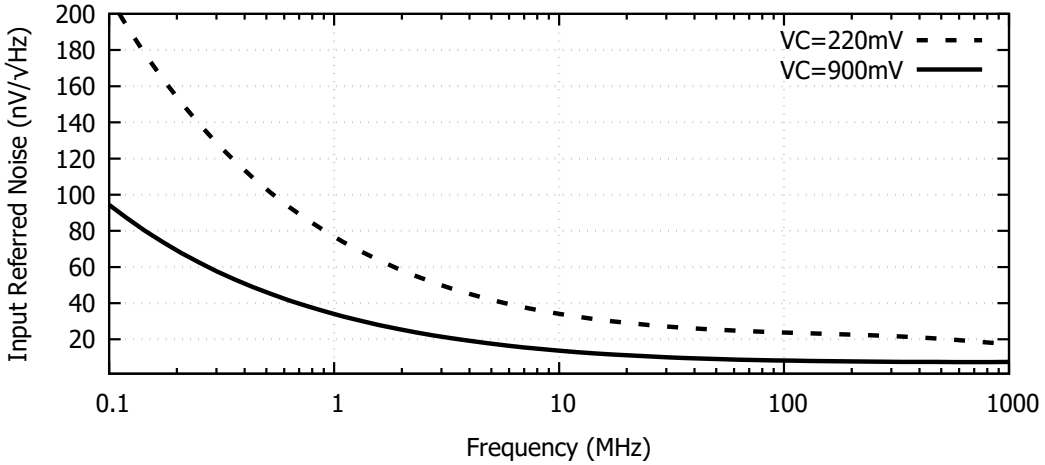


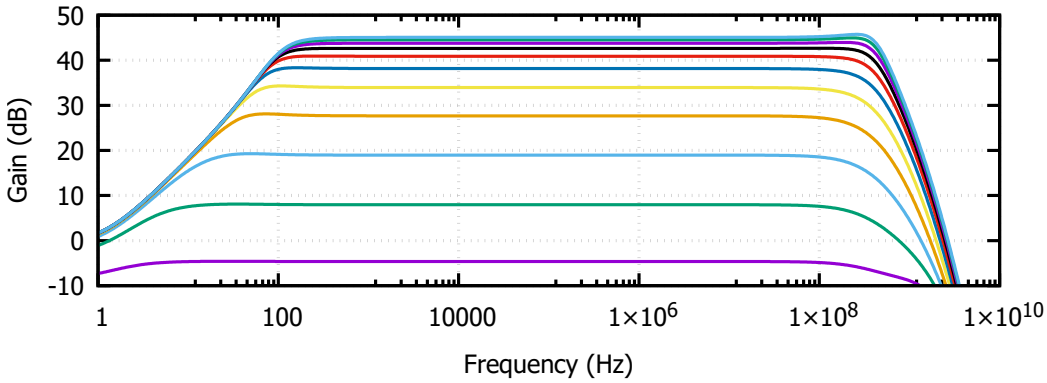
Figure 4.9: Input Referred noise spectrum.

The Input-Referred Noise (IRN) is slightly higher than the required specifications when $V_{ctrl} = 220mV$ is selected. Even thought the noise hand calculations are similar to the simulation results, Figure 4.9 shows that the flicker noise has a dominant contribution for frequencies lower than 10MHz and its effect should have been carefully studied. The variation of the input-referred noise and the output noise in RMS voltage, integrated from 100KHz to 1GHz, against the gain control voltage are shown in Figures 4.10(d) and 4.10(e) respectively, interestingly lower gains have lower RMS noise voltage, therefore a better time and charge measurement performance is expected when a large number of cells are fired.

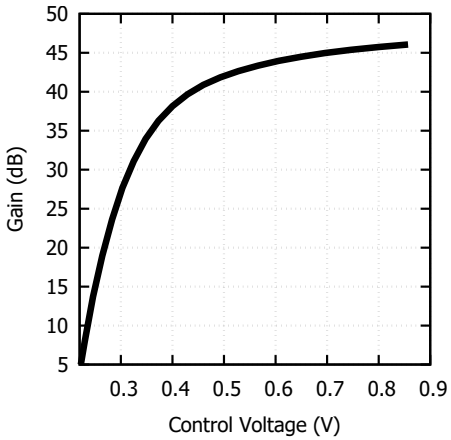
One of the main advantages of the use of fully-differential typologies is a higher immunity of common mode and power source variations, quantified by the Common Mode Rejection Ratio (CMRR) and the Power Source Rejection Ratio (PSRR), in comparison to the single ended approach. The proposed voltage amplifier exhibits a higher CMRR and PSRR when a high gain is selected. The Input Dynamic Range is limited by the Differential Difference Amplifier to just $\pm 260mV$, therefore is expected that the totality of the microcells may not be readable. Finally, the slew rate of the proposed amplifier remains relatively constant regardless of the selected voltage gain, given the lower RMS output noise for a lower gain values, a better jitter performance is expected when low gain values are selected.

Parameter	V_{ctrl} @ 900mV	V_{ctrl} @ 220mV
V_{supply}	$1.8V, \pm 0.9V$	$1.8V, \pm 0.9V$
Power Consumption	$11.4mW$	$11.4mW$
Gain	$46dB$	$4dB$
Bandwidth ($C_L, 0.5pF$)	$501MHz$	$363MHz$
Cut-off Frequency	$123Hz$	$2.7Hz$
IRN @ 10MHz	$13.8nV/\sqrt{Hz}$	$34nV/\sqrt{Hz}$
IRN (RMS)	$268\mu V$	$600\mu V$
Output Noise (RMS)	$40mV$	$1mV$
$A_{V,CM}$ @ 10MHz	$-255dB$	$-137dB$
$CMRR$ @ 10MHz	$301dB$	$183dB$
$PSRR+$ @ 10MHz	$278dB$	$144dB$
$PSRR-$ @ 10MHz	$279dB$	$144dB$
Input Range	$\pm 260mV$	$\pm 260mV$
Output Range	$114mV/864mV$	$114mV/864mV$
Rise Time ($500mV_{pp}$)	$986ps$	$1.47ns$
Fall Time ($500mV_{pp}$)	$928ps$	$1.17ns$
Slew Rate+ ($500mV_{pp}$)	$331(V/\mu s)$	$245(V/\mu s)$
Slew Rate− ($500mV_{pp}$)	$352(V/\mu s)$	$297(V/\mu s)$

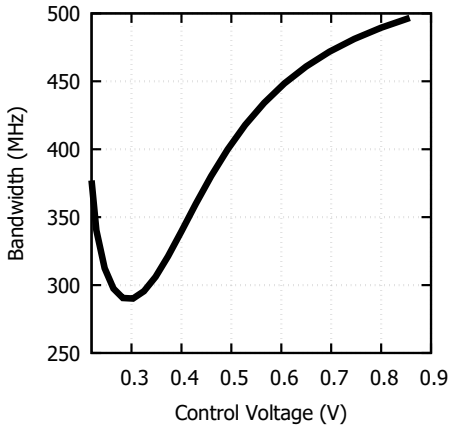
Table 4.6: Electrical characterization of the proposed voltage amplifier



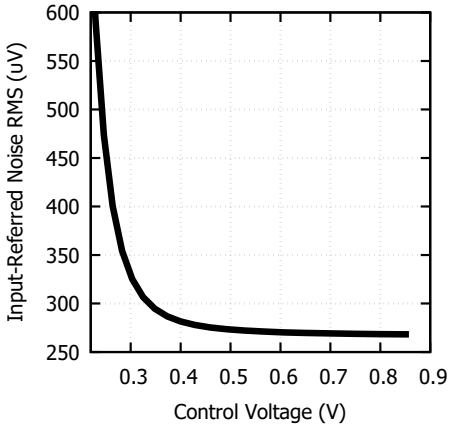
(a) AC Response with Vctrl variation



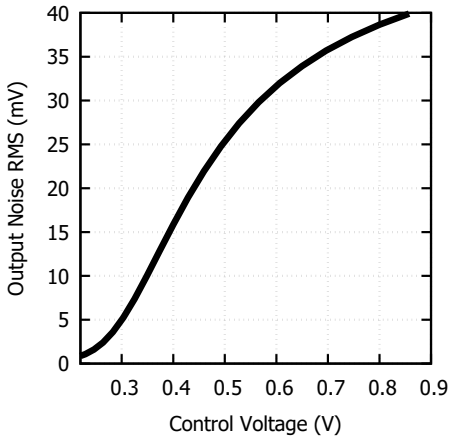
(b) Gain vs Control Voltage



(c) Bandwidth vs Control Voltage



(d) Input Noise RMS vs Control Voltage



(e) Output Noise RMS vs Control Voltage

Figure 4.10: AC analysis of the voltage amplifier.

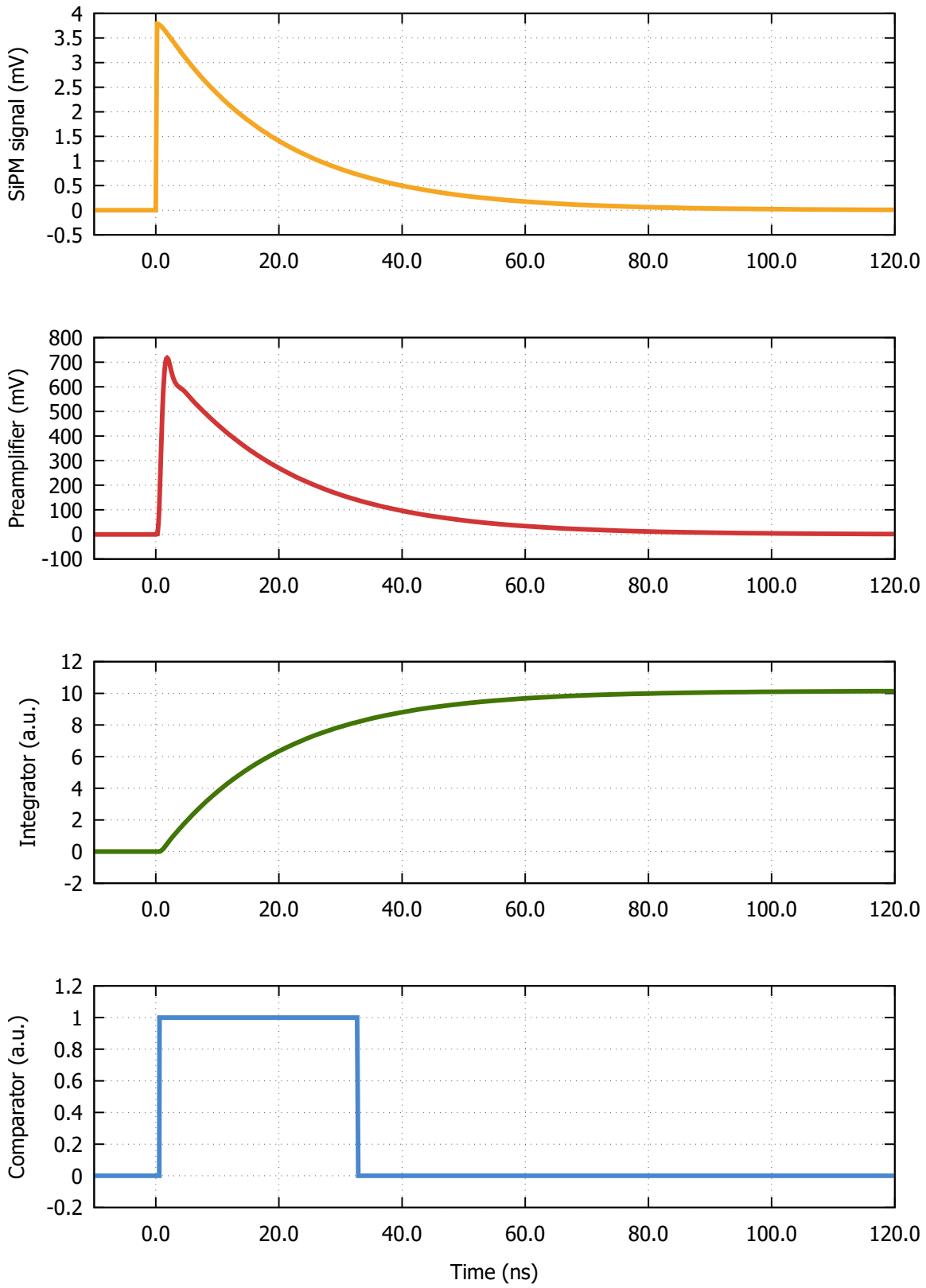


Figure 4.11: Waveforms of the SiPM signal, proposed voltage preamplifier, integrator and comparator when 10 microcells are fired.

4.2.3 Radiation detector measurements

The input range of the preamplifier is $\pm 260mV$, from equation 2.24 the peak voltage of a single fired microcell is $V_{peak,in} = 400\mu V$, thus 650 microcells are detectable before saturation. Considering the slew rate of the preamplifier as its maximum slope, equation 1.8 leads to a theoretical time jitter of 113ps and 4ps for V_{ctrl} of 900mV and 220mV respectively, which is considerably lower than the required specifications.

For the energy measurements, the peak value of the slow component of the SiPM signal is calculated with equation 2.12, for V_{ctrl} of 900mV expression 2.20 leads to a Noise-to-Microcell Ratio of 0.61 and 1.37 for V_{ctrl} 220mV, even thought the NMR has an acceptable range, the use of a sharper or an integrator with BW_{min} would reduce the RMS noise of the signal and dramatically increase the charge resolution of the radiation detector.

To evaluate the discussed theoretical estimations, the proposed voltage amplifier is coupled to the SiPM, a comparator and an integrator as seen in Figure 4.12. The resulting waveforms of all the components form the firing of 10 microcells are illustrated in Figure 4.11.

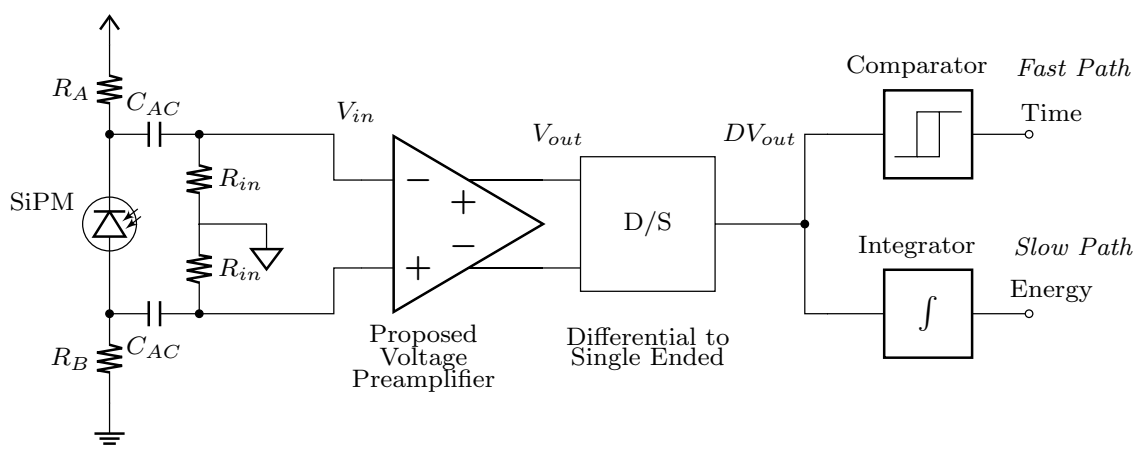


Figure 4.12: Proposed voltage amplifier signal path for time and energy measurements.

Dynamic Range

SiPM signal with an increasing number of fired microcells is sent to the preamplifier, the maximum number of readable microcells is accomplished when the peak output voltage reaches its 1dB compression ratio. Simulations results in Figure 4.13 where the dynamic range of the preamplifier is shown for multiple gain values selected. It is important to mention that the number of fired microcells is proportional to the total charge generated from the SiPM, therefore the fire of each mircocell is proportional to $Q_{1\mu cell} = 160fC$.

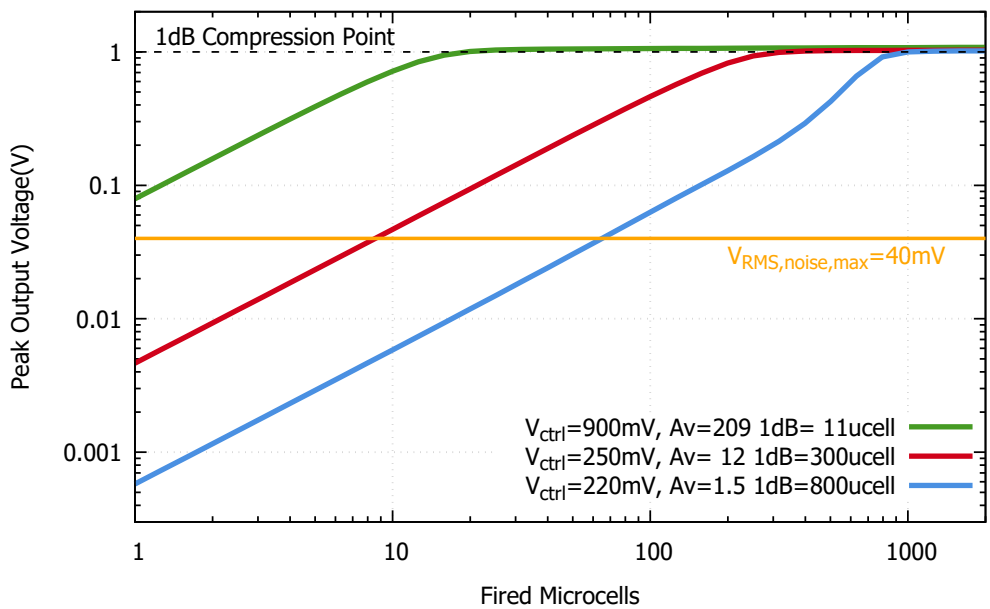


Figure 4.13: Voltage amplifier output to detected photoelectrons.

When the maximum voltage is selected, peak voltage of a single fired microcell is $\approx 80mV$, considering that the RMS output noise of the preamplifier for the same amplification factor is $40mV$, the resulting signal-to-noise ratio is 2. The 1dB compression point of the output peak value varies with respect to the selected gain, for a 46dB gain (209V/V) its located at $11\mu cell$, and for a voltage gain of 4dB (1.5V/V) at $800\mu cell$, however an increase of the slope is visible at $400\mu cell$ caused by the limitations of the input-dynamic range. As expected the preamplifier is unable to read the totality of the microcells from the SiPM.

From equation 2.17 the charge of an event is obtained by integrating the output voltage of the amplifier, by using an integrator with a voltage gain of A_{VInt}, its output peak voltage $V_{peak,Int} = (A_{VInt}A_vR_{in})Q_{in}$ is directly proportional to the input charge Q_{in}.

Interestingly even after the preamplifier reaches saturation, the information of the charge remains uncompressed for a few more microcells as visualized in Figure 4.14 where the normalized peak value of the integrator is ploted. As visualized in figure 1.13(a), the slow component of the SiPM actually has a lower peak value than the fast component. Therefore even thought saturation begin when $800\mu cell$ are fired, the front-end electronics is capable to detect the charge of up to $1800\mu cell$.

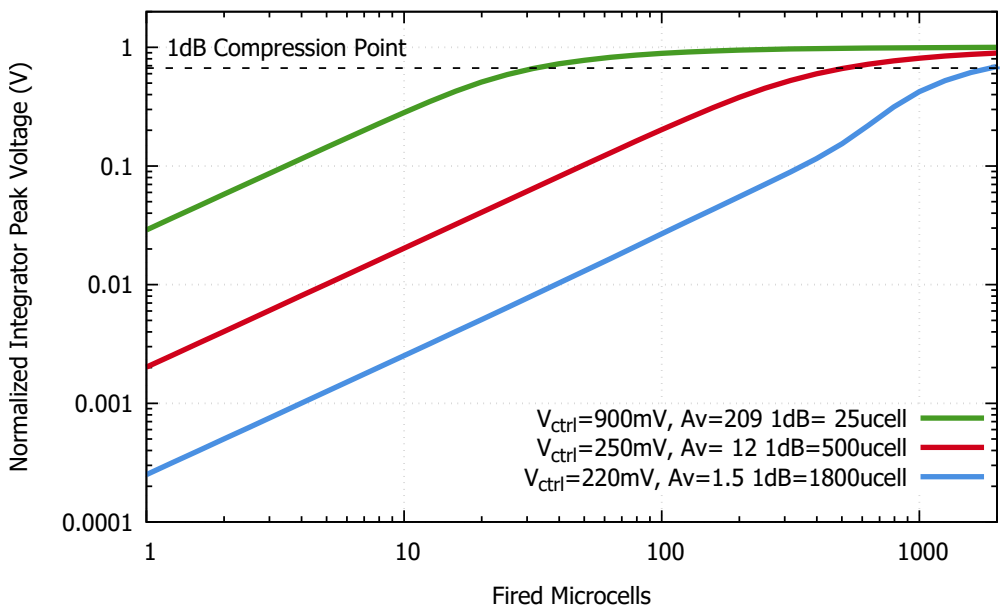
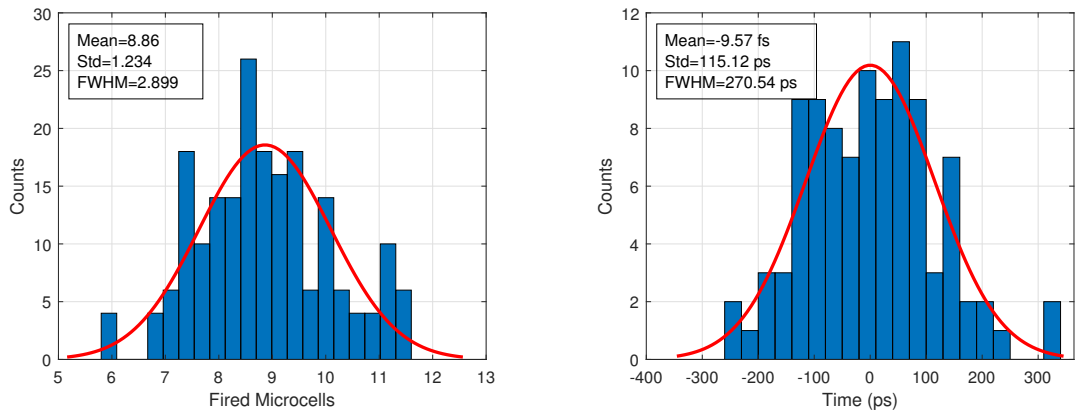


Figure 4.14: Normalized integrator peak output to detected photoelectrons.

Time and Charge Resolution

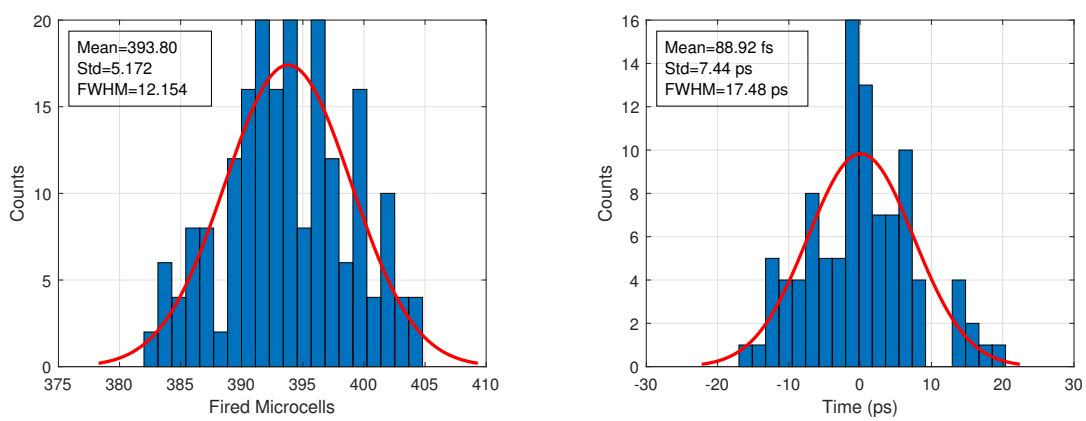
To evaluate the time and charge resolution of the preamplifier, transient noise is activated in the simulation and 200 periodical pulses with the same number of fired microcells are send to the preamplifier, the amplified fully-differential signal is converted into single ended and then used by a comparator to measure the time jitter and by

an integrator to measure the number of detected microcells and its uncertainty, figures 4.2.3 and 4.2.3 illustrate the result of the simulations the firing of 10 and 400 $\mu cell$ respectably.



(a) Charge Resolution. (b) Time Jitter.

Figure 4.15: Charge and Time Resolution of the voltage preamplifier for $N_F = 10$, $V_{ctrl} = 900mV$ and $A_V = 209V/V$.



(a) Charge Resolution. (b) Time Jitter.

Figure 4.16: Charge and Time Resolution of the voltage preamplifier for $N_F = 400$, $V_{ctrl} = 220mV$ and $A_V = 1.5V/V$.

The measured charge resolution for a V_{ctrl} of 900mV results in 1.34 and 5.17 for V_{ctrl} of 220mV , this results are higher than the theoretical NMR of 0.61 and 1.37, this

variation is attributable to the fact the the use of $V_{peak,in}$ is actually a simplification of its real value, in reality, as seen in figure 1.13(a), the peak value of the slow component is lower, calculating $V_{peak,in,slow}$ from equation A.21, results in a peak value of $234\mu V$ and a maximum detectable number of microcells of 984, a closer value to the simulations. However the use of the NMR gives a good approximation of the expected charge resolution of the voltage preamplifier.

In the case of the time resolution, the measured jitter is 115ps and 7.4ps for a V_{ctrl} of 900mV and 220mV respectively, the estimated values of 113ps and 4ps are actually very close which demonstrates the accuracy of the jitter expression. Both measured time resolutions exceed by far the required specification of $1\mu s$.

4.3 Proposed Current Buffer Design

4.3.1 Calculations

The design of the FVFCS, visualized in figure 4.17, is divided in two parts, first the transimpedance amplifier consisting by transistors M1 and M2 is designed to achieve the input impedance and frequency response requirements, later the voltage amplifier formed by transistor M3 and the load resistor R_L is configured to achieve the required transimpedance gain.

Since the pulse duration depends on the input impedance of the FVFCS, special attention is this parameters is taken, according to its low frequency equation 4.9, R_{in} depends on the intrinsic gain of transistor M2 and the transconductance of M1.

$$R_{in_{LF}} = \frac{1}{g_{m1}g_{m2}(r_b||r_{o2})} \tag{4.9}$$

Assuming that the output impedance of all transistors and the current source are equal $r_b = r_{o2} = r_o$, then $r_b||r_{o2} = r_o/2$ and considering that the intrinsic gain of transistor M2 is $g_{m2}r_o \approx 100$, the required transconductance of M1 to achieve a $R_{in} = 5\Omega$ is $g_{m1} = 4mS$. The saturation voltage is proposed to be at $V_{sat} = 0.2V$, thus the use of the relationship $I_D = V_{sat}g_m/2$ delivers a required bias current of $I_b = 400\mu A$.

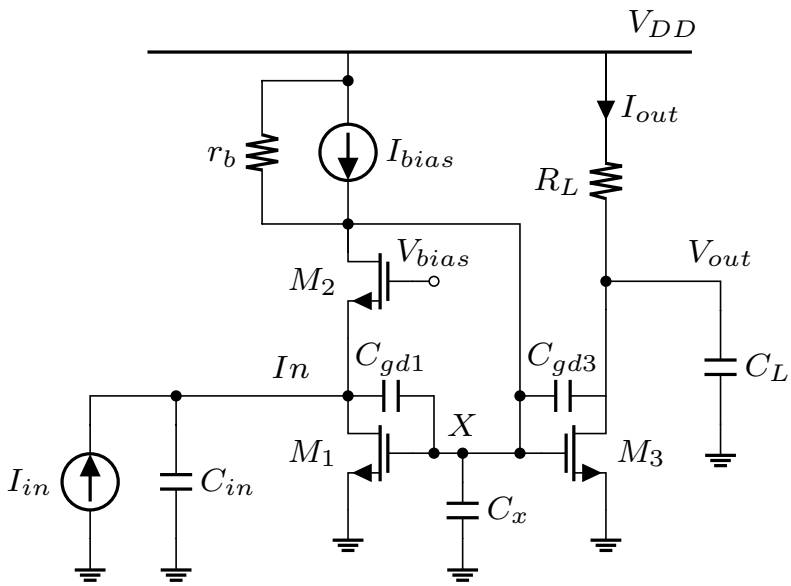


Figure 4.17: Proposed current buffer preamplifier.

Assuming a channel-length modulation $\lambda = 0.1$, then the output impedance of transistor M1 is $r_o \approx 1/\lambda I_d = 25k\Omega$. Considering a constant process of $\mu_n C_{ox} = 213\mu A/V$ for the TSMC $0.18\mu m$ technology and using $L = 2L_{min} = 0.36\mu m$ equation 4.6 leads to a transistor width of $W_1 = 67.6\mu m \approx 68\mu m$.

With the aid of the transistor width, the parasitic capacitances that rule the frequency response of the proposed circuit are calculated[2]. For transistor M1 $C_{gs1} = C_{gd1} = 50fF$, and for transistor M3 is taken the case where $W_1 = W_3$ so $C_{gs3} = C_{gs1}$, since C_X is composed by $C_X = C_{gs1} + C_{gs3}$ thus $C_X = 100fF$.

To satisfy the frequency requirements of the design, the poles and zeros should be larger than the required bandwidth. The zero affects the input impedance by increasing its value until it reaches the poles, as seen in figure 3.16(a), in the proposed design $F_{Z_{Rin}} = 83.7MHz$ which is sufficient for charge measurements but low for time measurements, therefore the output signal is expected to deliver the calculated pulse duration but with a lower peak output current due to the increment of R_{in} for higher

[2]The gate to source and gate to drain capacitances are equal to $C_{gs} = WC_{gso}$ and $C_{gd} = WC_{gdo}$ where W is the width of the transistor and C_{gso}, C_{gdo} are the capacitance overlap density, for the TSMC $0.18\mu m$ $C_{gso} = C_{gdo}$ is equal to $7.45 \times 10^{-10} F/m$

frequencies. The zero of the transimpedance function, assuming that M1 and M2 are matched transistors, is located at $F_{Z_X} = 12.9GHz$ which is a very high frequency.

The poles of both input impedance and transimpedance transfer functions are located in the same positions. The input pole is dependent on the equivalent capacitance of the SiPM thus for energy measurements $C_{in} = C_S = 307pF$ is located at $F_{P1_{Rin}} = F_{P1_X} = 103MHz$ which is close to the required specifications and for time measurements $C_{in} = C_S = 65pF$ its magnitude is $F_{P1_{Rin}} = F_{P1_X} = 489MHz$, a very large value thanks to the very low input impedance of the circuit. Finally the pole at the node X is located at $F_{P2_{Rin}} = F_{P2_X} = 125MHz$, higher than the required specifications.

The load resistor R_L converts the copied current signal into voltage, its selection needs to fulfill the required bandwidth and transimpedance specifications, additionally its DC baseline must be as close to V_{DD} to increase the output dynamic range of the proposed circuit. Starting with the output pole, for a proposed $C_L = 0.25pF$, a load resistor of $R_L = 5k\Omega$ delivers an output pole of $F_{P1_O} = 127MHz$. If the copied current has a $\beta = 1$, its DC baseline is equal to $-1.1V$ which is larger than the negative power rail, a proposed $\beta = 0.1$ delivers a DC baseline at $0.7V$ and a transimpedance gain of $R_o = \beta R_L = 500\Omega$ an output voltage swing of $-0.7 < V_{out} < 0.7$ and a maximum input current of 2.8mA before transistor M3 reaches saturation. With the proposed $\beta = 0.1$, the zero of the voltage amplifier is located at very high frequencies $F_{Z_O} = 12.56GHz$ and would not interfere in the FVFCS performance.

With the proposed values, expression 3.38 delivers an input referred noise of $\overline{I_{n,in}} = 27pA/\sqrt{Hz}$ which is lower than the design parameters. Finally the bias voltage V_{bias} must satisfy expression 3.36 to ensure the correct polarization of the circuit even for the maximum input current. Evaluating the discussed expression for $I_{in} = 0$ delivers $-0.21V < V_{bias} < 0.04V$ and for the maximum input current $I_{in} = 2.8mA$ gives $0.01 < V_{bias} < 0.2V$, the middle point between both evaluations is located approximately at $0V$, therefore a $V_{bias} = 0V$ is selected.

4.3.2 Simulations

The calculated transistor dimensions, bias current and voltages sources are introduced into the CAD software Cadence Virtuoso to adjust its value. The final transistor sizes and operating points are visualized in table 4.3.2, and the passive elements are shown in table 4.3.2.

Transistor	W	L	gm	gds	Cgd	Cgs	Vsat	Id
M1	$50\mu m$	$0.36\mu m$	$4.85mS$	$272\mu S$	$21.1fF$	$107fF$	$137mV$	$496\mu A$
M2	$50\mu m$	$0.36\mu m$	$5.07mS$	$103\mu S$	$19.7fF$	$106fF$	$136mV$	$496\mu A$
M3	$5\mu m$	$0.36\mu m$	$575\mu S$	$3.77\mu S$	$1.5fF$	$10.6fF$	$137mV$	$58.18\mu A$

Table 4.7: Sizes and operating point of the transistors form the proposed current buffer

Parameter	Value
R_L	$5K\Omega$
I_{bias}	$500\mu A$
V_{bias}	$0V$

Table 4.8: Design parameters of the current buffer

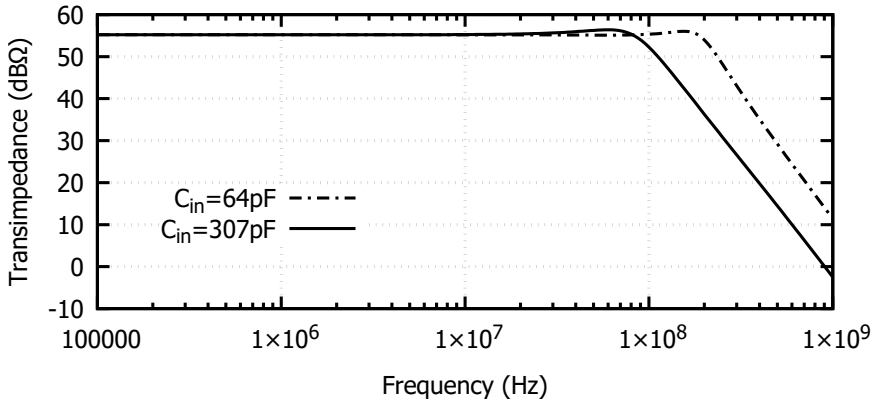
The complete characterization of the proposed current buffer for the two equivalent input capacitances of the SiPM sensor are shown in table 4.3.2. For energy measurements, the input impedance remains very close to the required specifications, the transimpedance gain has a variation of 1.15 from the theoretical 500Ω value, caused by the mismatch of V_{DS} in transistors M1 and M3 resulting in a deviation of the copied current. The maximum input current is reduced to 2mA.

For time measurements, the transimpedance bandwidth, seen Figure 4.18(b), surpass the specifications, the input impedance, Figure 4.18(a), starts to increase at $\approx 50MHz$ to reach a maximum value of 24Ω at $190MHz$, thus a lower peak output value is expected than the original. The input referred current noise spectrum from

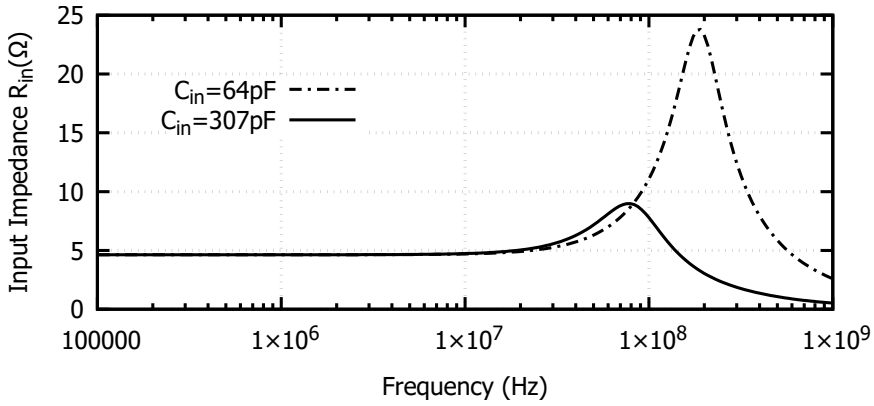
100KHz to 1GHz is visualized in Figure 4.18(a), it is observable that for higher frequencies than $10MHz$, high frequency components begins to be prominent for $C_{in} = 307pF$, as a result the RMS output noise is greater for energy measurements.

Parameter	$C_{in} = 64pF$	$C_{in} = 307pF$
V_{supply}	$1.8V, \pm 0.9V$	
Power Consumption	$1.3mW$	
Input Impedance R_{in} @ 26MHz	5.1Ω	
Input Impedance R_{in} @ 100MHz	11.8Ω	7.78Ω
Transimpedance @ 26MHz	575Ω	
Bandwidth ($C_L = 0.25pF$)	$217MHz$	$100MHz$
IRN @ 10MHz	$86pA/\sqrt{Hz}$	$197pA/\sqrt{Hz}$
IRN (RMS)	$23\mu A$	$113\mu A$
Output Noise (RMS)	$2.7mV$	$5mV$
Maximum input current	$2mA$	
Output Range	$-554mV/609mV$	
Rise Time ($500mV_{pp}$)	$1.56ns$	$2.4ns$
Fall Time ($500mV_{pp}$)	$2ns$	$3.2ns$
Slew Rate+ ($500mV_{pp}$)	$185(V/\mu s)$	$138(V/\mu s)$
Slew Rate− ($500mV_{pp}$)	$146(V/\mu s)$	$109(V/\mu s)$

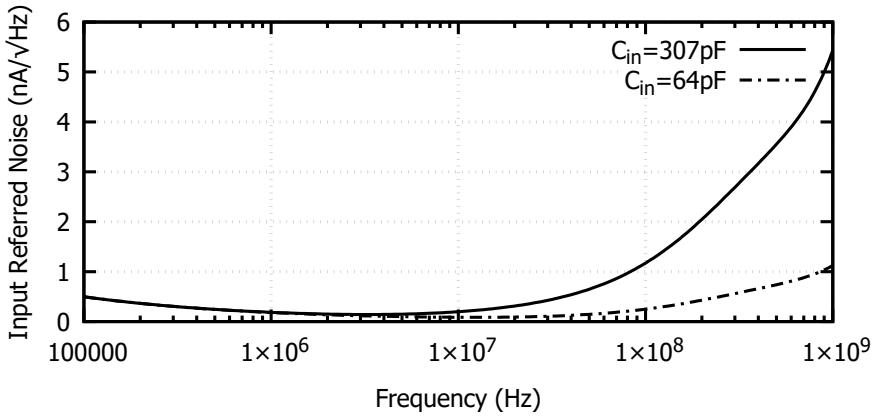
Table 4.9: Electrical characterization of the proposed current buffer



(a) Transimpedance gain variation to C_{in} of $64pF$ and $307pF$



(b) Input Impedance R_{in} variation to C_{in} of $64pF$ and $307pF$



(c) Input Referred Noise variation to C_{in} of $64pF$ and $307pF$

Figure 4.18: AC analysis of the current buffer.

4.3.3 Radiation Detector measurements

Likewise the voltage amplifier, the output signal of the current buffer preampliferes requires to be processed by an integrator and a discriminator to extract the energy and time information of an event. From the electrical characterization of the proposed preamplifer an estimation of its performance is realized.

Since the maximum input impedance is $R_{in} = 24\Omega$, the expected maximum peak voltage now is, calculated with expression 2.25, $I_{peak,in} = 16.61\mu A$. Given that the maximum input current is 2mA, 120 microcells are detectable before the circuit reaches saturation. For time measurements, considering the positive Slew Rate and the output RMS voltage noise when a input capacitance of $C_{in} = 64pF$ is coupled, expression 1.8 leads to a theoretical jitter of 15pF. For energy measurements, the peak value of the slow component of the SiPM signal is calculated with equation 2.12, for an output RMS voltage noise when $C_{in} = 307pF$ expression 2.23 leads to a Noise-to-Microcell Ratio of 1.28.

With the objective to measure the discussed theoretical estimations, the proposed current buffer preamplifier is coupled to the SiPM sensor, an integrator and a comparator as seeen in figure 4.19. The resulting waveforms of all the components form the firing of 50 microcells are visualized in figure 4.20.

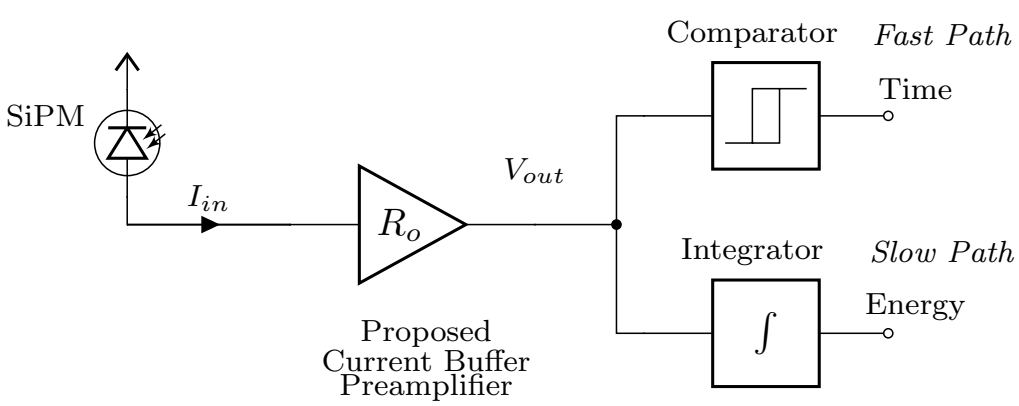


Figure 4.19: Proposed current buffer preamplifier signal path for time and energy measurements.

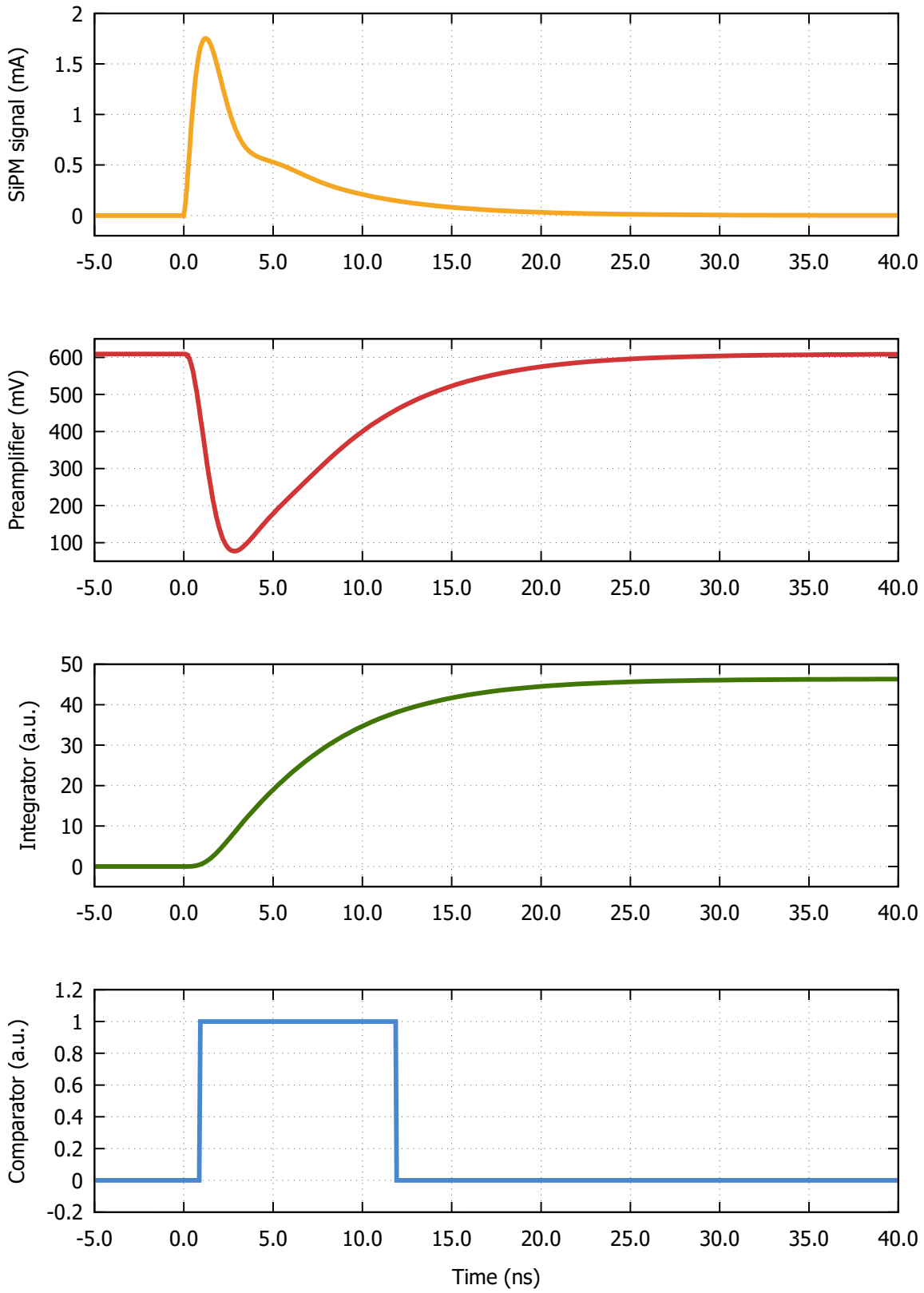


Figure 4.20: Waveforms of the SiPM signal, proposed current buffer preamplifier, integrator and comparator when 50 microcells are fired.

Dynamic Range

In order to calculate the maximum number of readable microcells, a SiPM signal with an increasing number or fired microcells is sent to the current buffer, the maximum dynamic range of the preamplifier arrives when the peak output voltage reaches its 1dB compression point.

The simulation of the circuit results in figure 4.21, the voltage of a single fired microcell is $\approx 9.2mV$ and the noise floor is located at $5mV$ thus the signal-to-noise ratio of the peak voltage is ≈ 1.84 similar to the voltage preamplifier. The 1dB compression point of the peak value is reached at $123\mu cell$, and the response of the output signal has a non-linear behavior. The observed non-linear behavior is caused due to the channel length modulation, V_{th} mismatch and other high frequencies nonidealities involving the parasitic capactances of the transistors, a thorough analysis of this effects is carried out by Koli et at [53].

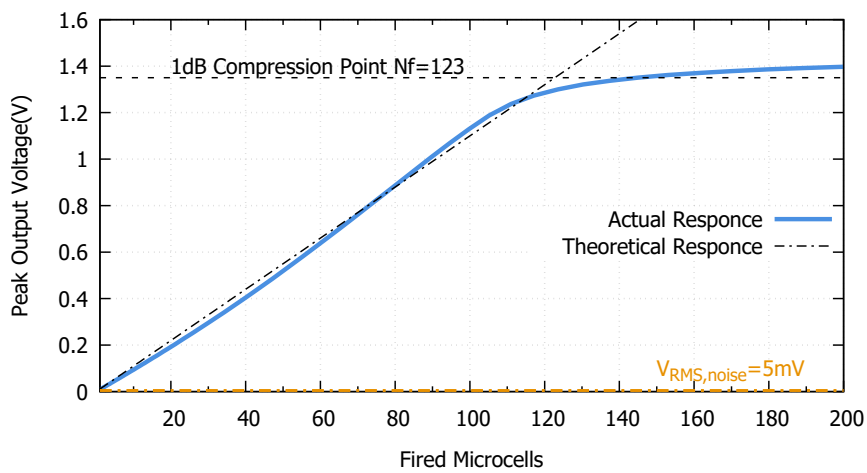
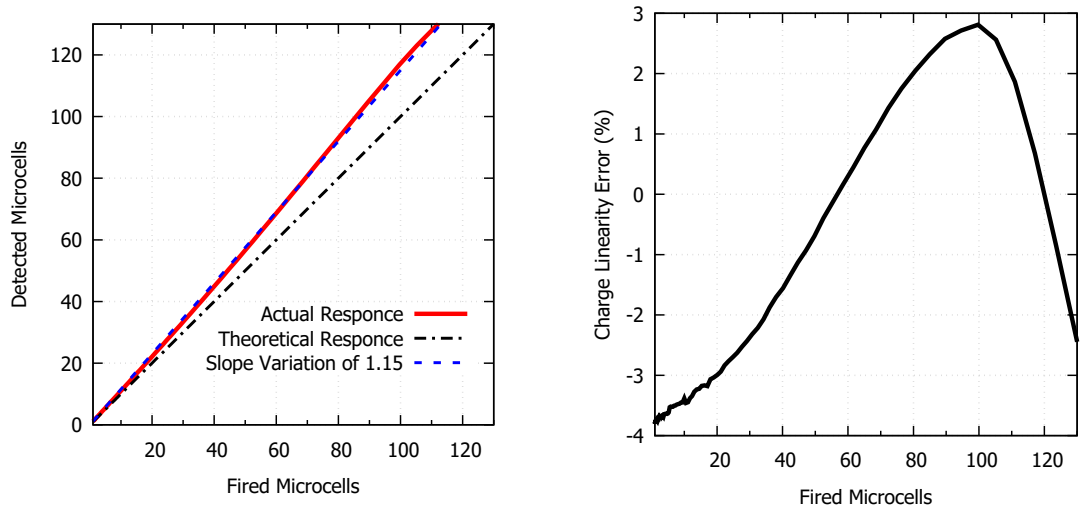


Figure 4.21: Current buffer output to detected photoelectrons.

From equation 2.21 the charge of an event is calculated by integrating the output voltage of the preamplifier, if an integrator with a voltage gain of $A_{V,Int}$ is used, its peak voltage value $V_{peak,Int} = (A_{VInt}\beta R_{in})Q_{in}$ is proportional to the input charge in a linear way.

Figure 4.22(a) gives the relationship between the fired and the detected microcells, ideally the ratio should be a 1 to 1 association, however the actual response delivers a

1.15 variation on its slope, this is attributed to a current copy error due to a mismatch of V_{DS} form transistors M1 and M3, as a consequence the transimpedance gain varies form the theoretical 500Ω value to a measured 575Ω, that is a variation of 575Ω/500Ω = 1.15. From a topological perspective, the use of cascode current mirrors reduces this voltage variation at an expense of a lower output dynamic range. The linearity error of the detected charge varies to a maximum of 4% as seen in figure 4.22(b).



(a) Detected vs fired microcells variation.

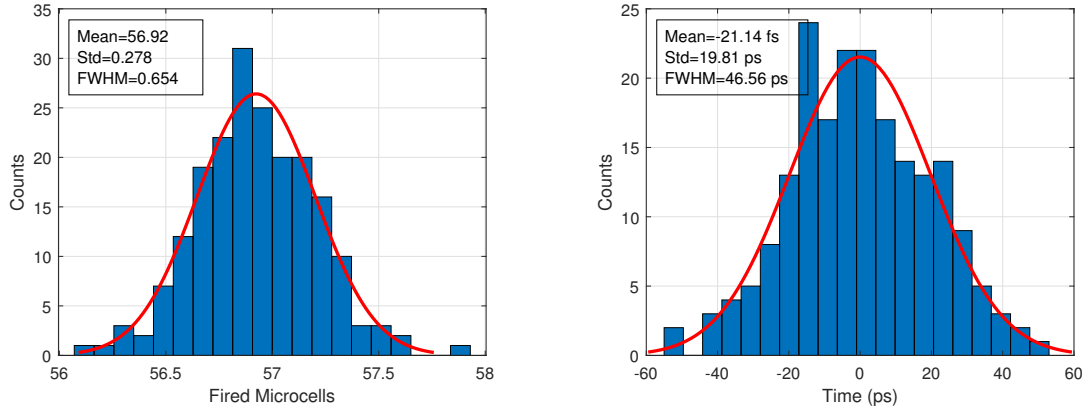
(b) Charge Linearity error variation.

Figure 4.22: Current buffer charge variation to detected photoelectrons.

Time and Charge Resolution

To evaluate the time and charge resolution of the preamplifier, transient noise is activated in the simulation and 200 periodical pulses with the same number of fired microcells are send to the current buffer, the amplified signal is used by a comparator to measure the time jitter and by an integrator to measure the number of detected microcells and its uncertainty, figure 4.3.3. illustrate the result of the simulations.

The measured charge resolution results in a standard deviation of 0.28, this result is lower than the theoretical NMR of 1.28, interestingly if the RMS noise when the fast equivalent capacitance is coupled to the preamplifier is taken, the theoretical NMR is equal to 0.26. In the case of the time resolution, the measured jitter is equal to 19.18ps,



(a) Charge Resolution.

(b) Time Jitter.

Figure 4.23: Charge and Time Resolution of the current buffer preamplifier for $N_F = 50$.

the estimated values of 15ps are actually very close which demonstrates the accuracy of the jitter expression. Both measured charge and time resolutions exceed the requested specifications.

4.4 Conclusions

In this chapter the design of a preamplifier using the voltage amplifier and current buffer readout approach was made to accomplish the required radiation detector specifications. In both cases a similar methodology was carried out: First the calculation of the input resistance R_{in} is made according to the required Event Count Rate (ECR) and Pile-Up error.

Secondly from the selected input resistance and the Charge and Time resolution requirements, the design parameters such as bandwidth and the input referred noise of the proposed preamplifiers is estimated. Subsequently, the analog circuit is designed to achieve the calculated specifications. Next with the electrical characterization of the preposed preamplifiers, an estimation of the input dynamic range, charge and time resolution is made to ensure that the proposed circuit satisfy the radiation detector specifications.

Finally, the SiPM model, a comparator and an integrator are connected to the proposed preamplifier and simulations are carried out to verify the performance of the preamplifier. From the simulated results, it is visible that the proposed methodology ensures that the final design accomplishes the required specifications of the radiation detector.

Comparing the results form the voltage amplifier and the current buffer, the voltage amplifier has a better input dynamic range thanks to its variable gain mechanism, and a very high time resolution when a large number of microcells are fired, on the other hand the current buffer exhibits a better charge and time resolution for a lower number of microcells thanks to its lower output noise, using only a half of the bandwidth and one tenth of the power in comparison to the voltage amplifier.

Parameter	V_{ctrl} @ 900mV	V_{ctrl} @ 220mV
V_{supply}	$1.8V, \pm 0.9V$	$1.8V, \pm 0.9V$
Power Consumption	$11.4mW$	$11.4mW$
Gain	$46dB$	$4dB$
Bandwidth ($C_L, 0.5pF$)	$501MHz$	$363MHz$
Cut-off Frequency	$123Hz$	$2.7Hz$
IRN @ 10MHz	$13.8nV/\sqrt{Hz}$	$34nV/\sqrt{Hz}$
IRN (RMS)	$268\mu V$	$600\mu V$
Output Noise (RMS)	$40mV$	$1mV$
$A_{V,CM}$ @ 10MHz	$-255dB$	$-137dB$
$CMRR$ @ 10MHz	$301dB$	$183dB$
$PSRR+$ @ 10MHz	$278dB$	$144dB$
$PSRR-$ @ 10MHz	$279dB$	$144dB$
Input Range	$\pm 260mV$	$\pm 260mV$
Output Range	$114mV/864mV$	$114mV/864mV$
Rise Time ($500mV_{pp}$)	$986ps$	$1.47ns$
Fall Time ($500mV_{pp}$)	$928ps$	$1.17ns$
Slew Rate+ ($500mV_{pp}$)	$331(V/\mu s)$	$245(V/\mu s)$
Slew Rate− ($500mV_{pp}$)	$352(V/\mu s)$	$297(V/\mu s)$

Table 4.10: Electrical characterization of the proposed voltage amplifier

Parameter	$C_{in} = 64pF$	$C_{in} = 307pF$
V_{supply}	$1.8V, \pm 0.9V$	
Power Consumption	$1.3mW$	
Input Impedance R_{in} @ 26MHz	5.1Ω	
Input Impedance R_{in} @ 100MHz	11.8Ω	7.78Ω
Transimpedance @ 26MHz	575Ω	
Bandwidth ($C_L = 0.25pF$)	$217MHz$	$100MHz$
IRN @ 10MHz	$86pA/\sqrt{Hz}$	$197pA/\sqrt{Hz}$
IRN (RMS)	$23\mu A$	$113\mu A$
Output Noise (RMS)	$2.7mV$	$5mV$
Maximum input current	$2mA$	
Output Range	$-554mV/609mV$	
Rise Time ($500mV_{pp}$)	$1.56ns$	$2.4ns$
Fall Time ($500mV_{pp}$)	$2ns$	$3.2ns$
Slew Rate+ ($500mV_{pp}$)	$185(V/\mu s)$	$138(V/\mu s)$
Slew Rate− ($500mV_{pp}$)	$146(V/\mu s)$	$109(V/\mu s)$

Table 4.11: Electrical characterization of the proposed current buffer

Parameter	**Voltage Amplifier**	**Current Buffer**
ECR @ 10% PE	$\leq 1MHz$	$\leq 3.5MHz$
Input Resistor	50Ω	5.1Ω
Dynamic Range	$1 - 1800\mu cell$	$1 - 123\mu cell$
Time Resolution	$115ps$	$19.81ps$
Time Resolution (FWHM)	$270ps$	$46.5ps$
Charge Resolution	$5.17\mu cell$	$0.27\mu cell$
Charge Resolution (FWHM)	$12.14\mu cell$	$0.63\mu cell$
Power consumption	$11.4mW$	$1.3mW$

Table 4.12: Proposed Voltage and Current Buffer Preamplifier Performance.

Chapter 5

Post-layout results

As a part of the analog electronic design, both circuit require to be transformed from the schematic level to the physical design, also called layout. In this chapter the layout of both preamplifiers is made in a 6 metal 1 poly standard 180μm CMOS Technology from TSMC and then their the electrical characterization and performance when used in a radiation detector is evaluated.

5.1 Voltage Amplifier

5.1.1 Electrical Characterization

The layout of the proposed voltage amplifier is shown in figure 5.1, and has an area footprint of $197\mu m \times 36.5\mu m$. The post-layout characterization of the proposed voltage amplifier when a large and a low gain is selected is shown in table 5.1.1.

Regardless of the amplification value, the power consumption still remains constant. The voltage gain has been reduced from the schematic simulation, however it is successfully selected form 39.2dB to 0dB, the cut-off frequency varies form 37Hz to 1.7Hz, and the total bandwidth has been increased to 2.5GHz when the maximum gain is selected due to the appearance of the zero inside of its bandwidth, as seen in figure 5.2, as a result, a peaking at 530MHz is observable and an overshoot of 14% is appreciated in the output signal.

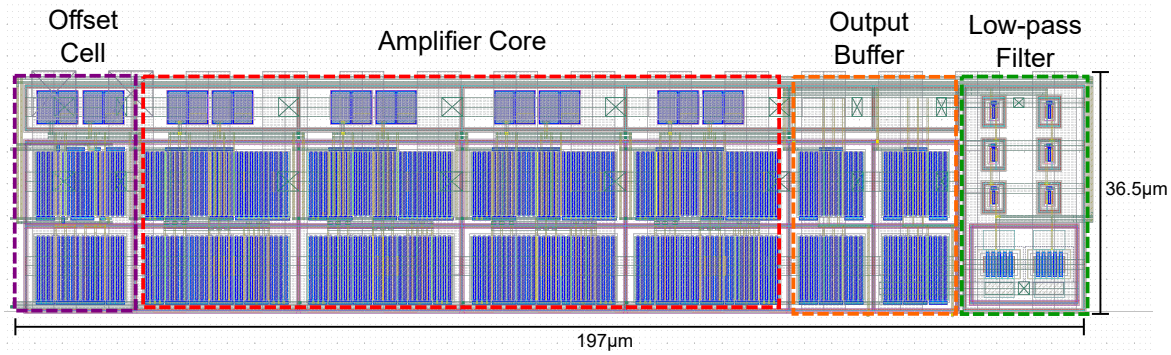


Figure 5.1: Layout of the proposed voltage preamplifier.

The Input-Referred Noise (IRN) is close to the maximum design specifications when $V_{ctrl} = 200mV$. The proposed voltage amplifier experiences a significant reduction of its CMRR and PSRR caused to the parasitic elements of the layout.

The Input Dynamic Range remains constant to $\pm 260mV$ and, finally, the slew rate of the proposed amplifier remains relatively constant regardless of the selected voltage gain. In summary the voltage preamplifier experiences a reduction of the differential gain, a peaking caused by the appearance of the zero and an increase of its bandwidth and its overshoot percentage.

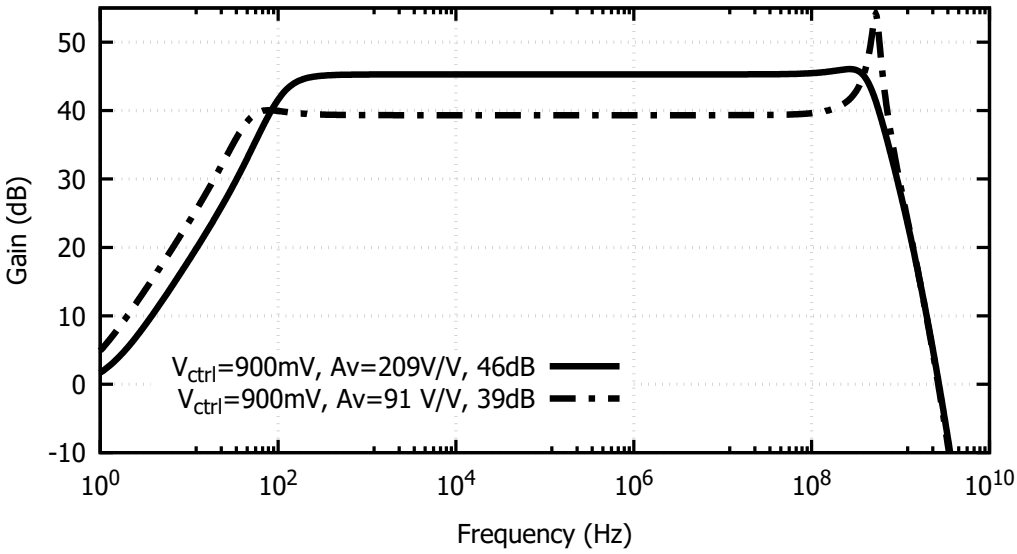


Figure 5.2: Post-Layout AC response with Vctrl variation.

Parameter	V_{ctrl} @ 900mV	V_{ctrl} @ 200mV
V_{supply}	$1.8V, \pm 0.9V$	
Power Consumption	$13.87mW$	
Gain	$39.25dB$	$0dB$
Bandwidth ($C_L, 0.5pF$)	$2.5GHz$	$1.13GHz$
Cut-off Frequency	$37Hz$	$1.5Hz$
IRN @ 10MHz	$13.8nV/\sqrt{Hz}$	$35.13nV/\sqrt{Hz}$
IRN (RMS)	$268\mu V$	$708\mu V$
Output Noise (RMS)	$46.2mV$	$894\mu V$
$A_{V,CM}$ @ 10MHz	$-16.4dB$	$-56.9dB$
$CMRR$ @ 10MHz	$55dB$	$56.9dB$
$PSRR+$ @ 10MHz	$33.25dB$	$51.7dB$
$PSRR-$ @ 10MHz	$32.85dB$	$31.7dB$
Input Range	$\pm 260mV$	$\pm 260mV$
Output Range	$114mV/864mV$	$114mV/864mV$
Rise Time ($500mV_{pp}$)	$929ps$	$1.1ns$
Fall Time ($500mV_{pp}$)	$895ps$	$1.14ps$
Slew Rate+ ($500mV_{pp}$)	$360(V/\mu s)$	$282(V/\mu s)$
Slew Rate− ($500mV_{pp}$)	$362(V/\mu s)$	$270(V/\mu s)$
Overshoot ($500mV_{pp}$)	14%	4.3%

Table 5.1: Electrical characterization of the proposed voltage amplifier

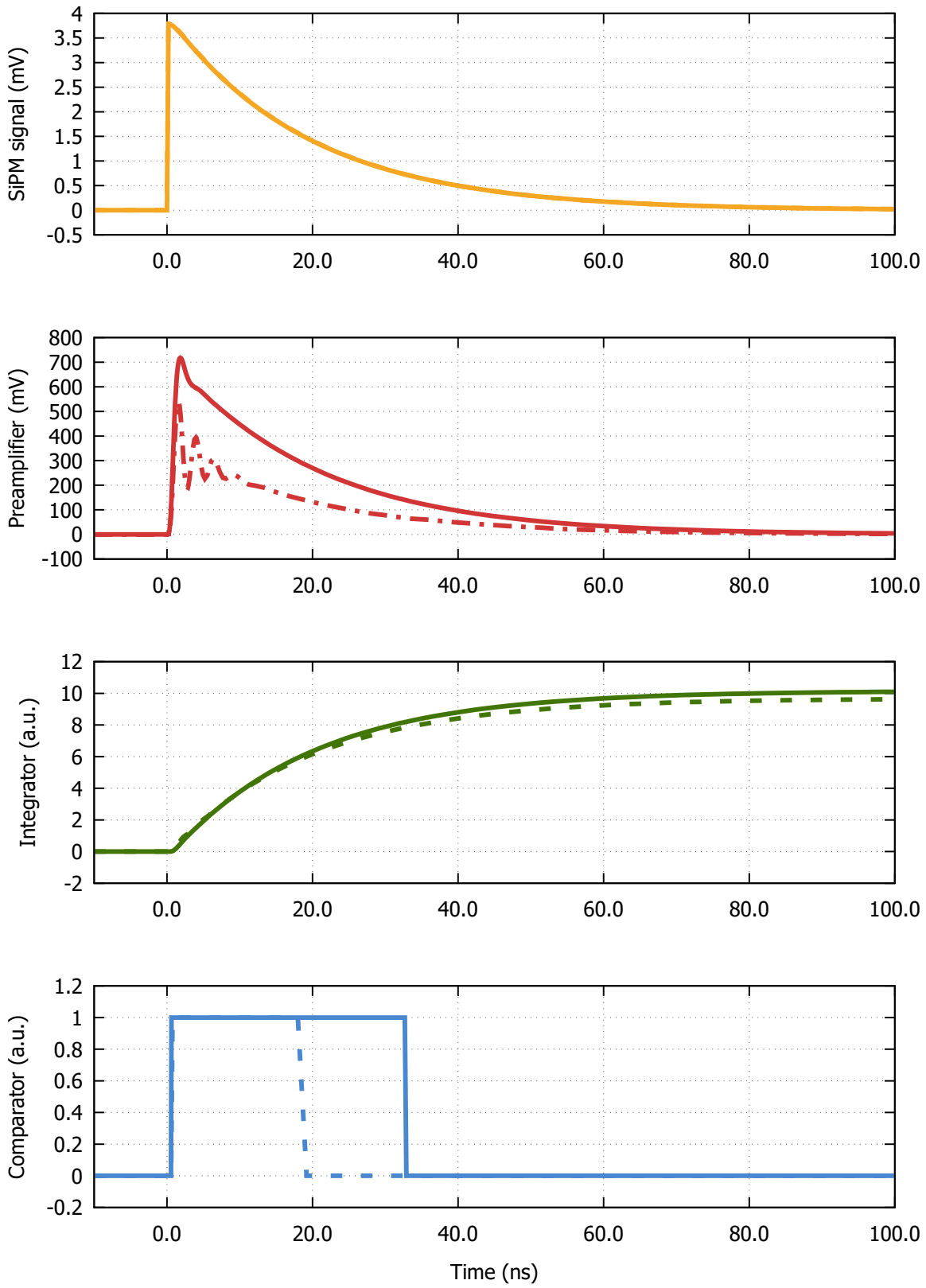


Figure 5.3: Waveforms of the SiPM signal, proposed voltage preamplifier, integrator and comparator when 10 microcells are fired. Post-layout simulations shown as doted lines.

5.1.2 Radiation detector measurements

The transient signals comparison from the schematic and post-layout simulations for the SiPM sensor, the preamplifier, the integrator and the comparator are visible in figure 5.3, even thought an overshoot is visible in the output of the preamplifier, the charge integration is not affected.

Dynamic Range

Using the same methodology form section 4.2.3, simulations results in Figure 5.4 where the dynamic range of the preamplifier is shown for multiple gain values selected, the post-layout simulations are visualized with doted lines and compared with the schematic simulations using the same V_{ctrl} values.

The 1dB compression point of the output peak value varies with respect to the selected gain, for a 39dB gain (91V/V) its located at $12\mu cell$, and for a voltage gain of 0dB (1V/V) at $800\mu cell$, however an increase of the slope is visible at $400\mu cell$ caused by the limitations of the input-dynamic range. As expected the preamplifier is unable to read the totality of the microcells from the SiPM.

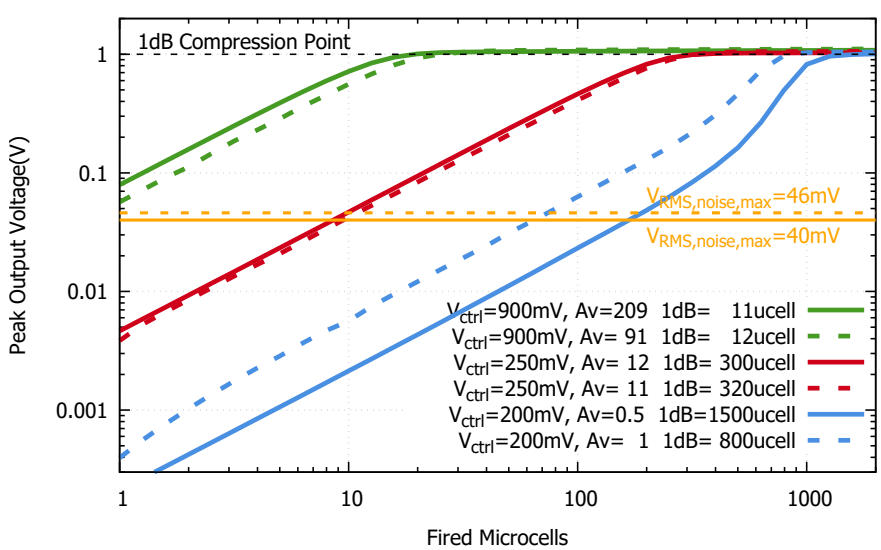


Figure 5.4: Voltage amplifier output to detected photoelectrons, post-layout simulations shown as doted lines.

Interestingly even after the preamplifier reaches saturation, the information of the charge remains uncompressed for a few more microcells as visualized in Figure 5.5 where the normalized peak value of the integrator is ploted. Even thought the 1dB compression point begins when 800$\mu cell$ are fired for a voltage gain of 0dB (1V/V), the front-end electronics is capable to detect the charge of up to 1700$\mu cell$.

Comparing the schematic vs post-layout simulations, the voltage amplifier gain is greatly affected by the parasitic elements, selecting the same control voltage value V_{Ctrl} results in a variation of the amplification factor, thus affecting the number of detectable microcells, the mitigation of this effect requires to be addressed in future works.

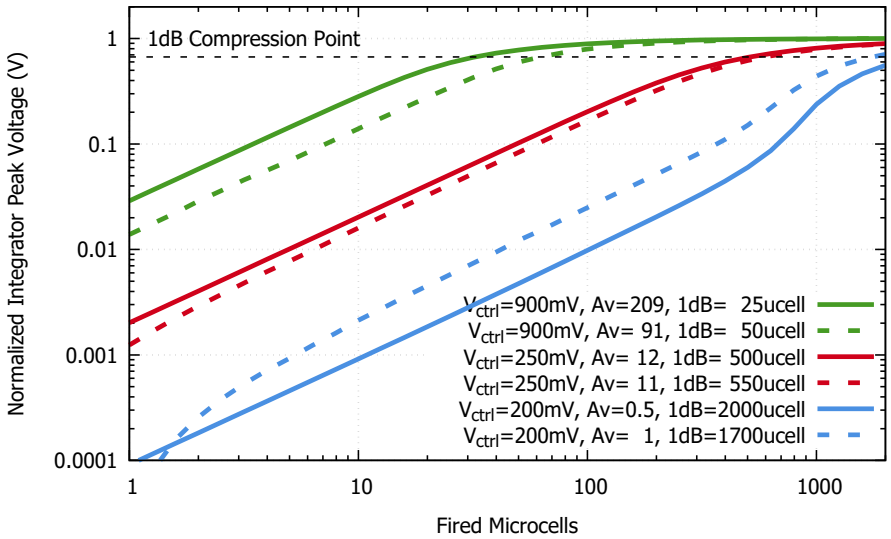
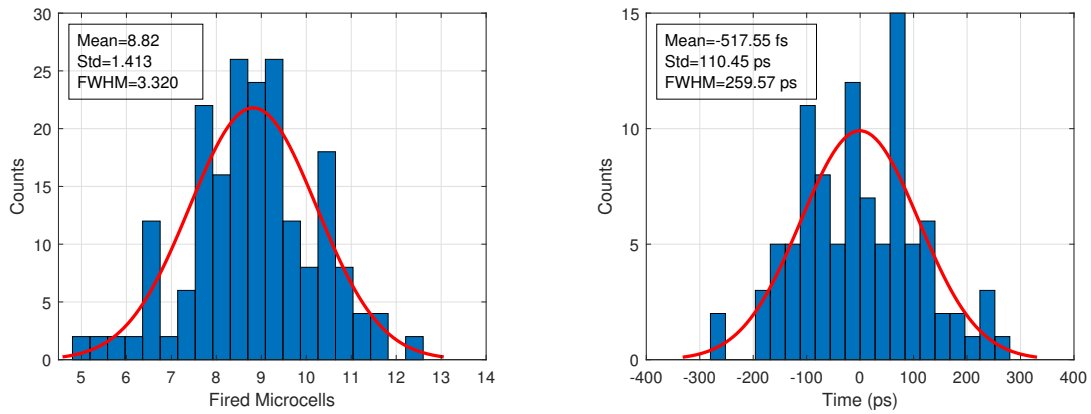


Figure 5.5: Normalized integrator peak output to detected photoelectrons, post-layout simulations shown as doted lines.

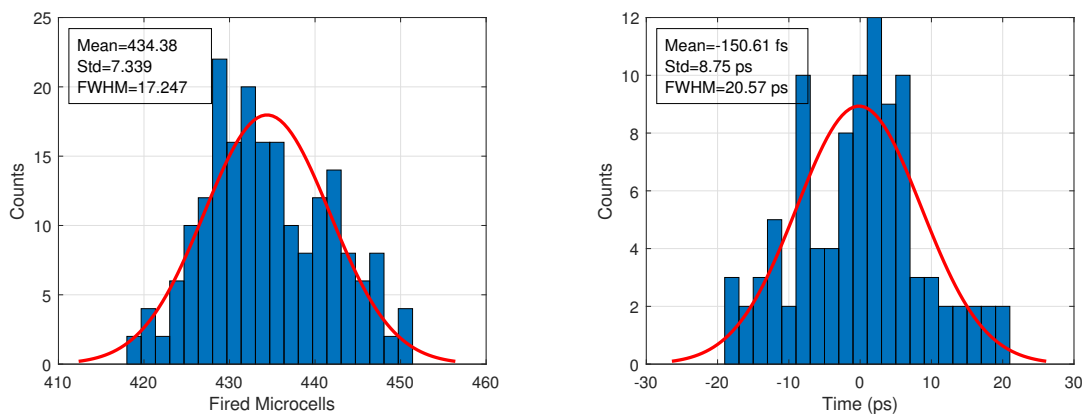
Time and Charge Resolution

Following the methodology of section 4.2.3, figures 4.2.3 and 4.2.3 illustrate the result of the firing of 10 and 400 $\mu cell$ respectably. The measured charge resolution for a V_{ctrl} of 900mV results in 1.4 and 7.3 for V_{ctrl} of 200mV. In the case of the time resolution, the measured jitter is 110ps and 8.75ps for a V_{ctrl} of 900mV and 200mV respectively. Both measured time resolutions exceed the required specification of 1μs.



(a) Charge Resolution. (b) Time Jitter.

Figure 5.6: Charge and Time Resolution of the voltage preamplifier for $N_F = 10$, $V_{ctrl} = 900mV$ and $A_V = 91V/V$.



(a) Charge Resolition. (b) Time Jitter.

Figure 5.7: Charge and Time Resolution of the voltage preamplifier for $N_F = 400$, $V_{ctrl} = 200mV$ and $A_V = 1V/V$.

5.2 Current Buffer

5.2.1 Electrical Characterization

The layout of the proposed current buffer is shown in 5.8 and has an area of $53.8\mu m \times 36.5\mu m$. The post-layout characterization of the proposed current buffer for the two equivalent input capacitances of the SiPM sensor are shown in table 5.2.1.

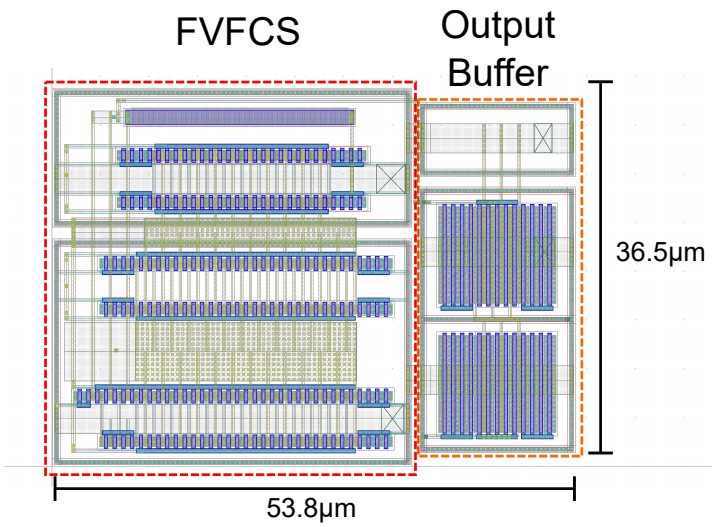


Figure 5.8: Layout of the proposed current buffer preamplifier.

For energy measurements the input capacitance is set at $C_{in} = 307pF$, the input impedance remains very close to the required 5Ω specification, the transimpedance gain has a variation of 1.22 from the theoretical 500Ω value the bandwidth surpasses the $26MHz$ requirement by three times and the input referred noise remains inside the $400pA/\sqrt{Hz}$ range.

For time measurements the input capacitance is set at $C_{in} = 64pF$, the transimpedance bandwidth, surpass the specifications by almost the double, the input impedance, reaches 7.8Ω at the required bandwidth, thus a lower peak output value is expected than with and ideal resistor and the input referred noise is four times lower than the maximum required value.

Parameter	$C_{in} = 64pF$	$C_{in} = 307pF$
V_{supply}	$1.8V, \pm 0.9V$	
Power Consumption	$1.3mW$	
Input Impedance R_{in} @ 26MHz	5.4Ω	5.7Ω
Input Impedance R_{in} @ 100MHz	13.2Ω	7.83Ω
Transimpedance @ 26MHz	584Ω	610Ω
Bandwidth ($C_L = 0.25pF$)	$195MHz$	$92MHz$
IRN @ 10MHz	$89.4pA/\sqrt{Hz}$	$202pA/\sqrt{Hz}$
IRN (RMS)	$23.4\mu A$	$112\mu A$
Output Noise (RMS)	$2.38mV$	$4.64mV$
Maximum input current	$2mA$	
Output Range	$-554mV/609mV$	
Rise Time ($500mV_{pp}$)	$1.53ns$	$2.45ns$
Fall Time ($500mV_{pp}$)	$2ns$	$2.9ns$
Slew Rate+ ($500mV_{pp}$)	$189(V/\mu s)$	$115(V/\mu s)$
Slew Rate− ($500mV_{pp}$)	$140(V/\mu s)$	$97(V/\mu s)$
Overshoot ($500mV_{pp}$)	7.17%	26%

Table 5.2: Electrical characterization of the proposed voltage amplifier

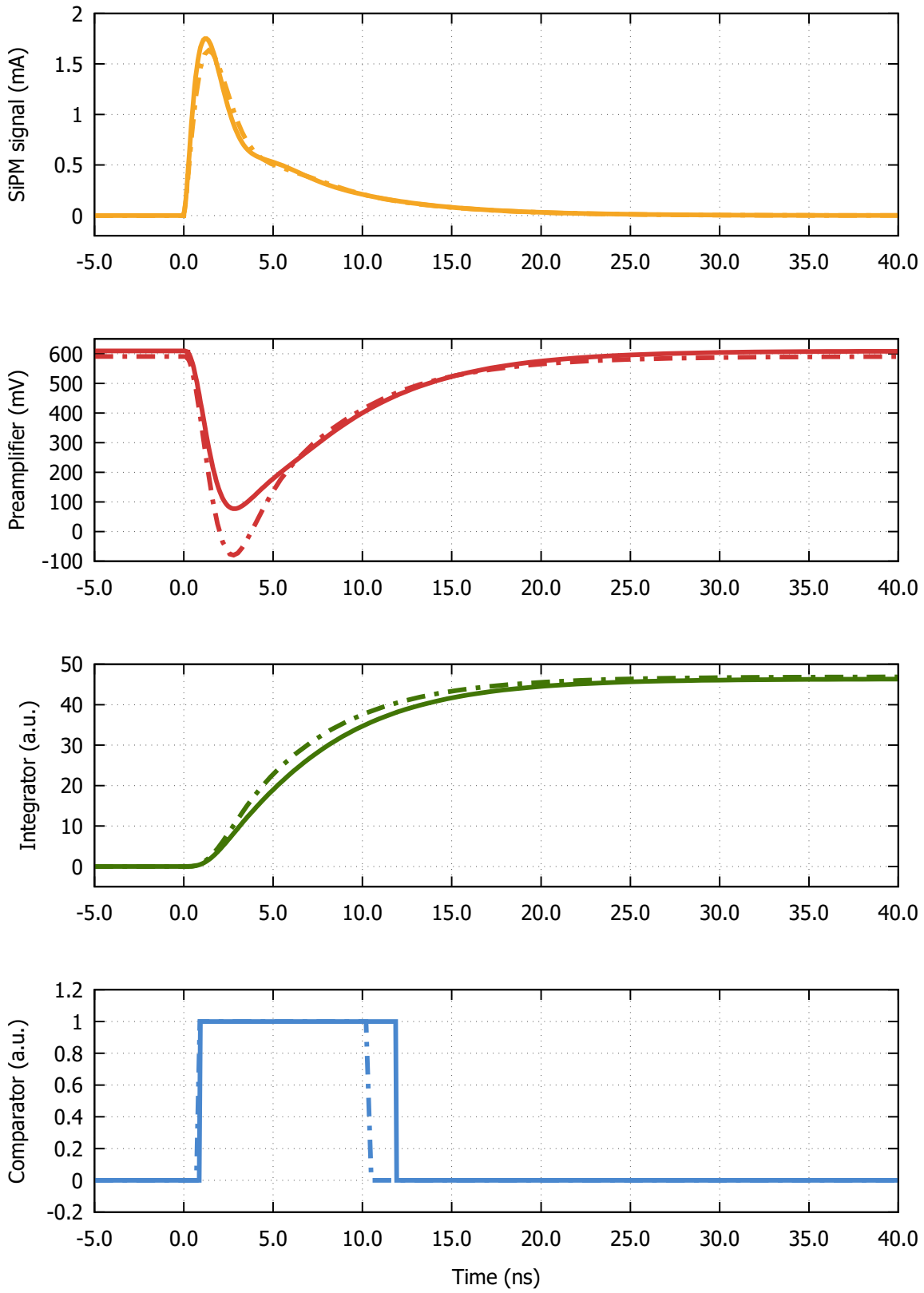


Figure 5.9: Waveforms of the SiPM signal, proposed current buffer preamplifier, integrator and comparator when 50 microcells are fired. Post-layout simulations shown as doted lines.

5.2.2 Radiation detector measurements

The transient signal comparison form the schematic and post-layout simulations of the SiPM sensor, the current buffer preamplifier, the integrator and the comparator are visible in figure 5.9. Is visible a great similitude to the ones obtained in the schematic level simulation.

Dynamic Range

Following the methodology of section 4.3.3, the dynamic range of the preamplifier is shown in figure 5.10 where the post-layout results are displayed with doted lines. The 1dB compression point of the peak value is reached at $104\mu cell$, a reduction of $19\mu cell$ from the schematic level.

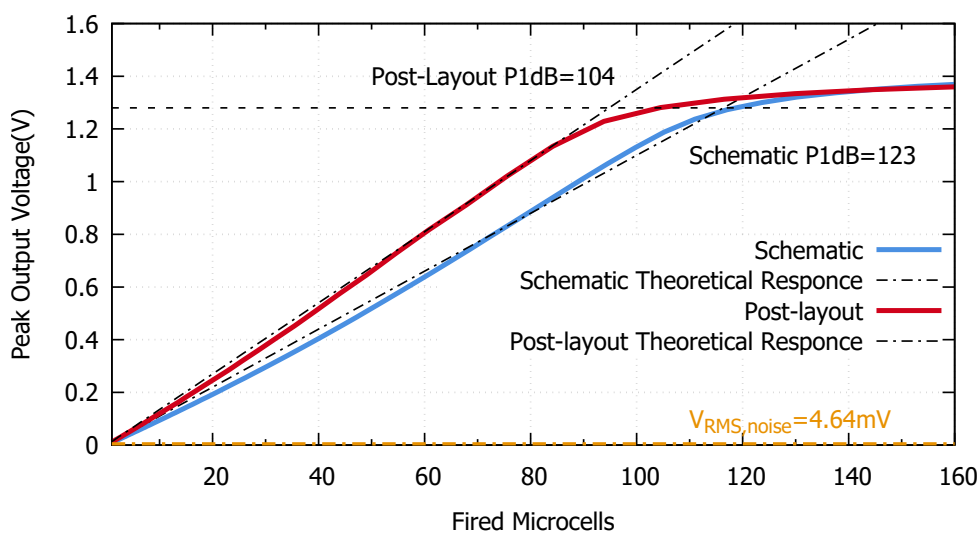
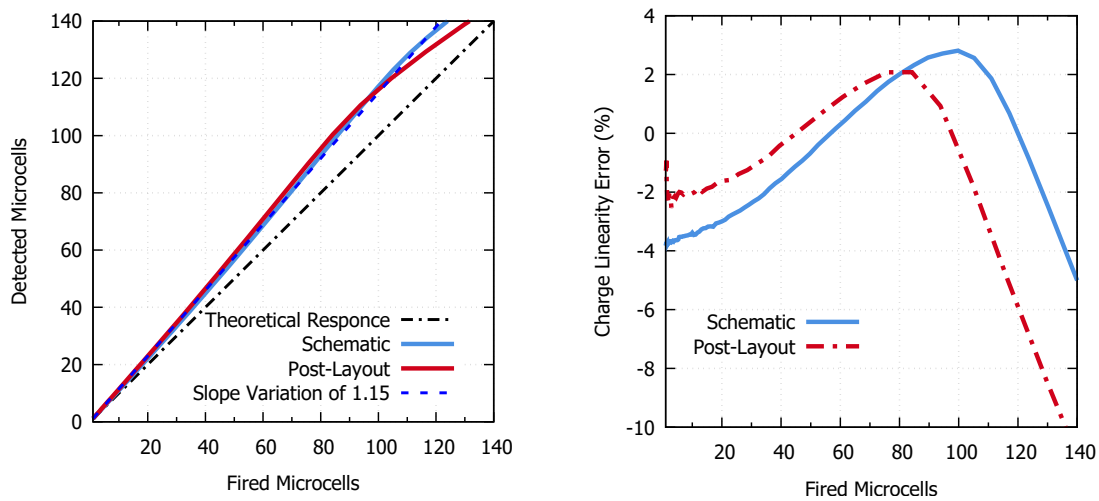


Figure 5.10: Proposed current buffer preamplifier.

Figure 5.11(a) gives the relationship between the fired and the detected microcells, the transimpedance gain varies form the theoretical 500Ω value to a measured 584Ω, that is a variation of $554\Omega/500\Omega = 1.168$. The linearity error of the detected charge varies ±2% until reaching the 1dB point where it starts to increase continuously as seen in figure 4.22(b).



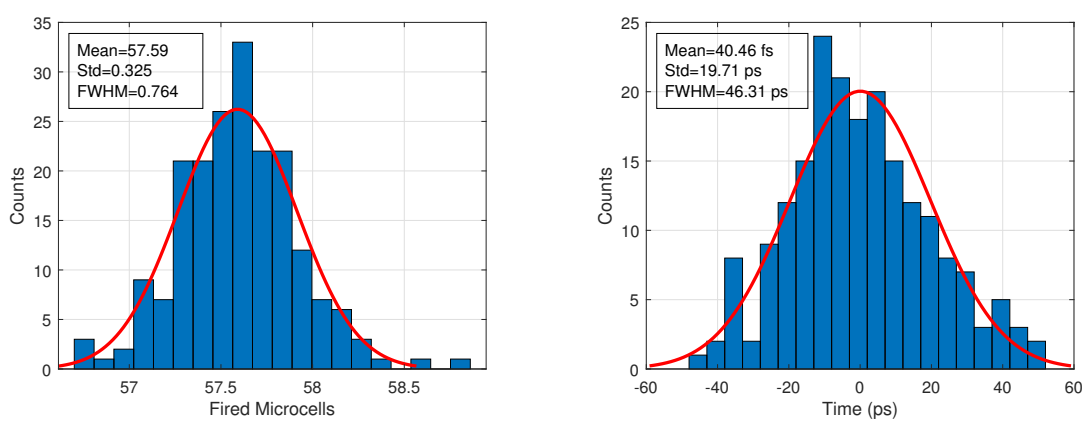
(a) Detected against fired microcells variation.

(b) Charge linearity error variation.

Figure 5.11: Input referred noise against the degeneration resistor R_S.

Time and Charge Resolution

To evaluate the time and charge resolution of the preamplifier, the procedure of section 4.3.3 is pursued, figure 4.3.3 illustrate the result of the simulations. The measured charge resolution results in a standard deviation of 0.32, and in the case of the time resolution, the measured jitter is equal to 19.17ps. Both measured charge and time resolutions exceed the requested specifications.



(a) Time Jitter.

(b) Charge Resolition.

Figure 5.12: Charge and Time Resolution of the current buffer preamplifier for $N_F = 50$.

5.3 Conclusion

In this chapter was presented the post-layout electric characterization and the performance in radiation detectors of the proposed preamplifiers realized in a 6 metal 1 poly standard 180μm CMOS Technology from TSMC.

Tables 5.3 and 5.3 compares the electrical characterization of the voltage amplifier and current buffer preamplifiers in schematic and post-layout simulation levels. In the case of the voltage amplifier, the voltage gain is reduced due to the presence of the parasitic elements of the layout, even thought the gain is controlled with V_{ctrl}, its value diverges from the schematic, the zero in the transfer function affects the frequency response as a result a peaking at 530MHz appears, the input referred noise remains inside the required specifications, and the common mode gain is significantly degraded. For the current buffer, the input impedance, bandwidth and input referred noise remains inside the specifications with a maximum variation of 7% for the bandwidth.

Tables 5.5 and 5.6 summarizes the schematic and post-layout performance of both preamplifiers for radiation detectors. The voltage amplifier experiences a input dynamic range difference of 5%, and a charge and time resolution variation of 4% and 21% respectively. The current buffer preamplifier experiences a variation of 13% in its input dynamic range, of 12% in its charge resolution and 0.5% in its time resolution.

Comparing the results, the voltage amplifier still has a better input dynamic range, and a very high time resolution when a large number of microcells are fired, on the other hand the current buffer exhibits higher Event Cout Rate, and better charge and time resolution using only one tenth of the power and a one third of the total area in comparison to the voltage amplifier approach.

Parameter	**Schematic**	**Post-Layout**
V_{supply}	$1.8V, \pm 0.9V$	
Power Consumption	$11.4mW$	$11.4mW$
Gain	$46dB$	$39.25dB$
Bandwidth ($C_L, 0.5pF$)	$501MHz$	$2.5GHz$
Cut-off Frequency	$123Hz$	$37Hz$
IRN @ 10MHz	$13.8nV/\sqrt{Hz}$	$13.8nV/\sqrt{Hz}$
IRN (RMS)	$268\mu V$	$268\mu V$
Output Noise (RMS)	$40mV$	$46.2mV$
$A_{V,CM}$ @ 10MHz	$-255dB$	$-16.4dB$
$CMRR$ @ 10MHz	$301dB$	$55dB$
$PSRR+$ @ 10MHz	$278dB$	$33.25dB$
$PSRR-$ @ 10MHz	$279dB$	$32.85dB$
Input Range	$\pm 260mV$	$\pm 260mV$
Output Range	$114mV/864mV$	$114mV/864mV$
Rise Time ($500mV_{pp}$)	$986ps$	$929ps$
Fall Time ($500mV_{pp}$)	$928ps$	$895ps$
Slew Rate+ ($500mV_{pp}$)	$331(V/\mu s)$	$360(V/\mu s)$
Slew Rate− ($500mV_{pp}$)	$352(V/\mu s)$	$362(V/\mu s)$
Overshoot ($500mV_{pp}$)	2%	14%

Table 5.3: Schematic and Post-layout comparison of the electrical characterization of the proposed voltage amplifier with V_{ctrl} @ 900mV

Parameter	Schematic	Post-Layout
V_{supply}	$1.8V, \pm 0.9V$	
Power Consumption	$1.3mW$	$1.3mW$
Input Impedance R_{in} @ 26MHz	5.1Ω	5.4Ω
Input Impedance R_{in} @ 100MHz	11.8Ω	13.2Ω
Transimpedance @ 26MHz	575Ω	584Ω
Bandwidth ($C_L = 0.25pF$)	$217MHz$	$195MHz$
IRN @ 10MHz	$89pA/\sqrt{Hz}$	$89.4pA/\sqrt{Hz}$
IRN (RMS)	$23\mu A$	$23.4\mu A$
Output Noise (RMS)	$2.7mV$	$2.38mV$
Maximum input current	$2mA$	$2mA$
Output Range	$-554mV/609mV$	$-554mV/609mV$
Rise Time ($500mV_{pp}$)	$1.56ns$	$1.53ns$
Fall Time ($500mV_{pp}$)	$2ns$	$2ns$
Slew Rate+ ($500mV_{pp}$)	$185(V/\mu s)$	$189(V/\mu s)$
Slew Rate− ($500mV_{pp}$)	$146(V/\mu s)$	$140(V/\mu s)$
Overshoot ($500mV_{pp}$)	2.1%	7.17%

Table 5.4: Schematic and Post-layout comparison of the electrical characterization of the proposed current buffer preamplifier with C_{in} @ 64pF

Parameter	Schematic	Post-layout
ECR @ 10% PE	$\leq 1MHz$	$\leq 1MHz$
Input Resistor	50Ω	50Ω
Dynamic Range	$1 - 1800\mu cell$	$1 - 1700\mu cell$
Time Resolution	$115ps$	$110ps$
Time Resolution (FWHM)	$270ps$	$258ps$
Charge Resolution	$5.17\mu cell$	$7.3\mu cell$
Charge Resolution (FWHM)	$12.14\mu cell$	$17.15\mu cell$
Power consumption	$11.4mW$	$11.4mW$
Area	NA	$197\mu m \times 36.5\mu m$

Table 5.5: Proposed voltage preamplifier schematic vs post-layout performance.

Parameter	Schematic	Post-layout
ECR @ 10% PE	$\leq 3.5MHz$	$\leq 3.5MHz$
Input Resistance	5.1Ω	5.7Ω
Dynamic Range	$1 - 123\mu cell$	$1 - 104\mu cell$
Time Resolution	$19.81ps$	$19.71ps$
Time Resolution (FWHM)	$45.5ps$	$46.4ps$
Charge Resolution	$0.28\mu cell$	$0.32\mu cell$
Charge Resolution (FWHM)	$0.64\mu cell$	$0.75\mu cell$
Power consumption	$1.3mW$	$1.3mW$
Area	NA	$53.8\mu m \times 36.5\mu m$

Table 5.6: Proposed current buffer preamplifier schematic vs post-layout performance.

Chapter 6

Summary and Conclusion

In this chapter, first a summation of the thesis is made, later the main conclusions are listed, and lastly suggestions for future work are given.

6.1 Summary of the Thesis

Chapter 1

A radiation detector is a complex system whose main objective is to extract the timing and energy information from the incident radiation and convert it to a steam of data for storage and future analysis. The electronic circuitry that composes it, called the front-end electronics, is built out of multiple smaller blocks, given that the preamplifier requires to condition the sensor signal, amplify it and send it to the following stages, this circuit rules a great part of the performance of the whole system.

In the design of a radiation detector key parameters are defined by the input preamplifier and in spite of being an analog circuit, this parameters are different or variations of the usually used in analog circuit design such as dynamic range, charge resolution and time resolution. Finally, understanding the internal working mechanism of the SiPM sensor, its signal shape and its equivalent electrical model is mandatory to correctly design the front-end electronics of the radiation detector.

Chapter 2

Given that the SiPM signal is formed by the superposition of a fast and a slow components, the complete electrical model of the SiPM sensor is simplified for hand calculations and simulations purposes. The Charge-Sensitive Amplifier (CSA) is a type of preamplifier commonly used in radiation detectors because the current generated from the sensor is directly integrated and converted into voltage, however given the large number of microcells of the SiPM sensor its input dynamic range, and time resolution is highly limited by the parasitic capacitance of the sensor and the feedback capacitance used to integrate the charge.

The two remaining preampfier approaches are the voltage amplifier and the current buffer, the mathematical analysis of the SiPM signal lead to define the key parameters required for the design of the preamplifiers: the input resistor R_{in} defines the duration of the pulse, thus the maximum Event Cout Rate, the minimum bandwidth ω_{min} defines the minimum required speed of the preamplifier, the parameters Noise-to-Microcell Ratio (NMR) and Noise-to-Slope Ratio (also called Jitter) estimate the charge and time resolution of the preamplifier respectively. Both preamplifier readouts require an additional integrator and comparator to estimate the charge and energy information of an event, furthermore given that the NMR and the Jitter have an opposite relationship to the bandwidth of the preamplifier a dual path topology is recommended, that is the preamplifier should be designed to accomplish the high bandwidth requirements of the time resolution and then its bandwidth reduced by means of a shaper or a band-pass filter to acheive the specified charge resolution. Finally the state of the art indicates that the current buffer approach is better suited for the implementation in integrated circuits due to its lower power consumption and high achievable bandwidths.

Chapter 3

With the objective to study the performance of the remaining readout approaches, a voltage amplifier and a current buffer preamplifier proposals are presented and analyzed. Given the high gain and bandwidth requirements for the time resolution of a radiation

detector based on a SiPM sensor, the voltage amplifier is based in the topology of the limiting amplifier, a topology commonly used in optical communications systems, which is constructed by a core amplifier, a cascade of low gain fully-differential amplifiers, and a differential offset compensation circuit, in order to increase the input dynamic range of the preamplifier and avoid saturation in the output, a mechanism to modify its gain value is added.

The current buffer approach is based on the Flipped Voltage Follower Current Sensor (FVFCS) topology, where its very low input impedance is exploited to reduce the pulse duration and increase the maximum Event Count Rate. Given that the FVFCS behaves as a current mirror, the output current form the SiPM sensor is copied to a high impedance node and then converted into voltage by means of a load resistor. In this circuit a tread-off between bandwidth, output dynamic range, transimpedance gain and noise should be made due to the fact that all of the discussed parameters are affected by the load resistor.

Chapter 4

The design of both preamplifiers is realized by using the following methodology, first is necessary to interpret the specifications of the radiation detector to calculate the required input resistor R_{in}, bandwidth, gain and input referred noise. From the design requirements, the voltage, currents, resistors and transistor sizes are calculated and simulations are carried out to evaluate the compliance of the specifications. Finally the preamplifiers are coupled to a discriminator and an integrator to evaluate its energy and time measurement performance. Comparing the performance of both preamplifiers, the voltage amplifier has approximately 16 times the input dynamic range of the the current buffer due to its incorporated variable gain mechanism, however the FVFCS has 3.5 times the maximum Event Count Rate, 6 and 20 times better time and charge resolution respectively by using only 1/10 of the power consumption of the voltage amplifier.

Chapter 5

As part of the analog design, both preamplifiers are transformed from the schematic level to the physical design, their layout was made in a 6 metal 1 poly standard 180 μm CMOS technology from TSMC. The electrical characterization of both preamplifiers is made and the same methodology form Chapter 4 is carried out and to evaluate their performance when used in a radiation detector. The results are similar to the schematic level simulations, the voltage amplifier has approximately 16 times the input dynamic range of the current buffer. The FVFCS has 3.5 times the maximum Event Count Rate, 5.5 and 23 times better time and charge resolution respectively by using only 1/10 of the power consumption and and 1/4 the total area of the voltage amplifier.

6.2 Contributions

- This work introduces a methodology that translates the requirements of a radiation detector using SiPM sensors into electronic design specifications and from a given design specifications the radiation detector performance can be estimated, furthermore it introduces a procedure to simulate analog circuits to obtain radiation detector parameters.

- By using the presented methodology the architect of the integrated circuit project can calculate and deliver the electrical design specifications to the engineers. They in turn can focus only on the design of the functional blocks and do not spend time in the understanding of the mechanics of the sensor or the radiation detector measurements nature.

- Table 6.1 details the results obtained in this work compared to published SiPM front-end electronics. It is observed that the voltage amplifier approach performs similarly to the reported integrated circuits with the same topology and process, it has superior time resolution to the ones implemented in SiGe technology. The FVFCS approach has the lowest input impedance form all of the current buffer

approaches, one of the lowest time resolution, a very low power consumption and an average input dynamic range.

- From the compassion of the performance of both proposed preamplifiers, the voltage amplifier has a better input dynamic range, however the current buffer approach outperforms it in almost every aspect, making it the ideal architecture in the implementation of a integrated circuit for radiation detector for SiPM sensors.

- Radiation detector are complex system that require a multidisciplinary approach, this often lead to communication, terminology, perspective difficulties who could lead to the unsatisfactory performance of the system. In this work those issues are addressed by standardizing the terminology used by physicist and designers.

6.3 Recommendations of Future Work

- In Chapter 2 the calculation of the electrical design specifications from the SiPM sensor parameters is made. Therefore, in the design of a radiation detector with a different SiPM sensor, the new parameters only need to be substituted and the new design specifications can be calculated.

- Given that the calculation of the total charge depends on the value of voltage gain and that the voltage gain of the voltage amplifier is highly sensible to the control voltage and to the layout parasitics, a discrete method to control the gain values is recommended.

- The addition of either more copy branches, or a mechanism to cancel the bias current from the copied SiPM signal to the proposed FVFCS is recommended to increase its dynamic range.

Work	Name	Readout	Architecture	Process	Bandwidth	Dynamic Range	Time Resolution	Gain	Input impedance	Power	Channels	Year
[33]	VATA64HDR16	Charge	CSA	0.35μm CMOS		Up to 10μA				15mW	64	2010
[54]	FLC	Voltage	Opamp VGA	0.8μm CMOS				40dB	50Ω	25mW	18	2005
[36]	SPIROC	Voltage	Opamp VGA	AMS 0.35μm SiGe		320pC	1ns	40dB	50Ω	25μW	32	2007
[34]	EASIROC	Voltage	Opamp VGA	AMS 0.35μm SiGe		320pC	0.3ns	40dB	50Ω	4mW	32	2011
[37]	PETIROC	Voltage	Opamp VGA	AMS 0.35μm SiGe	10GHz	320pC	0.3ns	40dB	50Ω	3.6mW	32	2013
[39]	PETA	Voltage	LA	0.18um CMOS	900MHz		20ps	26dB	50Ω	86mW	16	2014
[55]	IMOTEPAD	Voltage	VGA	0.35μm CMOS	500MHz	Up to 104pC	42ps		180Ω	16.8mW	64	2010
-	This Work	Voltage	VGA LA	TSMC 0.18μm CMOS	1.2GHz	Up to 270pC	258ps	39dB	50Ω	11mW	-	2020
[56]	MPPC32	Current	Current Conveyor	TSMC 0.35μm CMOS			67ps		10Ω	16mW	32	2013
[35]	NINO	Current	CGA	IBM 0.25μm CMOS	500MHz		100ps	62dB	40Ω	20mW	8	2014
[57]	IRPICS	Current	CGA	IBM 0.25μm CMOS			25ps		30-200Ω	10mW	32	2011
[58]	STIC3	Current	CGA	UMC 0.18μm CMOS			20ps		30Ω	25mW	64	2014
[42]	DIET	Current	CGA	0.18μm CMOS	300MHz	Up to 5mA	25ps		50Ω	1mW readout	64	2017
[59]	EXYT	Current	CGA	0.18μm CMOS	200MHz	Up to 1mA	30ps	1	46Ω	675uW fast readout	64	2016
[60]	TOFPET2	Current	RCGA	110nm CMOS	300MHz		100ps	25dB		2.5mW	64	2016
[61]	BASIC	Current	RCGA	0.35μm CMOS	250MHz		400ps rise time		17Ω	2.6mW	8	2009
-	This Work	Current	FVFCS	TSMC 0.18μm CMOS	195MHz	2mA or 16pC	47ps		5.7Ω	1.3mW	-	2020

Table 6.1: Comparison of SiPM readout ASICs

Appendix A

SiPM Electrical Model

A.1 Loading effects on the SiPM signal

To analyze the loading effects of a generic front-end[1], consider a SiPM sensor connected to an input resistor R_{in} as seen in Figure A.1.

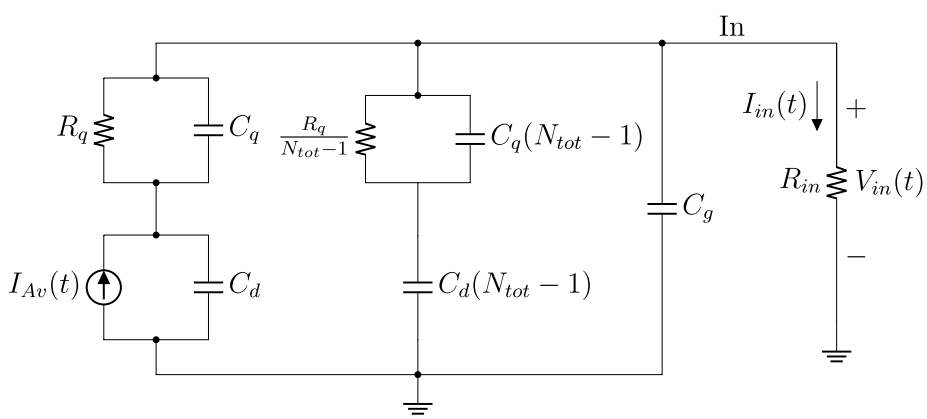


Figure A.1: SiPM model coupled to a generic front-end.

When a microcell is fired, a fraction of the total charged generated from avalanche breakdown Q_F travels very fast trough C_d and C_q arriving to the input node.

$$Q_F = Q_{1\mu cell}\frac{C_q}{C_d + C_q} \tag{A.1}$$

[1]This analysis is based on the work of Calo et al. [11] and Turchetta et al. [26].

Once in the input node, the charge is stored in the equivalent fast capacitance C_F formed by the parasitic non-fired microcells and the grid capacitance C_g.

$$C_F = C_g + (N_{tot} - 1)\frac{C_d C_q}{C_d + C_q} \approxeq C_g + N_{tot}\frac{C_d C_q}{C_d + C_q} \tag{A.2}$$

Since this equivalent capacitance C_F is connected to the input resistance R_{in}, it starts to discharge Q_F at a fast time constant τ_F formed by R_{in} and C_F.

$$\tau_F \approxeq R_{in} C_F \tag{A.3}$$

As a result, the voltage in the node V_{in} experiences an abrupt pulse and then descents at a time constant of τ_F, that is:

$$V_{in_{F_{Ideal}}}(t) = \frac{Q_q}{C_F} e^{-\frac{t}{\tau_F}} \tag{A.4}$$

In reality the abrupt pulse is slowed down by a time constant τ_d conformed by the parallel connection of R_d with R_q and the series connection of C_d and C_q.

$$\tau_d = (R_d || R_q)(C_d || C_q) = \frac{R_d R_q}{R_d + R_q}(C_d + C_q) \tag{A.5}$$

Since $R_d \ll R_q$, R_d remains dominant.

$$\tau_d \approxeq R_d(C_d + C_q) \tag{A.6}$$

This fast rising contribution is then expressed by the following approximate expression:

$$V_{in_F}(t) = \frac{Q_F}{C_F}\frac{\tau_F}{\tau_F - \tau_d}\left(e^{-\frac{t}{\tau_F}} - e^{-\frac{t}{\tau_d}}\right) \tag{A.7}$$

Its peak value is obtained by:

$$V_{in_{F,peak}} = \frac{Q_F}{C_F}\frac{\tau_F}{\tau_F - \tau_d}\left[\left(\frac{\tau_F}{\tau_d}\right)^{\frac{\tau_d}{\tau_d - \tau_F}} - \left(\frac{\tau_F}{\tau_d}\right)^{\frac{\tau_F}{\tau_d - \tau_F}}\right] \tag{A.8}$$

The rest of the total charge Q_S reaches the input node with a rising constant τ_F.

$$Q_S = Q_{1\mu cell}\frac{C_d}{C_d + C_q} \tag{A.9}$$

The parasitic capacitor C_d then discharges its current $I_d(t)$ trough the parallel connection of C_q and R_q at a constant time of τ_r, this is also called the recovery time of the SiPM.

$$\tau_r = R_q(C_d + C_q) \tag{A.10}$$

$$I_d(t) = \frac{Q_S}{\tau_r}e^{-\frac{t}{\tau_r}} \tag{A.11}$$

As $I_d(t)$ is discharged, a secondary discharge path is constructed trough the equivalent slow capacitance C_S formed by the the parasitic non-fired cells and the grid capacitance C_g and the input resistance R_{in}.

$$C_S = C_g + N_{tot}C_d \tag{A.12}$$

This path increases the overall discharge at a slow constant time rate τ_S equal to.

$$\tau_S \approxeq \tau_r + R_{in}C_S \tag{A.13}$$

This approximate analysis leads to a slow contribution to the output voltage $V_{in_S}(t)$.

$$V_{in_S}(t) = R_{in}\frac{Q_S}{\tau_S - \tau_F}\left(e^{-\frac{t}{\tau_S}} - e^{-\frac{t}{\tau_F}}\right) \tag{A.14}$$

Whose peak value is calculated by:

$$V_{in_{S,peak}} = R_{in}\frac{Q_S}{\tau_S - \tau_F}\left[\left(\frac{\tau_S}{\tau_F}\right)^{\frac{\tau_F}{\tau_F - \tau_S}} - \left(\frac{\tau_S}{\tau_F}\right)^{\frac{\tau_S}{\tau_F - \tau_S}}\right] \tag{A.15}$$

Finally the SiPM pulse in voltage $V_{in}(t)$ is constructed by the superposition of its fast and the slow components:

$$V_{in}(t) = V_{in_F}(t) + V_{in_S}(t) \tag{A.16}$$

The complete expression results in the following equation and each individual function is ploted in figure A.2:

$$V_{in}(t) = \frac{Q_F}{C_F}\frac{\tau_F}{\tau_F - \tau_d}\left(e^{-\frac{t}{\tau_F}} - e^{-\frac{t}{\tau_d}}\right) + R_{in}\frac{Q_S}{\tau_S - \tau_F}\left(e^{-\frac{t}{\tau_S}} - e^{-\frac{t}{\tau_F}}\right) \tag{A.17}$$

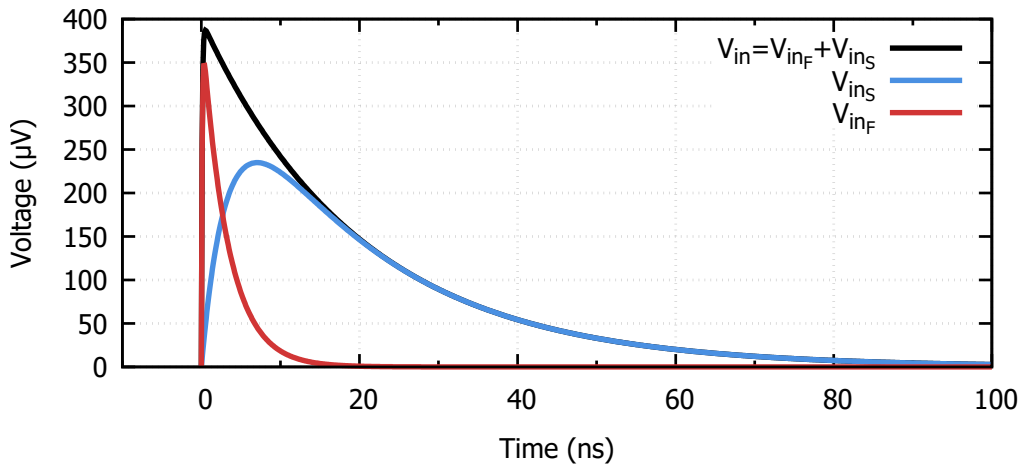


Figure A.2: Slow and Fast components of the SiPM signal, parameters form the Hamamatsu S10931-050P.

In case that the output current is sensed with a current buffer, the input current is calculated by dividing the expression by the input resistance R_{in}.

$$I_{in_F}(t) = \frac{Q_F}{C_F R_{in}}\frac{\tau_F}{\tau_F - \tau_d}\left(e^{-\frac{t}{\tau_F}} - e^{-\frac{t}{\tau_d}}\right) \tag{A.18}$$

$$I_{in_S}(t) = \frac{Q_S}{\tau_S - \tau_F}\left(e^{-\frac{t}{\tau_S}} - e^{-\frac{t}{\tau_F}}\right) \tag{A.19}$$

Where their peak values are calculated by:

$$I_{in_{F,peak}} = \frac{Q_F}{R_{in}C_F}\frac{\tau_F}{\tau_F - \tau_d}\left[\left(\frac{\tau_F}{\tau_d}\right)^{\frac{\tau_d}{\tau_d - \tau_F}} - \left(\frac{\tau_F}{\tau_d}\right)^{\frac{\tau_F}{\tau_d - \tau_F}}\right] \tag{A.20}$$

$$I_{in_{S,peak}} = \frac{Q_S}{\tau_S - \tau_F}\left[\left(\frac{\tau_S}{\tau_F}\right)^{\frac{\tau_F}{\tau_F - \tau_S}} - \left(\frac{\tau_S}{\tau_F}\right)^{\frac{\tau_S}{\tau_F - \tau_S}}\right] \tag{A.21}$$

Interestingly, even thought the peak value of the fast component increases by reducing the R_{in} value, the slow componenent remains relatively constant to its variation. Finally the SiPM pulse in voltage $I_{in}(t)$ is constructed by the superposition of its fast and the slow components:

$$I_{in}(t) = I_{in_F}(t) + I_{in_S}(t) \tag{A.22}$$

The complete expression for the input current results in:

$$I_{in}(t) = \frac{Q_F}{C_F R_{in}} \frac{\tau_F}{\tau_F - \tau_d} \left(e^{-\frac{t}{\tau_F}} - e^{-\frac{t}{\tau_d}} \right) + \frac{Q_S}{\tau_S - \tau_F} \left(e^{-\frac{t}{\tau_S}} - e^{-\frac{t}{\tau_F}} \right) \tag{A.23}$$

The equations obtained in this analysis are compared with the equivalent electrical model using the parameter form the Hamamatsu S10931-050P. In figure A.3 can be seen that the equations recreate with high accuracy the shape of the SiPM signal.

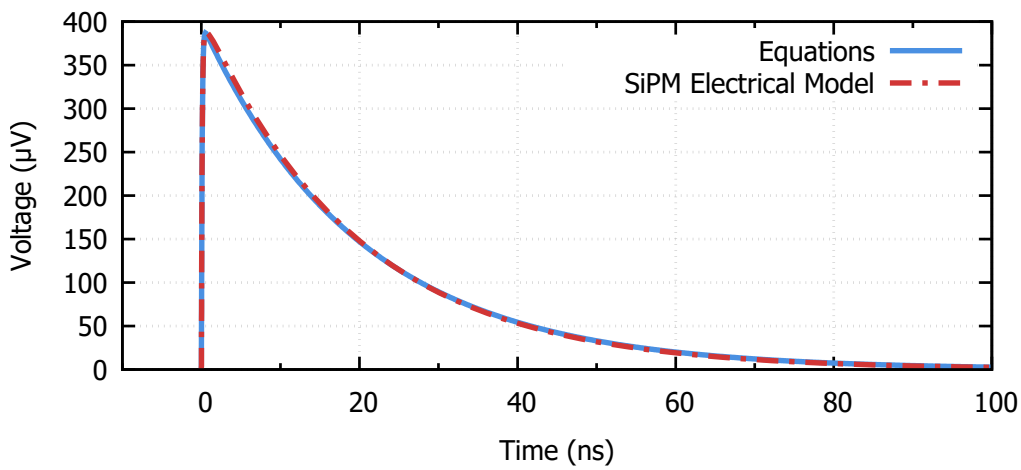


Figure A.3: Comparison between the calculated equations and the SiPM electrical model using the parameters form the Hamamatsu S10931-050P.

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