J Electron Test (2013) 29:289–299
DOI 10.1007/s10836-013-5358-z

Process Variations-Aware Statistical Analysis Framework for Aging Sensors Insertion

J. C. Vazquez · V. Champac · J. Semião · I. C. Teixeira · M. B. Santos · J. P. Teixeira

Received: 9 March 2012 / Accepted: 7 February 2013 / Published online: 3 March 2013
© Springer Science+Business Media New York 2013

Abstract As process technology continues to shrink, Process Variations and Aging effects have an increasing impact on the reliability and performance of manufactured circuits. Aging effects, namely due to Negative Bias Temperature Instability (NBTI) produce performance degradation as time progresses. This degradation rate depends on a) Operational conditions (e.g., V_{DD}, Temperature and time of electrical stress on MOS transistors) and b) Static technological parameters defined in the fabrication process. Moreover, performance of electronic systems for safety-critical applications which operate for many years in harsh environments are more prompt to be impacted by aging. In order to guarantee a safe operation in advanced technologies, aging monitoring should be performed on chip using built-in aging sensors. The purpose of this work is to present a methodology to determine the correct location for aging sensor insertion, considering the combined impact of process variations (PV) and aging effects (namely due to NBTI). In order to implement the methodology, a path-based statistical timing analysis framework and tools have been developed. It is shown that delay path reordering, associated with PV and aging, may justify the insertion of a few additional sensors, to cover abnormal delays of signal paths that become critical, under long system operation (e.g., 10 years).

Keywords Aging sensors · Error prediction · Nanometer technologies · Process variations · Reliability

Responsible Editor: M. Violante

J. C. Vazquez · J. Semião · I. C. Teixeira · M. B. Santos · J. P. Teixeira (✉)
INESC-ID/IST, R. Alves Redol, 9,
1000-029 Lisbon, Portugal
e-mail: paulo.teixeira@ist.utl.pt

J. C. Vazquez · V. Champac
Instituto Nacional de Astrofísica, Óptica y Electrónica (INAOE), Tonantzintla,
Puebla, Mexico

J. Semião
ISE, Universidade do Algarve, Faro, Portugal

I. C. Teixeira · M. B. Santos · J. P. Teixeira
IST, UTL, Av. Rovisco Pais,
1049-001 Lisbon, Portugal

M. B. Santos
SiliconGate, R. Alves Redol, 9,
1000-029 Lisbon, Portugal

1 Introduction

Digital circuit performance and its variability depend on different sources of parametric variations. These variations can be lumped into two categories: Static and Dynamic. Static variations are mainly determined in the manufacturing step by the Process Variations (PV) phenomena [3] and do not change over time. On the other hand dynamic variations, such as changes in Temperature, power supply Voltage and Aging change over time. Among the possible sources of dynamic variations, Negative Bias Temperature Instability (NBTI) has been reported as the most important phenomena causing semiconductor aging in CMOS designs, which represents the main limitation of product lifetime in nanometer technologies [10].

NBTI primarily affects PMOS transistors working in the ON state (negative V_{GS}) degrading its threshold voltage, $|V_{thP}|$, along the time. V_{thP} degradation depends on time, power supply voltage (V_{DD}), temperature (T) and workload experienced by each PMOS transistor. V_{thP} degradation increases the circuit delays, degrading performance and, may, ultimately, cause a system logic failure, due to possible loss of synchronism.

The impact of NBTI degradation on reliability and circuit performance has become an important issue in advanced

technologies [4, 10]. This may pose reliability problems in high-performance products designed to operate for long periods of time. As an example, automotive products must operate for 10 years, for cars, and 15 years, for trucks in harsh environments [14]. Even more, in safety-critical applications, digital system errors are unacceptable. Reliable and dependable system operation is thus mandatory. Therefore, aging effects must be monitored, during product lifetime, to prevent harm.

Research on built-in aging sensors has been significant. Our research team has made in the past significant contributions on this area (see e.g., [5, 8, 9]). Associated with a Circuit Under Test (CUT), sensors observe the propagation delay time of its critical paths (those exhibiting longer propagation delays). If error *prevention* is targeted, sensors verify if a given delay threshold is not exceeded. If this occurs, NBTI mitigation techniques can be used, e.g., by increasing V_{DD} or decreasing the clock frequency, in a synchronous design. However, cost-effective aging monitoring requires not only low-cost sensors, but also an *accurate methodology for sensor insertion* to constrain the number of sensors to be inserted, and to guarantee that they monitor *the* signal paths that may really introduce excessive delays under aging. In our previous work [5], the methodology to insert the aging sensors used a Static Timing Analysis tool (e.g., PrimeTime™). The delay paths were ranked according to their delay values. The longest critical path and a set of Critical Paths (CPs) are selected for sensor insertion. The CP set is composed by all those paths whose delay is close to the delay of the longest critical path within a user's defined acceptable percentage.

It has been shown that NBTI can lead to reordering of the possible critical paths as time progresses [10]. Using static timing analysis without NBTI, the delay of circuit paths do not change over time. However, under NBTI effect, some critical paths may become noncritical while others may turn into critical if they experience large aging. This will depend on the static PV (the rate of aging depends on the technological parameters), and on the operational conditions (V_{DD}, T) and the workload (which depends on the signal probability at its inputs) [13]. Circuit aging strongly depends on PV, producing shifts on both the mean and the variance of circuit timing responses [11]. The relevance of the *combined effect* of PV and NBTI has been stressed in [7], where the authors develop an analytical model to describe it. Since the PMOS degradation due to NBTI is aggravated in the presence of PV, a static timing analysis (even considering aging effect) cannot capture such combined effect of PV and NBTI. Therefore, the insertion of aging sensors based on the static timing analysis information can be insufficient. *Statistical* timing analysis, together with NBTI, is required.

In [2] a technique for selecting paths to be tested for aging during on-line circuit failure prediction is proposed. This is based on a non-path enumerative technique which analyzes and compares the required and arrival times with respect to time zero and aging delays in each one of the lines in the circuit. In that paper, a line is defined as one which connects the output of a gate or a primary input to the input of another gate or to a primary output. A line is canceled from the list only if all the paths passing through that line do not need to be tested for aging. After the cancelation process, all the paths consisting only of the remaining lines (e.g., not cancelled lines) are selected to be tested if they were previously identified as testable paths after ATPG process. The main drawback of this technique is that Static Timing Analysis is used to determine the arrival and required times in each net of the circuit under analysis. Therefore, it does not consider the impact of PV and aging evolution.

The purpose of this paper is to present a new methodology to more accurately determine the correct locations to insert the aging sensors to allow predictive error detection. The proposed methodology takes into account NBTI evolution, critical path reordering and the worst input signal probabilities by using a *statistical* timing analysis framework and tools. The paper is organized as follows. Section 2 briefly reviews NBTI phenomena and its impact on performance. In section 3, predictive error detection and aging sensors are presented. In section 4, the proposed sensor insertion methodology is presented. Section 5 describes the Static and Statistical tools implemented in the proposed methodology. Section 6 presents the simulation results. Finally, section 7 summarizes the main conclusions.

2 NBTI Phenomena and Impact

NBTI is characterized by a positive shift in the absolute value of the PMOS threshold voltage ($|V_{thP}|$), which occurs when the device is placed under stress conditions ($V_{GS} = -V_{DD}$), especially at high temperatures. As PMOS oxide thickness shrinks, the threshold voltage shift caused by NBTI can become a dominant limiting factor in device lifetime. NBTI produces drain current degradation in PMOS transistors. From the digital point of view, this effect gradually slows down logic gate transition speed and eventually can produce a failure. As referred, the degradation rate of circuit performance caused by NBTI depends on both process variations and operation conditions, such as supply voltage (V_{DD}), temperature (T) and *input signal probability* (α) [10].

In [12] it has been shown that for any activated signal path in a digital system there exists a worst value of the *signal probability input* (α) which produces the maximum delay degradation on the propagation delay timing response. The value of this worst α value depends on: (1) the type of

logic gates in the path and (2) how these gates are arranged in the path. The focus in [12] was the propagation delay of the signal path, defined as the average propagation delay for both input transitions ($t_P = (t_{PLH} + t_{PHL})/2$). In this work, the goal is to determine the α value that produces the maximum aging in a path delay for a given transition applied to its *main input*. We refer as *main input* to the switching input which activates a logic path from the input to its output. For any signal path, its two propagation delay responses, t_{PLH} (low to high) and t_{PHL} (high to low), at its output have been analyzed. The paths considered in this work are based on static CMOS gates having inverter behavior (e.g., NOT, NAND and NOR primitive gates). Signal paths are activated with only one input signal switching at a time and all remaining input signals disabled. These latter are tied to non-controlling logic values. This way, we make sure that all the gates in the analyzed path will exhibit an inverter behavior and the signal probability on the nets of the path will be alternated between α and (1-α) values. In order to illustrate the delay behaviour of these considered paths, note that: (1) NBTI mainly impacts the path delay in gates performing a 0–1 transition at their outputs because this kind of transition is driven by the P-network, and (2) for an activated path with a given degradation signal probability of its main input (α_{IN}), the signal probability of degradation at the odd gates is α_{IN} and the signal probability of degradation at the even gates is (1-α_{IN}) [12]. As an example, Fig. 1 shows a 4-inverter chain with a 0–1 transition at its main input. Under this stimulus, the odd-inverters perform 1-0 transitions and even inverters perform 0–1 transitions. A low value of α_{IN} produces a high value of α at the input of the even gates, inducing high degradation in the threshold voltage of their PMOS transistors. On the other hand, a high value of α_{IN} produces a low value of α at the input of the even gates inducing a lower degradation of their PMOS.

Consequently, for 0–1 transition applied at the main input, the path will exhibit maximum degradation as α_{IN} decreases (see Figs. 1 and 2). These data has been obtained by circuit-level simulation, using a 65 nm CMOS technology. If a similar analysis is performed considering a 1-0 transition applied at its main input, we will find that for low values of α_{IN} the degradation on odd gates will be low. On the other hand, high values of α_{IN} will produce high degradation on even gates.

Based on the above observations it is possible to state that:

1. Paths having a 0–1 transition at its main input exhibit high delay degradation for low values of α_{IN}.
2. Paths having a 1-0 transition at its main input exhibit high delay degradation for high values of α_{IN}.

As it will be explained in section 4, in order to determine the paths to be monitored with aging sensors a set of selected paths will be analyzed statistically taking into account statements 1 and 2.

3 Predictive Error Detection and Aging Sensors

For robust electronic system operation, error *detection* is useless since erroneous functionality jeopardizes safe operation. In this case, as systems experience long-term degradation, what it is needed is *predictive error detection*, i.e., the ability to identify the conditions that will lead to a faulty behavior if further timing degradation occurs. In fact, there is a need to detect *almost-faulty* behaviors, so corrective action may take place before harm occurs. On-line *built-in aging sensors* are thus used to monitor system's degrading timing response [8].

In a synchronous digital system, data signals processed in combinational modules are usually registered in storage elements, namely in Flip Flops (FFs). Aging sensors can be inserted in parallel with the terminating FFs of both the longest CP and those paths whose delay is close to the longest CP within a certain percentage [8] (Fig. 3). The sensor checks the path output signal transitions during an *observation interval*, referred as Tg (time guardband) (Fig. 3). Assuming that data are captured by the FFs in the positive transition of the clock signal, Tg is established before this positive clock transition. When the circuit is young (without aging) all the transitions occur before Tg. As circuit ages, transitions will be delayed and eventually they will occur inside Tg. If any transition occurs inside the Tg interval, the sensor flags the existence of an abnormal delay (signal transition close to the positive clock edge), thus identifying a delay error *prediction* [8].

Figure 3 also illustrates a possible behavior of the CP response for a system suffering severe aging. Under this condition, the CP output can switch *after* the positive transition of the clock signal, and the FF will capture an erroneous value, unacceptable in a safety-critical system.

In previous works [5, 8] the authors have proposed different aging sensors topologies. The main advantages of these sensors are: a) Low sensitivity to Process, Voltage, Temperature and Aging (PVTA) variations, b) Programmable Tg (allowing the identification of several threshold levels of delay time degradation due to aging), c) Minimal load sensor impact at the end of the CP and d) Sensor's performance degradation due to aging works in favor of the predictive error detection.

In this work, the goal is to develop a methodology to determine the correct location of these sensors and not, to introduce new aging sensor architectures.

The importance of determining the correct location of the sensors is highlighted with the following example. Let us assume that, due to aging, a transition in any path occurs

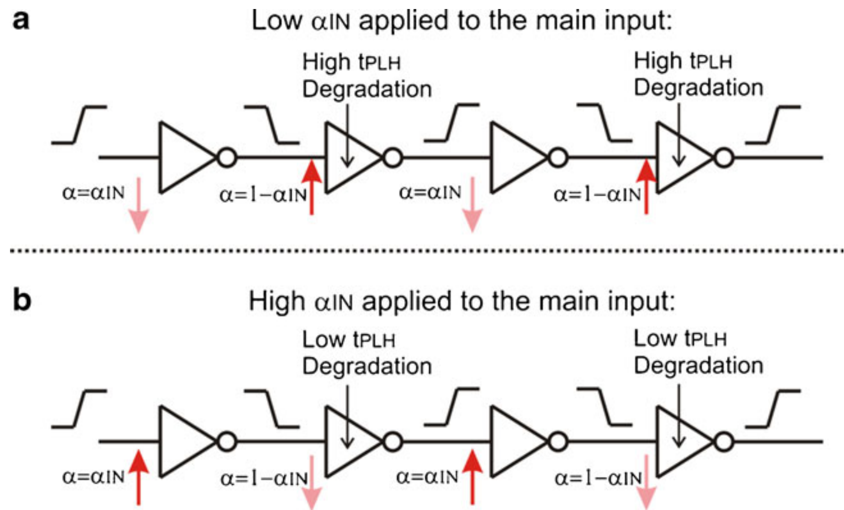

Fig. 1 A 4-inverter chain with 0–1 transition at its main input for two cases: **a** low α_{IN} and **b** high α_{IN}

after the positive transition of the clock signal and this degraded transition was not detected previously because no aging sensor is located at the end of the path. Since this abnormal transition is never detected, the monitoring framework will be unreliable to avoid functional errors occurrence. Therefore, it is crucial to determine the correct location of the aging sensors to be inserted in the digital system.

In the following section, the proposed sensor insertion methodology is explained. This methodology considers statistical analysis, aging impact under statistical responses, path reordering and worst case delay degradation in the paths.

4 Sensor Insertion Methodology

Modern integrated circuits may have millions of signal paths. However, only a limited subset of these paths needs to be monitored for predictive degradation due to aging. In this section, a sensor insertion methodology is proposed to identify the location of the output nodes (ending critical paths) where to insert the aging sensors.

The methodology is composed by three steps as illustrated in the flow diagram of Fig. 4. The first step makes pre-filtering of the paths using static timing analysis. A set composed of the critical paths and the *Potentially Critical Paths (PCPs)* is obtained. *PCPs* are those paths that, after fabrication, at time zero, are not critical but they could

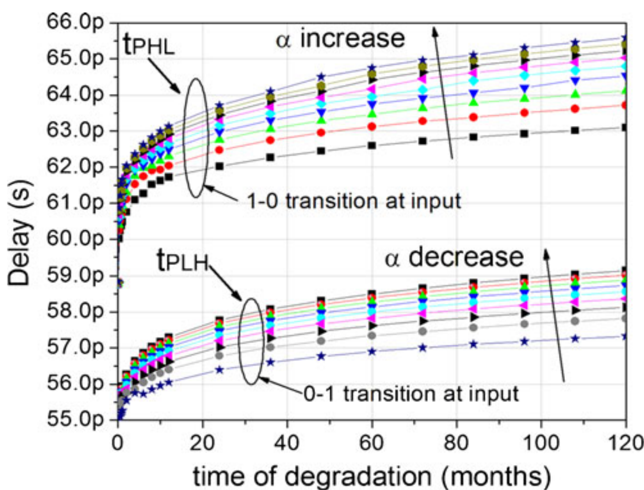

Fig. 2 t_{PHL} and t_{PLH} degradation for the 4-inverter chain of Fig. 1

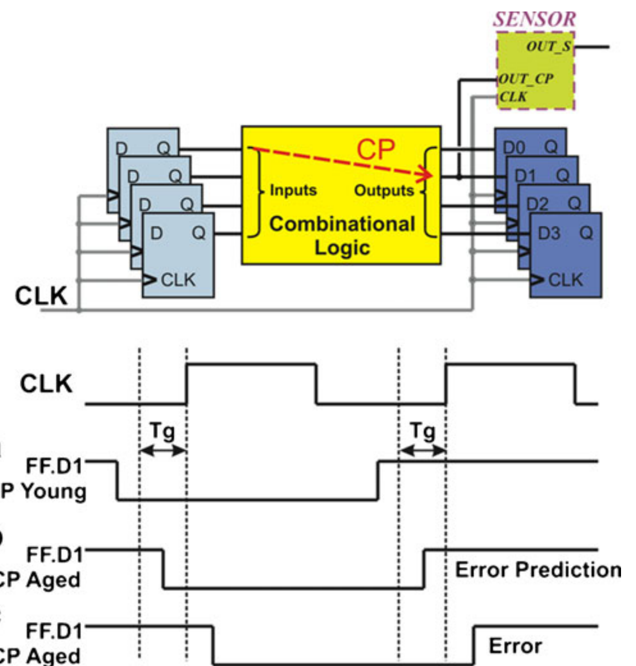

Fig. 3 Error prediction concept in a synchronous digital system. Transitions in the CP for three cases: **a** Young circuit; **b** Partially aged circuit, transitions occur inside Tg and circuit error is predicted by the aging sensor, **c** Completely aged circuit, transitions occur after of the positive transition in the CLK signal producing an error

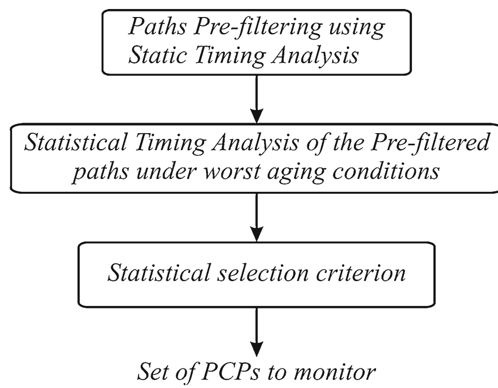

Fig. 4 Flow diagram of the sensor insertion methodology

become critical due to aging effects after some period of time has elapsed. The second step performs statistical timing analysis on the previous pre-filtered paths under worst case aging conditions. Finally, a subset of paths that need to be monitored for aging degradation is selected using a Statistical Selection Criterion. The result is the identification of the output circuit nodes for insertion of aging sensors.

4.1 Paths Pre-Filtering Using Static Timing Analysis

Figure 5 illustrates the methodology to make pre-filtering of the paths. Let us assume that there are N paths in a circuit. The timing delay information associated with each one of these paths is obtained by using traditional static timing analysis for two process corner models: a) Fast-Fast (FF) and b) Slow-Slow (SS).

These paths are ranked and labeled according to their time delay values as P_1, P_2, P_3, ···, P_{N-1}, P_N, where P_1 is the longest Critical Path and P_N represents the path with the smallest delay. Once delay time values for the two corners are obtained, also two delay time values are defined for each path, namely TSn (Time delay for the SS corner) and TFn (Time delay for the FF corner) where n indicates the nth path.

TF_1, that represents the fastest timing response for the longest CP (P_1), is used as the *threshold value* to obtain the pre-*filtered paths set*. As Fig. 5 illustrates, once all the paths are ranked it is possible to identify a set P_2,P_3,…, P_j paths, whose delay satisfies the condition: $TSn > TF_1$. These paths together with P_1 are defined as critical paths. Since the paths in this set impose the operating clock frequency, they will be considered later for further statistical analysis. Figure 5 also illustrates that there will exist P_{j+1},P_{j+2},…, P_k paths, called PCPs, whose delay is lower than TF_1 but they satisfy: $TSn \times (1 + p\%) > TF_1$, where $p\%$ is the worst case degradation parameter and represents the highest degradation percentage a circuit delay may suffer. If the worst delayed response of any path (TSn) from P_{j+1} to P_N multiplied by (1 + p%) factor reaches or exceeds the TF_1 value it means that it is likely

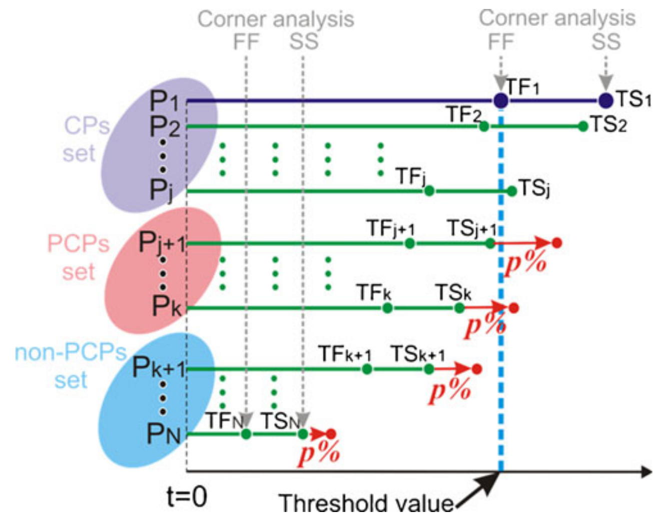

Fig. 5 Criteria to make pre-filtering of the paths. Red arrows represent the $p\%$ quantity of degradation on TSn. If $TSn > TF_1$ or $TSn(1 + p\%) > TF_1$, then the nth path is pre-filtered

that for some manufactured chips, those paths could exhibit a greater delay than path P_1 for a given aging time. Hence, these paths also need to be filtered for next statistical analysis step.

In [10] it was shown that the maximum timing degradation for a path due to NBTI effect is 20 % after 10 years. This data has been obtained considering a similar technology to the one used in this work. Therefore, based on this reported value, a $p\%$=20 % has been selected. As referred, $p\%$ parameter value depends on several conditions, such as the technology, the circuit itself and the operating conditions. The selected $p\%$ value, used in this work, is larger than the percentage of maximum delay degradation that any path could experience. By using this overestimated value, more PCPs are selected but it is assured that no path with possible reordering endangering correct circuit operation will be left out.

The paths pre-filtering methodology assures that for the non-PCP set (paths from P_{k+1} to P_N in Fig. 5) even working under worst case aging degradation conditions, they cannot become critical paths. Hence, these paths are not monitored for aging effects detection.

4.2 Statistical Timing Analysis of the Pre-Filtered Paths Under Worst Aging Conditions

The paths pre-filtering step was made taking into consideration FF and SS corners of the manufacturing process. However, the scenario with *all* process parameters in their worst/best values is too pessimistic, i.e., it corresponds, in practice, to a very low probability of occurrence. For this reason, statistical timing analysis is applied to the set of pre-filtered paths. A *path-based statistical timing analysis tool*

has been developed to analyze these paths for young (no-aging) and old (aging for a given period of time, namely the specified system lifetime (e.g., 5 or 10 years)).

Statistical analysis of the pre-filtered paths delay is performed considering worst case NBTI degradation and worst case α_{IN} parameter value as described in section 2. In this work, low/high values of α_{IN} are 0.1/0.9 are assumed. Under these circumstances, we statistically analyze the paths delay responses with α_{IN}=0.1/0.9 for paths with a 0–1/1-0 transition at their main input. The result of the statistical analysis is the *mean* (μ_p) and *standard deviation* (σ_p) values of the delays of all the pre-filtered paths for young (μ_{p0}, σ_{p0}) and worst case aged ($\mu_{p\text{-}Aged}$, $\sigma_{p\text{-}Aged}$) paths.

4.3 Statistical Selection Criterion

The final set of the paths to be monitored and, thus, the sensor insertion location is determined using a *Statistical Selection Criterion* applied to the delay information obtained with the statistical timing analysis. In order to determine the paths to monitor, the statistical delay distribution of P_1 (path with maximum delay) under no-aging is compared with the worst aged statistical delay distribution for each path of the pre-filtered paths set.

If an overlap between these distributions exists, then, it is likely that some delays of the analyzed pre-filtered path could reach or exceed the delay of longest critical path P_1. Therefore, aging sensors must be inserted at the end of critical path P_1 and at the end of the pre-filtered path if an overlap area exists between the worst aged statistical delay distribution of this pre-filtered path and the delay distribution of path P_1. In a Gaussian distribution, the area under the curve from -3σ to $+3\sigma$ with respect to its μ covers the 99.7 % of all the possible outcomes in the delay. Hence, if the $\mu_{p\text{-}Aged} + 3\sigma_{p\text{-}Aged}$ value is greater than the $\mu_{P1}\text{-}3\sigma_{P1}$ value, the two distributions overlap. Therefore, the *selection criterion for aging sensor insertion* is as follows:

For each pre-filtered path ending at output ***g***, if $\mu_{p\text{-}Aged} + 3\sigma_{p\text{-}Aged} > \mu_{P1}\text{-}3\sigma_{P1}$, then this pre-filtered path must be monitored, thus requiring that an aging sensor must be inserted at output ***g***.

Furthermore, the following questions should be answered: why it is important to analyze path degradation due to aging using statistical timing analysis? Is it not enough to do it only without aging? For this purpose, let us consider a digital circuit with four outputs (O1, O2, O3 and O4) as an example. Figure 6 shows the delay statistical distributions for paths ending at O1, O3 and O4 nodes *without aging*. In this example, the statistical distribution of the greater delay path (P1) ends in O1 (mean μ_1 and standard deviation σ_1 values). On the other hand, the statistical distribution for the second/third most delayed path that ends in O3/O4 and it has a mean μ_3/μ_4 and standard deviation σ_3/σ_4.

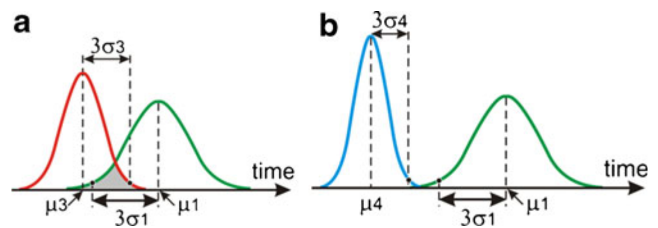

Fig. 6 **a** Overlap area between PCP ending at O1 and PCP ending at O3 distribution, **b** No-overlap area between PCP ending at O1 and PCP ending at O4

Since the $\mu_3 + 3\sigma_3$ value exceeds the value of $\mu_1\text{-}3\sigma_1$ (i.e., there exists an overlapped area between the path delay distributions ending at O3 and O1), then, an aging sensor should be inserted at O3. On the other hand, since the $\mu_4 + 3\sigma_4$ value does not exceed the value of $\mu_1\text{-}3\sigma_1$ (no area overlap between O4 and O1), no aging sensor should be inserted at O4.

However, if the path ending in O4 experiences severe aging, the degraded distribution of O4 will be shifted over time and the condition: $\mu_{4\text{-}Aged} + 3\sigma_{4\text{-}Aged} > \mu_1\text{-}3\sigma_1$ may occur. In this case, a failure in the path ending at O4 could occur and remain undetected, as no aging sensor was inserted at O4. Therefore, in order to make a safe aging prediction to avoid logical failures in a safety-critical digital system, statistical distributions of the pre-filtered paths with aging must be determined.

5 Static and Statistical Timing Analysis Tools

As referred, a *static* timing analysis tool (to make the pre-filtered step) and a *statistical* timing analysis tool (to analyze the statistical delay response of these paths) have been developed. The pre-filtered paths are analyzed using a *path-based* statistical timing analysis. In this section, a description of how these tools have been implemented is provided. The corresponding algorithm has been implemented in C++ code.

5.1 Static Timing Analysis

The gate propagation delay mainly depends on a) its load capacitance (C_L) and its input signal Slew Rate (SRin) [6]. In order to determine the dependence of the gate delay on these parameters, static simulations were performed for each gate of the considered cell library using HSPICE and the process corner model of a 65 nm CMOS technology. t_{PHL} and t_{PLH} values are computed for a transition at each input with the remaining inputs tied to non-controlling logic values. This process is made for different values of C_L and

SRin parameters. The delay data information is then accommodated into look-up tables whose rows are the SRin values and columns are the C_L values. Look-up tables are built for SS and FF design corners.

The path-based static timing analysis lies into the path enumeration technique. It has been assumed SRin=20 ps at the main input and the average C_L value of each gate is determined according to its fan-out. Initially, the tool identifies all signal paths in the digital circuit under analysis. When a topological path is identified, a transition is injected to its main input. Then, the signals are propagated from the main input to the path's output. Knowing the value of SRin and C_L at a gate, its delay is determined accessing the look-up tables. The propagation delays and the Slew Rates are propagated from gate to gate through the gates in the path. The total path delay is determined as the sum of each individual gate's delay in the path

5.2 Path-Based Statistical Timing Analysis

At present, the assumed random process parameters in the tool are channel length (L), transistor width (W), oxide thickness (t_{ox}) and threshold voltage (V_{th}). These parameters are described by normal distributions and assumed mutually independent. The parameters such as length, width and oxide thickness exhibit spatial correlations among different transistors close to each other. The correlation is captured using the rectangular grid model proposed in [1]. In this model, the die area is divided by a multi-level quad-tree partitioning, as shown in Fig. 7.

All MOSFET transistors in a particular grid are assumed to experience the same parameter variations. The spatial correlation among transistors in different grids is governed by their parent grids. For every grid at all levels, a single random variable is used to represent the variation on its process parameter. The total parameter variation of a transistor in any grid at the bottom level is the sum of the variation in that specific grid and the variations in all its

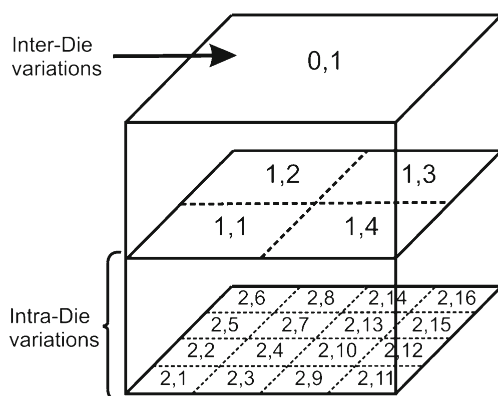

Fig. 7 Rectangular grid model [1]

parent grids. For example, the total variation of the channel length of the transistors located in the grid 2,4 and 2,16 are:

$$L(2,4) = L_0 + \Delta L_{2,1} + \Delta L_{1,1} + \Delta L_{0,1}$$
$$L(2,16) = L_0 + \Delta L_{2,16} + \Delta L_{1,3} + \Delta L_{0,1}$$

At circuit level, gates that lie within close proximity of each other will have many common intra-die device parameter components, resulting in a strong correlation. Gates, which lie far apart on a grid, share few common components and, therefore, exhibit a weak correlation.

5.2.1 Considering PV and NBTI-Induced Variations

A first-order linear model to describe the statistical gate delay is used [1]. In this model, each gate delay is approximated by the sum of its nominal value (D_0) and the deviation in all process parameters weighted by pre-characterized coefficients as in Eq. 5.1.

$$D = D_0 + \sum s_i \cdot X_i \tag{5.1}$$

D_0 is obtained with the pre-determined look-up tables (considering typical values on fabrication), X_i represents the variation of each one of considered random process parameters (L, W, t_{ox} and V_{th}), and s_i is the sensitivity coefficient of the gate delay propagation with respect to the process parameter X_i. Every s_i is extracted through HSPICE simulation.

The statistical analysis is made considering *m* number of runs. In each of these runs, different variations for each grid of the rectangular grid model (Fig. 7) are assigned. Thus, *m* values of *D* are obtained for each gate in the circuit. Analyzing statistically these *m* delay values of D (Eq. 5.1), the mean and standard deviation for all the gate delays in the circuit are obtained. This analysis is performed for each young gate i (no aging) in the path under analysis. The mean and standard deviation of each gate in the path for a given time (μ_{Tdi}(t), σ_{Tdi}(t)) of aging is computed using the following equations [11]:

$$\mu_{Tdi}(t) = \mu_{Tdi}(0) \cdot (1 + AS_{ti}t^n) \tag{5.2a}$$

$$\sigma_{Tdi}(t) = \sigma_{Tdi}(0) \cdot (1 + AS_V t^n) \tag{5.2b}$$

where $\mu_{Tdi}(0)$ and $\sigma_{Tdi}(0)$ are the mean and standard deviation without aging respectively. $\boldsymbol{A}$ is a factor that depends on technology parameters and operating conditions, $\boldsymbol{S_{ti}}$ is the nominal sensitivity of gate delay to PMOS V_{th} shift, $\boldsymbol{S_V}$ is the nominal sensitivity of NBTI-induced degradation of V_{th} due to PV and *n* is the time exponential constant. For a better understanding of $\boldsymbol{A}$, $\boldsymbol{S_V}$ and $\boldsymbol{S_{ti}}$ coefficients, please refer to [11].

The degradation of the mean and standard deviation for each gate in a path are determined taking into account the

correct values of $\boldsymbol{A}$ and $\boldsymbol{S_V}$ which depend on signal probabilities considering α_{IN}=0.1/0.9 for paths presenting a 0–1/1-0 transition at their main input. The statistical behavior is determined for the worst case aging condition. Knowing the mean and standard deviation for a given aging time for all the gates in the path, the PDF of the path is obtained making a linear combination of the PDFs of the gate delays. In this way, the mean and variance of the delay distribution of a path ($\mu_{p\text{-}Aged}$, $\sigma_{p\text{-}Aged}$) delay are given by [11]:

$$\mu_{p-Aged} = \sum_i^k \mu_{Tdi}(t) \tag{5.3a}$$

$$\sigma^2_{p-Aged} = \sum_i^k \sum_j^k \sigma_{Tdi}(t) \cdot \sigma_{Tdj}(t) \cdot \rho_{ij} \tag{5.3b}$$

where k is the total number of gates along the path under analysis, $\mu_{Tdi}(t)$ is the aged mean of the ith gate which is obtained with Eq. 5.2a, $\sigma_{Tdi}(t)$ and $\sigma_{Tdj}(t)$ are the aged standard deviation of the ith and j^{th} gates respectively which are determined with Eq. 5.2b and ρ_{ij} is the correlation coefficient between gates i and j.

6 Simulation Results

The methodology has been applied to several ISCAS benchmark circuits implemented using 65 nm cell library which is composed by 14 logic gates: one inverter, one buffer, two to four-inputs ANDs, two to four-inputs NANDs, two to four-inputs ORs and two to four-inputs NORs.

To illustrate how our tool works and to show how to interpret the results, let us consider a low complexity circuit.

Figure 8 shows the C17 ISCAS'85 benchmark circuit which is constituted by 6 NAND gates.

The tool identifies all the topological (signal) paths ending at N22 and N23 outputs. Six paths ending at N22 and 5 paths ending at N23 are identified. Among all 11 paths, path N3-x7-x6-x9-N22 is identified as the longest CP (e.g. P_1 in Fig. 5). The delay of the path at the FF design corner represents the threshold value that is used to obtain the pre-filtered paths.

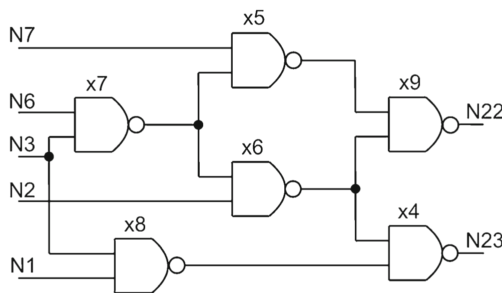

Fig. 8 C17 circuit

Considering $p\%$=20 %, the tool pre-filters 10 paths (including P_1): 5 ending at N22 output, and 5 ending at N23. Then, the statistical responses (mean and standard deviation), of the pre-filtered paths are determined for a) young circuit (μ_{p0}, σ_{p0}) and b) aged circuit ($\mu_{p\text{-}Aged}$, $\sigma_{p\text{-}Aged}$).

Figure 9a shows the pre-filtered paths ending at N22 output (without aging). An aging sensor must be connected at N22 output since it includes the longest CP (e.g. P_1). Figure 9b shows the pre-filtered paths ending at N23 output (without aging) and the path P_1 is also included. Three pre-filtered paths (pf_3, pf_4 and pf_8) have delay distributions overlapping the distribution of the longest CP (P_1). Therefore, an aging sensor must also be inserted at the N23 output.

As shown in Fig. 9b, the delay distributions of pf_9 (N2-x8-x4-N23) and pf_{10} (N1-x8-x4-N23) without aging, do not overlap with the delay distribution of the longest CP (P_1). However, statistical analysis considering aging on these both pre-filtered paths reveals that their aged-delay distributions shift over time and a portion of them overlap with the delay distribution of P_1. This means that there is a possibility that within 10 years the delays of paths pf_9 and pf_{10} could become larger than the maximum delay path of the circuit.

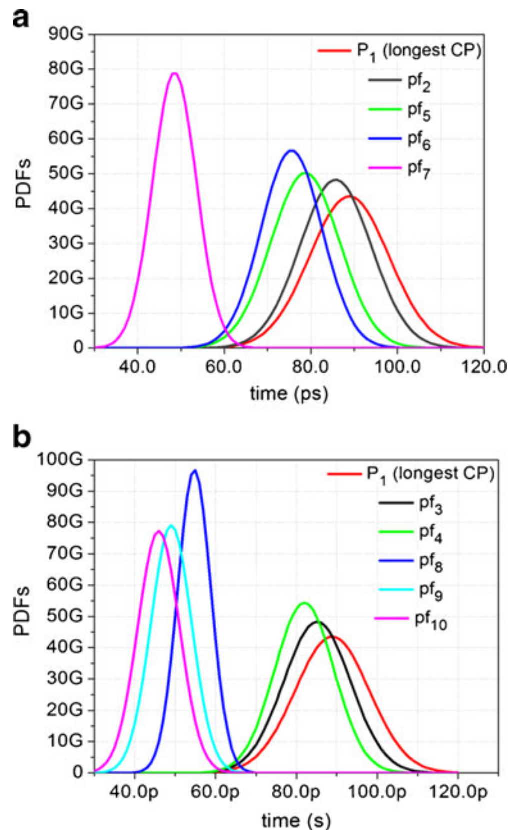

Fig. 9 PDFs of the Pre-filtered paths without aging for the C17 circuit. **a** Pre-filtered (pf) paths ending at N22 output. **b** Pre-filtered (pf) paths ending at N23 output together with the P_1

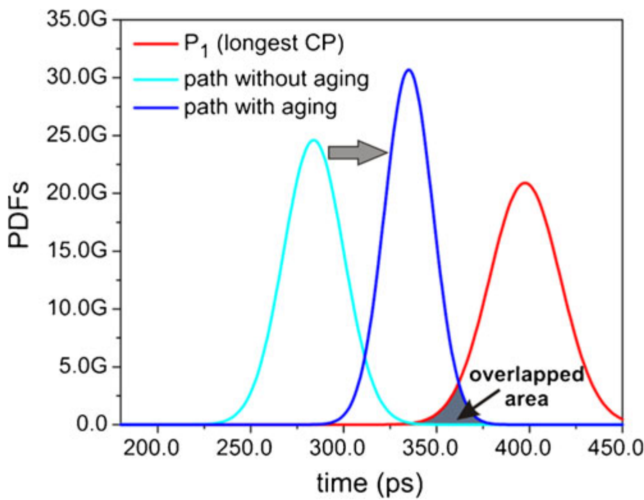

Fig. 10 Example of overlap between the aged delay distribution of a given pre-filtered path and the delay distribution of the longest CP for the ISCAS s510 circuit. This leads to insert an aging sensor at the path's output

Therefore, these paths need to be monitored with an aging sensor. Since the statistical timing analysis without aging already leads to aging sensor insertion at output N23, the reordering exhibited by pf_9 and pf_{10} is irrelevant from the point of view of aging sensor insertion because these two paths also end at N23 output. However, for other safety-critical circuits, some pre-filtered paths with reordering may end at outputs at which none non-aged delay distribution overlap with the P_1 delay distribution. Therefore, a non-aged statistical analysis could render ineffective aging sensor insertion.

Figure 10 shows an illustrative example of path reordering due to aging for a path of ISCAS s510. For this path, its statistical delay distribution without aging does not overlap with the longest CP. However, after 10 years aging, its delay distribution overlaps with that of the longest CP. Unlike the pf_9 and pf_{10} paths in ISCAS C17 circuit, this path ends at a different output than the path outputs with non-aged delay distribution overlapping the delay distribution of P_1. Because of this, an aging sensor must be inserted.

Table 1 shows the results of applying the proposed methodology to some sequential and combinational ISCAS benchmark circuits. Columns 2 and 3 show the number of paths and node end-points (i.e., nodes where a set of paths ends) respectively for the considered circuits. Columns 4 and 5 indicate the results of step1 of the methodology (static timing analysis, see section 4.1) (# of *pf*, or pre-filtered, means the number of CP + PCPs in Fig. 5). Columns 6 and 7 indicate the results of performing statistical timing analysis of the pre-filtered paths under no-aging. This step is not required in the proposed methodology; it has been performed only for comparison purposes. Columns 8 and 9 display the results of applying steps 2 and 3 of the methodology (see sections 4.2 and 4.3). Finally, column 10 presents the total computational costs (CPU time) of using our tools to implement the methodology (steps 1, 2 and 3). The experiments were performed on a Toshiba computer using an Intel Core 2 Duo CPU at 2.1 GHz. The tools can be further optimized to reduce the computing time.

For s510 benchmark circuit, the static timing analysis (performed to make paths pre-filtering) selected 236 paths ending at 9 different output nodes. Making a statistical timing analysis without aging for all these paths, there exists 161 paths satisfying the condition: $\mu_{p0} + 3\sigma_{p0} > \mu_{P1}\text{-}3\sigma_{P1}$, and all of them end at 5 different output nodes.

Then, applying the statistical selection criterion and considering $t = t_{Aged} = 10$ years, there exists 13 additional different paths that must be monitored. All these paths (161+13) satisfy the condition: $\mu_{p\text{-}Aged} + 3\sigma_{p\text{-}Aged} > \mu_{P1}\text{-}3\sigma_{P1}$. This could be irrelevant if all the additional 13 paths

Table 1 Results for some ISCAS'85 and 89 circuits. *pf* means *pre-filtered*

Circuit	Number of paths	Number of node end-points	Static timing analysis		Statistical analysis without aging		Statistical analysis with aging, *p%*=20 % and t_{Aged}=10 years		
			# of *pf* paths	Nodes to monitor	# of *pf* paths	Nodes to monitor	# of selected paths	Nodes to monitor	Computational time (seconds)
s510	378	13	236	9	161	5	161+13	5+1	8.2
s820	656	24	450	8	141	5	141+9	5+0	11.6
s832	635	24	448	9	210	7	210+23	7+1	12.1
s1196	5968	32	3931	17	616	13	616+742	13+2	367.1
C432	79822	7	65106	6	22364	4	22364+8892	4+0	1862.3
C880	9230	26	7104	9	1608	9	1608+126	9+0	420.4
C1355	7648	32	7616	32	5648	32	5648+343	32+0	160.6
C2670	3490	50	1461	8	567	5	567+80	5+1	175.8
C3540	212678	22	198388	17	107751	14	107751+3494	14+1	44167.8

would end at the same output nodes already under monitoring (161 paths). However, 2 of these 13 additional paths end at one different output node, thus requiring one more sensor to be inserted.

Based on the results, the accuracy gains obtained with the proposed methodology are clear. If we define aging sensor insertion based only on static timing analysis information, many sensors need to be inserted (9, for s510) leading to unacceptable area overhead. If we define aging sensor insertion based on the statistical information without considering aging effects (only PV), the number of aging sensors reduces (from 9 to 5, for s510); however, the designer is under the risk of missing monitoring of those PCPs that could pose a reordering due to NBTI effect. When aging analysis is made with statistical timing analysis information (i.e., when the *combined* effect of PV and NBTI is taken into account), the number of inserted aging sensors may increase (as compared with statistical analysis without aging) (5 to 6, for s510). However, it is significantly lower than using static analysis. As PV and aging are considered, there is no risk of timing violations due to path delay reordering.

Results in Table 1 show that the proposed methodology increases the accuracy of sensor insertion in 5 of the 9 considered benchmark circuits. In these 5 circuits, the reordering effect is an important fact for the determination of additional aging sensors compared with sensors determined by a statistical analysis without aging. This shows that the proposed methodology makes performance monitoring more reliable, which is mandatory in safety-critical applications.

7 Conclusion

In this paper, a methodology to determine the correct location for aging sensor insertion, considering the combined impact of process variations and aging effects (namely, due to NBTI) has been proposed. The proposed methodology can be useful in all applications for which long operation times (e.g., 10 years), high performance and reliable operation are key product specifications. In order to implement the methodology, a path-based statistical timing analysis framework and tools have been developed.

For a target IC technology, and using the pre-characterized cell library, the designer can perform step 1 of the proposed methodology, using our *Static Timing Analysis* tool, to define CPs, PCPs and non-PCP subsets. The *Statistical Timing Analysis* tool can then be applied to the CP and PCP set, to perform steps 2 and 3 of the proposed methodology. As a result, additional output nodes can be flagged for sensor insertion.

Simulation results show that sensor insertion based only on Static Timing Analysis typically overestimates the number of aging sensors that need to be inserted, thus leading to unacceptable area overhead. On the other hand, statistical timing analysis, without considering aging effects, often underestimates the number of aging sensors to be inserted (with the risk of not monitoring signal paths that could become critical under aging). In the proposed methodology, statistical timing analysis of the pre-filtered paths under no-aging is not required. However, results have been presented, to show that no-aging statistical timing analysis fails, in a significant number of case studies, to identify the correct location of aging sensors to be inserted in the digital system.

Therefore, it was shown that the proposed methodology leads to a more accurate solution than the ones previously available, to determine the correct location of the aging sensors by considering a Statistical Timing Analysis taking PV and aging effects into account, according to the expected product lifetime.

Acknowledgments To the CONACYT (México) for the support given through the PhD scholarship nº. 207069/204311. This work has also been partially supported by the European ENIAC SE2A Project, and by Portuguese national funds through FCT – Fundação para a Ciência e a Tecnologia, under project PEst-OE/EEI/LA0021/2011.

References

1. Agarwal A, Blaauw D, Zolotov V et al (2003) Statistical delay computation considering spatial correlations. Proc IEEE ASP-DAC, pp. 271–276, January
2. Baba AH, Mitra S (2009) Testing for transistor aging. Proc IEEE VLSI Test Symposium (VTS), pp. 215–220
3. Borkar S et al (2003) Parameter variation and impact on circuits and microarchitecture. Proc ACM/IEEE Design Automation Conference (DAC), pp. 338–342
4. Chan T-B, Sartori J, Gupta P, Kumar R (2011) On the efficacy of NBTI mitigation techniques. Design, Automation & Test in Europe Conference (DATE), pp.1–6
5. Martins CV, Semião J, Vazquez JC, Champac V, Santos M, Teixeira IC, Teixeira JP (2011) Adaptive error-prediction flip-flop for performance failure prediction with aging sensors. Proc IEEE VLSI Test Symposium (VTS), pp. 203–208
6. Sakurai T, Newton AR (1990) Alpha-power law mosfet model and its application to CMOS inverter delay and other formulas. IEEE J Solid State Circuits 25(2):584–594
7. Siddiqua T, Gurumurthi S, Stan MR (2011) Modeling and analyzing NBTI in the presence of process variations. Proc IEEE Int Symp On Quality Electronic Design (ISQED), pp. 28–35
8. Vazquez JC, Champac V, Ziesemer AM Jr, Reis R, Teixeira IC, Santos MB, Teixeira JP (2012) Delay sensing for long-term variations and defects monitoring in safety-critical applications. Analog Integr Circ Sig Process J 70(2):249–263, Springer
9. Vazquez JC et al (2010) Low sensitivity to process variations aging sensor for automotive safety-critical applications. Proc IEEE VLSI Test Symposium (VTS), pp. 238–243
10. Wang W, Cao Y, et al (2007) The impact of NBTI on the performance of combinational and sequential circuits. Proc ACM/IEEE Design Automation Conference (DAC), pp. 364–369, Jun

11. Wang W, Reddy V, Yang B, Balakrishnan V, Krishnan S, Cao Y (2008) Statistical prediction of circuit aging under process variations. Proc IEEE Custom Integrated Circuits Conference (CICC), pp. 13–16
12. Wang W, Wei Z, Yang S, Cao Y (2007) An efficient method to identify critical gates under circuit aging. Proc ICCAD, pp. 735–740
13. Wang W, Yang Sh, Bhardwaj S, Vrudhula S, Liu F, Cao Y (2010) The impact of NBTI effect on combinational circuit: modeling, simulation, and analysis. IEEE Trans VLSI Syst 18, Nº. 2, Feb
14. Wayne Johnson R et al (2004) The changing automotive environment: high-temperature electronics. IEEE Trans EPM 27(3):164–176

Julio Vazquez received the M.Sc. degree in VLSI circuit design from National Institute for Astrophysics Optics and Electronics (INAOE) of Mexico. He is currently pursuing for his Ph.D. degree VLSI circuit design from INAOE. His research interests include the design, production and lifetime test of VLSI electronic systems.

Victor Champac received the Ph.D. degree in 1993 from the Polytechnic University of Catalonia (UPC), Spain. Since 1993 he is with the National Institute for Astrophysics, Optics and Electronics (INAOE-Mexico) where he is Titular Professor. Dr. Champac was co-founder of the Test Technology Technical Council-Latin America of IEEE Computer Society. Dr. Champac was co-General Chair of the 2nd. and 9th. IEEE Latin American Test Workshop held in Mexico in 2001 and 2008, respectively. He is member of the Board Director of Journal of Electronics Testing: Theory an Applications (JETTA). His research lines are: defect modeling in nanometer technologies, development of new test strategies for advanced technologies, verification of signal integrity, process variation and noise tolerant VLSI Circuit Design.

Jorge Semião received a M.Sc. and a Ph.D. degree in electrical engineering from Instituto Superior Técnico (IST), Technical University of Lisbon, Portugal. He is an Assistant Professor in the Electrical Engineering Department of the Engineering Institute, in the University of Algarve, and a researcher in INESC-ID, Lisbon. His research interests include design for testability, fault tolerance and fault detection.

Isabel C. Teixeira received a Ph.D. in electrical engineering from Instituto Superior Técnico (IST), Technical University of Lisbon, Portugal. She is an Associate Professor of the Electrical and Computer Engineering Department of IST and a senior researcher in INESC-ID, Lisbon. Her research interests include design and test of Hardware/Software Systems, mainly on the development of models, methodologies and metrics.

Marcelino B Santos received the M.Sc. and Ph.D. degrees in electrical engineering from IST, Technical University of Lisbon, Portugal. He is an Associate Professor of the Electrical and Computer Engineering Department of IST and a senior researcher in INESC-ID, Lisbon. His research interests include testability of digital circuits, optimization of dc–dc converters, and educational issues on microelectronics. He is also cofounder of Silicongate.

João Paulo Teixeira received a Ph.D. in electrical engineering from Instituto Superior Técnico (IST), Technical University of Lisbon, Portugal. He is a retired Full Professor of the Electrical and Computer Engineering Department of IST and a senior researcher in INESC-ID, Lisbon. His research interests include the analysis, specification, design, verification, production and lifetime test and diagnosis of highly dependable hardware/software electronic systems.