FinFET SRAM hardening through design and technology parameters considering process variations

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***Abstract*—Radiation-induced soft errors have become one of the most important reliability concerns in the nanometer regime. In this paper, we analyze two alternatives to improve FinFET-based SRAM cell hardening. One is related to increasing the number of fins of the transistors composing the cross-coupled inverters. This option provides a significant increase of the cell critical charge (Q_{crit}), but with a cost in area. The other alternative increases the transistors fin height. Results show that a similar Q_{crit} gain is achieved by increasing the fin height instead of the number of fins without area overhead. The impact of process variations has been considered. Q_{crit} distribution has been modeled through an statistical approach based on *Design of Experiments*. Results are presented for a 10nm-SOI Trigate FinFET technology.**

I. Introduction

Traditional CMOS scaling beyond the 22nm technology node is severely constrained by *short channel effects*, and process variations due to *Random Dopant Fluctuations* (RDF). Hence, FinFET technology projects as the most promising candidate to continue CMOS scaling. FinFET devices have a stronger electrostatic control over the channel due to the gate wraps around a thin slice of silicon, that is known as *fin*. This results in improved short channel behavior. In addition, high channel doping is not required in FinFETs dismishing the threshold voltage variations due to RDF. However, the impact of process variations in fin thickness, fin height, channel length, and oxide thickness on FinFET performance must be analyzed in detail.

Alpha particles from the packaging materials, high energy neutrons from cosmic radiations and the interaction of cosmic ray thermal neutron are three major sources of radiation inducing soft errors [1]. In SRAM cells a soft error is typically due to *Single Event Upset* (SEU), and occurs when a particle strike at a storage node in the cell induces a transient voltage pulse that causes a bit flip in the SRAM cell.

There is a considerable amount of works modeling single-event effects (SEEs) in FinFETs. In [2] the charge collection in FinFETs was investigated through laser experiments. In [3] three-dimensional (3D) TCAD simulations were employed to model the response to radiation of FinFETs. However, the improvement of radiation-hardening of SRAM cells considering process variations has not been thoroughly studied. In [4] various FinFET-based SRAM cells for SEU immunity were analyzed and their performance was compared for superthreshold and subthreshold supply voltage operation. However, no detailed analysis about the impact of process variations was reported. In [5] five FinFET-based SRAM configurations to reduced the SEU sensitivity were proposed, reporting good results in SEU robustness, although the cost in area overhead was high.

In this work, we analyze the effect of increasing the number of fins, and the fin height of the cross-coupled inverters transistors of FinFET-based SRAM cells to improve the cell radiation-hardening in presence of process variations. The critical charge (Q_{crit}) is the parameter used to quantify the radiation-hardening of a cell. In this work, Q_{crit} is modeled by an statistical approach based on *Design of experiments* (DOE) to determine the impact of process and design parameters on Q_{crit} distribution. The efficiency of this statistical method was also evaluated by [6]. The rest of the paper is organized as follows: Section II presents the basic FinFET-based SRAM cell and the statistical model of Q_{crit} distribution used in this work. The impact of increasing the number of *fins*, and the *fin* height are analyzed in Section III while Section IV discusses the impact of increasing *NFIN* and *HFIN* on SRAM cell performance. Finally, in Section V the conclusions are given.

II. FinFET-based SRAM Cell Modeling

A. FinFET Device

The basic structure of a Trigate FinFET device is shown in Fig. 1a. It is formed with a silicon fin that is wrapped around by the gate. *L* is the channel length, *HFIN* is the fin height, *TFIN* is the fin thickness and *TOX* is the oxide thickness. The effective width (W_{eff}) of a Trigate FinFET is defined as

$$W_{eff} = NFIN \times (2HFIN + TFIN) \quad (1)$$

where *NFIN* is the number of fins and takes integer values. *HFIN* and *TFIN* are usually fixed for a given technology, and their value is limited by the $HFIN/TFIN$ ratio of the manufacturing process [7].

B. 6T-FinFET SRAM Cell

Fig.1b shows the circuit schematics of the basic FinFET-based SRAM cell. *Mp1* and *Mp2* are the pull-up transistors,

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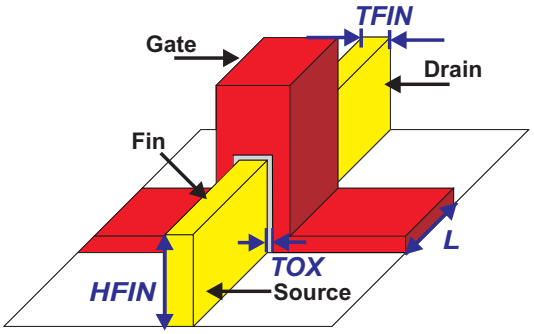
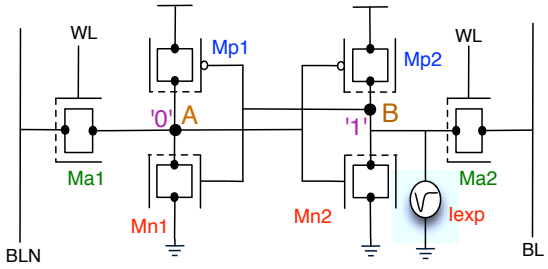
Mn1 and *Mn2* are the pull-down transistor, and *Ma1* and *Ma2* are the access transistors. *A* and *B* are the storage nodes. Assume the radiation particle impacts node *B* where a logic '1' is stored. *Iexp* is a double-exponential current source that models the radiation-induced transient current waveform of the ion track of a radiation particle. Our analysis is based on 10nm-SOI Trigate FinFET model card. Detailed transistors parameters are given in Table I.



(a) Trigate FinFET Device.



(b) FinFET-based SRAM Cell.

Fig. 1. FinFET Technology

C. Process Variations

Process variations are often separated in local and global contributions. For local variations, transistors within the SRAM cell vary independently of each other. For global variations, all transistors within SRAM cell vary equally. The most important sources of local variations in FinFETs (See Fig. 1a) are *L* and *TFIN* due to *Line Edge Roughness* (LER)[8]. Local variations of *HFIN* and *TOX* are negligible [8]. To analyze the impact of process parameter variations on Q_{crit} distribution, the effect of local and global variations of parameters (*L, TFIN, HFIN, TOX*) have been considered concurrently (See Eq. 2). The global variation component is generated for each simulation for all transistors while the local variation component generated for each transistor of the cell for each simulation. Electrical simulation have been done in HSPICE BSIM-CMG model for 10nm-SOI Trigate FinFET. Parameter variations have been taken from [9].

$$P_{ij} = P_{nominal} + \Delta P_{global,j} + \Delta P_{local,ij} \quad (2)$$

P_{ij} is the parameter value for the i^{th} transistor during the j^{th} simulation. $P_{nominal}$ is the nominal parameter value. $\Delta P_{global,j}$ is the global variation component and is generated for each simulation for all transistors. $\Delta P_{local,ij}$ is the local variation component generated for each transistor of the SRAM cell for each simulation.

TABLE I
FINFET'S PARAMETERS USED IN THIS WORK

L(nm)	TFIN(nm)	HFIN(nm)	TOX(nm)	V_{DD}(V)
10	5	12.5	0.585	0.8

D. Critical Charge (Q_{crit}) Distribution Modeling

The Q_{crit} of a SRAM cell depends on variations of process parameters (*TFIN, L, TOX*, and *HFIN*). Since process parameters are considered random variables, the Q_{crit} variation of a SRAM cell can also be considered a random variable and its variations can be approximated to follow a normal distribution. The mean of Q_{crit} (μ_{Qcrit}) and the variance of Q_{crit} (σ^2_{Qcrit}) can be estimated by an multi-variable Taylor-series expansion [10]. Assuming process parameters to be independent, then,

$$\mu_{Qcrit} = Q_{crit0} + \frac{1}{2}\sum_{i=1}^{n}\left(\frac{\partial^2 Q_{crit}(x_1, x_2, .., x_n)}{\partial x_i^2}\right)\sigma_{xi}^2 \quad (3)$$

$$\sigma^2_{Qcrit} = \sum_{i=1}^{n}\left(\frac{\partial Q_{crit}(x_1, x_2, ..., x_n)}{\partial x_i}\right)^2 \sigma_{xi}^2 \quad (4)$$

Where Q_{crit0} is the critical charge of the SRAM cell for nominal values of process parameters, x_i represents the corresponding process parameter, ∂Q_{crit} / ∂x_i is the sensitivity of Q_{crit} with respect to each process parameter, and σ_{xi} is the parameter standard deviation.

To determine the sensitivity of Q_{crit} with respect to each process parameter and evaluate Eq. 3 and 4, we model Q_{crit} by an statistical approach based on *Design of Experiments* (DOE) [11]. DOE is a powerful statistical method that allows estimating the effect of each process and design parameters and their interactions on the Q_{crit} which allows modeling accurately the behavior of Q_{crit} with respect to the variations of process and design parameters. The main advantage of using DOE instead of classical analytical Q_{crit} models is that the designer can analyze a more detailed behavior of the Q_{crit} with respect to process and design parameters.

To model Q_{crit}, an initial screening DOE has been done to identify negligible parameters and interaction among parameters to reduce the number of variables of the final model. For screening, a simple full factorial DOE at 2 levels has been used. Then, through *Analysis of Variance* (ANOVA) [11] the significance level of each variable is estimated. From screening, the variations of process and design parameters of access transistors are negligible and are not considered for final model. This is logical, since the Q_{crit} is estimated for hold operation of the SRAM cell. Hence, with all variables corresponding to the cross-coupled inverters of the SRAM cell (See Fig. 1a), a full factorial DOE at 5 levels has been done,

obtaining a third degree polynomial function. This function is of the shape,

$$Q_{crit} = \beta_0 + \beta_1.TFIN_{Mn1} + \beta_2.TFIN_{Mp1} + ... + \beta_i.TOX.HFIN + ... + \beta_n.HFIN^3 \quad (5)$$

where $\beta_0, \beta_1, ...\beta_n$ are the polynomial coefficients.

Eq. 5 is used to determine the sensitivity of Q_{crit} with respect to each process parameter to calculate μ_{Qcrit} and σ^2_{Qcrit} with Eq. 3 and 4 respectively. The model coefficient of determination for the regression, R^2, of Eq. 5 is 99.92%, that indicates the polynomial model has a good agreement with simulation data. From ANOVA, a *Pareto chart of effects* of the process and design parameters was elaborated and shown in Fig. 2. The signs (+) and (-) represent positive and negative effects respectively. Each variable is labeled by a letter in brackets (i. e. *(A)* corresponds to *NFIN*). The combination of letters indicates an interaction between variables (i.e. *B*C* indicates the interaction between *HFIN* and *TFIN*). The *Pareto chart* shows that the main effects correspond to *NFIN* and *HFIN*. The effect of *TFIN* and *L* are smaller than the effect of *NFIN* and *HFIN*. Linear, second order and third order interactions among parameters are negligible in comparison with the effect of *NFIN* and *HFIN*.

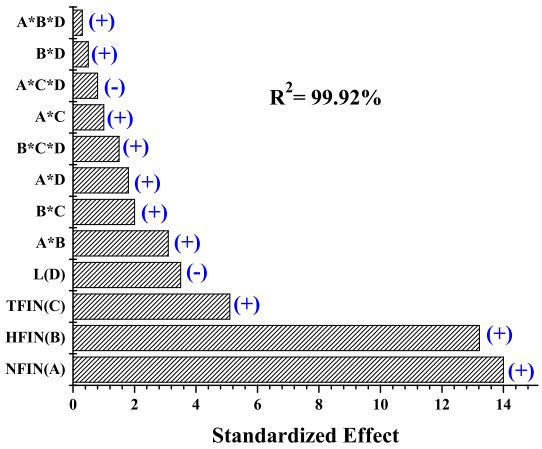


Fig. 2. Pareto of effects of process and design parameters on Q_{crit}. Labels: *NFIN* is A, *HFIN* is B, *TFIN* is C, *L* is D. A*B is the interaction between *NFIN* and *HFIN*. A*C*D is the interaction among *NFIN*, *TFIN*, and *L*.

III. FinFET SRAM Cell Hardening through Design and Technology Parameters

According to *the Pareto chart of effects* (See Fig. 2) from ANOVA analysis, *NFIN* and *HFIN* are the main parameters with a stronger impact on Q_{crit} than *TFIN* and *L*. In this section, the impact of increasing *NFIN*, and increasing *HFIN* on Q_{crit} considering process variations will be analyzed.

A. SRAM hardening by increasing NFIN

The μ_{Qcrit} and the σ_{Qcrit} are computed according to Eqs. 3, 4 and 5, and are a function of *NFIN*. Assume a logic '1' is stored at node *B*. Taking the 6T SRAM with parameters in Table I and *NFIN*=1 as the reference memory cell ($SRAM_{ref}$), we compute $\Delta\mu_{Qcrit}$ ($\Delta\sigma_{Qcrit}$) as the difference between the μ_{Qcrit} (σ_{Qcrit}) as increasing *NFIN* and such reference cell values, μ^{ref}_{Qcrit} (σ^{ref}_{Qcrit}), normalized to μ^{ref}_{Qcrit} (σ^{ref}_{Qcrit}). Table II indicates the impact of increasing *NFIN* of the transistors of the cross-coupled inverters on μ_{Qcrit} and σ_{Qcrit}. It is observed that as NFIN increases, $\Delta\mu_{Qcrit}$ also increases. The behavior of $\Delta\mu_{Qcrit}$ is logical due to the increase of W_{eff}. However, as *NFIN* increases, $\Delta\sigma_{Qcrit}$ also tends to increase. According to the results in Table II, if *NFIN* is equal to 2, the μ_{Qcrit} increases significantly, about 88% with respect to the basic SRAM cell. In addition, the ratio $3\sigma_{Qcrit}/\mu_{Qcrit}$ decreases as *NFIN* increases, improving the variability of the cell. Hence, increasing *NFIN* may be an attractive alternative for design hardening. However, the cost in *Area* is the main constraint of increasing *NFIN* in SRAM cells. This will be discussed in Section IV.

TABLE II
Impact of NFIN on μ_{Qcrit} and σ_{Qcrit}

	NFIN=1	*NFIN*=2	*NFIN*=3	*NFIN*=4
$\Delta\mu_{Qcrit}$ (%)	-	88%	170.26%	251.74%
$3\sigma_{Qcrit}/\mu_{Qcrit}$	0.361	0.2392	0.2029	0.1871

B. SRAM hardening by increasing HFIN

The Pareto chart (See Fig. 2) indicates that *HFIN* is another parameter with a significant impact on Q_{crit}. Assuming a logic '1' stored at node *B*, Fig. 3 shows the behavior of $\Delta\mu_{Qcrit}$ and $\Delta\sigma_{Qcrit}$ as a function of *HFIN*. It is observed that as *HFIN* increases, $\Delta\mu_{Qcrit}$ and $\Delta\sigma_{Qcrit}$ also increase. For *HFIN*=21nm, μ_{Qcrit} increases significantly (69.8%) and σ_{Qcrit} increases by 30%. For *HFIN*=23nm, μ_{Qcrit} increases by 87.55%, and σ_{Qcrit} increases by 37.5%. Fig. 4 shows the impact of increasing *HFIN* on variability. The ratio $3\sigma_{Qcrit}/\mu_{Qcrit}$ decreases as *HFIN*. The results observed for *HFIN*=23nm suggest that it is possible obtain a similar μ_{Qcrit} gain increasing *HFIN* instead of *NFIN*. The cost in *Area* will be discussed in next section.

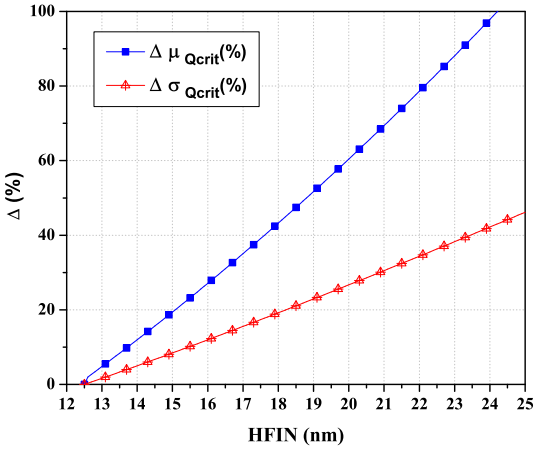


Fig. 3. Impact of HFIN on μ_{Qcrit} and σ_{Qcrit}. *TFIN*=5nm.

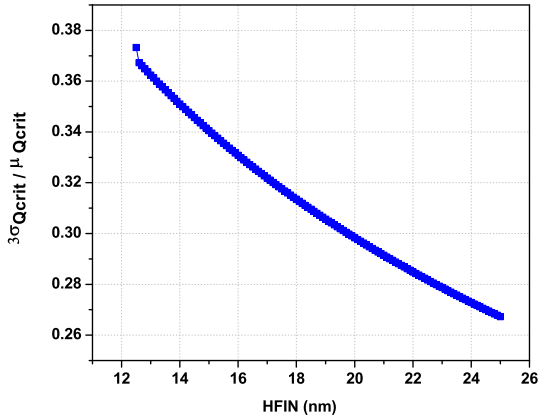


Fig. 4. Impact of HFIN on Q_{crit} variability. *TFIN*=5nm.

As mentioned earlier, *HFIN* is a fixed parameter for a given technology and depends on the $HFIN/TFIN$ ratio of the manufacturing process. For the technology used in this work, the $HFIN/TFIN$=2.5. Thus, increasing *HFIN* implies manufacturing FinFETs with $HFIN/TFIN$ >2.5. To generalize this analysis, Fig. 5 shows the $\Delta\mu_{Qcrit}$ and $HFIN/TFIN$ ratio as a function of *HFIN*. To obtain a similar μ_{Qcrit} gain when *NFIN*=2, $HFIN/TFIN$ must increase to 4.6. The typical value of $HFIN/TFIN$ is 2 [7], however, in recent works values of $HFIN/TFIN$ >2 are reported. For example [12] and [3] report fabricated FinFET devices with $HFIN/TFIN$=5. Moreover, [13] and [14] studied SRAM optimization with FinFET devices with $HFIN/TFIN$ being 4 and 3 respectively. Furthermore, [15] successfully fabricated Trigate FinFETs with $HFIN/TFIN$=6. Hence, fabrication of FinFET-based SRAM cells with $HFIN/TFIN$=4 or $HFIN/TFIN$=5 for radiation hardened applications might be feasible.

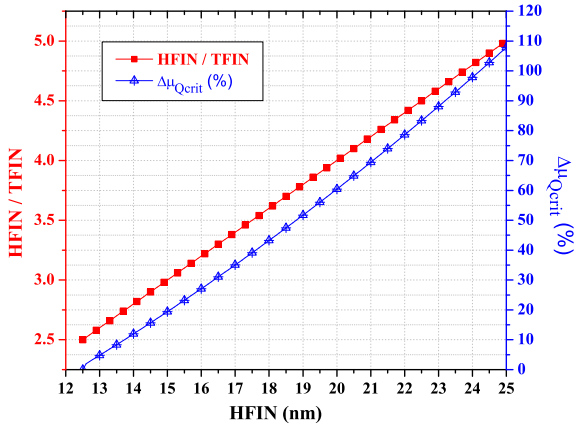


Fig. 5. Q_{crit} gain as a function of HFIN/TFIN ratio. *TFIN*=5nm.

IV. Impact on SRAM Cell Performance

The results obtained in the previous section show that increasing HFIN to 23nm improves Q_{crit} similarly to increasing the number of fins to *NFIN*=2. Thus, we analyze the impact of increasing *NFIN*, and increasing *HFIN* on SRAM cell performance.

A. Q_{crit} and area overhead

Let us define SRAM-I and SRAM-II as the SRAM cells with cross-coupled inverters designed according to the parameters presented in Table III. The access transistors have been designed with parameters in Table I considering *NFIN*=1. Table IV indicates the impact of different SRAM cells (SRAM-I and SRAM-II) on μ_{Qcrit}, $3\sigma_{Qcrit}/\mu_{Qcrit}$ and *Area* with respect to SRAM_{ref}. For SRAM-I and SRAM-III the impact on Q_{crit} distribution is similar. The improvement in μ_{Qcrit} is 88% and 87.55% respectively. In addition, the improve in variability is lightly higher for SRAM-I. However, the cost in *Area* for SRAM-I is 21% and for SRAM-II is 0%. Hence, it is possible to obtain similar improvement in Q_{crit} increasing *HFIN* instead of *NFIN*, but without *Area* overhead.

TABLE III
SRAM PARAMETERS FOR COMPARISON

Parameter	$SRAM_{ref}$	SRAM-I	SRAM-II
NFIN	1	2	1
HFIN (nm)	12.5	12.5	23
TFIN (nm)	5	5	5

TABLE IV
Q_{crit} AND *Area* COMPARISON WITH RESPECT TO SRAM_{ref}

Case	$\Delta\mu_{Qcrit}$	$3\sigma_{Qcrit}/\mu_{Qcrit}$	$\Delta Area$
SRAM_{ref}	-	0.3610	-
SRAM-I	88%	0.2392	21%
SRAM-II	87.55%	0.2787	0%

B. Read Failure

A read failure occurs while reading the cell shown in Fig. 1b (V_B='1' and V_A='0'), the voltage at node A increases to a positive value V_{READ} due to the voltage divider formed by *Ma1* and *Mn1*, and if V_{READ} is higher than the trip point of the inverter *Mp2* - *Mn2*, the cell flips the stored data. Table V and Fig. 6 show the impact of increasing *NFIN* and *HFIN* on the voltage at node A in the read operation (V_{READ}) of the SRAM cell respectively. It is observed that V_{READ} voltage decreases as *NFIN* and *HFIN* increases. This indicates that increasing *NFIN* or *HFIN* of the transistors of the inverters of the cell improves the read stability of the cell. However, V_{READ} is lower decreasing *NFIN* than increasing *HFIN*.

C. Write Failure

In the write operation, while writing a '0' to a cell storing '1', the node B discharges through BL to a low value determined by the voltage divider formed by *Mp2* and *Ma2*. If the the voltage at node B cannot be reduced below the trip point of the inverter *Mp1-Mn1* within the time when the word-line is high (T_{WL}), a write failure occurs. Table V and

TABLE V
IMPACT OF NFIN ON SRAM CELL PERFORMANCE

	NFIN=1	*NFIN=2*	*NFIN=3*
V_{READ} (V)	0.2536	0.1568	0.1325
T_{WRITE} (ps)	6.02	18.53	31.46
T_{access} (ps)	6.498	6.474	6.471
$I_{leakage}$ (nA)	16.63	27.82	38.84

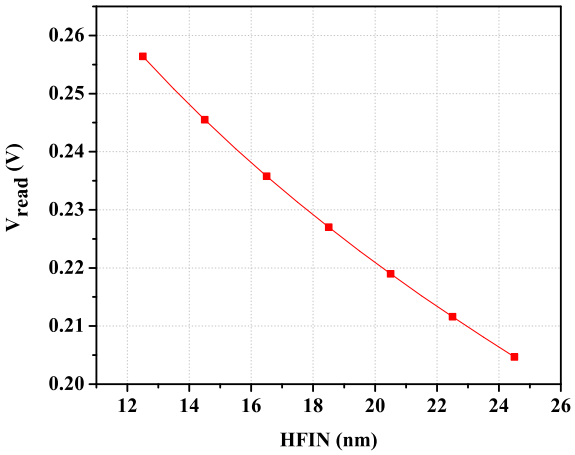


Fig. 6. Impact of increasing HFIN on V_{read}.

Fig. 7 show the impact of increasing *NFIN* and *HFIN* on T_{WRITE} respectively, where T_{WRITE} is the time required to pull-down the voltage at node B to the trip point voltage of the inverter *Mp1-Mn1*. It is observed T_{WRITE} increases as *NFIN* and *HFIN* increases. The increment of T_{WRITE} is larger increasing *NFIN* than increasing *HFIN*. This result indicates the stability of the cell in the write operation requires an adequate selection of the T_{WL} that considers the values of the *NFIN* and *HFIN* of the FinFET transistors of the cross-coupled inverters of the SRAM cell.

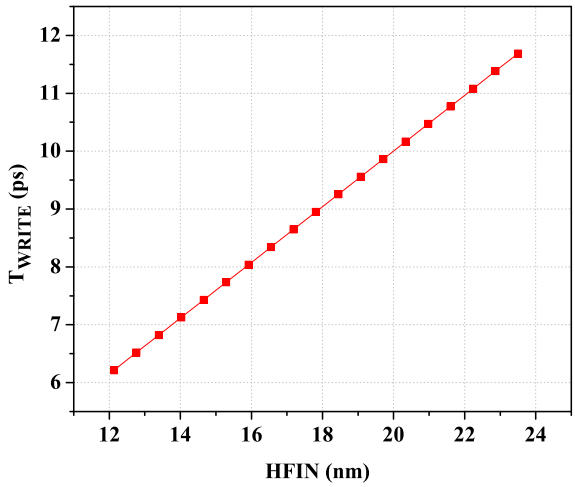


Fig. 7. Impact of increasing HFIN on T_{WRITE}.

D. Access Time Failure

The access time (T_{access}) is defined as the time required to produce a voltage difference ($\approx 0.1V_{DD}$) between the two bit-lines. Hence, access time failure occurs when the access time of the cell is longer than the maximum tolerable limit stablished. Table V and Fig. 8 show the impact of increasing *NFIN* and *HFIN* on T_{access} respectively. It is observed T_{access} decreases lightly as *NFIN* and *HFIN* increases.

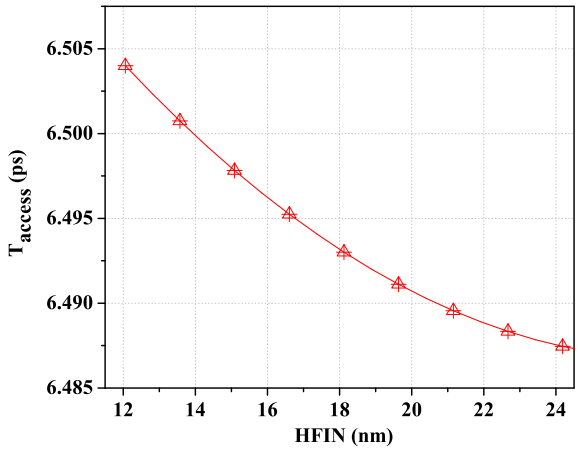


Fig. 8. Impact of increasing HFIN on T_{access}.

E. Leakage Current

The main components of leakage current in FinFET devices are: sub-threshold current and tunneling current from gate to channel and from gate to source/drain region (See Fig. 9). However, the sub-threshold current is the largest component to leakage current, thus it is the only component considered for analysis in this work.

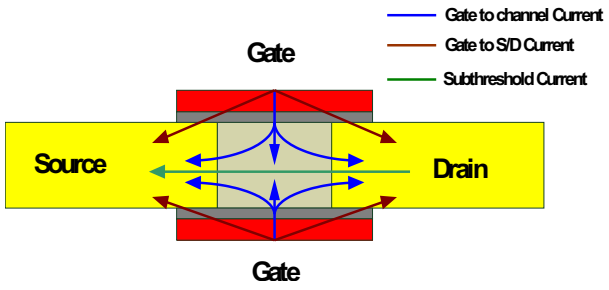


Fig. 9. Leakage Components in FinFET devices.

For SRAM cell (See Fig. 1)b, the transistors *Mp1*, *Mn2*, and *Ma2* are the major contributors to the total leakage current (See Fig. 10).

Table V and Fig. 11 show the impact of increasing *NFIN* and *HFIN* on leakage current respectively. It is observed that the leakage current increases considerably as *NFIN* and *HFIN* increase. This result indicates that the SRAM cell power consumption also increases significantly as *NFIN* and *HFIN* increases to improve Q_{crit}.

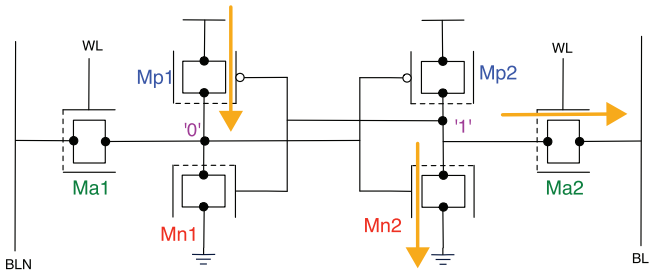


Fig. 10. Leakage Contributions in SRAM Cell.

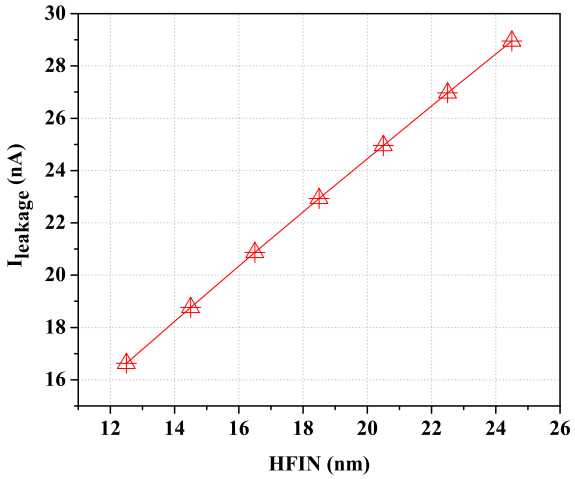


Fig. 11. Impact of increasing HFIN on leakage current.

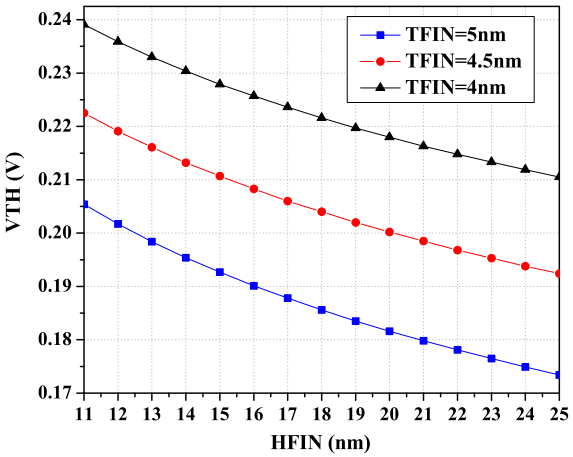


Fig. 12. Impact of HFIN and TFIN on VTH.

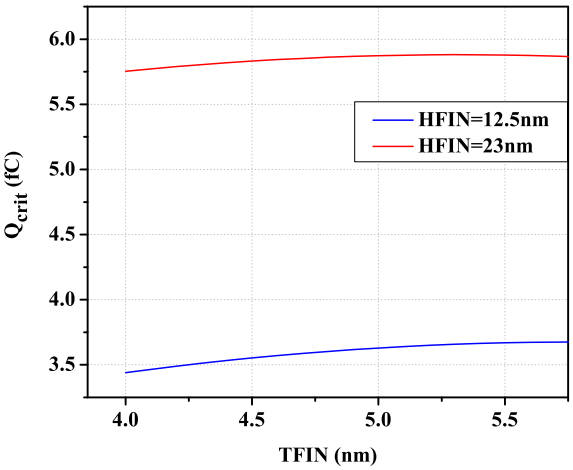


Fig. 13. Impact of TFIN variation on Q_{crit}.

The leakage current increase can be controlled by increasing the control of the gate over the channel modulating the thickness of the fin (TFIN). Fig. 12 shows the threshold voltage (V_{TH}) variation as function of *HFIN* for different *TFIN* values indicating that V_{TH} decreases (increasing leakage current) as *HFIN* increases but increases reducing *TFIN*. Hence, the technology parameter *TFIN* can be used to determine an optimal power consumption level.

However, the impact of reducing *TFIN* on Q_{crit} must be quantified. According to the *Pareto chart of effects* (See Fig. 2) the impact of *TFIN* on Q_{crit} is not significantly with respect to *HFIN* and *NFIN*. For validation, Fig. 13 shows the SRAM cell Q_{crit} as a function of the FinFET *TFIN* for *HFIN*=12.5nm and *HFIN*=23nm. It is observed the Q_{crit} increase as *TFIN* increases is not significantly.

V. Conclusions

The effect of increasing the number of fins (*NFIN*) and the fin height (*HFIN*) of the transistors composing the cross-coupled inverters of FinFET-based SRAM cells to improve radiation-hardening considering process variations has been analyzed. Results show that it is possible to obtain similar improvement in critical charge by increasing *HFIN* instead of *NFIN* without *Area* overhead. The impact of increasing *NFIN* and *HFIN* on Q_{crit} distribution is similar, μ_{Qcrit} increases and $3\sigma_{Qcrit}/\mu_{Qcrit}$ decreases as *NFIN* and *HFIN* increase. Additionally, the impact of increasing *NFIN* and *HFIN* on SRAM cell performance has been analyzed. The read operation stability increases as *NFIN* and *HFIN* increase. However, the T_{WRITE} and leakage current increase as *NFIN* and *HFIN* increase. Nevertheless, the increment in leakage current can be controlled modulating *TFIN* without Q_{crit} penalization.

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References

[1] R. C. Baumann, "Soft errors in advanced semiconductor devices-part I: the three radiation sources," *IEEE Trans. Device and Materials Reliability*, vol. 1, no. 1, pp. 17–22, 2001.

[2] F. El-Mamouni, E. Zhang *et al.*, "Laser-and heavy ion-induced charge collection in bulk FinFETs," *IEEE Trans. Nuclear Science*, vol. 58, no. 6, pp. 2563–2569, 2011.
[3] M. Turowski, A. Raman, and W. Xiong, "Physics-based modeling of nonplanar nanodevices (FinFETs) and their response to radiation," in *Proc. 18th Int. Conf. MIXDES*. IEEE, 2011, pp. 460–465.
[4] S. Rathod, A. Saxena, and S. Dasgupta, "Comparative Analysis of SEU in FinFET SRAM Cells for Superthreshold and Subthreshold Supply Voltage Operation," *IEEE Trans. Electron Devices*, vol. 58, no. 10, pp. 3630–3634, 2011.
[5] S. Rathod *et al.*, "DG-FinFET-based SRAM Configurations for increased SEU immunity," *J. Circuits, Syst., and Comp.*, vol. 21, no. 04, 2012.
[6] C. Maufront and R. Ferrant, "Advanced Statistical Methodology for 6T-SRAM Design," in *IEEE 14th ICECS*. IEEE, 2007, pp. 756–758.
[7] M. Alioto, "Comparative evaluation of layout density in 3T, 4T, and MT FinFET standard cells," *IEEE Trans. Very Large Scale Integration Systems*, vol. 19, no. 5, pp. 751–762, 2011.
[8] D. D. Lu, C.-H. Lin, A. M. Niknejad, and C. Hu, "Compact modeling of variation in finfet sram cells," *IEEE Design & Test of Computers*, vol. 27, no. 2, pp. 44–50, 2010.
[9] Z. Jaksic and R. Canal, "Comparison of SRAM Cells for 10-nm SOI FinFETs Under Process and Environmental Variations," *IEEE Trans. Electron Devices*, vol. 60, pp. 49–55, 2013.
[10] A. Papoulis and S. Pillai, *Probability, random variables and stochastic processes*. McGraw Hill Higher Education, 2002.
[11] D. C. Montgomery, *Design and analysis of experiments*. Wiley, 2008.
[12] Y. Liu, K. Endo *et al.*, "Fin-height controlled PVD-TiN gate finFET SRAM for enhancing noise margin," in *Proc. Euro. ESSDERC*. IEEE, 2010, pp. 202–205.
[13] M. Kang, S. Song *et al.*, "FinFET SRAM optimization with Fin thickness and surface orientation," *IEEE Trans. Electron Devices*, vol. 57, no. 11, pp. 2785–2793, 2010.
[14] A. B. Sachid and C. Hu, "Denser and More Stable SRAM Using FinFETs With Multiple Fin Heights," *IEEE Trans. Electron Devices*, vol. 59, no. 8, pp. 2037–2041, 2012.
[15] N. Collaert *et al.*, "Tall triple-gate devices with TiN/HfO2 gate stack," in *Symp. VLSI Technology*. IEEE, 2005, pp. 108–109.