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Modeling the Al/Si rich oxide (SRO)/Si structure

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Al/SRO/Si devices produced on *N*-type silicon are experimentally characterized to understand their behavior. Different values were used for the nitrous oxide/silane gas flow ratio (R_o) to control the excess silicon. Depending on the silicon excess, the devices could be operated in various modes; from surface accumulation to deep depletion or to a reverse biased *PN* junction. Modeling of the different devices is presented. © *2002 American Vacuum Society.* [DOI: 10.1116/1.1498277]

I. INTRODUCTION

The off-stoichiometry silicon oxide, or silicon rich oxide (SRO), also known as semi-insulating polysilicon (SIPOS), is a two-phase material formed by silicon dioxide with excess silicon.[1] The silicon excess can be as high as 90% for SIPOS.[2] This material is normally obtained by chemical vapor deposition (CVD) from silane and nitrous oxide as the reactive gases. In this method, the gas flow ratio, $R_o = [N_2O]/[SiH_4]$, is used as the parameter that determines the silicon excess. SRO obtained by silicon implantation into silicon oxide has also been reported.[3]

It has previously been shown that compared to a regular metal–oxide–semiconductor (MOS) structure,[4–6] the devices obtained by deposition of SRO on silicon, and covered with a metal electrode, show strikingly different properties depending on both the SRO and underlying Si. This means that the Al/SRO/Si device depends both on the SRO silicon excess and the type and impurity concentration of the silicon substrate.

Two main devices have been under development using the SRO/Si structure, one is a surge suppresser,[7] and the other is a radiation sensor.[8–10] Both of these devices have a specific behavior depending on R_o and the characteristics of the silicon substrate. However, until now there has not been a consistent model that takes into account R_o and the silicon substrate to explain the behavior of the SRO/Si junction.

One of these behaviors is twofold, i.e., it has a dual component: as a MOS capacitor and as a reverse biased *PN* junction. In such a device, which we call capacitor NP, the MOS structure can produce an inversion layer in the silicon surface under the appropriate bias, which in our case occurs if the top contact is negative with respect to the *n*-type substrate. Under these conditions, the current of the induced *PN* junction must be conducted through the SRO layer. So the capacitor NP will be able to detect radiation impinging on it.[11,12]

Since Hielscher and Preier[12] presented their paper on nonequilibrium capacitors, many researchers have been trying to use the induced *PN* junction on different devices. The SRO/Si structure has demonstrated that it is possible to use the induced junction in a controllable manner, as shown in the experimental data of Fig. 1(a).[9,11] In spite of the controversy as to whether it is a *PN* induced junction or a stable deep depletion region, behavior like the reverse bias *PN* diode is observed.

In addition, our more recent results, shown in Fig. 1(b), confirm the *PN* behavior in this structure.[13] Figure 1(b) shows the same structure used to obtain Fig. 1(a), but illuminated under pulsed light. The upper part of Fig. 1(b) shows the response of the device when the bias was low. The curve is like that expected as if the device were a MOS capacitor. When the voltage is increased the response changes to that of a *PN* junction. This is more evidence of the double behavior of such a structure.

Understanding the physics involved in such a structure is not only important for the devices mentioned, but there are other possibilities including the emission of light in such devices.[14]

In this article, experimental $I-V$ and $C-V$ characteristics of the SRO/Si diode are presented for different R_o values. A link between both behaviors is made. Modeling the device by using *PN* and deep depletion approximations is also presented. Understanding the physical phenomena involved in the SRO/Si junction will contribute to better designing of the novel devices mentioned previously.

II. EXPERIMENTAL PROCEDURE

A. Sample preparation

SRO films with $R_o = 15$, 20, and 30 were deposited on (100) *N*-type Si wafers with nominal resistivity 2–5 Ω cm [impurity concentration $0.9-2.5\times10^{15}$ cm^{-3} (Ref. 15)]. A

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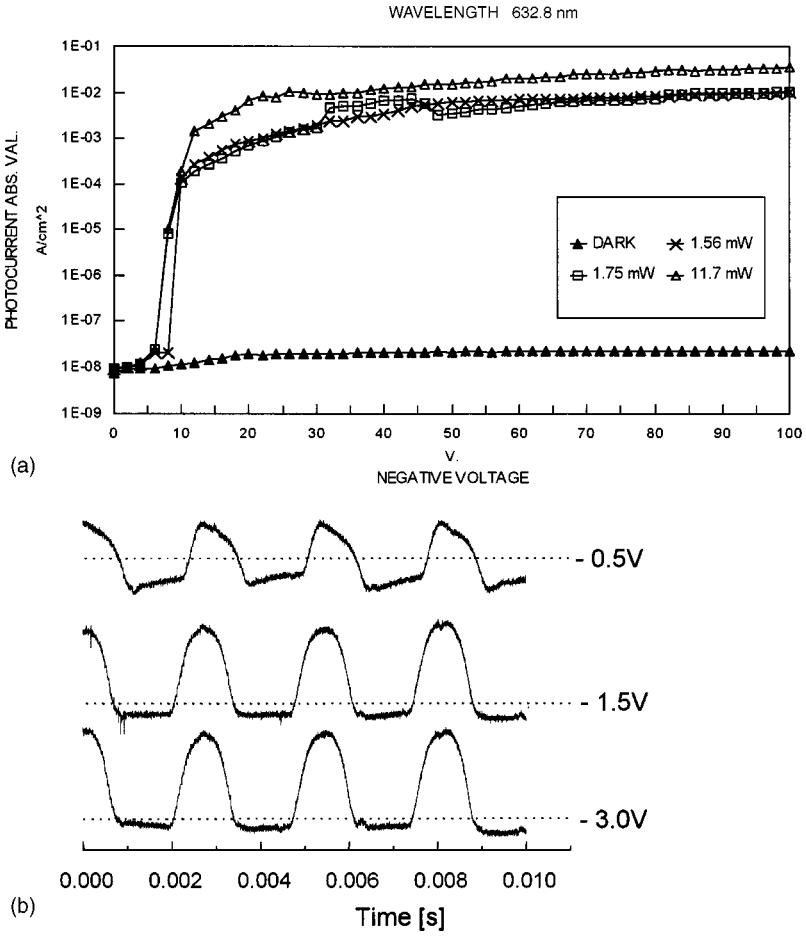

FIG. 1. SRO/Si structure has experimentally demonstrated that it is possible to use the induced junction in a trustworthy manner. (a) SRO/Si response to light vs voltage. Note that a voltage different than zero is required (Ref. 9). (b) Relative response to pulsed light (Ref. 13), as the negative bias increases the response changes from that of a MOS capacitor to that of a *PN* junction.

hot wall low pressure CVD system was used, and the reactive gases used were nitrous oxide and silane. The deposition temperature was 700 °C, and the pressure was varied from 1.9 to 2.4 Torr. In order to have good contacts at the back of the wafers, N^+ implantation was performed. Al gate electrodes with an area of 9×10^{-4} cm^2 were patterned on the SRO layer. Al was also evaporated for the back contact. Finally, the samples were sintered at 450 °C in forming gas. The SRO thickness was measured just after deposition using an ellipsometer Gaertner L117 with a 632.8 nm He–Ne laser. The average SRO thickness is presented in Table I.

B. Measurements

$I-V$ and $C-V$ characteristics were measured using computer-controlled systems. For current measurements an electrometer Keithley 617, and a power supply Keithley 230 were used. A two-second-step ramp voltage was applied for all $I-V$ curves. The $C-V$ characteristics were measured at 100 kHz. A Keithley model 590 and a power supply 230 were used. The samples were measured first from accumulation to inversion. Then, they were measured from inversion to accumulation, with illumination at the beginning to avoid deep depletion.

TABLE I. Average values for different parameters.

R_o	t_{SRO} (Å)	ϵ_{SRO}	V_{on} (V)	Max V_{on} (V)	Min V_{on} (V)
15	1584	4.81	11.3	16.5	5.0
20	1207	4.31	19.75	21.0	15.0
30	1587	3.85	66.5	53.0	74.5

III. RESULTS

Figures 2, 3, and 4 show the typical device characteristics $I-V$ and $C-V$ for $SRO_{15,20,30}$ (the subindex indicates $R_o = 15$, 20, and 30). The current and capacitance are plotted on the same graph for comparison. In general, as the R_o value increases the current reduces. From these graphs it is possible to obtain the V_{on}, which is defined as the voltage where the high current regimen starts[4,5] when the capacitor is in accumulation. In addition, from the capacitance curve in accumulation the relative permittivity, ϵ_{SRO}, of SRO, is obtained as the well-known formula

$$\epsilon_{SRO}=\frac{t_{SRO}C_{max}}{A\epsilon_0}, \tag{1}$$

where t_{SRO} is the thickness of the SRO, C_{max} is the capacitance in accumulation, A is the capacitor area, and ϵ_0 is the permittivity of vacuum. Both the average relative permittivity, ϵ_{SRO}, and V_{on} are recorded in Table I for each R_o value.

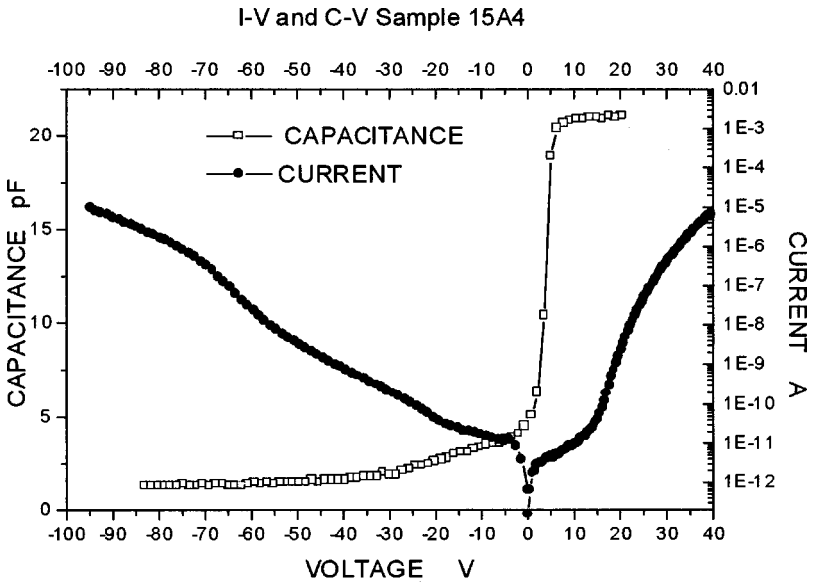

FIG. 2. $I-V$ and $C-V$ typical characteristics for $Al/SRO_{15}/Si$ plotted on the same graph for comparison. The current shows a clear asymmetry for positive and negative voltage. V_{on} is 14 V. Capacitance vs voltage curve was obtained starting in accumulation and finishing in inversion.

In reverse bias, that is, when the capacitor is in surface inversion, the capacitance varies with voltage. Moreover, when R_o increases, the current is reduced and the capacitance variation is less dependent on the applied voltage. For example, for SRO_{15}, in forward bias, that is when the surface is in accumulation, the current at 40 V is in the range of 10^{-5} A, but at -40 V is only 10^{-9} A. For SRO_{20} it is 10^{-8} A for $+40$ V and 10^{-10} A for -40 V. However, for SRO_{30}, the current is only around 10^{-12} A in negative bias and there is no variation with voltage.

For $R_o=30$, two different $C-V$ characteristics were found. Figure 4(a) was measured from accumulation to inversion. The $C-V$ curve in Fig. 4(a) looks similar to those corresponding to SRO_{15} and SRO_{20} in Figs. 2 and 3, respectively. In this case, the current is the smallest for all R_o values presented. In the forward bias there is no V_{on} before 100 V, which is our equipment maximum. A few devices show V_{on} higher than 100 V, and they were not counted in the average shown in Table I. From about 15 to 0 V the current decreases and then slightly increases, as discussed in Ref. 4. The current in reverse bias is as low as some picoamperes at 100 V.

However, Fig. 4(b) shows another behavior of the devices with SRO_{30}. In this case the measurement was done from inversion to accumulation, and the positive charge trapped in the SRO produces the $C-V$ curve shift in the negative direction. The shift of the $C-V$ curve is due to the trapped charge, as observed in Refs. 4 and 5. As expected, the trapped charge effect is less with lower R_o. For $R_o=15$ there is no evidence of the trapped charge effect.

Figure 4(b) is interesting because it clearly exhibits the behavior of the SRO layer on silicon. The SRO layer with $R_o=30$ has a high resistivity. Due to the fixed positive charge in the SRO layer, a silicon surface is accumulated for voltages more positive than -55 V. Thus, the capacitance is a maximum, namely, that of the SRO layer alone. Between

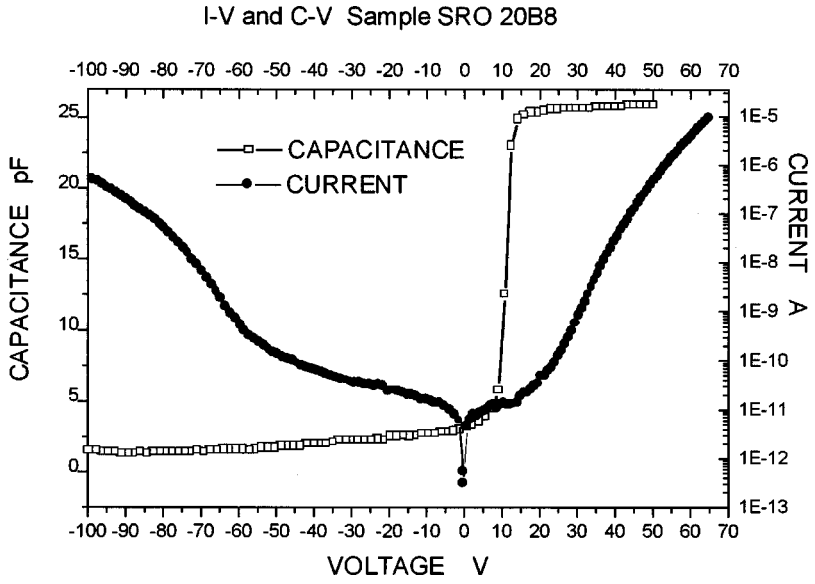

FIG. 3. $I-V$ and $C-V$ typical characteristics for $Al/SRO_{20}/Si$ plotted on the same graph for comparison. The current shows a clear asymmetry for positive and negative voltage. V_{on} is 16 V. Capacitance vs voltage curve was obtained starting in accumulation and finishing in inversion.

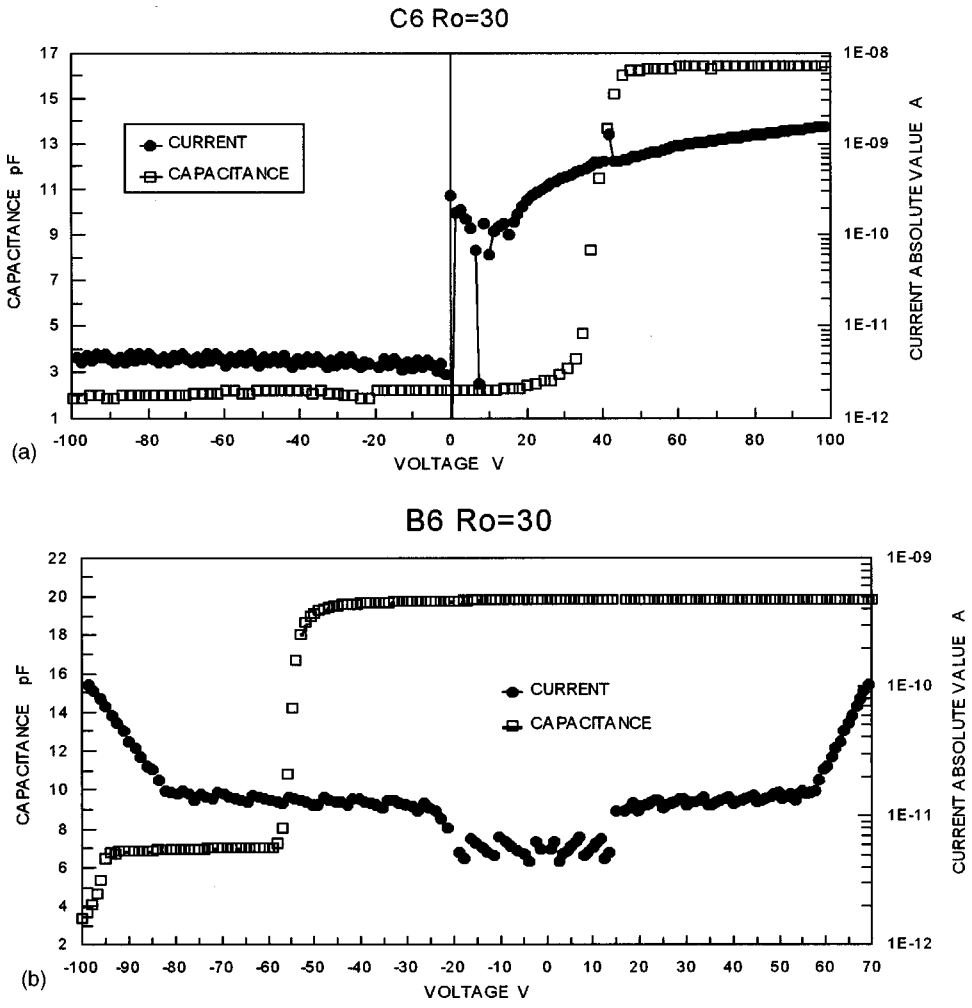

FIG. 4. $I-V$ and $C-V$ typical characteristics for $Al/SRO_{30}/Si$ plotted on the same graph for comparison. The current shows a clear asymmetry for positive and negative voltage. (a) Capacitance vs voltage curve was obtained starting in accumulation and finishing in inversion. For this specific device V_{on} is higher than 100 V. (b) V_{on} is 67 V, $C-V$ curves were recorded from inversion to accumulation. Capacitance shows a clear shift due to charge trapping in the SRO compared with (a).

-60 and -95 V the capacitance is reduced to about 7 pF due to the inversion layer at the silicon surface, according to the standard MOS capacitance theory. In part of this region, the external current is around 10^{-11} A, but from -85 V, the external current begins to drain the inversion layer. However, it is only until at about -95 V that the capacitance decreases from the inversion value of 7 pF.

IV. DISCUSSION

The inversion layer in the SRO/Si device is formed depending on various parameters: silicon type and bulk concentration, SRO resistivity, and applied voltage. On the other hand, the current through the SRO is limited by the conduction mechanisms. Basically, electrons can move in the SRO, but holes cannot.

We have previously shown that in *P*-type silicon as soon as $+V_{on}$ is reached the electrons from the inversion layer are swept out, giving way to a deep depletion. Experimental $I-V$ curves of SRO/$P-$Si are quasisymmetrical,[16] that is, the high current regimen starts at both polarities. For *N*-type substrates the polarity that produces an inversion surface layer results in a low value of current for voltages much larger than the V_{on}.

For SRO/*N*-Si, as shown in Fig. 4(a), an inversion layer is formed and sustained even to -100 V, showing similar behavior to a MOS capacitor. Also, in Fig. 4(b), even when the SRO drains current at about -80 V, the $C-V$ curve does not change until -95 V. That indicates that the depletion layer does not vary, and the surface inversion is sustained at least until 95 V. That gives way to a P^+ induced layer associated with a depletion layer on *N*-type substrate similar to a *PN* junction. In this case the inversion layer is not swept out, contrary to the results on a *P* substrate, because the holes cannot move through the SRO. The low hole current appears to be dominated by the recombination of holes from the inversion layer and electrons moving through the SRO from the Al gate.

The limiting factor of this recombination should be the resistivity of the SRO and the generation process in the depleted region of the silicon. The generation process will provide new holes to replace holes recombining at the surface inversion layer. The SRO resistivity has to be high enough to keep the flow of electrons low. As the magnitude of the voltage increases, the current increases but it is still possible for the inversion layer to be preserved; for example, in Fig. 4(b) for voltages from -80 to -95 V. In this case the depletion layer will grow and a behavior similar to that of a reverse-

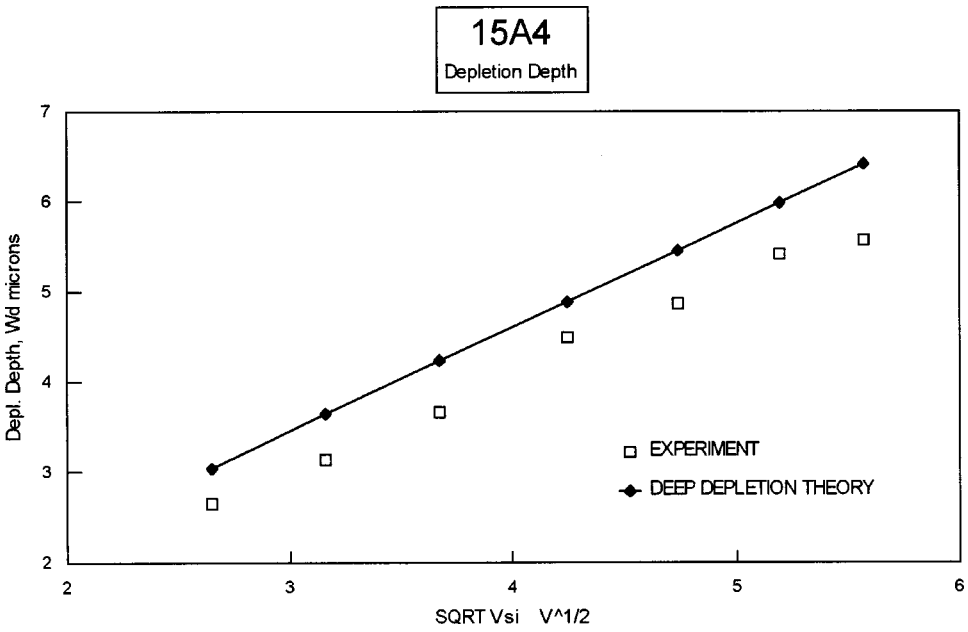

FIG. 5. Depletion width as a function of square root of voltage for sample 15A4, deep depletion approximation for $C_B = 1\times10^{15}$ cm^{-3}.

biased *PN* junction takes place. However, that is not the case in Fig. 2 where the current grows too fast to keep the inversion layer.

For SRO_{15} the current at negative voltage increases continually. This leads us to believe that an inversion layer is not formed, in spite of the fact that we do not observe a standard MOS deep depletion capacitance behavior. Evidently, more research has to be done on this structure.

By contrast, for $SRO_{20,30}$ the current increases slowly until a certain voltage, then the slope, changes, and the current increases faster. It can be proposed that the current increases faster because the inversion layer was swept out completely. In the slow-increase current regimen the current is predominately due to generation in the depletion region, as in a *PN* junction.

Then, it is possible to study the devices from two points of view: that with SRO_{15} as a deep depleted MOS capacitor, and devices with $SRO_{20,30}$ as a MOS capacitor and a *PN* junction depending on the voltage applied.

A. Analysis for SRO_{15}

From the $C-V$ curves it is possible to estimate the depletion width from the well-known formula

$$\frac{1}{C}=\frac{1}{C_{\max}}+\frac{1}{C_S}\approx\frac{1}{C_S}, \tag{2}$$

where C_S is the semiconductor capacitance.

Furthermore, the voltage at the silicon surface, V_S, can be found by subtracting the voltage across the SRO layer from the applied voltage. The voltage across the SRO layer is found from the $I-V$ characteristics of the SRO–silicon device when the applied voltage is positive and the silicon surface is in accumulation. It is assumed that the voltage across the silicon is negligible under this condition. The flatband voltage from the capacitance curve must be used to correct for any fixed charge. The depletion depth, W_d, from capacitance measurements versus the square root of V_S for sample 15A4 is shown in Fig. 5 along with the theoretical depletion depth obtained from

$$W=\sqrt{\frac{2\epsilon_{\mathrm{Si}}V_s}{qC_B}}. \tag{3}$$

The correlation between the measured and theoretical values is reasonably good.

B. Analysis for SRO_{20} and SRO_{30}

The depletion widths for these devices are shown in Figs. 6(a) and 6(b) as a function of voltage. Two regions can be observed: the MOS capacitor and *PN* junction regions. In the MOS capacitor region, a constant capacitance due to a maximum depletion width is manifested, and a variable width as a function of voltage is also presented.

A simple approximation is to model the depletion region as a MOS capacitor and as a *PN* junction at the respective voltage region.

In the *PN* junction the width is obtained from[15]

$$W(V)=\sqrt{\frac{2\epsilon_{\mathrm{Si}}|\phi_b-V|}{qC_B}}, \tag{4}$$

where φ_b is the built-in potential and V is the applied voltage. In this case, φ_b does not have the same meaning as in a *PN* junction because in a standard *PN* junction the φ_b is a result of the transfer of charge between the *P* and *N* semiconductor, and depends only on the bulk concentration. In the capacitor NP, the *PN* junction is a result of a voltage-induced surface inversion, and depends on the voltage applied and the bulk concentration among other parameters. In a simple way, the voltage where the *PN* behavior starts will be considered as φ_b for these devices.

From Eq. (4), plotting W^2 against V, we obtain a linear function with slope m, and then

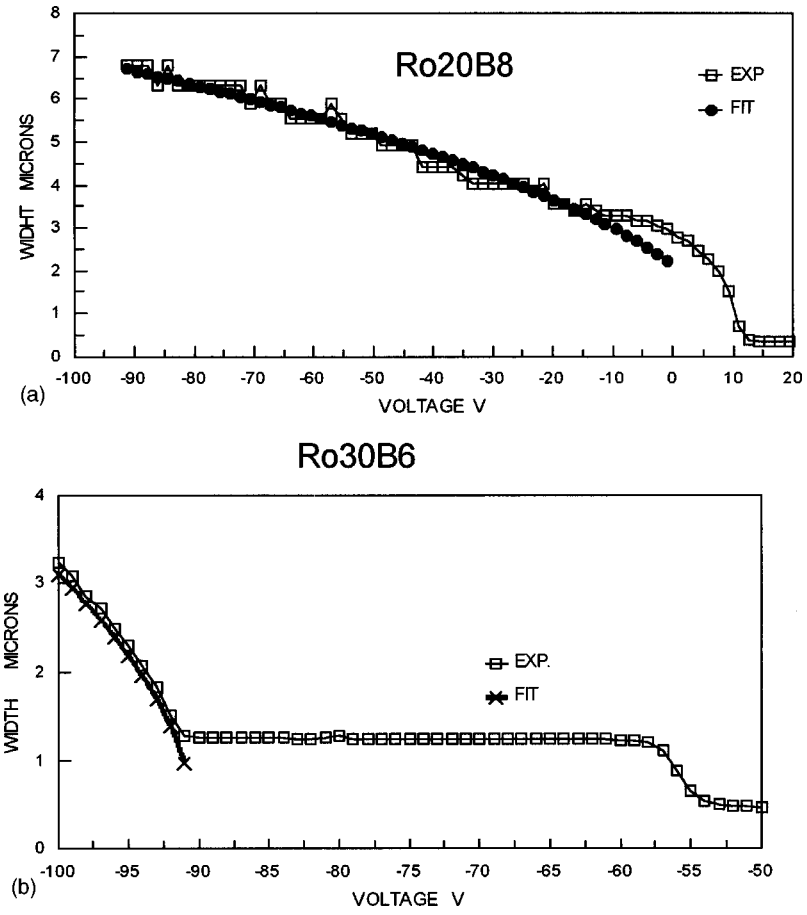

FIG. 6. Depletion width as a function of voltage using *PN* approximation, (a) sample 20B8, $C_B=2.8\times10^{15}$ cm^{-3}, $\phi_b=10$ V; (b) sample 30B6, $C_B=1.3\times10^{15}$ cm^{-3}, $\phi_b=90$ V.

$$C_{\text{Befe}}=\frac{2\epsilon_{\text{Si}}}{qm}, \tag{5}$$

where C_{Befe} is the effective bulk concentration. Thus, the applied voltage appears to affect the substrate concentration, and a different bulk concentration is obtained for each sample. In any case, the effective bulk concentration is not inconsistent with the nominal variation stated by the vendor. The effective concentrations for the specific samples used in Figs. 6(a) and 6(b) are recorded in the figure captions.

It has already been proposed that under inversion voltage the current is limited by the thermal generation in the depletion region.[4,17] In such a case, the current can be expressed as

$$I=\frac{qn_iW(V)}{2\tau_g}A, \tag{6}$$

then the generation lifetime, τ_g, can be estimated as

$$\tau_g=\frac{qn_iW(V)}{2I}A. \tag{7}$$

From Figs. 6(a) and 6(b), W and I are used to estimate the lifetimes of SRO_{20} and SRO_{30}, and the values obtained are 1.52×10^{-6} and 5.48×10^{-6} s, respectively. In previous work,[18] we found for these types of wafers that $\tau_{\text{gen}}\approx1\times10^{-6}$ s.

V. CONCLUSIONS

$I-V$ and $C-V$ characteristic curves were obtained for the Al/SRO/Si devices with various R_o. The depletion widths were obtained from these curves. The widths were modeled using a *PN* deep depletion approximation and it was found that good agreement existed between the experimental results and the fitted curves. In the *PN* region an effective bulk concentration has to be used.

As R_o increases, the MOS-like structure dominates, and the trapped charge is more relevant. As R_o decreases it is possible that the *PN* behavior is not obtained, and the trapped charge does not have an important role.

It was shown that it is possible to use the Al/SRO/Si structure to estimate characteristic constants of the materials constituents, for example, the generation lifetime. So, another possible application for this structure is as an analytic tool.

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