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FGMOS flip-flop for low-power signal processing

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In this paper, a family of latches based on floating-gate MOS (FGMOS) transistors is presented. This family takes advantage on the fact that FGMOS logics process data using mostly passive devices, achieving small area and low-power, which is a requirement in modern electronics. Post-layout SPICE simulations using ON-Semiconductors 0.5μm CMOS process parameters show improvements over conventional CMOS logic families, making FGMOS latches ideal for low-power applications.

Keywords: digital integrated circuits; low-power integrated circuits; FGMOS transistors

1. Introduction

Modern electronics present important challenges to design low-power, highly integrated data processing. To face these demands, digital design has developed many topologies to reduce power-delay product. Among these, floating-gate MOS (FGMOS) transistors have demonstrated to achieve power reductions while still maintaining speed in many high performance applications (Aunet, Berg, Tjore, Næss, & Sæther, 2001).This is possible due to the fact that FGMOS transistors process data within the capacitive network coupled to their gate (Shibata & Ohmi, 1992). As data processing is carried using mostly passive devices at gate level, no switching nodes or leaky devices are involved achieving virtually no power dissipation.

2. Positive feedback floating-gate logic

Unfortunately, additionally to the input network, several parasitic capacitances are coupled to the floating-gate of the FGMOS transistors (Molinar-Solís, Ponce-Ponce, García-Lozano, Diaz-Sanchez, & Rocha-Pérez, 2010). These parasitic couplings make the floating-gate susceptible to noise coming from different sources, affecting the performance of the FGMOS circuit. Furthermore, if small input capacitors are used, the weight of the parasitic coupling within the input network increases and thus noise-sensibility. Previous works have analysed some of these problems (Cisneros-Sinencio, Díaz-Sánchez, & Ramirez-Angulo, 2011). Positive feedback floating-gate logic (PFFGL) uses a positive-feedback loop to improve gain in order to reduce errors due to process variability or noise (Wang & Harjani, 1995). This way, using smart layout techniques, noise is diminished by

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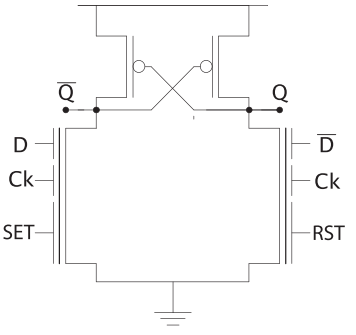

Figure 1. Latch D implementation using floating-gate transistors.

the common-mode rejection characteristics of the logic. This way is possible to use small input capacitances, allowing reductions in power and area.

3. PFFGL sequential gates

PFFGL sequential gates take advantage of the p-MOS semi-latch used as pull-up circuit to save the last output data. Consider the D latch shown in Figure 1. During normal operation, SET and RST inputs are set to zero. As these inputs have twice the weight of the other inputs, the transistor threshold voltage will be reached only if the clock input (Ck) is high. If Ck and SET/RST inputs are zero, no matter the state of the input D, both FGMOS transistors will be off and the data at the outputs will be retained. If eventually Ck flips to a high state, the state of D will be sufficient to trigger the latch. In the case that SET or RST has a high state, a change at the output will occur immediately; as these inputs has twice the weight of the other inputs will override the state of D or Ck. To achieve the set or reset process, Ck needs to be low to avoid the possibility that both input FGMOS transistor be turned on simultaneously resulting in an invalid output.

Due to their small transistor count, the proposed latch solves problems as body effect; implementations as CMOS or pass-transistor latches uses long chains of series transistors, resulting in a degradation of the output data. To restore output noise, buffers can be used. Although this solution can effectively restore output levels, it will increase both power and delay of the gate.

4. Comparison of results

In this section, post-layout simulations are performed to compare the proposed PFFGL sequential gates against conventional logic families. The gate selected for this comparison is a D flip-flop. The floating-gate flip-flop proposed for evaluation is shown in Figure 2. It consists in two D latches in series. Whenever the clock input Ck has a high state, the first D latch will pass the input data to its output. If Ck flips to zero, the input data will be stored at the first latch. Simultaneously, the second D latch will pass the held data to the output Q. When Ck flips back to high, the first gate will admit a new input data while the output latch will be holding the last output state.

Complementary pass-transistor logic (CPL) and standard CMOS versions of the D Flip-Flop (Weste & Eshraghian, 1998) are shown in Figures 3 and 4. The latching operation is realized by two cross-coupled inverters. The feedback of the inverters will

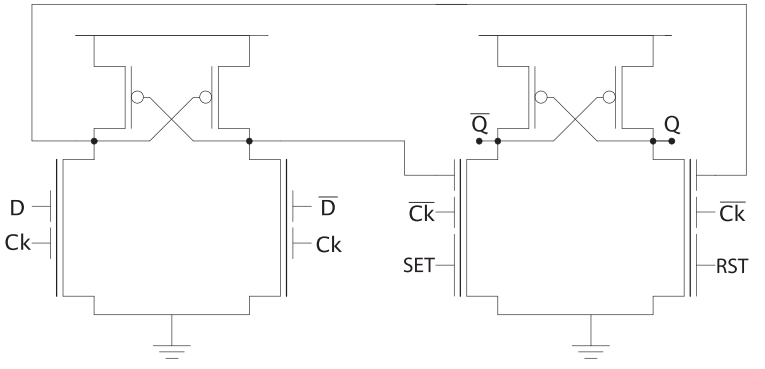

Figure 2. Proposed circuit for the implementation of a D flip-flop.

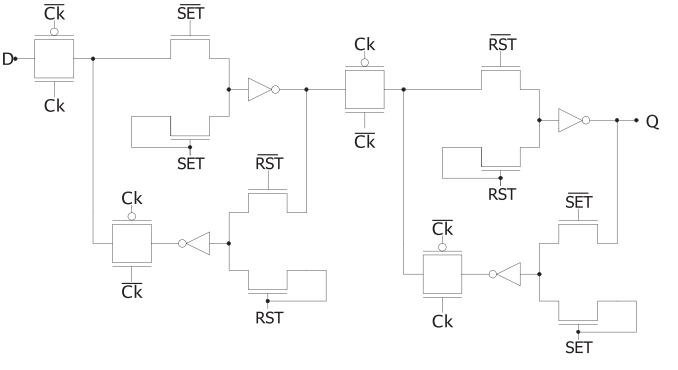

Figure 3. Complementary pass-transistor D flip-flop.

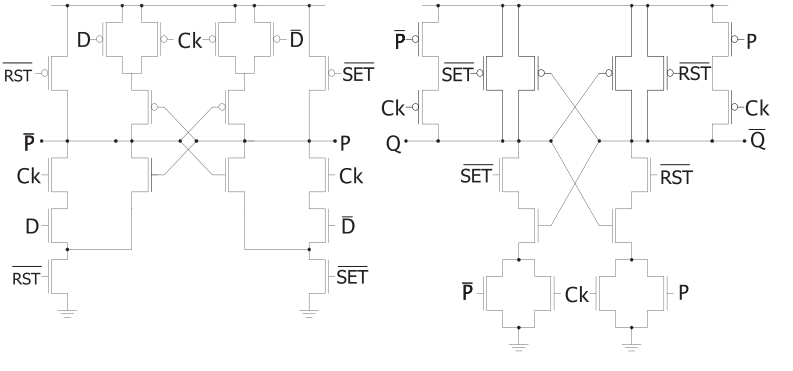

Figure 4. CMOS D flip-flop.

make possible the data holding. To modify the stored data, pass-gate transistors at the input of each of the two D latches are used. When Ck have a high state, the first pass-gate will allow data acquisition by the first latch while isolate the second. If Ck changes to low, the first latch will hold the last input data, passing through the second latch to the output Q. When a SET/RST procedure is carried out, the feedback loop between the latching

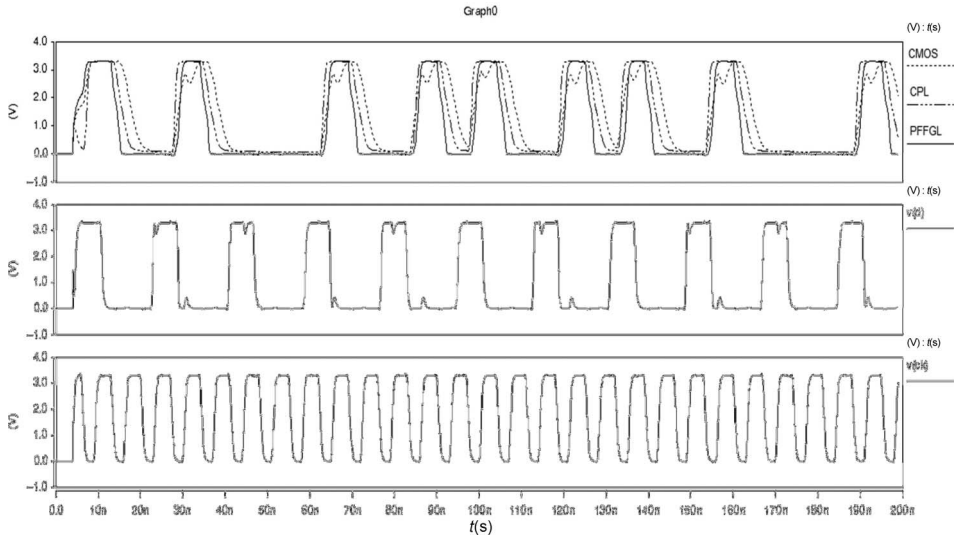

Figure 5. SPICE simulation results for the three D flip-flop implementations.

inverters is opened. Once the feedback loop is open, the SET/RST data is applied. When this procedure is finished, the feedback loop is restored.

The CMOS D flip-flop is shown in Figure 4. In this scheme, cross-coupled transistors are used for data memorization. As well as the previous circuits, it consists in two D latches in series. This implementation requires five transistors in series, making the flip-flop to operate at very low frequency. Besides, the power requirement rises, making the implementation not suitable for low voltage. The voltage requirement, the transistor tree height and the large count of transistors and switching nodes, makes this implementation improper for energy efficient battery driven applications.

Simulations were performed using H-SPICE with a BSIM3 ON-Semiconductors 0.5-µm CMOS process parameters. To achieve realistic results, the technique discussed in (Rodriguez-Villegas, Huertas, Avedillo, Quintana, & Rueda, 2001) is employed for simulation of floating-gate transistors. For each of the implementations, a load similar to a flip-flop of the same family was used at the output. Figure 5 shows the simulation results for all of the flip-flop implementations. Even when FGMOS and CMOS were able to work at lower voltage, the simulations were performed at 3.3 volts. The long transistor chain of CPL implementation was not able to work properly below this voltage.

By using a high gain amplifier as comparator, PFFGL is able to use the smallest transistors allowed by the technology. This condition let using small input capacitances for the FGMOS transistors, achieving the smallest input capacitance of the comparison. The resulting input capacitance of the PFFGL flip-flop is less than 19 fF. Low voltage and small capacitance internal nodes allow PFFGL to show significant improvements in power characteristics. Figure 6 shows an energy comparison between all the flip-flop implementations. CPL showed the worst case, consuming an amount of energy equal to 10.67 pJ along the test cycle. CMOS showed similar power characteristics, wasting 10.39 pJ along the cycle. The best power performance was reached by the PFFGL implementation, with a reduction of 28% in energy consumption resulting in an energy

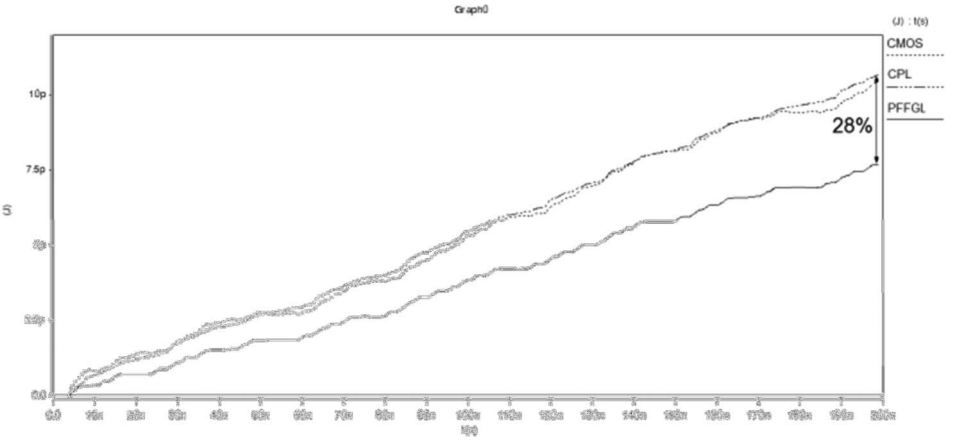

Figure 6. PFFGL D flip-flop showed better power performance.

Table 1. Simulation results.

	t_d (ns)	t_r (ns)	t_r (ns)	Input capacitance. (fF)	Transistor count
CPL	2.01	0.90	2.49	40.05	26
CMOS	4.00	2.07	3.03	89	32
PFFGL	2.31	0.97	1.67	<18.9	8

waste of 7.69 pJ. It was expected CMOS to have the worst performance in the comparison due to its large count of transistors and the long transistor trees. Even though, CPL resulted to be the worst case in voltage and power consumption.

Table 1 shows the comparison of the three flip-flops. It can be seen that the floating gate flip-flops have the smaller transistor count in the comparison, requiring an area of 51×28 μm^2. Besides the area reduction due to a small transistor count, there is an improvement due to a simplification of routing. Smaller devices and simplified routing leads to improvements in circuit integration.

From Table 1, it can be seen that CMOS shows the worst propagation delay in the comparison. The latency of the CMOS flip-flop is significantly bigger than its counterparts. Moreover, CMOS achieved the worst rise/fall times, reducing its frequency of operation. The best speed characteristics were achieved by the PFFGL flip-flop, being able to work at 600 MHz while CMOS frequency of operation is about only 330 MHz and CPL is able to operate at a frequency of 400 MHz. Again, the small capacitance internal nodes led to performance improvements.

As example of application considers an eight-stage shift register. The test circuit is constructed using eight Flip-Flops as the one in Figure 2 connected in series as is shown in Figure 7. From the graph in Figure 8, it can be seen that the input data (d) is passed to the output of the first flip-flop (ql) accordingly to the clock signal (ck). Also, it can be seen the data shifting among the outputs of the register (ql–q8).

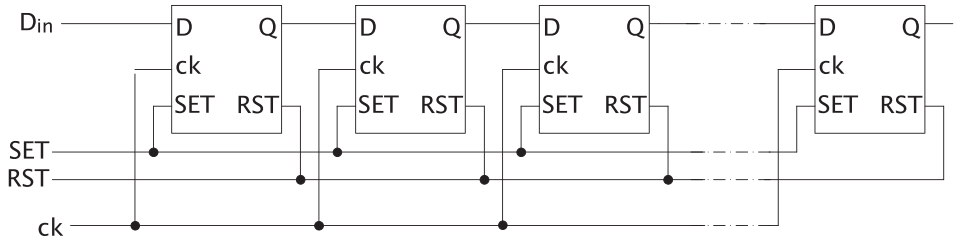

Figure 7. Eight-stage PFFGL shift-register.

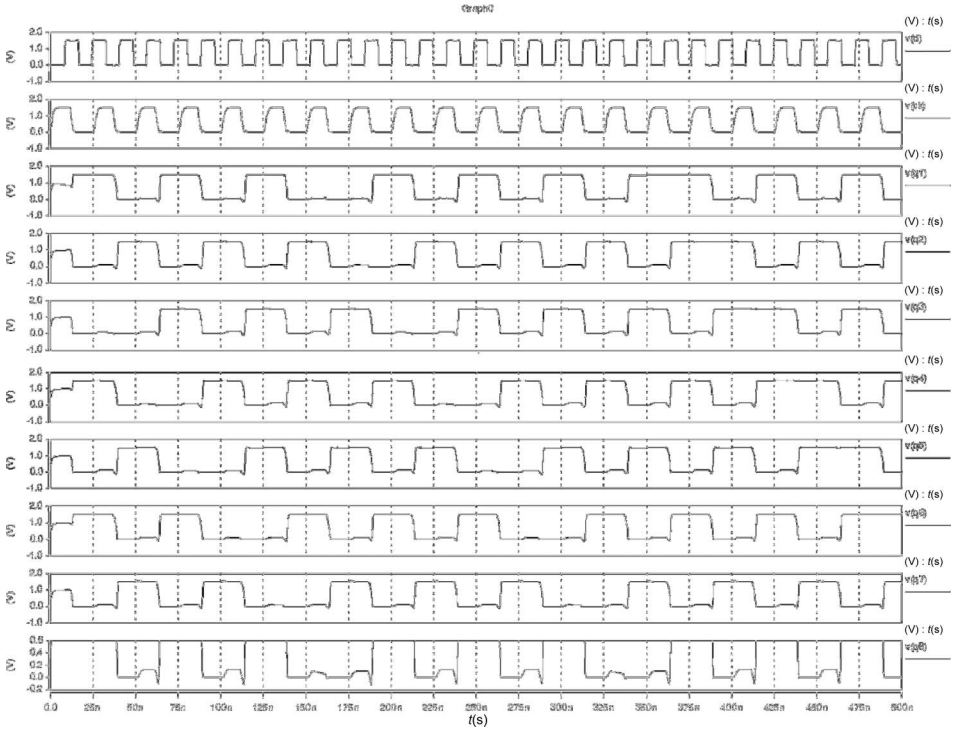

Figure 8. Simulation results of the eight-stage PFFGL shift-register.

5. Conclusion

A new sequential logic family featuring floating-gate transistors was introduced. The principal features of this design style are low power and high scale of integration. The logic style in which this family is based allows robustness to the typical problems of the floating-gate logics while still maintaining its advantages. FGMOS transistors as inputs allow data processing in a very compact circuit. The proposed gates require less area than similar implementations in the comparison. Positive feedback realizes a fast establishment of the output state. The frequency of operation of the floating-gate sequential logic is higher than conventional sequential gates.

The sequential logic proposed in this paper will allow the construction of low power circuits. Sequential logic is essential in digital data processing. Thus, high performance low-power sequential logic is vital in the construction of circuitry for biomedical applications. FGMOS logic gate has been successfully used to construct processing and arithmetic blocks as adders and multipliers (Cisneros-Sinencio, Díaz-Sánchez, & Ramirez-Angulo, 2004). These processing blocks will fulfil the energy-efficient, low-voltage, high-integration requirements of applications like cochlear implants or machine-brain interfaces while still maintaining speed.

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