Identifying the Diffusion and Drift Conduction Regions in MOSFETs Through S-Parameters

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***Abstract*—A method for characterizing low-voltage-operating MOSFETs through small-signal S-parameters is introduced. The method allows extracting the drain-to-source channel resistance at zero drain-to-source voltage, which is not feasible with dc conventional methods. Furthermore, this zero drain-to-source voltage RF method identifies the gate voltage where the diffusion and drift conduction mechanisms overlap. This is really helpful in defining the appropriate subthreshold drain current model and its corresponding impact at RF operating conditions. The proposed experimental RF method is validated and compared with a dc-based method for an 80-nm-channel-length nMOSFET.**

***Index Terms*—RF-MOSFET, S-parameters, subthreshold.**

I. Introduction

NOTWITHSTANDING the low-power-consumption specification of some analog IC applications requires the operation within or near the transistor subthreshold regime [1], [2], little research effort has been done to study this operating regime from an RF perspective [3], [4]. The RF low-power operating condition requires the identification and appropriate modeling of the transport mechanisms associated to the drain current (I_d), which is fundamental for a proper IC design [5]. In this low-voltage regime, the diffusion and drift transport mechanisms coexist in a very intricate way because of their gate-to-source voltage dependence. Nevertheless, there is a transitional voltage $(V_{\rm tr})$ that establishes a frontier between the gate-to-source voltage $(V_{\rm gs})$ regions at which both diffusion and drift transport mechanisms cross over; this is the voltage at which both mechanisms present equivalent contribution to the drain current. Research has been previously carried out to obtain $V_{\rm tr}$ based on the fact that the diffusion mechanism presents a positive and exponential temperature coefficient, whereas that associated with carrier drift is linear and negative [6], [7]. In this case, $V_{\rm tr}$ is determined at the voltage at which I_d–$V_{\rm gs}$ curves obtained at different temperatures intersect at a fixed drain-to-source voltage $(V_{\rm ds})$ [8].

Even though dc measurements at a single temperature can be used to obtain $V_{\rm tr}$, the application of a drain-to-source voltage $V_{\rm ds}$ different from zero is still required in alternative techniques [9], which introduces a longitudinal electric field that impacts the extraction of $V_{\rm tr}$ [10]. Furthermore, the presence of parasitic series resistances requires the use of transistors with different channel lengths, from where the source-to-drain resistance is extracted through linear regressions. Conversely, small-signal S-parameter measurements allow obtaining the channel resistance $(R_{\rm ch})$ at practically $V_{\rm ds} = 0$ V [11]. Moreover, using an S-parameter-based characterization approach is desirable since RF device prototypes are typically configured for testing using coplanar ground–signal–ground (GSG) probes, avoiding further experiments once the S-parameters are measured.

Thus, when measuring S-parameters at $V_{\rm ds} = 0$ V while sweeping $V_{\rm gs}$ from the subthreshold to the strong-inversion operation region, an accurate characterization of the subthreshold region can be carried out. In fact, by using these data, a method to obtain $V_{\rm tr}$ can be proposed as explained through this work. Thus, for formulating and verifying the proposal, experiments were performed using an 80-nm-channel-length nMOSFET.

II. Description of Experiments

Common source/bulk nMOSFETs were fabricated in an RFCMOS process with a gate mask length $L_m = 80$ nm, a finger width (W_f) of 3 μm, and eight gate fingers (NF). To characterize these devices, on-wafer S-parameter measurements were performed up to 50 GHz at $V_{\rm ds} = 0$ V and different $V_{\rm gs}$'s using a vector network analyzer (VNA) and GSG-configured probes with a pitch of 150 μm. For this purpose, the VNA setup was previously calibrated up to the probe tips using a line–reflect–match off-wafer algorithm, whereas the effect of the probing pads was de-embedded using a two-step procedure [12]. Furthermore, to maintain the measured device within small-signal operation conditions, the maximum power applied to the device's input and output terminals was −20 dBm.

In addition to S-parameters, current–voltage (I–V) curves were measured on the same devices using a semiconductor parameter analyzer and dc probes. As shown in the following, these measurements allow carrying out a comparison of the RF method with that using dc data.

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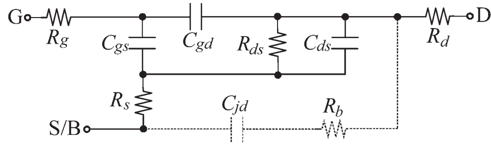

Fig. 1. Small-signal model for a bulk MOSFET at $V_{\text{ds}} = 0$ V. The dashed elements represent the drain-to-source coupling through the substrate.

III. Modeling and Characterization Approach

When measuring S-parameters, at $V_{\text{ds}} = 0$ V and $V_{\text{gs}} > 0$ V, the MOSFET is considered a two-port network that can be represented using the equivalent circuit shown in Fig. 1. This circuit includes the intrinsic capacitances (i.e., C_{gs}, C_{gd}, and C_{ds}), the intrinsic drain-to-source resistance (R_{ds}), the extrinsic series resistances (i.e., R_g, R_d, and R_s), and the substrate elements (i.e., C_{jd} and R_b). Notice that, since R_{ds} is associated with the conduction path through the channel region, this element experiences the effects associated with the charge carrier scattering mechanisms affecting I_d even under subthreshold operation. Thus, when this element is properly determined, the behavior of a MOSFET can be analyzed in this region, which is explained hereafter.

Notice in Fig. 1 that two paths for the current flowing from the drain to the source terminal are considered: the intrinsic channel region and the parasitic substrate path represented by the series connection of R_b and C_{jd}. Even in bulk MOSFETs, the effect of R_b and C_{jd} has been previously neglected without a significant penalization of accuracy in the extraction of the intrinsic elements from RF measurements at frequencies of some gigahertz [11]. This assumption, however, is only valid when the device is operated in strong-inversion conditions well above the threshold (i.e., when R_{ds} is much smaller than the substrate impedance). However, for MOSFETs operating within or near subthreshold, the magnitude of the intrinsic impedance may become comparable to that of the substrate, which impedes neglecting R_b and C_{jd}. This is particularly applicable to a MOSFET scaled down to sub-100-nm dimensions, where the drain-to-source parasitic coupling may be considerably stronger than that for larger devices. Thus, for obtaining R_{ds} from experimental S-parameters, removing the effect of the substrate elements is necessary. Fortunately, these components can be determined from OFF-state S-parameter measurements and subsequently de-embedded from other measurements due to their weak gate-bias dependence [13].

In accordance to Fig. 1, once the effect of the substrate elements is removed, the equivalent circuit can be easily analyzed by converting the corresponding S-parameters to Z-parameters. In fact, R_{ds} and the parasitic source and drain series resistances can be simultaneously obtained after determining the slope and intercept with the ordinate axis of the linear regression of experimental $-\omega/\text{Im}(Z_{22})$-versus-$\omega^2$ data [11], where ω is the angular frequency in radians per second. Notice that this regression is performed on ω for a single device and at a fixed-bias condition, which allows obtaining R_{ds} as a function of V_{gs} for identifying the type of conduction mechanism occurring as shown afterward, with no need of using different-channel-length devices.

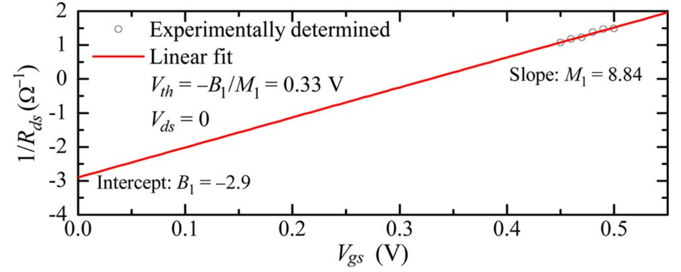

Fig. 2. Experimental determination of the model parameters for R_{ds} assuming the drift conduction mechanism.

IV. Modeling the Small-Signal R_{ds}

When $V_{\text{gs}} > 0$ is approaching the threshold voltage (V_{th}) in an nMOSFET, a conduction path for the charge carriers is originated even at $V_{\text{ds}} = 0$. In this regard, as V_{gs} rises from zero, the first conduction mechanism that is present is diffusion, and R_{ds} exponentially decays with V_{gs}. Furthermore, when V_{gs} increases even more and is close to V_{th}, the drift mechanism arises. Assuming that this is the main mechanism contributing to define R_{ds}, the following expression can be written:

$$R_{\text{ds}} = \frac{L_{\text{eff}}}{\text{NF}W_f\mu_{\text{eff}}C_{\text{ox}}}\frac{1}{V_{\text{gs}} - V_{\text{th}}} \tag{1}$$

where C_{ox} is the gate oxide capacitance and L_{eff} and μ_{eff} are the effective channel length and mobility, respectively. Thus, when defining $A = L_{\text{eff}}/\text{NF}W_f\mu_{\text{eff}}$, (1) can be rearranged in an alternative form; this is

$$R_{\text{ds}}^{-1} = M_1 V_{\text{gs}} + B_1 \tag{2}$$

where $M_1 = C_{\text{ox}}/A$ and $B_1 = -C_{\text{ox}}V_{\text{th}}/A$. Bearing in mind that relatively small changes in V_{gs} introduce small changes in C_{ox}, μ_{eff}, and L_{eff}, it is a reasonable assumption to consider M_1 and B_1 as bias independent within a range of some millivolts. Hence, using extracted data for R_{ds} within a 50-mV range, M_1, B_1, and V_{th} are obtained as shown in Fig. 2. It is important to remark the fact that M_1 and B_1 remain approximately constant for the fabricated device within the range of V_{gs} above the extrapolated V_{th} and up to 0.5 V, which was verified by repeating the linear regression at different ranges in a similar way as explained in [14]. Nevertheless, for some devices and within wider V_{gs} ranges, the consideration of the bias-dependent parameters that impact M_1 and B_1 in (2) can be required for improving the accuracy of the results.

For modeling R_{ds} in the diffusion region, the following expression can be used:

$$R_{\text{ds}} = \gamma A e^{-\frac{V_{\text{gs}} - V_{\text{th}}}{m V_T}} \tag{3}$$

where V_T is the thermal voltage, whereas γ and m are empirical parameters dependent on the technology [4]. In this case, (3) can be rearranged in the form

$$\ln(R_{\text{ds}}) = M_2 V_{\text{gs}} + B_2 \tag{4}$$

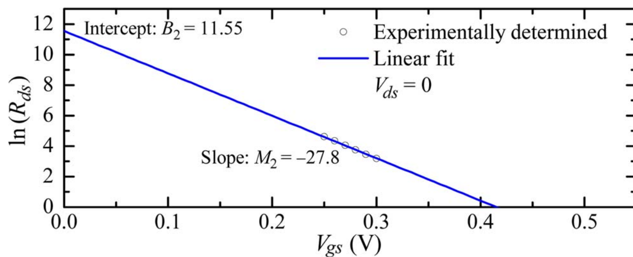

Fig. 3. Experimental determination of model parameters for $R_{\rm ds}$ assuming the diffusion conduction mechanism.

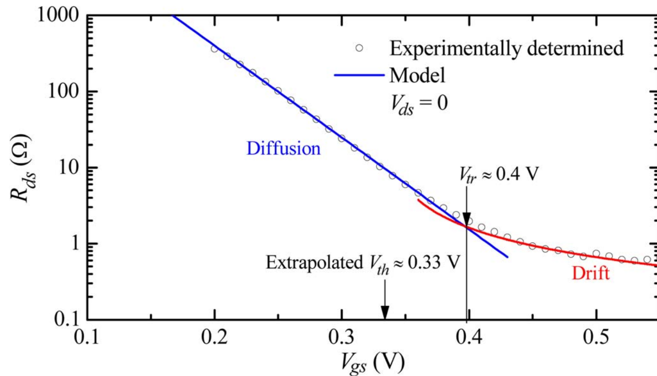

Fig. 4. Model–experiment correlation for $R_{\rm ds}$ using (1) and (3) after determining the corresponding parameters from the measured S-parameters.

where $M_2 = -1/mV_T$ and $B_2 = \ln(\beta A) + V_{\rm th}/mV_T$. Similarly, as in the case of (2), (4) can be used to obtain the model parameters in (3) by assuming that, at voltages near the subthreshold region, M_2 and B_2 are approximately independent of $V_{\rm gs}$. In this case, the corresponding extraction is shown in Fig. 3, where good linearity is observed in the region where the diffusion transport mechanism occurs.

V. Results and Discussion

Once B_1, B_2, M_1, M_2, and $V_{\rm th}$ have been determined, the rest of the parameters in (1) and (3) can be obtained in a direct way. Thus, when implementing the models for $R_{\rm ds}$ given by (1) and (3), excellent model–experiment correlation is achieved in both the drift and diffusion regions, respectively. This can be observed in the plot shown in Fig. 4. Notice also that, from this plot, the voltage $V_{\rm tr}$ at which the drift and diffusion models yield the same value for $R_{\rm ds}$ can be obtained. This point defines the gate voltage at which both carrier diffusion and drift cross over (i.e., where both mechanisms considerably contribute to I_d), which is an important figure of merit when implementing models for carrying out low-voltage IC design. Notice that, in a mathematical way, $V_{\rm tr}$ can be obtained by equating (1) and (3) and solving for $V_{\rm gs}$. Nevertheless, since there is no simple analytic solution for the resulting equation, the straightforward way illustrated in Fig. 4 is preferred to obtain $V_{\rm tr}$.

It is important to remark the fact that $V_{\rm tr}$ in the studied device is 70 mV higher than $V_{\rm th}$, which indicates that the so-called moderate-inversion operation region occurs up to some tens of millivolts above the extrapolated threshold voltage. In fact, there is not a simple relationship between $V_{\rm tr}$ and $V_{\rm th}$ since (1) and (3) include other parameters that vary with technology, geometry, and operation conditions. On the other hand, obtaining $V_{\rm tr} > V_{\rm th}$ is not surprising for nanoscaled devices where the gradient of charge carriers may contribute to I_d in a more accentuated way (even above $V_{\rm th}$) than in micrometer-scaled devices such as those analyzed in classic textbooks [9]. In fact, this effect has been observed within the dc regime by varying the operation temperature to distinguish between carrier drift and diffusion currents [8].

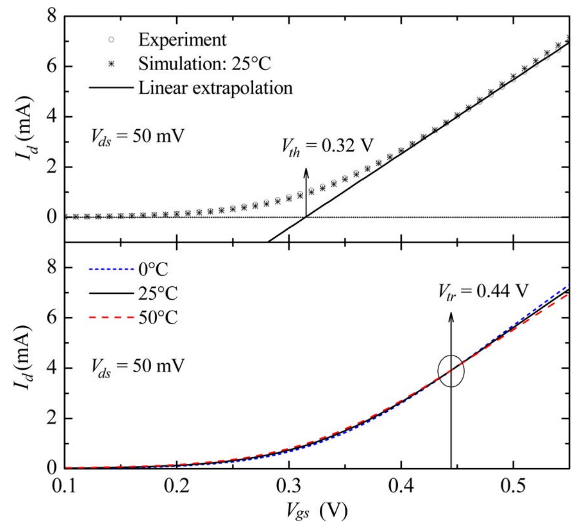

Fig. 5. (Top) Comparison between dc measured data and a TCAD simulation showing also the extrapolated $V_{\rm th}$. (Bottom) Extraction of $V_{\rm tr}$ from simulations at different temperatures.

In [15], it is suggested that $V_{\rm tr}$ can be determined by finding the value for $V_{\rm gs}$ at which the model for the carrier diffusion current, which has an exponential form, intersects that of the carrier drift current, which has a polynomial form. Mainly due to voltage drops in the parasitic series resistances, however, these models may not intersect, complicating the determination of $V_{\rm tr}$. For this reason, in this paper, a different approach is used for comparing our results with extractions from dc data. Once the I_d–$V_{\rm gs}$ curves are experimentally obtained at $V_{\rm ds} = 50$ mV (i.e., in order to minimize the effect of the lateral electric field), a device model was implemented for the studied MOSFET at 25°C in GTS Framework Software 4.3 from Global TCAD Solutions; Fig. 5 (top) shows the corresponding model–experiment correlation. Afterward, the drift–diffusion model was used to reproduce the I_d–$V_{\rm gs}$ characteristics at different temperatures. Fig. 5 (bottom) shows that, using these simulations, the crossover voltage $V_{\rm tr}$ can be extracted at the point where I_d is independent of temperature [8].

Notice the small difference between the extracted parameters from RF and dc measurements. This difference, however, is expected to occur because of the effects impacting conventional dc data. Among these effects is that of the parasitic series resistance (R_S) associated with the source and drain terminals. This resistance changes the slope of the experimentally obtained I_d–$V_{\rm gs}$ curve, introducing an error in the extrapolated threshold voltage. In contrast, the processing of the S-parameters proposed here allowed obtaining the intrinsic $R_{\rm ds}$ without the effect of R_S.

VI. Conclusion

This paper has exploited the potential of RF measurements to characterize features that are typically obtained from dc data. This yields to a straightforward extraction of fundamental MOSFET parameters from S-parameters measured to RF-configured test structures at $V_{\rm ds} = 0$. This paper focuses on the determination of the two $V_{\rm gs}$-delimited regions where carrier diffusion and drift cross over in the MOSFET channel. Thus, after the determination of the small-signal intrinsic resistance associated with the channel region, it is then possible to obtain the crossover voltage $V_{\rm tr}$ defining the boundary between the diffusion and drift current regions. When implementing IC-design-oriented models near or within the subthreshold region, this voltage becomes more relevant than the conventional extrapolated threshold voltage defined purely under strong-inversion operation conditions. This $V_{\rm tr}$ is relevant, among other reasons, because of allowing the determination of the temperature coefficient at low-voltage operating conditions.

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